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Research Article

Analytical Model of Symmetric Halo Doped DG-Tunnel FET

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Abstract

Two-dimensional analytical model of symmetric halo doped double gate tunnel field effect transistor has been presented in this work. This model is developed based on the 2-D Poisson's equation. Some important parameters such that surface potential, vertical and lateral electric field, electric field intensity and band energy have been modelled. The doping concentration and length of halo regions are varied and dependency of various parameters is studied. The halo doping is imparted to improve the ON current and to reduce the intrinsic ambipolarity of the device. Hence we can achieve improved ION/IOFF ratio. The scaling property of halo doped structure is analyzed with various dielectric constants.

Keywords: Halo Doping, Ambipolarity, Surface Potential, Tunnel FET, Poisson's equation, Double gate

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1.Introduction

The tunnel field effect transistors are the promising device to replace conventional MOSFETs for low power applications. The sub threshold swing of the tunnel FET can be reduced below 60 mV/dec [1], which is the main limitation of the MOSFET. The two major impediments of TFET are the lowest on-state current (I_{ON}) and the intrinsic ambipolarity. Several methods and various structures such as usage of lower band gap material [2], high-k dielectric [3], double gate [3], all around the gate [4], and strain engineering [5] are proposed for improving its ON current. However ON current of the TFET is still not adequate to compete with the MOSFET. Only few methods such as gate-drain under lap [6], heterogeneous gate (HG) dielectric (with high-k material at the source side and low-k at the drain end) [7], [8], using a spacer to separate gate and drain [9], and lower drain doping [10] are proposed to reduce the ambipolarity of the device. In this work, to enhance the ON current and reduce the ambipolarity, symmetric halo-doped DG-TFET has been proposed. The analytical modelling has been carried out for this structure. The structure of DG-TFET is basically a pin diode structure where the gate is surmounted above and below its intrinsic region. The channel region is divided into three parts R1, R2 and R3. The region R1 and R3 are n-doped halo regions and both have equal length but doping concentrations may vary. The region R2 is major part and it is an intrinsic part of the channel.

The working principle of TFET is entirely different from that of the MOSFET. If the gate bias voltage is not applied, tunnelling barrier width between the source and channel remains high. When gate voltage is increased, the width of this junction starts decreasing and at a voltage greater than the V_{TH}, the width of the junction is narrow enough so that electrons from the valance band of the source are able to tunnel into the conduction band of the channel via the junction. Then the electrons pass into the drain by drift-diffusion mechanism [11]. When the gate voltage is further increased above V_{TH}, more electrons tunnel in the channel increasing the tunnelling current. After certain gate voltage further reduction of junction width does not occur, so that drain current is saturated at this point. Another important parameter to consider is that the energy level of the channel is also decreasing, while increasing the gate voltage. When the energy level of the channel is reduced or increased it directly affects the tunnelling barrier width. The n halo doping near the source-channel junction is expected to reduce the energy level of the channel at that point. Thus switching speed of the device can be enhanced. For the long channel tunnel FET, the influence of ambipolartiy behaviour is negligible. But for the short channel less than 100 mm, the subthreshold current increases due to severe ambipolar behaviour [12]. Then halo doping at the drain end is expected to decrease the energy level of the channel at that point and results in the higher barrier width which stops the tunnelling leakage between them. Thus sub threshold current can be further reduced. Hence higher I_{on}/I_{off} ratio can be achieved.

2.Model Derivation

The structure schematic of the symmetric halo-doped DG-TFET has been shown in Fig 1. The halo doping concentration N_H is higher than the doping concentration N_{CH} in the rest of the channel.

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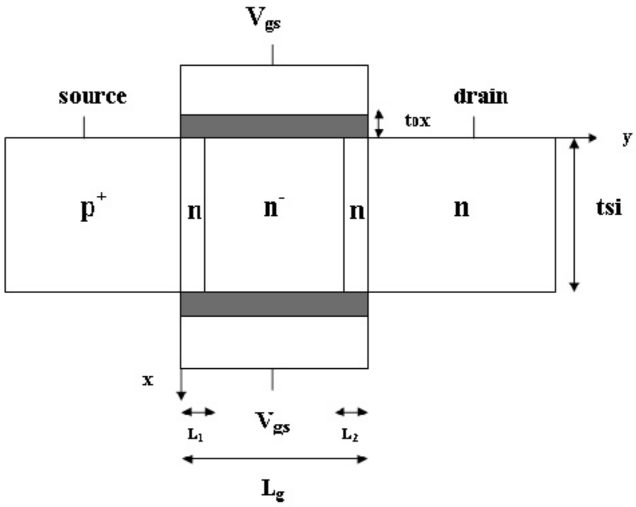

Fig. 1. Cross-section view of Symmetric Halo Doped Tunnel FET

We solve 2-D Poisson's equation on the three regions R1, R2 and R3 for the surface potential and channel electric field. Assuming that the influence of mobile charge and fixed oxide charges on the electrostatics of the device the negligible in the subthreshold regime, we can write the 2-D Poisson's equation of potential distribution along the channel as [13]

$$\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2}=-\frac{qN_s}{\varepsilon_s} \tag{1}$$

Where $\varphi(x,y)$ is the 2-D electrostatic potential, N_s is the effective film doping and is equal to N_1 in the region 1, N_2 in the region 2, and N_3 in the region 3, ε_s is the silicon dielectric constant. The potential distribution along the depth is considered to be parabolic in nature. it can be approximated as second-order polynomial equation [13] as

$$\varphi_j(x,y)=a_{j0}(y)+a_{j1}(y)x+a_{j3}(y)x^2 \tag{2}$$

Where j=1 for region 1, j=2 for region 2 and j=3 for region 3. The boundary conditions of symmetrical DG-TFET having front-gate potential $\varphi_f(y)=\varphi(0,y)$ and back-gate potential $\varphi_b(y)=\varphi(t_{Si},y)$ are

$$\varphi_f(y)=\varphi_b(y)=\varphi_s(y) \tag{3}$$

$$E_j(0,y)=\frac{\eta}{t_{Si}}(\varphi_s(y)-V'gs) \tag{4}$$

$$E_j(t_{Si},y)=-\frac{\eta}{t_{Si}}(\varphi_s(y)-V'gs) \tag{5}$$

Where η is the parameter equal to the ratio of the gate capacitance ($\eta=\frac{\varepsilon_{ox}}{t_{ox}}\frac{t_{Si}}{\varepsilon_{Si}}$) and film capacitance, and $V'gs=V_{gs}-V_{fb}$. By applying the boundary conditions (3), (4), (5) in (2), the variables $a_{j0}(y)$, $a_{j1}(y)$ and $a_{j2}(y)$ can be obtained as,

$$a_{j0}(y)=\varphi_{sj}(y) \tag{6}$$

$$a_{j1}(y)=\frac{\eta}{t_{Si}}(\varphi_s(y)-V'gs) \tag{7}$$

$$a_{j2}(y)=-\frac{\eta}{t_{Si}^2}(\varphi_s(y)-V'gs) \tag{8}$$

where as applying the boundary conditions (2) to (8) in (10), we get the differential equation of the surface potential as

$$\frac{\partial^2\varphi_{sj}(y)}{\partial y^2}-\alpha^2\varphi_{sj}(y)=\beta_j \tag{9}$$

Where

$$\alpha=\sqrt{\frac{2\eta}{t_{Si}^2}} \text{ and } \beta_j=-\frac{qN_i}{\varepsilon_{Si}}-\alpha^2(V_{gs}-V_{fb})$$

From the above equation, the general solution of the surface potential is expressed as

$$\varphi_{sj}(y)=A_je^{\alpha y}+B_je^{-\alpha y}-\frac{\beta_j}{\alpha^2} \tag{10}$$

(j=1, 2, 3 for region 1, 2 and 3 respectively)

The boundary conditions of the potential at the source end and the drain end of the channel are given as

$$\varphi_{s1}(0)=\frac{kT}{q}\ln\left(\frac{N_{source}}{n_i}\right) \tag{11}$$

$$\varphi_{s3}(0)=\frac{kT}{q}\ln\left(\frac{N_{drain}}{n_i}\right)+V_{ds} \tag{12}$$

Where k is the Boltzmann constant, T is the room temperature, q is the electronic charge, N_{source} is the source doping concentration, n_i is the intrinsic concentration, and N_{drain} is the drain doping concentration. The continuity of surface potential and electric field in the interface of 3 regions holds and its corresponding boundary conditions are given as [14],

$$\varphi_{sj}(x,L_j)=\varphi_{sj+1}(x,L_{j+1}),\ \text{(j=1, 2)} \tag{13}$$

$$\frac{d\varphi_{sj}(x,y)}{dy}\Big|_{y=L_j}=\frac{d\varphi_{sj+1}(x,y)}{dy}\Big|_{y=L_j}\ \text{(j=1,2)} \tag{14}$$

By using the conditions (11) to (14) in (10), the constants A_j and B_j are determined for each region R_1, R_2, and R_3. The vertical electric field and lateral electric field are expressed as

$$E_{xj}(x,y)=a_{j1}(y)+2a_{j3}(y)x \tag{15}$$

$$E_{yj}(x,y)=\alpha(A_j e^{\alpha y}-B_j e^{-\alpha y}) \tag{16}$$

In the next section, we compare the surface potential, electric field and energy level of symmetric halo-doped DG-TFET and simple TFET. The variations of each parameter in the halo-doped regions are clearly shown.

3. Results and Discussion

We have compared our model results with the simulated data [13] to establish validity of our model. Our analytical results are in excellent agreement with the simulated data in the undoped channel region, and just vary in the halo doped region of the channel. It confirms the accuracy of our model. The source region is heavily doped with acceptor atom and its doping concentration of $5*10^{20}$ cm^{-3}. The doping concentration of drain region is kept lower at 10^{18} cm^{-3} to reduce the ambipolarity effect.

The halo doping is done in the channel region near both source and drain regions but the length of the halo regions is kept symmetrical. The length of halo regions is varied from 5 nm to 20 nm and compared to verify the better performance.

Also the doping concentration of the halo regions is varied asymmetrically on both sides to compare the performance for various doping. The length of the halo regions is kept equal and doping concentrations have been kept unequal since the surface potential of the device depending mostly on the doping concentrations than the length of the halo regions.

The surface potential of simple TFET and halo doped TFET are comparatively shown in Fig 2 applying V_{GS} from 0 to 1.2 with steps of 0.4 V. The surface potential of halo doped TFET increases rapidly than that of the simple TFET and remains above the intrinsic region of the simple TFET. The surface potential in the intrinsic region of the halo doped TFET (our model) and simple TFET matches exactly.

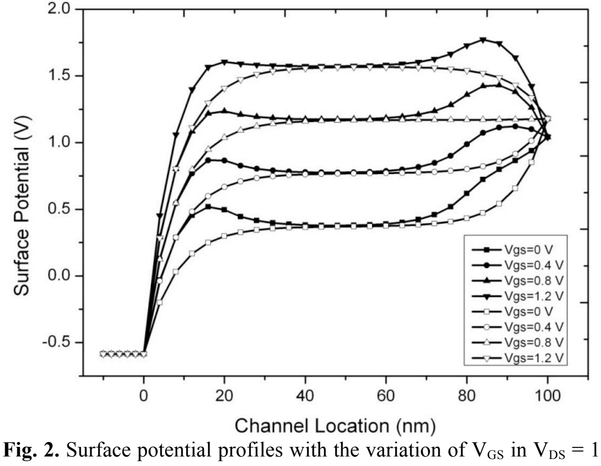

Fig. 2. Surface potential profiles with the variation of V_{GS} in V_{DS} = 1 V (L_g=100 m).

Due to the increase in surface potential the minimum surface potential will occur soon before that of the simple TFET. This results in the decrease of the threshold voltage. The lateral electric field (E_y) of TFETs is comparatively shown in Fig 3 with V_{GS} is 0 and 1.2 V. The electric field of the halo doped TFET at the Source-Channel junction is more than that of the simple TFET. it is less at the drain-channel junction than the simple TFET and equal in the intrinsic region.

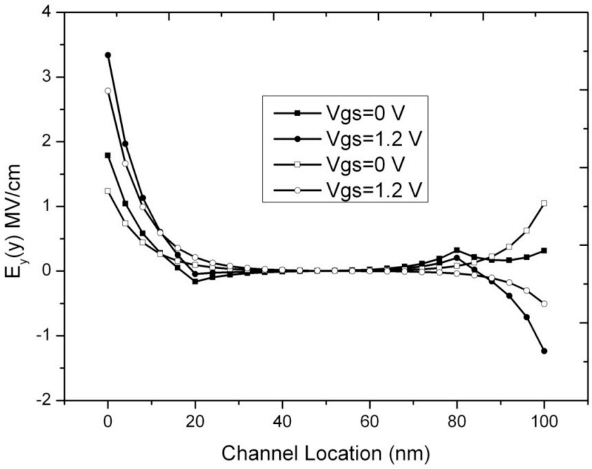

Fig. 3. Lateral Electric Field with the variation of V_{GS} in V_{DS} = 1 V (L_g=100 nm).

Due to increased electric field in the source-channel junction, the ON current will be improved, and decreased electric field in the drain-channel junction will decrease the ambipolarity of the device. The vertical electric field (E_x) and the electric field intensity $|E|=\sqrt{(E_x+E_y)}$ of both TFETs are comparatively shown in Fig 4 and Fig 5 respectively. The electric field deviation of the halo doped TFET is clearly visible from the figures.The energy band diagram of the halo doped TFET and simple TFET for ON state (V_{GS}=0) and OFF state (V_{GS}=1. 2) are comparatively shown in Fig 6.The energy level near source-channel junction and drain-channel junction of the halo doped TFET is reduced below that of the simple TFET. This improves the ON current of the device and reduces the ambipolar leakage respectively. Also we notice that energy level at the drain-channel junction is below that of the drain region of halo doped TFET due to the reduced doping concentration of drain region. This confirms the reduction of leakage current of the proposed structure.

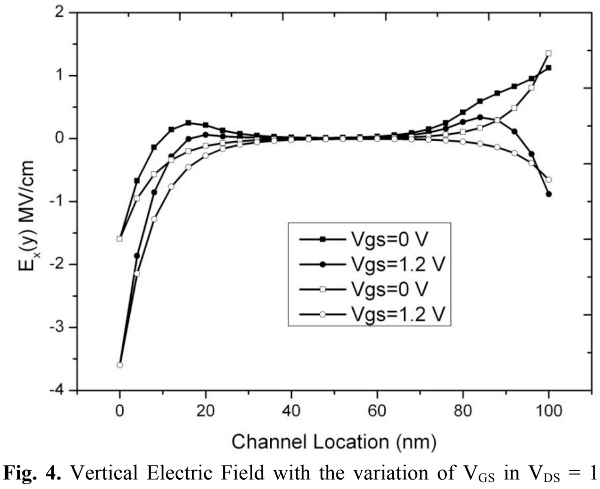

Fig. 4. Vertical Electric Field with the variation of V_{GS} in V_{DS} = 1 V (L_g=100 nm).

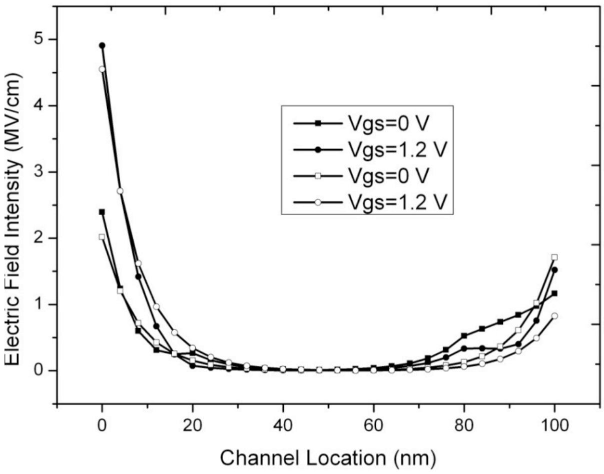

Fig. 5. Electric field intensity with the variation of V_{GS} in V_{DS} = 1 V (L_g=100 nm).

3.1. Optimization of Halo (Length)

The dependency of the surface potential and energy band on the length of the halo region can be studied by varying the halo length from 5 to 20 nm. The surface potential of the halo doped TFET for various halo lengths is compared with the simple TFET in Fig 7. The potential in the halo doped region is higher than that of the intrinsic region.

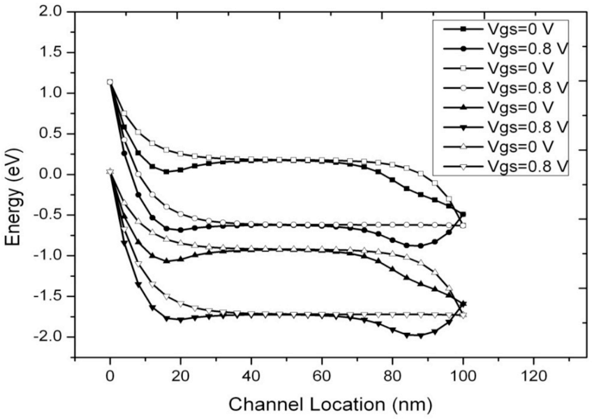

Fig. 6. Effect of HALO doping on the energy band diagram for ON (V_{GS}=1.2 V) and OFF (VGS=0) conditions with V_{DS}=0.8 V.

We can see that the potential decreases with the decrease in the halo length. However if the halo length is increased beyond 20 nm, the carrier transit time will increase due to scattering.

The energy band diagram of the halo doped TFET for various halo lengths is compared with the simple TFET in Fig 8. The energy level in the halo region of the halo doped TFET merges with the simple TFET if the halo length is reduced below 10 nm. But if the halo length increased beyond 20 nm, the band bending also increases rapidly and results in the increased leakage current.

So the halo length of 15 nm can be kept at optimum to optimize the surface potential and energy levels.

3.2. Optimization of Halo (Doping)

The dependency of surface potential, electric field and energy band diagram on the doping concentration of the halo doping can be studied by varying the doping concentration on both halo region from 10^{17} to 10^{19} and comparing it with the simple TFET.

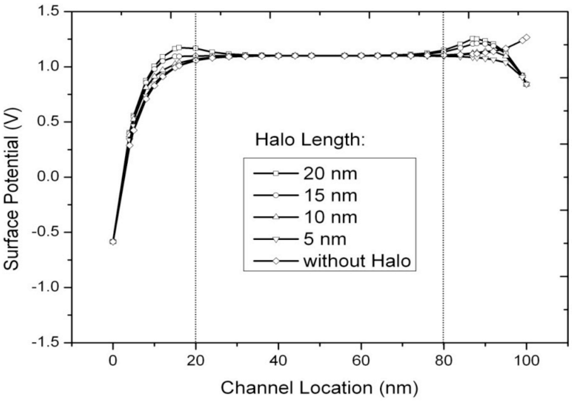

Fig. 7. Surface potential profiles varying the length of the halo region with V_{GS}=1.2 V and V_{DS}=1 V

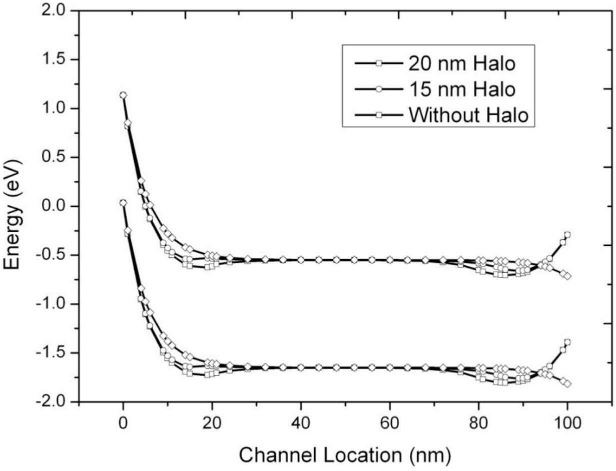

Fig. 8. Energy band diagram varying the length of the halo with V_{GS}=1.2 V and V_{DS}=1 V.

The surface potential of the halo doped TFET with various halo doping concentrations is compared with that simple TFET in Fig 9. The surface potential increases with an increase in the doping concentration. If the doping concentration is increased beyond $5*10^{18}$ cm^{-3}, the carrier transit time will increase similarly due to scattering. The lateral electric field of the halo doped TFET with various doping concentrations is compared with that of the simple TFET in Fig 10.

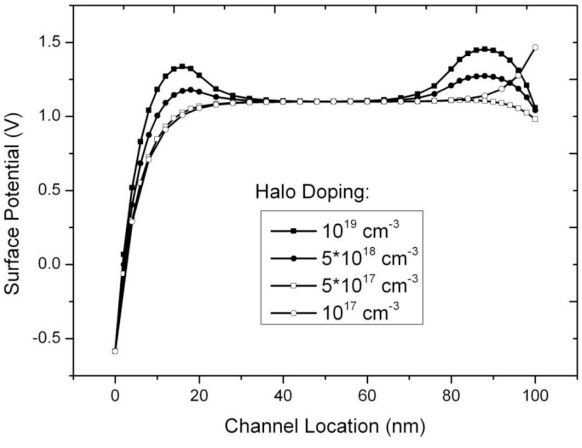

Fig.9. Surface potential profiles varying the doping concentration of the halo region with V_{GS}=1.2 V and V_{DS}=1 V.

If the electric field of the channel is increasing rapidly along the channel, generation of hot electrons will occur and increases the carrier transit time.

The energy band diagram of the halo doped TFET with various halo doping concentrations is compared with the simple TFET in Fig 11. The energy level in the halo region of the halo doped TFET merges with the simple TFET if the halo doping concentration is reduced below 10^{18}cm^{-3}.But if the halo doping concentration increased beyond 10^{19} cm^{-3} leakage currents also increase along with the ON current. So the halo doping concentration should be kept optimum say $5*10^{18}$ cm^{-3} to achieve better I_{ON}/I_{OFF} ratio.

3.3. Scaling

It is familiar that Tunnel FET exhibit less SCEs than the conventional MOSFET. However if the channel length of the device is reduced below 50 nm, it exhibits SCEs such as increased subthreshold swing and DIBL [15].

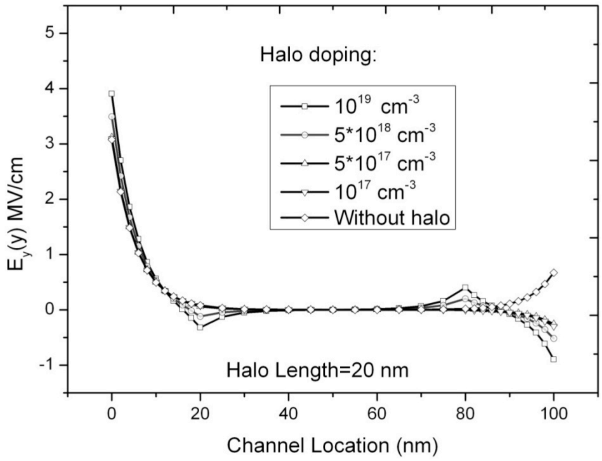

Fig. 10. Lateral Electric Field with the variation of doping concentration of the halo region with V_{GS}=1.2V and V_{DS}=1V

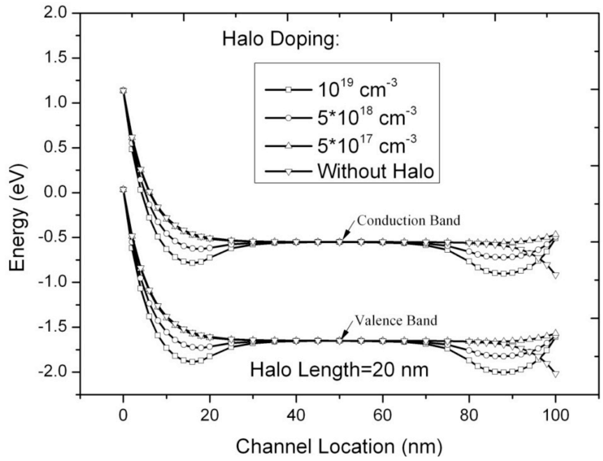

Fig. 11. Energy band diagram varying the doping concentration of the halo region with V_{GS}=1.2 V and V_{DS}=1 V

Voltage also starts playing a major role affecting the whole channel region. The variations of surface potential for the channel length of 50 nm and 20 nm are shown in Fig 12 and 13 respectively. In Fig 12 it is clearly visible that the surface potential varies rapidly in the whole channel region and it is evident that electric field intensity becomes higher than the long channel device.

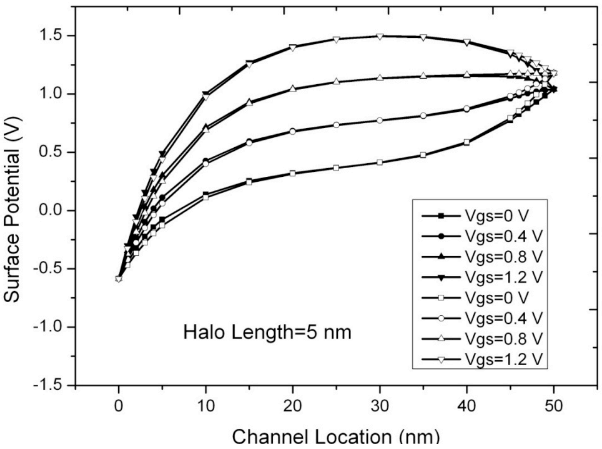

Fig. 12. Surface potential profiles with the variation of V_{GS} in V_{DS} = 1 V (L_g=50 nm).

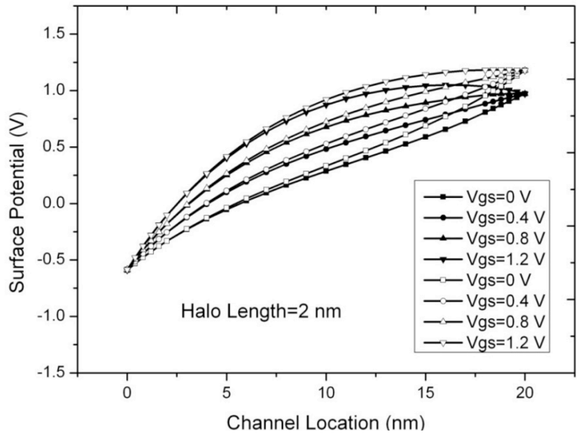

Fig. 13. Surface potential profiles with the variation of V_{GS} in V_{DS} = 1 V (L_g=20 nm).

To study the SCEs of symmetric halo doped TFET, we have calculated drain-induced electric field variations. It is defined as [16]

$$\Delta E_y(x,y) = E_y(V_{DS} = V_{DD}) - E_y(V_{DS} = 0) \tag{17}$$

$$\Delta E_x(x,y) = E_x(V_{DS} = V_{DD}) - E_x(V_{DS} = 0) \tag{18}$$

where V_{DD} is the operating voltage. The drain-induced electric field variability is calculated at the surface of the source-channel interface i.e., $\Delta E_y(0,0)$ and it is plotted for various channel Length in Fig 14. The parameter $\Delta E_x(0,0)$ is zero at this surface.

From Fig 14, we can see that when channel length is reduced below 50 nm, this parameter increases over the entire channel region i.e., the V_{DS} takes control over the device. Due to this effect I_{off} increases rapidly.

Simultaneously subthreshold swing is also increased degrading the basic advantage of tunnel FET. The reason for this degradation is that for short channel device the gate voltage losses control in the channel region. To maintain the gate control for the short channel device, high-k dielectric can be used. [13].

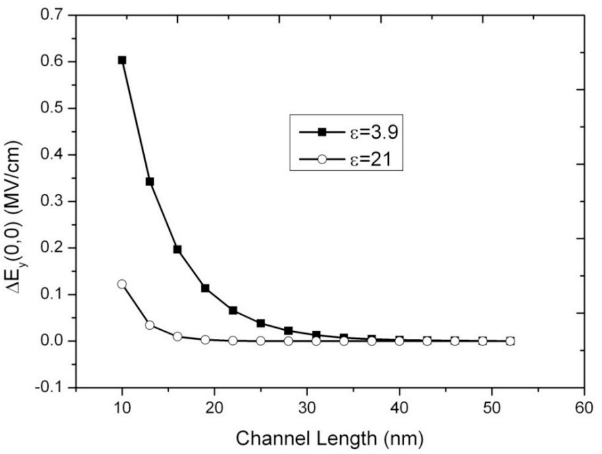

Fig. 14. $\Delta E_y(0,0)$ vs. Channel Length graph

In Fig 14, we have compared the parameter $\Delta E_y(0,0)$ of the device for $\varepsilon = 3.9$ and $\varepsilon = 21$. For low-k dielectric $\Delta E_y(0,0)$ increases rapidly when channel length is decreased and for high-k dielectric this parameter is much reduced and thus gate voltage can take control over the channel region.

4. Conclusions

In this work, an analytical model for halo doped DG-Tunnel FET has been developed. Some important parameters like surface potential, electric field and Energy band diagram are analyzed with various halo doping concentrations and for various lengths of halo region. The proposed model indicates that halo doping near source-channel junction and drain-channel junction will improve the ON current and reduces the OFF current by reducing energy levels respectively. So we can achieve better I_{ON}/I_{OFF} ratio. Further the scaling property of halo doped Tunnel FET structure is also discussed.

References

1. W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, “Tunnelling field-effect transistors (TFETs) with sub threshold swing (SS) less than 60 mV/dec,” *IEEE Electron Device Lett., vol. 28, no. 8, pp. 743–745, Aug. 2007.*
2. Krishnamohan, Tejas, Donghyun Kim; Raghunathan, Shyam; K. Saraswat, “Double-Gate Strained-Ge Heterostructure Tunnelling FET (TFET) with record high drive currents and ≪60mV/dec sub threshold slope”, *Electron Devices Meeting, 2008. IEDM 2008. IEEE International., pages 1 – 3.*
3. Kathy Boucart and Adrian Mihai Ionescu, “Double-Gate Tunnel FET with High-κ Gate Dielectric”, *IEEE Transactions on Electron Devices, VOL 54, NO 7, July 2007.*
4. M. T. Björk, J. Knoch, H. Schmid, H. Riel, and W. Riess, “Silicon nanowire tunnelling field-effect transistors”, *Applied Physics Letters , Volume 92, Issue 19.*
5. Peng-Fei Guo, Li-Tao Yang, Yue Yang, Lu Fan, Gen-Quan Han, Ganesh S. Samudra, and Yee-Chia Yeo, “Tunnelling Field-Effect Transistor: Effect of Strain and Temperature on Tunnelling Current”, *IEEE Electron Device Letters, vol. 30, NO. 9, September 2009.*
6. Hraziia, Andrei Vladimirescu, Amara Amara, Costin Anghel, “An analysis on the ambipolar current in Si double-gate tunnel FETs”, *Solid-State Electronics Volume 70, April 2012, Pages 67–72.*
7. Woo Young Choi, and Woojun Lee, “Hetero-Gate-Dielectric Field-Effect Transistors”, *IEEE Transaction on Electron Devices, vol. 57, NO. 9, September 2010.*
8. Brinda Bhowmick and Srimanta Baishya, “An Analytical Model for Fringing Capacitance in Double gate Hetero Tunnel FET and Analysis of effect of Traps and Oxide charges on Fringing Capacitance”, *International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012.*
9. Costin Anghel, Hraziia, Anju Gupta, Amara Amara, and Andrei Vladimirescu, “30-nm Tunnel FET With Improved Performance and Reduced Ambipolar Current”, *IEEE Transaction on Electron Devices, vol. 58, NO. 6, June 2011.*
10. Rakhi Narang, Manoj Saxena, R. S. Gupta, and Mridula Gupta, “Assessment of Ambipolar Behavior of a Tunnel FET and Influence of Structural Modifications”, *Journal of Semiconductor Technology and Science, vol.12, NO.4, December, 2012.*
11. Abhijit Mallik and Avik Chattopadhyay, “Drain-Dependence of Tunnel Field-Effect Transistor Characteristics: The Role of the Channel”, *IEEE Transaction on Electron Devices, vol. 58, NO. 12, December 2011.*
12. Jung-Shik Jang and Woo Young Choi, “Ambipolarity Factor of Tunneling Field-Effect Transistors (TFETs)”, *Journal of Semiconductor Technology and Science, vol.11, NO.4, December, 2011.*
13. Marie Garcia Bardon, Herc P. Neves, Robert Puers and Chris Van Hoof, “Pseudo-Two-Dimensional Model for Double-Gate Tunnel FETs Considering the Junctions Depletion Regions”, *IEEE Transaction on Electron Devices, vol. 57, NO. 4, April 2010.*
14. Binit Syamal, Chayanika Bose, C. K. Sarkar and N. Mohankumar, “Effect of Single HALO Doped Channel in Tunnel FETs: A 2-D Modeling Study”, *2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*
15. Joerg Appenzeller, Joachim Knoch, Mikael T. Björk, Heike Riel, Heinz Schmid, and Walter Riess, “Toward Nanowire Electronics”, *IEEE Transaction on Electron Devices, vol. 55, NO. 11, November 2008.*
16. Min Jin Lee, Woo Young Choi, “Analytical model of single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs)”, *Solid-State Electronics 63 (2011) 110–114.*