Test and Measurement Challenges for 3D IC Development

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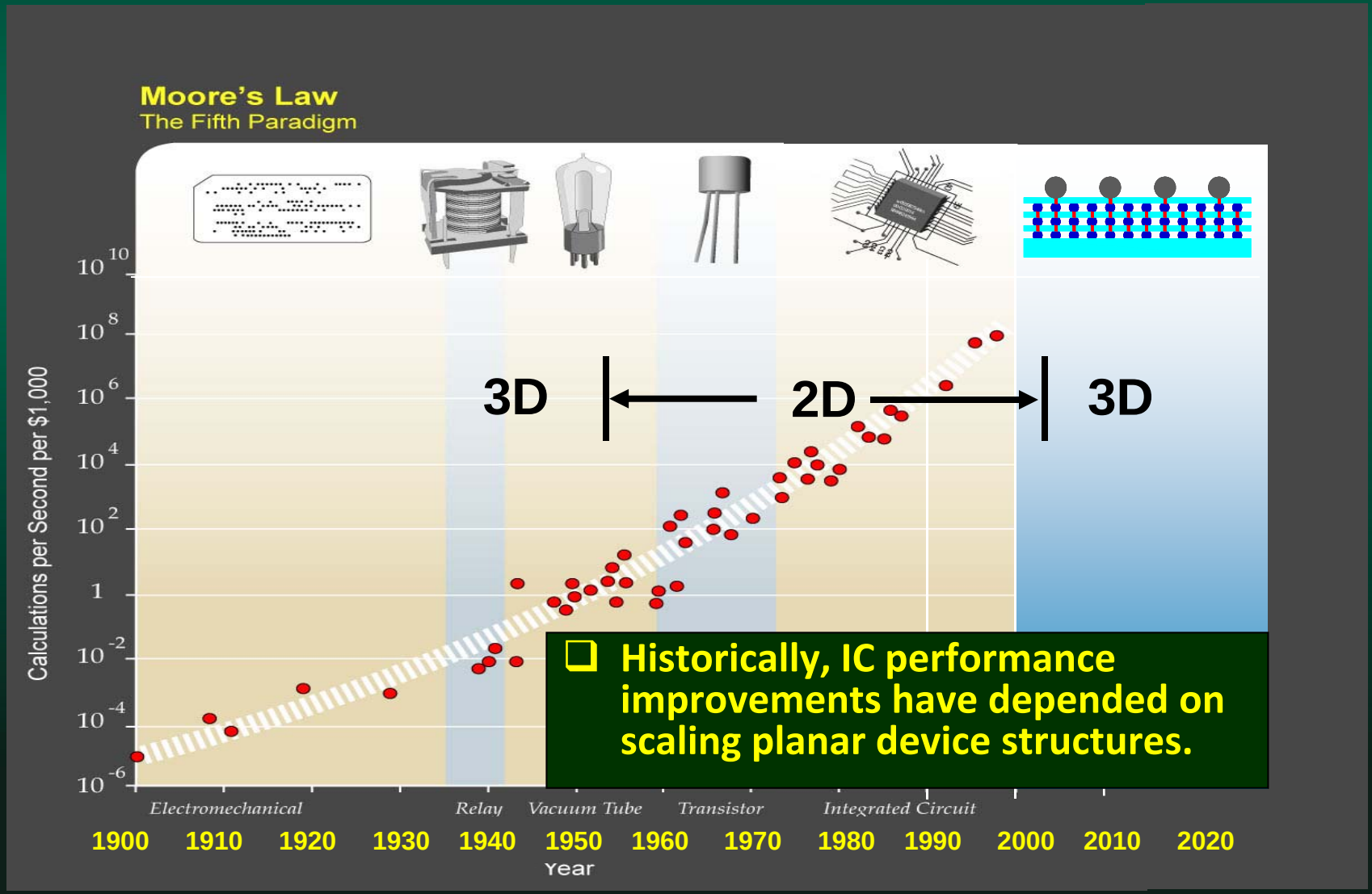
- **Probing**
  - Jerry Broz

Outline

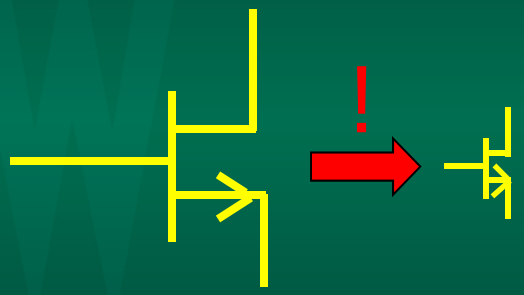
- **Motivation For 3D Integration**
- **3D Technology**
- **3D Test in a Research Environment**
  - Instrumentation
  - Supporting Test at Different Stages in The Build
  - Probing Challenges
  - Probe Over Active for KGD Screen
  - Diced Chip Test
- **Conclusions**

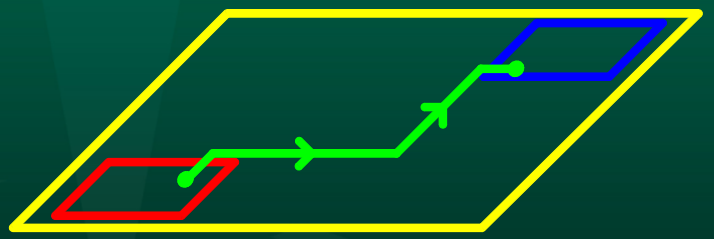
Moore's Law

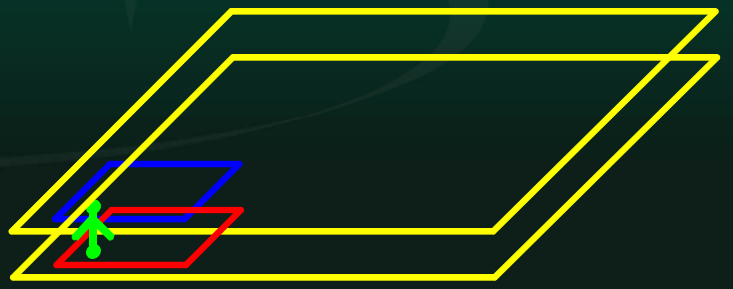

Moore's Law
The Fifth Paradigm
Calculations per Second per $1,000
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
1
10^{-2}
10^{-4}
10^{-6}
3D
2D
3D
Historically, IC performance improvements have depended on scaling planar device structures.
Electromechanical
Relay
Vacuum Tube
Transistor
Integrated Circuit
1900
1910
1920
1930
1940
1950
1960
1970
1980
1990
2000
2010
2020
Year

Why 3D?

- **Scaling of transistors and other circuit elements is becoming more difficult.**
  - Approaching fundamental physical limitations on device size.
- **Interconnect latency is beginning to limit IC performance.**
  - Vertical connections allow shorter connections (50 μm vs. 10 mm).
  - Expansion of numbers of interconnects through compact vertical connections.
- **Easier to include disparate technologies.**
  - Logic, EDRAM, opto-electronics, non-silicon based…





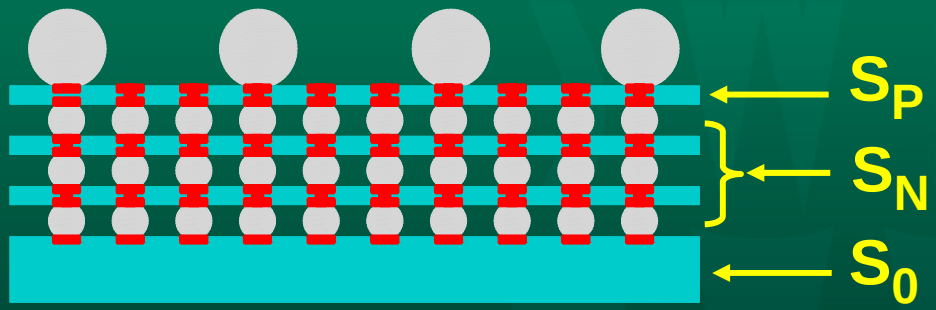


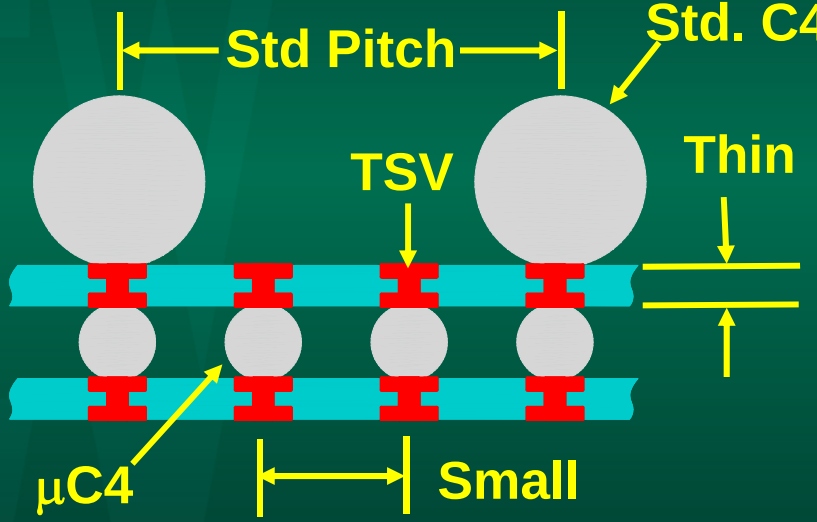
Challenges For 3D Integrated Circuits

- **Design**
  - Timing analysis, clocking.
  - DFT.
- **Process**
  - Functionality / yield at single stratum.
  - Characterization of 3D building blocks (TSV, bonding process).
- **Test**
  - Definition of test points: Where and what to set, KGD strategy.
  - How to test, ***probing.***

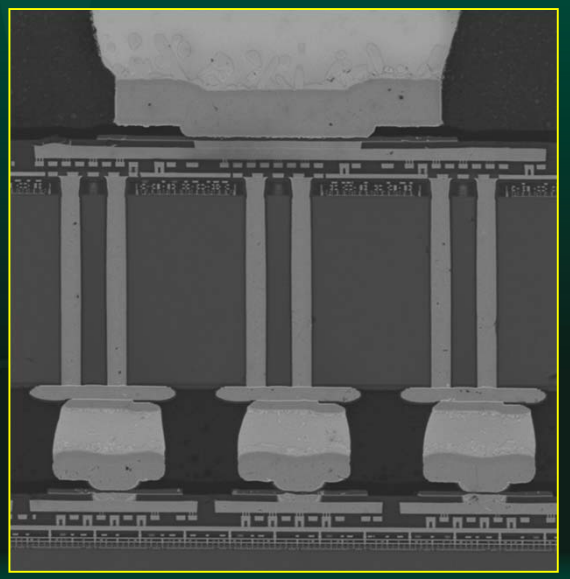
3D Technology Test Site

Stacked Chip Nomenclature



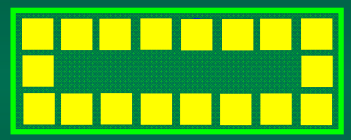


- Face to back stacking scheme.
- Cu TSV on small pitch, μ–C4 inter-strata interconnect.
- Package pitch Std C4 for package interconnect and final SP layer probing.

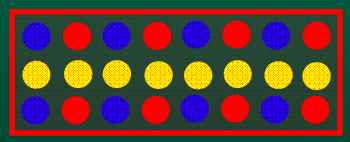


Test Site Probing

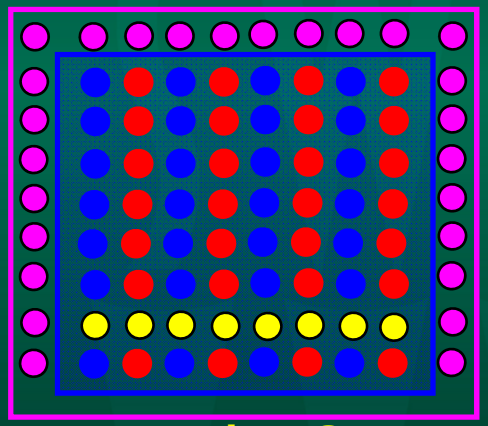
Reticule



Design A

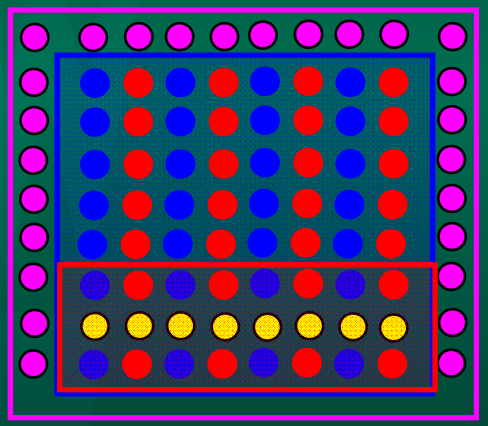


Design B



Design C

Area Array Probe Image

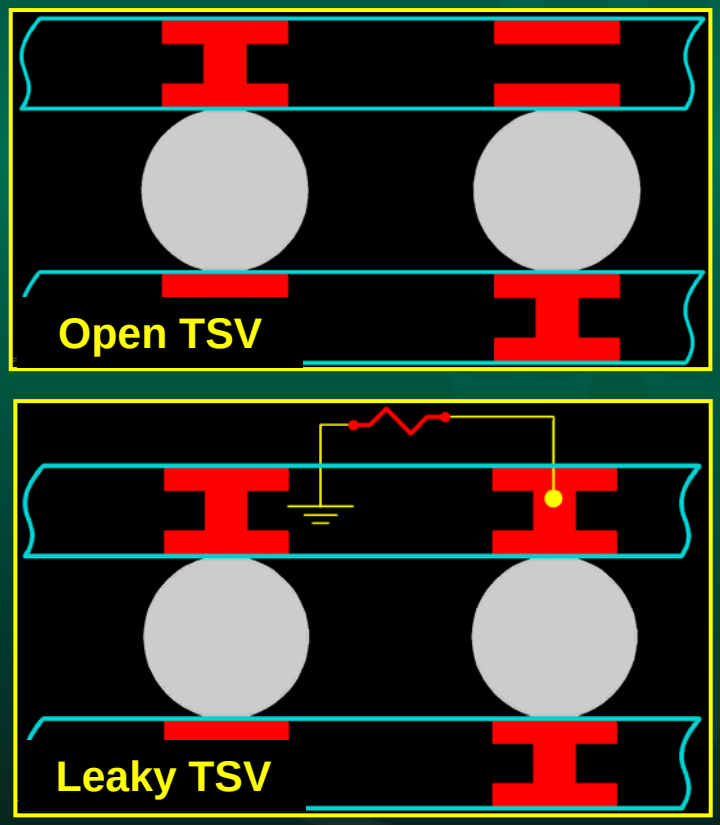


- Design “A”, pad cage macros, cantilever probes.
- Design “B”, “C”, area array probe set, need to support KGD for base and upper level die, parametric content on both designs.

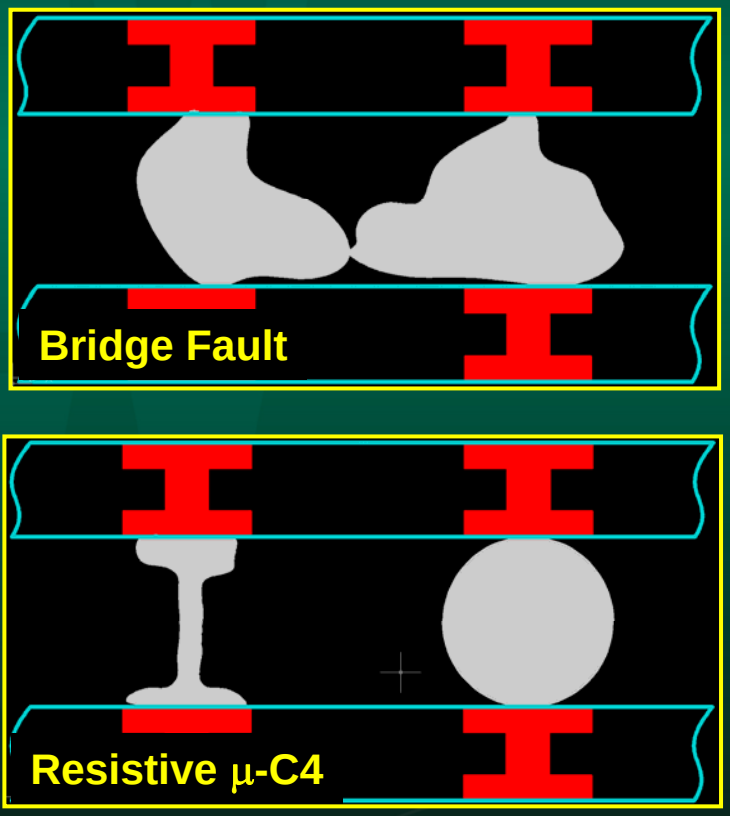
- Design “B ” & “C” images interleaved.
- Common package used for space transformer.
- Test set up changed by changing probe head.

3D Process Characterization

TSV Failure Modes



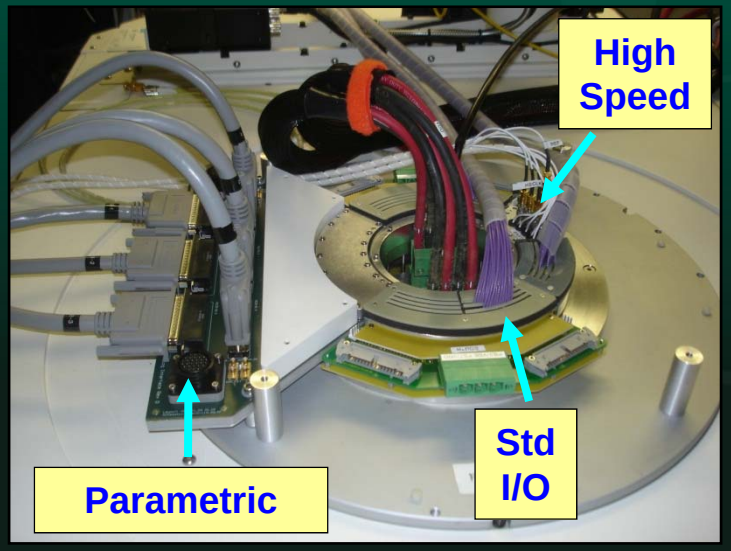
μ-C4 Failure Modes



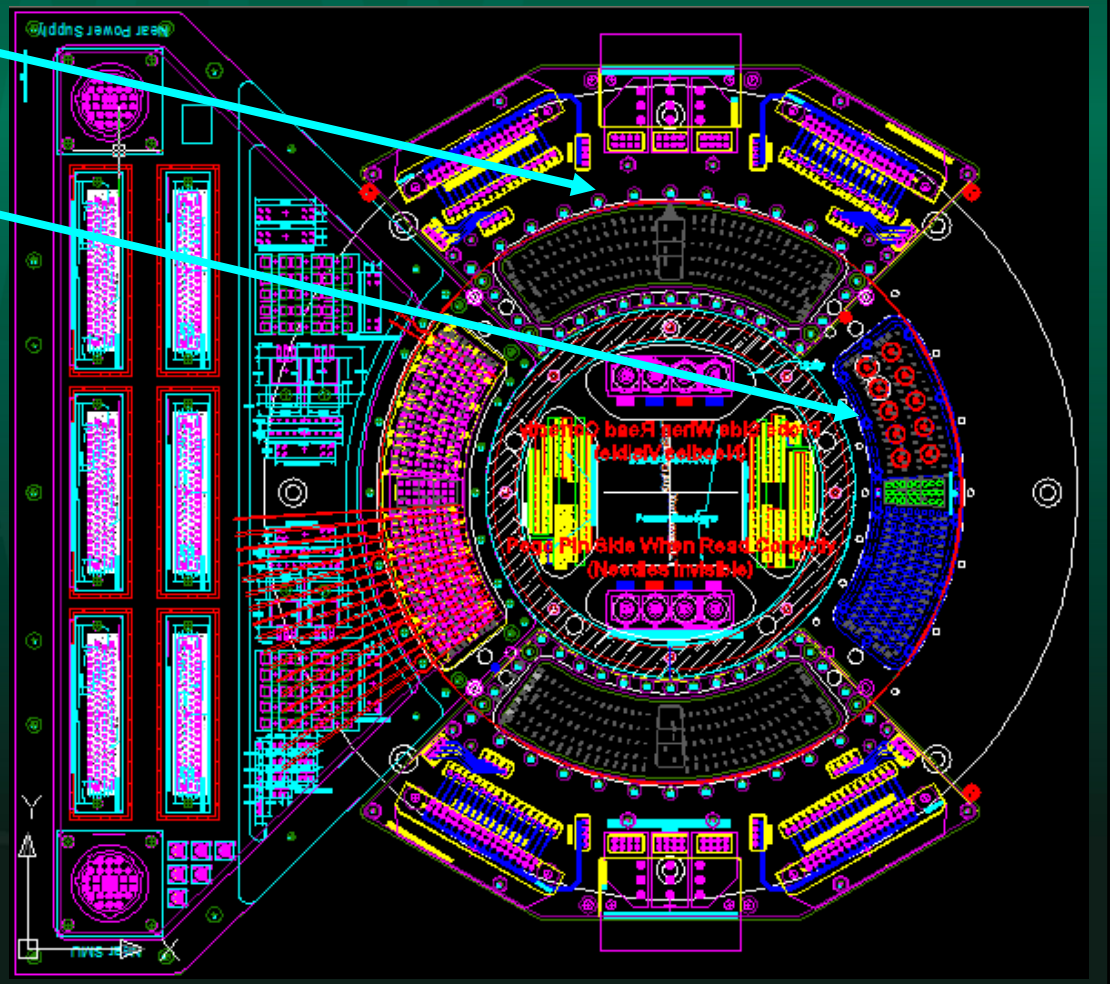
- 3D process characterization requires measuring resistances from 1mΩ ϒ 1GΩ *(>12 orders of magnitude*).
- True 4 point SMUs will be required to cover the low impedance range.

Interfacing To The Probe Card

- Cable-to-board signal modules
- Clock / 3 GHz Ports
- Parametric
  - Agilent 34980A interface for 2&4 point resistance measurements, leakage.

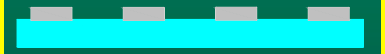
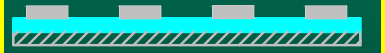
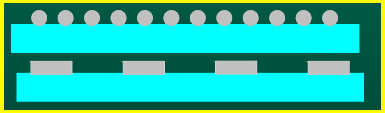
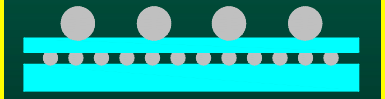
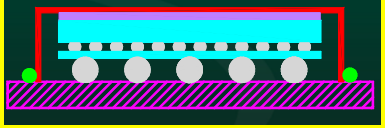


Modular Probe Interface



Test Points During Build

(Probe Options & Risk Assessment)

Build Level	VLSI	Technology	DUT
S_P (Thick)			
S_P (Thin)			
S_N			
Assembled, pre-packaged			
Assembled, packaged			

- Cantilever probes
- Pointed vertical, probe over active
- Flat vertical, chip tray
- No loss of yield observed
- PFA in progress
- Assumed OK

Single Stratum Probing Options

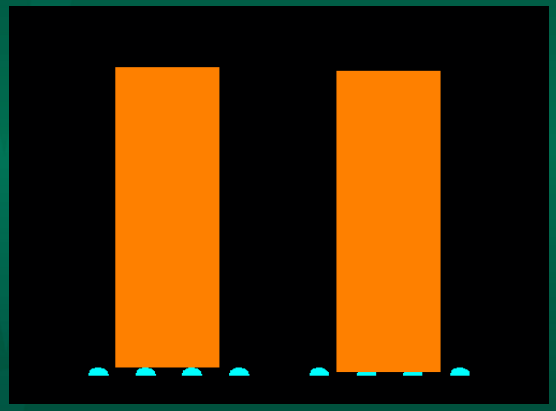
- **Single stratum test required:**
  - Design verification.
  - Known good die (KGD) prior to 3D stacking.
- **Current injection over full area of the chip for cache.**
- **Major issues for area array probing for single layer:**
  - No qualified probe technology for fine pitch uC4 probing.

➡ Drives choice to area array probe card, pointed probes contacting Al TD landing pads.

- **Areas of concern:**
  - Pad placement, where to probe.

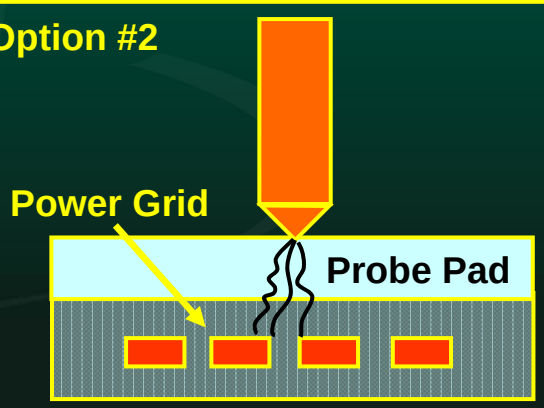
➡ **Damage introduced through probing process.**

Option #1



µC4 Cluster Probing, Flat Probes

Option #2

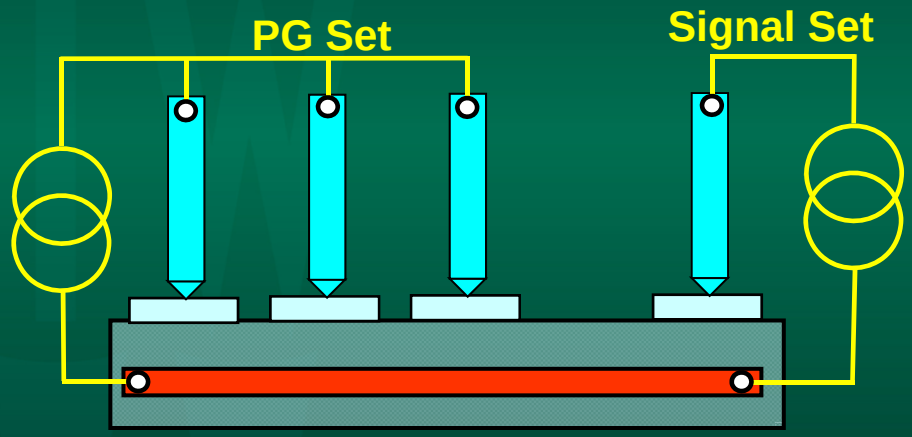


Al Pad Probing, Pointed Probes

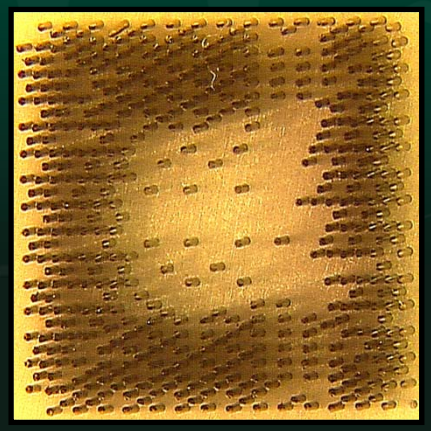
Probing / Damage Experiments: Test Vehicle

- **Top level film stacks similar to 3D test chips.**
- **Area array probe card used with 4/9 image.**
  - ~ 100 Power/ground contacts measured in parallel for leakage.
  - ~ 40 signal contacts measured individually.
  - ~ 100 sites probed/die.
- **Contactor**
  - 5 mil Palinaey-7 probe.
  - Probe tip diameter 10 μm
  - Overdrive 0-160 μm (0-6.5 mils).
- **Electrical leakage and SEM cross-sections evaluated after probing.**

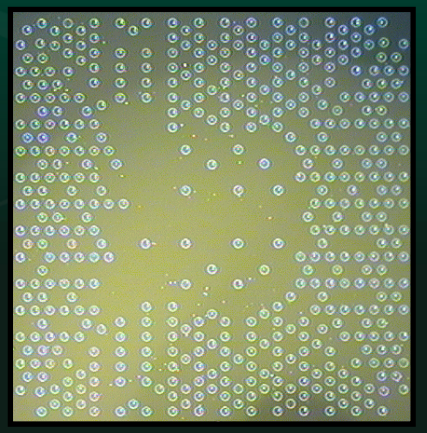
Electrical Set Up



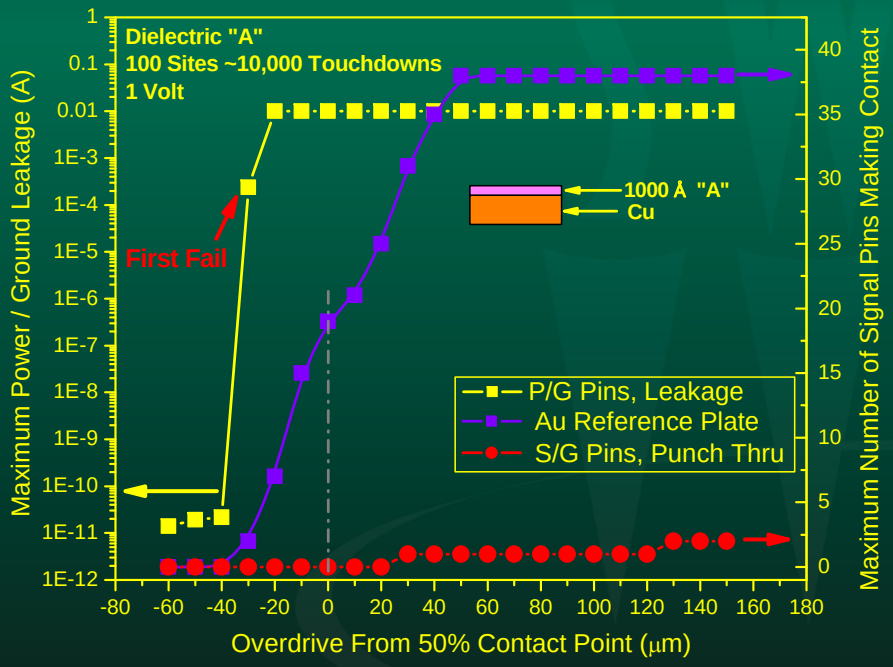
Probe Image

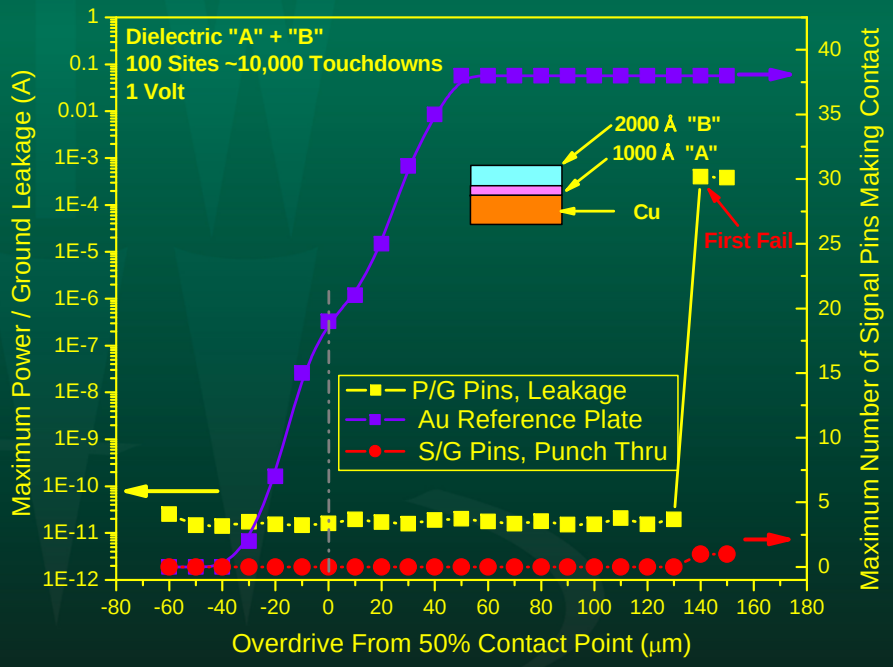


Test Vehicle



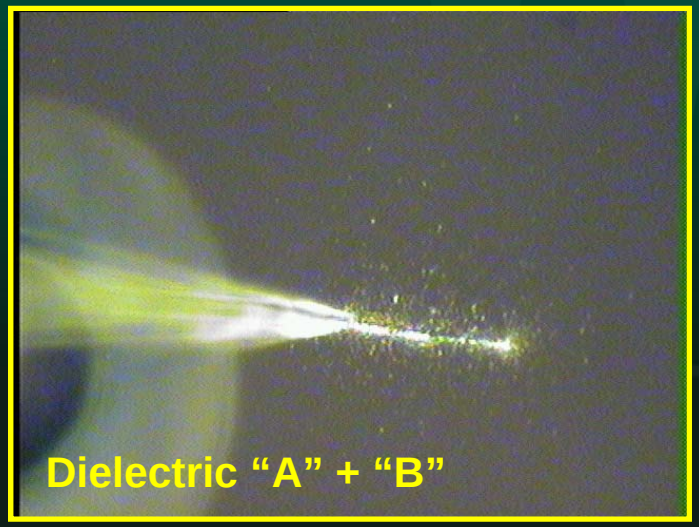
Probing / Damage Experiments: Test Vehicle Top Layer Dielectric Investigations





- Stack "A" dielectric fails at first probe contact.
- Stack "A" + "B" dielectric fails after 120 µm – 170 µm overdrive.

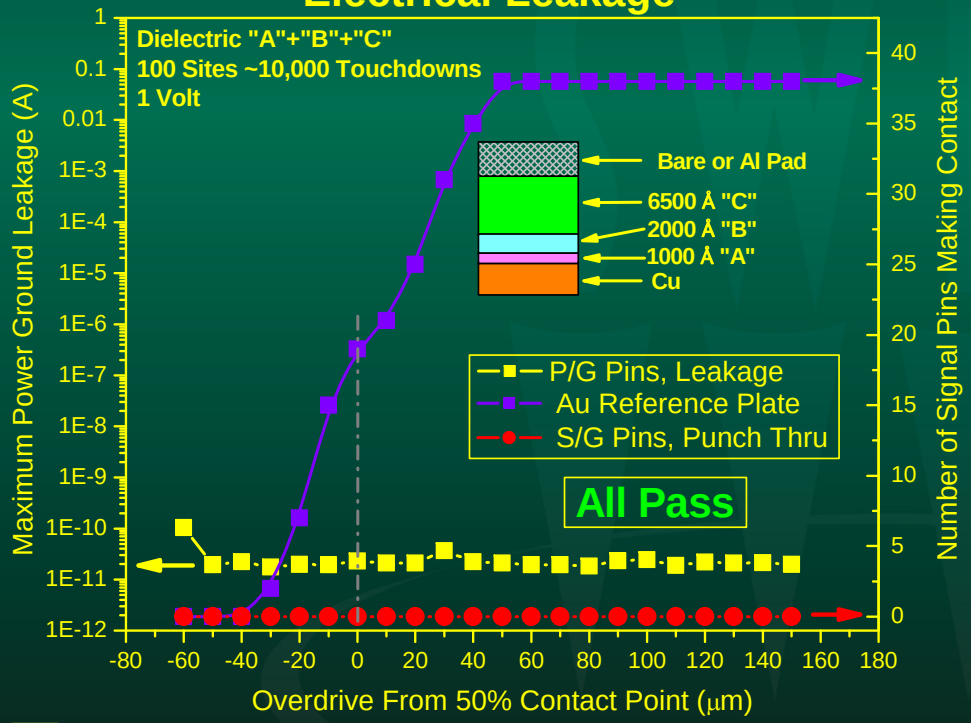
Probe Scratch Test



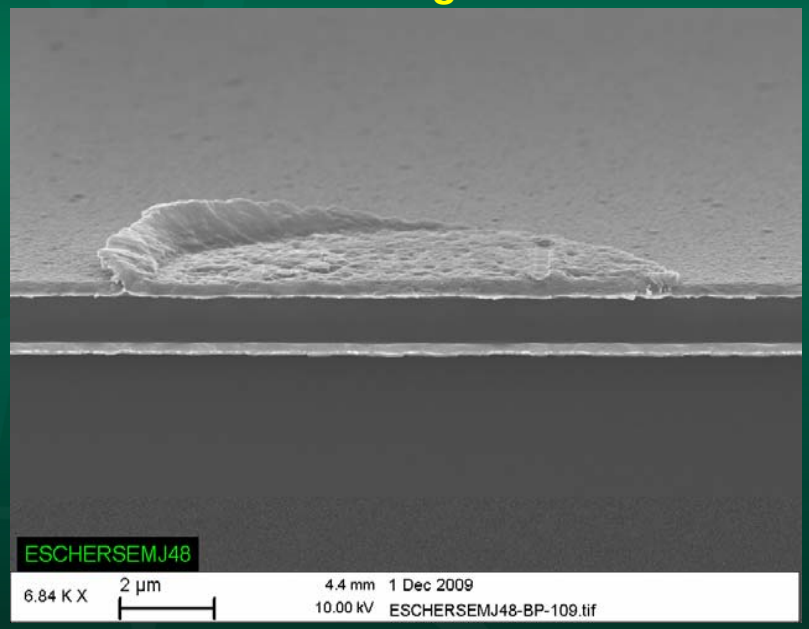
- Stack “A” dielectric fails with minimal probe scrub.
- Stack “A”+“B” fails at moderate probe force.
- Stack “A”+“B” +”C” shows no visual signs of failure, even with application of high probe force.

Probing / Damage Experiments: Test Vehicle Full Pad Stack

Electrical Leakage



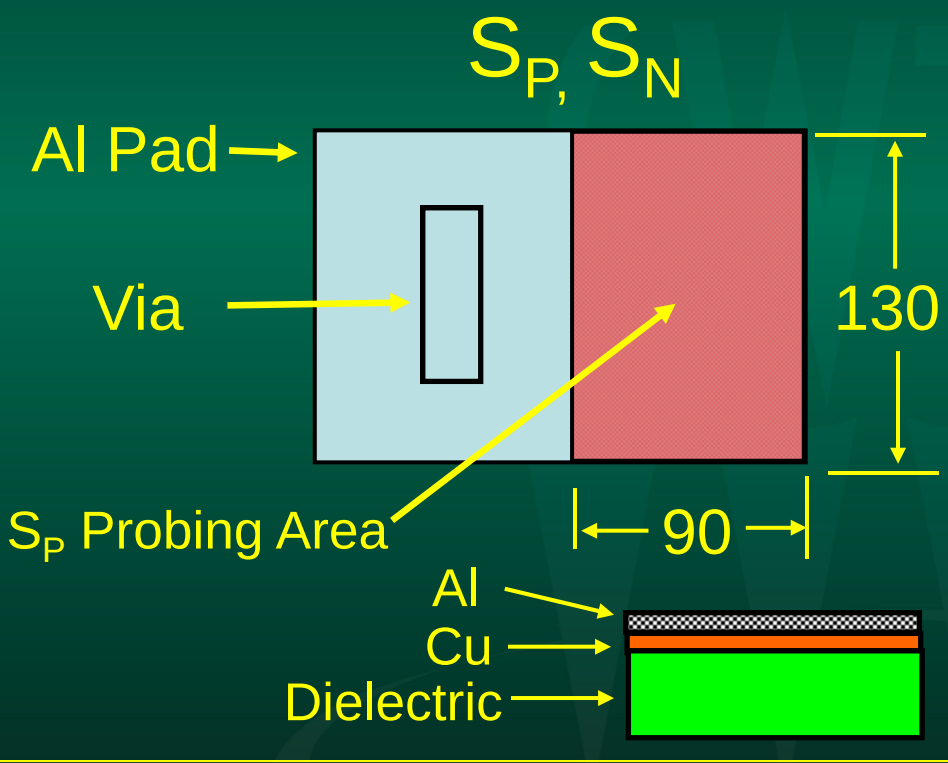
Film Stack Damage Assessment

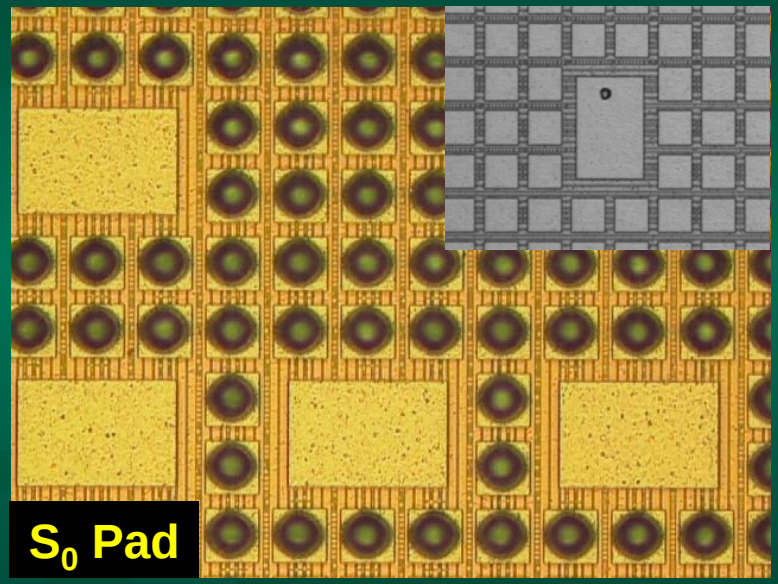


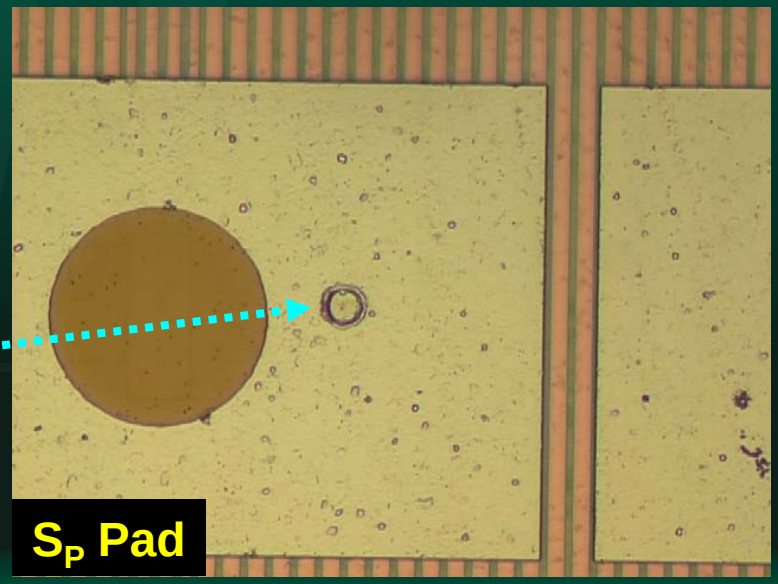
***N. B. J. Yorita, SWT 2004 !**

- Experiments done with and without Al pad layer.
- No fails observed for 10,000 probe/pad touchdowns.
- No observations of cracking from cross-sections*.

3D Test Site Probe Pads

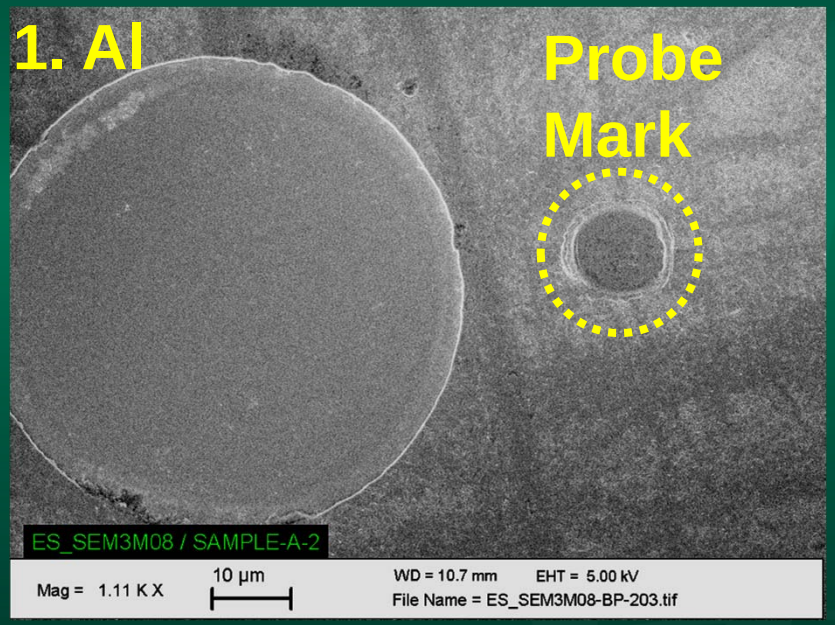


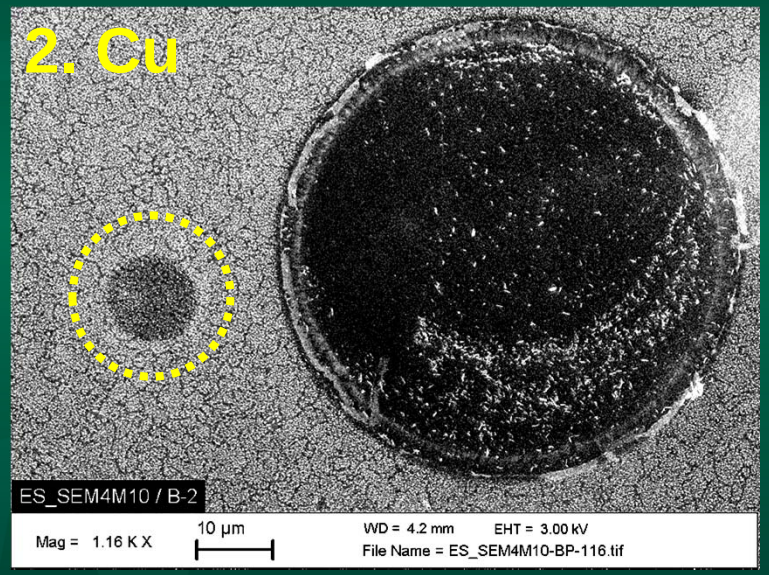


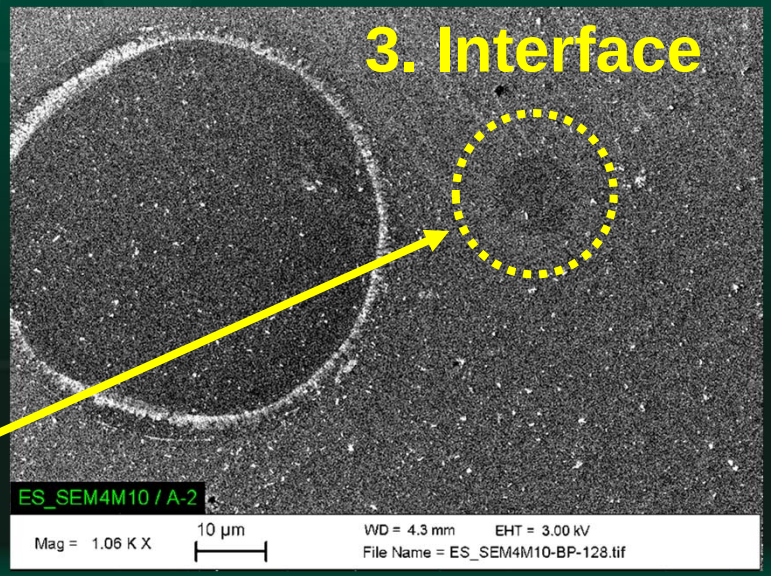


- S_n: No μ–C4 on probe pad, full pad available for probing.
- S_p: Std. C4 on each probe pad, probing zone offset from contact via / C4 attachment zone.
- 3 mil probes.

Top Down SEM on Pads

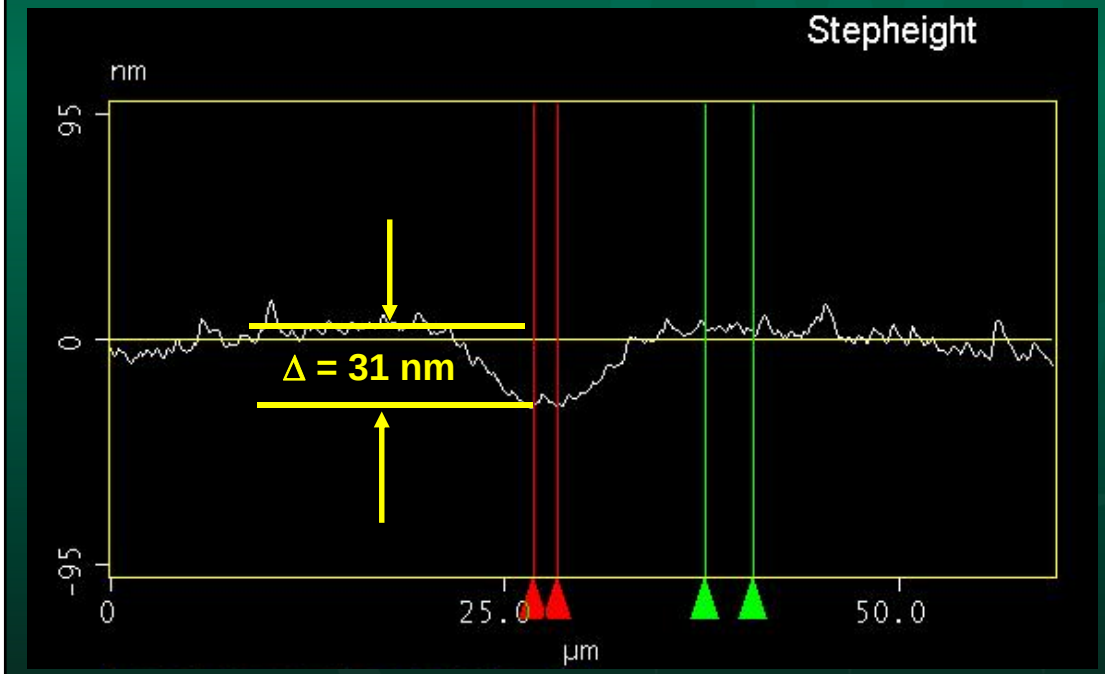


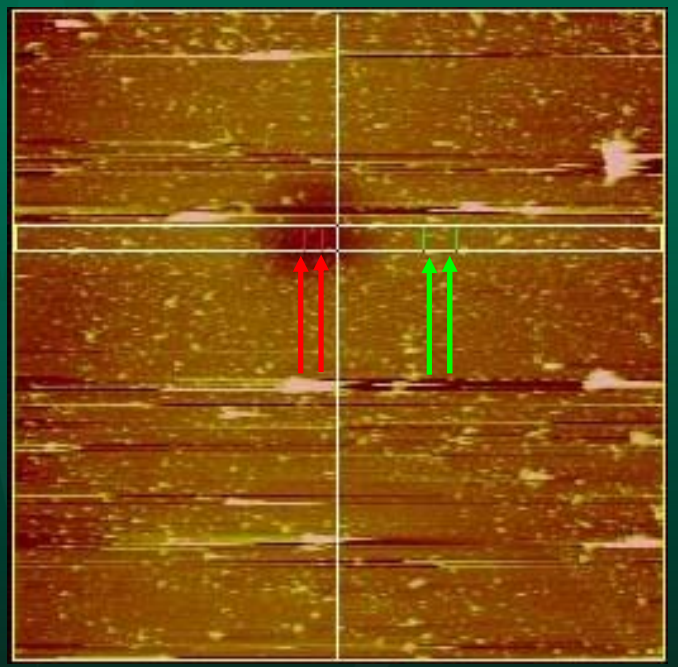




- Sequential etch of top pad metallization.
  1. Al/Cu/Dielectric.
  2. Cu/Dielectric.
  3. Adhesion Layer/Dielectric.
- Top down SEM reveals some disturbance of interfacial region.

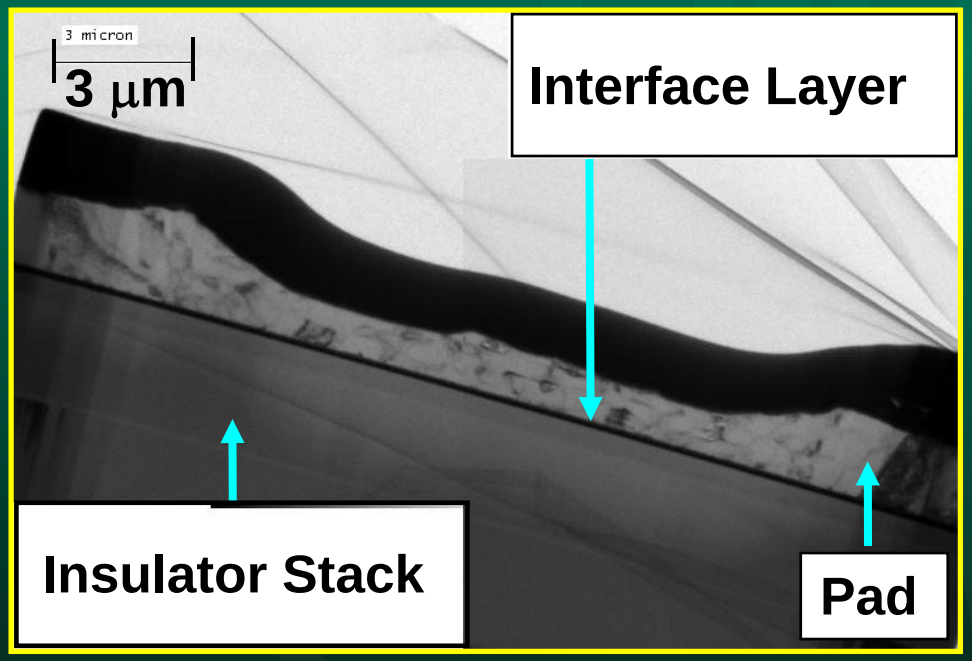
AFM On Probe Marks

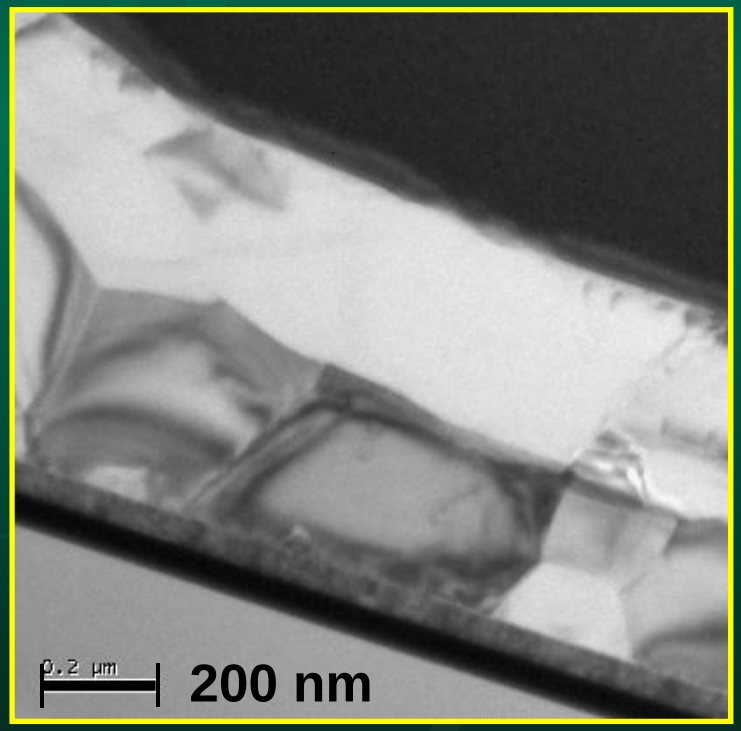




- AFM reveals 30 nm depression in top adhesion layer.

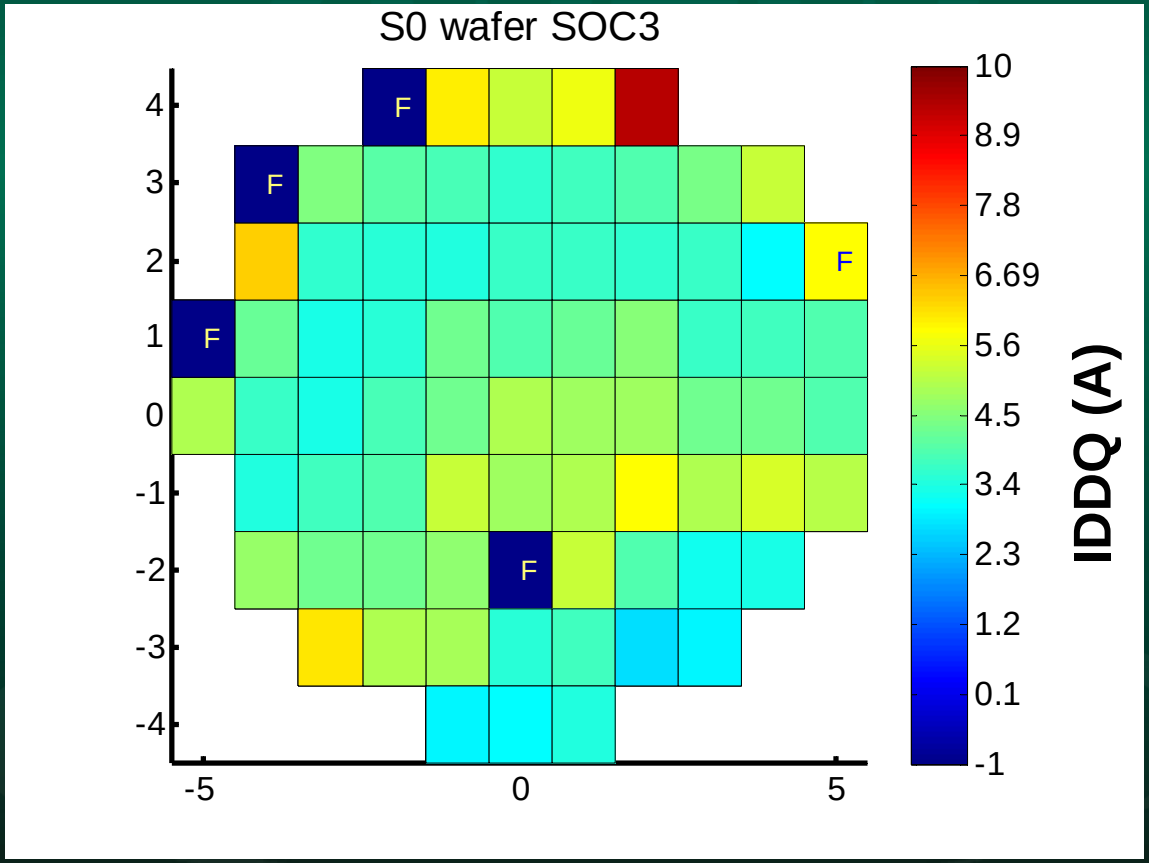
TEM Cross Sections on Probed Pads





- No evidence of damage or crack propagation in top insulating layer stack.

Screen Yield, Design "B", Using Probe Over Active

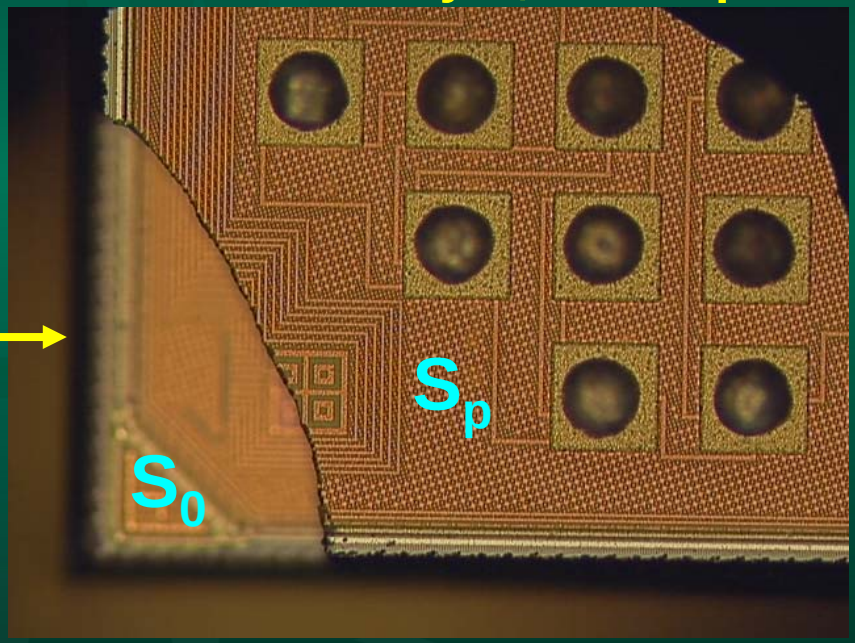


- Wafer screen data shows no increased yield fallout over standard C4 probing using pointed probe over active probing strategy.

Diced Chip Test

- In the research environment, we employed a chip to chip bonding strategy for 3D IC assembly.
- Supporting single die test of complex area array chips has always been problematic:
  - Vision systems in advanced probers not designed to work with single die efficiently.
  - Chip transfer to chuck requires attachment to handler wafer, with adhesive.
- 3D chip bonding process development greatly benefits from pre-packaged test:
  - Does the chip work, is it worth packaging?
  - Does the packaging process affect chip yield?
  - What does the chip look like visually after test?

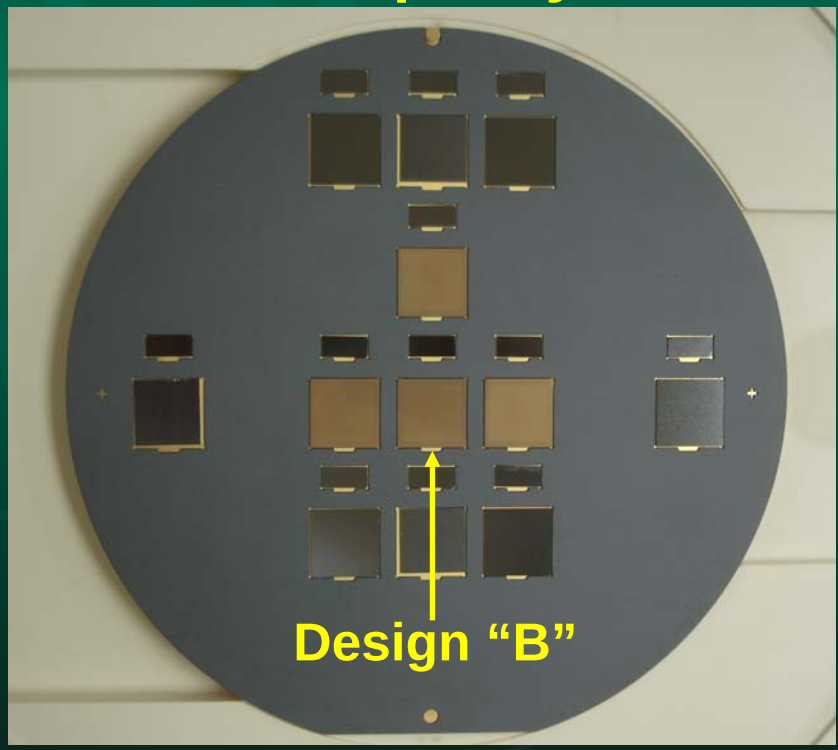
Double Layer, 3D Chip



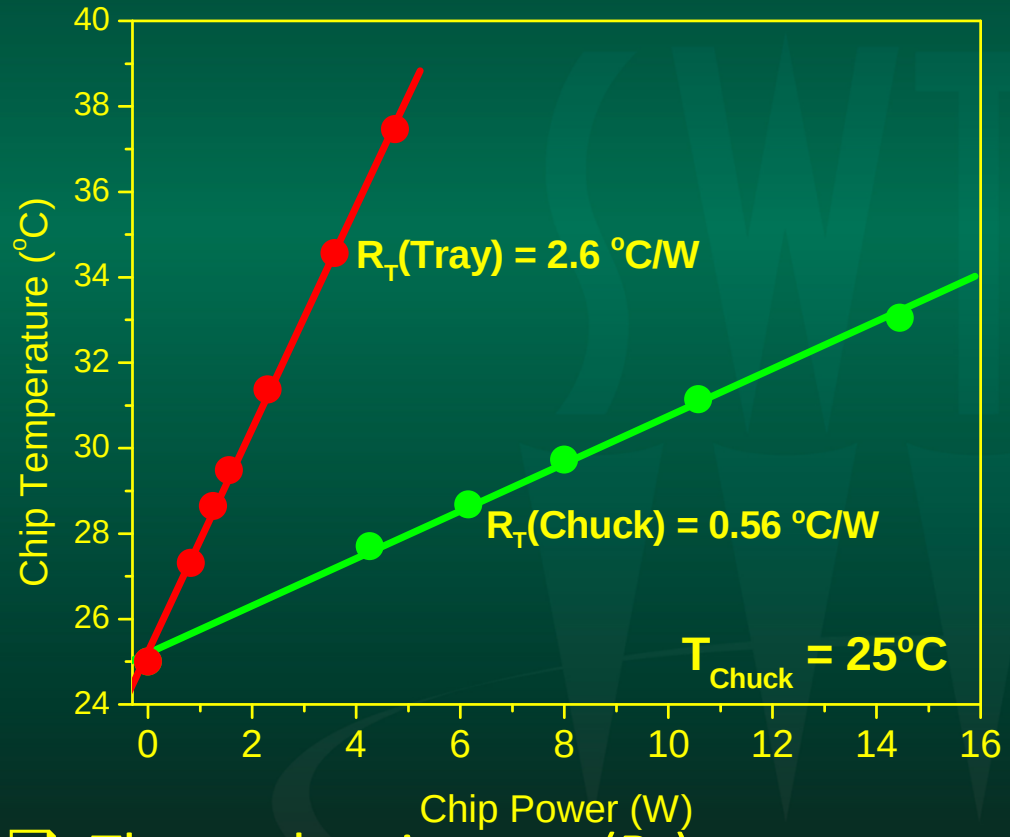
Diced Chip Tray

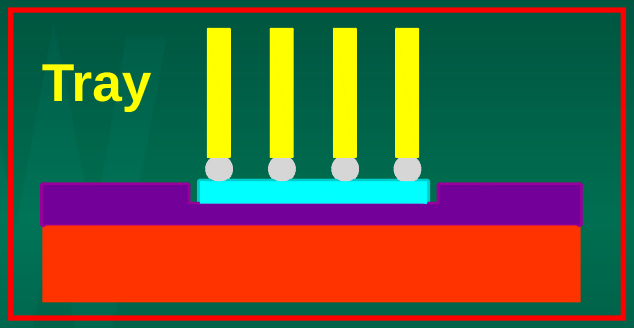
- TEL custom build chip tray for diced chip designs “B” &”C”.
- Clean, vacuum hold down technology which works with standard “Table Load” P12 wafer transfer procedure.
- Two piece design allows easily changing to another chip size, requires only replacing top guide.
- Alignment marks included for automated load, alignment and wafer scan.

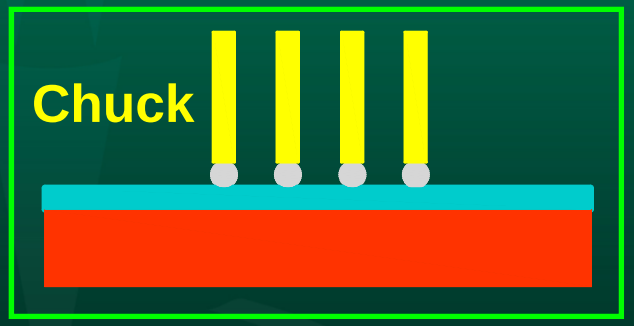
Chip Tray



Chip Tray Thermal Resistance







- Thermal resistance (R_T) measurements for chips in tray show resistance R_T ~4.6 x higher than measured with full wafer in contact with a Cu chuck.
- For VLSI designs “B” &”C”, no problem encountered in running low speed functional screen tests, or performance tests for brief periods.

Conclusions

- 3D introduces a number of new challenges in chip test, probing in particular.
- A hierarchical test strategy has proven essential in 3D bonding process development learning.
  - **Accessibility of test at all points in the build.**
  - **Access to on-board parametrics.**
  - **Ability to test diced, bonded chips, pre-packaged.**
- Fine pitch vertical probe/prober technology required to support current and future 3D fabrication technologies.