EE241 - Spring 2004
Advanced Digital Integrated Circuits

Borivoje Nikolic

Lecture 18
SOI Design
Power Distribution

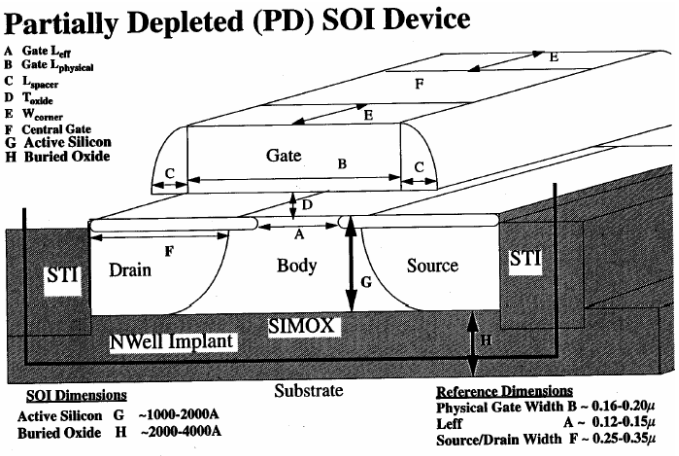
Announcements

- **Midterm project reports due tomorrow**
  - Please post links on your project web page
- **Homework #3 due after the Spring break**

Silicon on Insulator (SOI)

- **References:**
  - Chapter 5 by Shahidi, Assaderaghi, Antoniadis
  - K. Bernstein, N.J. Rohrer, "SOI Circuit Design Concepts," Kluwer 2000.
  - K. Bernstein, ISSCC'00 SOI Tutorial
  - 2001 Microprocessor Design Workshop, lectures by C.T Chuang and R. Preston
  - Articles from Chandrakasan/Brodersen, IEEE Press 1998.

SOI Transistor



Partially Depleted means channel inversion does not consume the entire body.

Bernstein, ISSCC'00

SOI Devices

- **Partially depleted (PD)**
  - Pros:
    - Easier to manufacture (Si thickness)
    - Scalable, tolerance to variations
    - Decoupling V_T from Si thickness
  - Cons:
    - Floating body effects: I-V kink, parasitic bipolar effect
- **Fully depleted (FD)**
  - Pros:
    - Significantly reduced floating body effects
    - Sharper subthreshold *S*
  - Cons:
    - V_T is a function of the charge in the body – varies
    - Manufacturability, compatibility with bulk CMOS

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Soi Microprocessors

Comp.	Processor	Freq.	Technology	Comment	Source
IBM	64b Power4	1.10 GHz	PD/SOI 0.08 um Leff, 7LM Cu		ISSCC 01
IBM	64b Power4 (Test Chip)	1.00 GHz	PD/SOI 0.08 um Leff, 7LM Cu		IEDM 99
IBM	64b Power4	1.00 GHz	PD/SOI 0.08 um Leff, 7LM Cu		Hot Chip 99 EE Times 99
IBM	64b PowerPC	660 MHz	PD/SOI 0.08 um Leff, 7LM Cu	Migration from 0.12 um Leff	ISSCC 00
IBM	64b PowerPC	550 MHz	PD/SOI 0.12 um Leff, 6LM Cu	Bulk 450 MHz 0.12 um Leff	ISSCC 99
IBM	32b PowerPC (PowerPC750)	580 MHz	PD/SOI 0.12 um Leff, 6LM Cu	Bulk 480 MHz 0.12 um Leff	ISSCC 99
Samsung	64b DEC Alpha	600 MHz	FD/SOI 0.25 um Lgate, 4LM Al	Bulk 433 MHz 0.35 um Lgate	ISSCC 99
DEC	StrongArm-110 (Core Only)	230 MHz (Tester Limit)	PD/SOI 0.35 um	20% Perf. Over Bulk	IEDM 97

From C.T. Chuang

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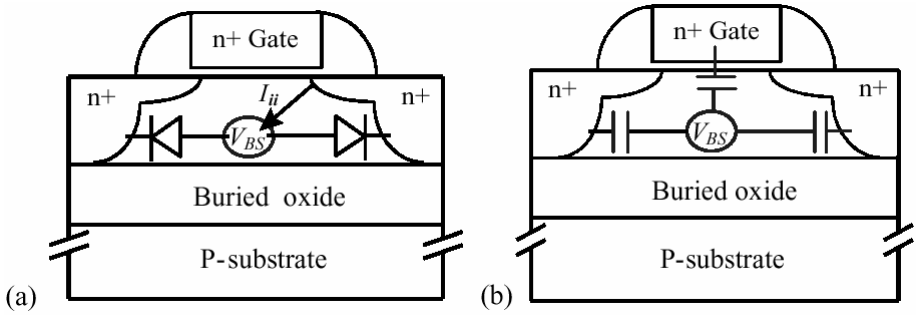
SOI Design

- **Advantages:**
  - Less Capacitance (~5-40%)
  - Lower power
  - Reduced effective V_T, short channel effects, body effect
  - Layout simplicity (no wells, plugs, …)
- **Disadvantages:**
  - History-dependent timing
  - Increased device leakage
  - Body effect issues
  - Self heating
  - Decoupling capacitance

SOI Timing Issues

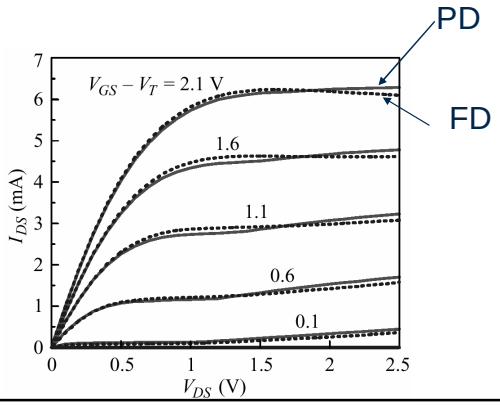


µs constants

ps constants

Floating Body Effects in PD SOI

- Neither S or D junction biased – body floats. Effects:
- Threshold Variability
- "Kink" in output characteristics



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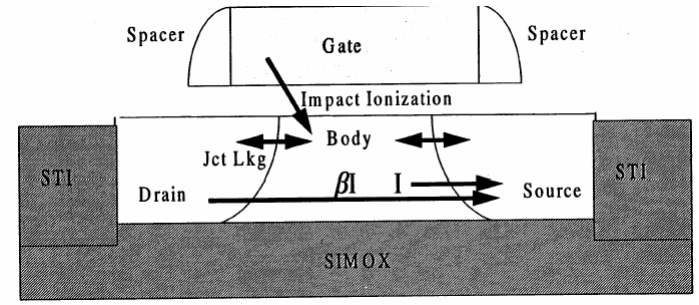
Floating Body Effects in PD SOI (cont'd)

- Parasitic Bipolar Transistor



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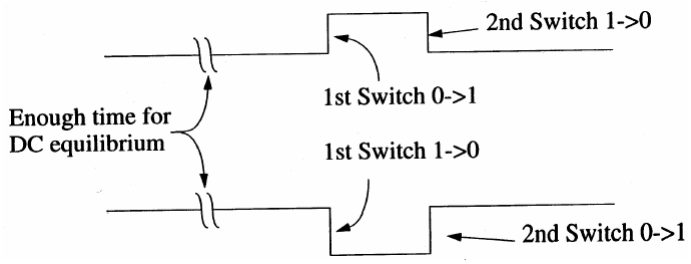
SOI Circuit Considerations

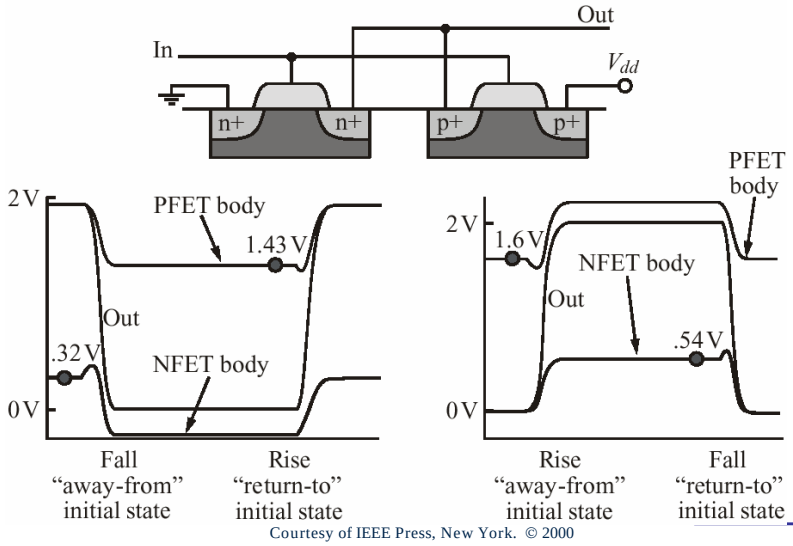
- **Static circuits – history-dependent delay**
- **First switch (often slowest) vs. second switch (often fastest)**



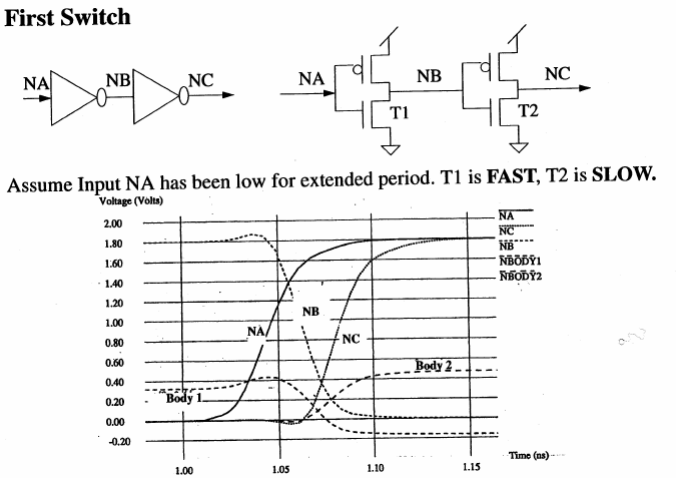
Initial State

- **Initial input at "low"**
  - nFET V_B determined by back-to-back diodes
  - pFET V_B at V_{DD} initially
  - pFET V_B before input falling transition determined by capacitive coupling
- **Initial input at "high"**
  - nFET V_B at GND initially
  - nFET V_B before input rising transition determined by capacitive coupling
  - pFET V_B determined by back-to-back diodes

First Two Transitions

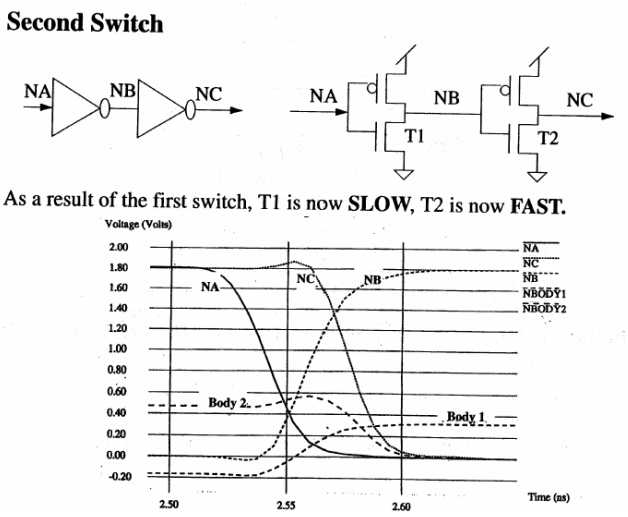


History-Dependent Delay



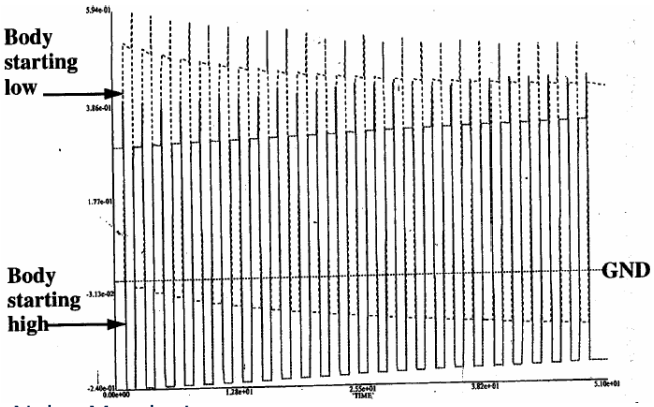
Bernstein, ISSCC'00

History-Dependent Delay



History-Dependent Delay

Convergence to steady state



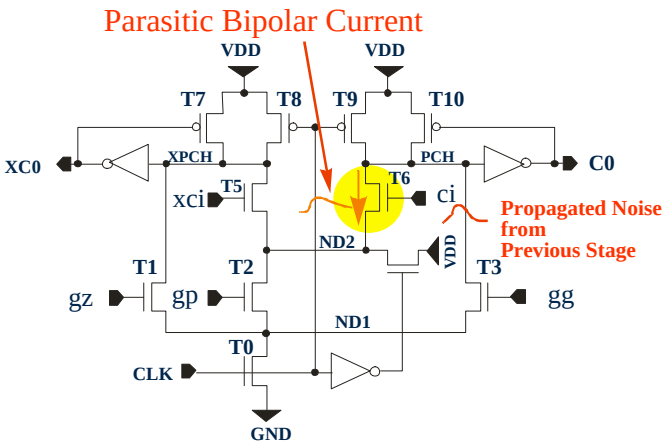
Noise Margins!

Dynamic Circuits in SOI

- Dynamic History
- Bipolar effect
- Less charge sharing

Parasitic Bipolar

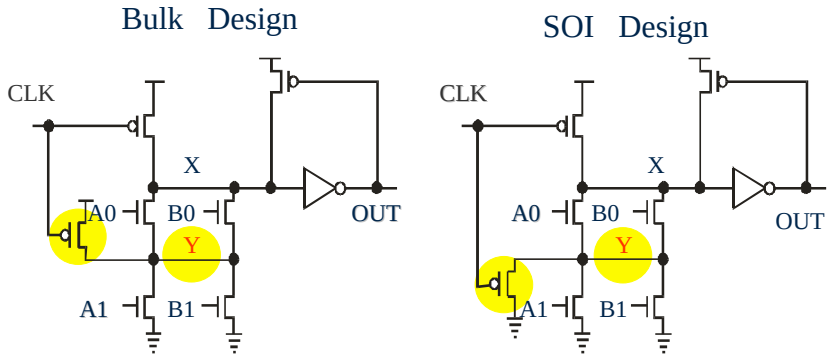
Dynamic lookahead adder
Cumulative Effect of Parasitic Bipolar Current and Propagated Noise Cause Data Corruption after 3rd Stage in The Chain



C.T. Chuang (M. Canada et al., ISSCC, 1999)

Pre-discharging Nodes

Intermediate nodes discharged to prevent parasitic bipolar effect



C.T. Chuang (D. H. Allen et al., ISSCC, 1999)

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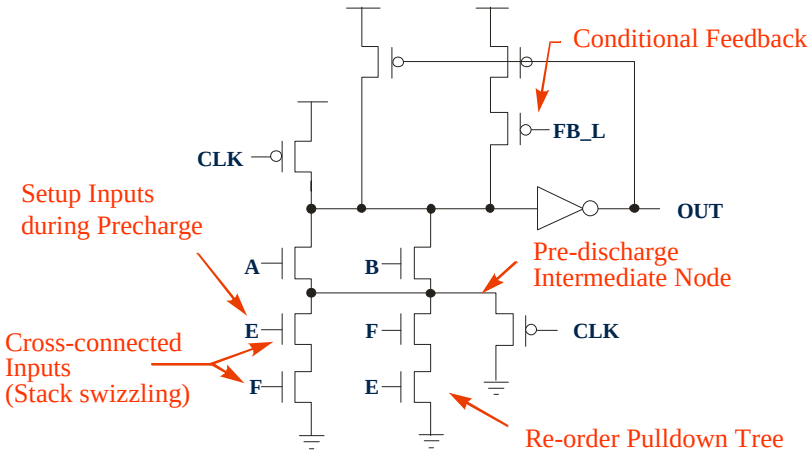
Dynamic Circuit Techniques



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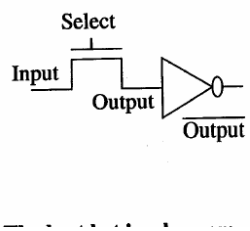
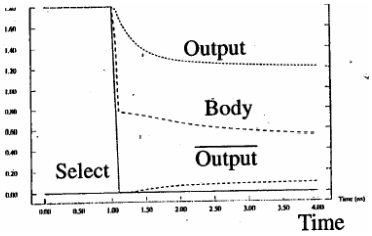
C.T. Chuang (D. H. Allen et al., ISSCC, 1999)

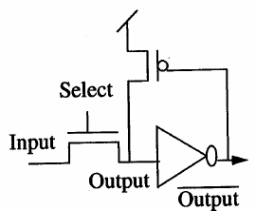
Pass-Transistor Logic in SOI

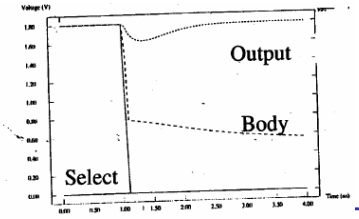
Inverter:





Keeper:





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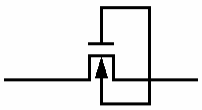
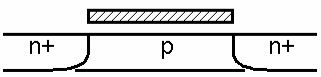
PTL in SOI

Body - gate connected MOS (SOI) (Assaderaghi 94): DTMOS



V_g low -> no body effect, low V_{T0}

V_g high -> forward bias, V_T reduces



voltage range limited by the forward biasing of the pn+ junctions

max V = ±0.8V

Example: V_T = 0.4V at 0 V; 0.17V at 0.5 V

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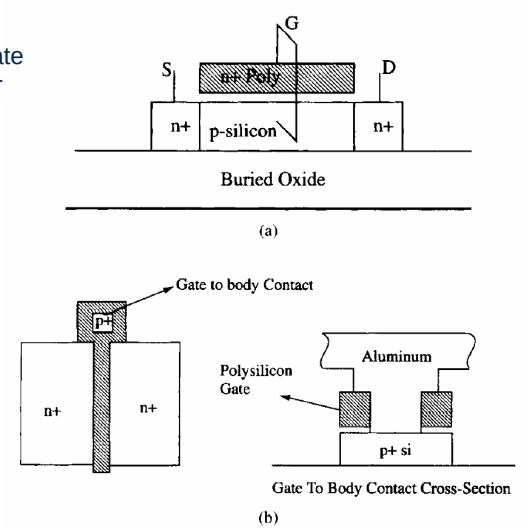
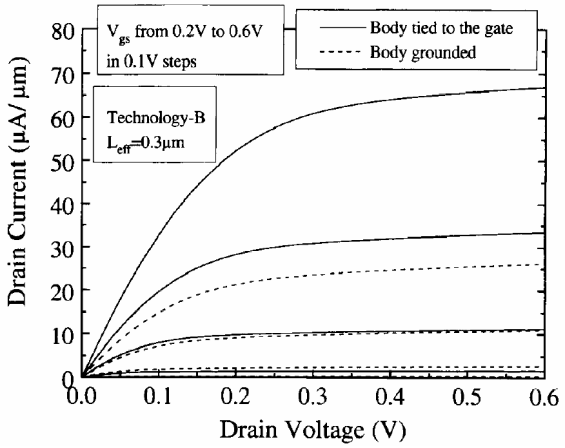
DTMOS

Body and gate tied together

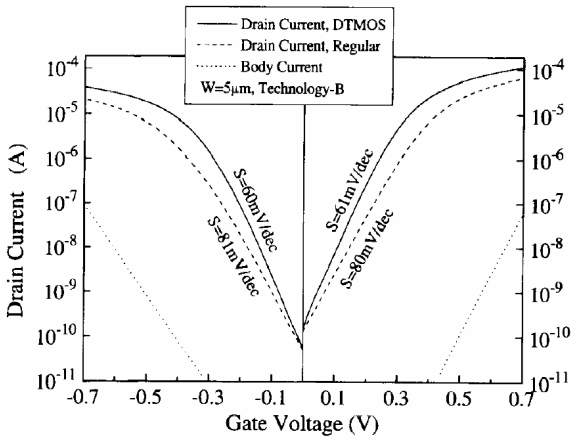


DTMOS



ID vs. VDS for normal and DT operation

DTMOS



Subthreshold currents for SOI NMOS and PMOS transistors with bodies grounded vs. DTMOS

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Power Distribution

- Chapter 24, Design and analysis of Power Distribution Networks by Blauuw, Panda and Chaudhury
- S. Lin, N Chang, ISSCC Microprocessor Design Workshop 2001

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Power Distribution

- Supply current is brought on chip at specific locations
  - » on the edge for most chips which are *peripherally bonded*
  - » distributed over the area of the chip for *area bonded* (C4, solder ball) chips
- Loads consume this current at different locations on the chip at different times
- There is often a large parasitic inductance associated with each bond-wire or solder-ball (0.1-10nH)
- Current is distributed from the bond pads to the loads on thin metal wires
  - » 0.04Ω/• typical
- Load currents may be very high
  - » average current may be as large as 20A for *very* hot chips (50W at 2.5V)
  - » peak current may be 4-5x this amount (100A!)
- L di/dt of bond wire and IR drop across on-chip wires are often a major source of supply noise

From [Dally]

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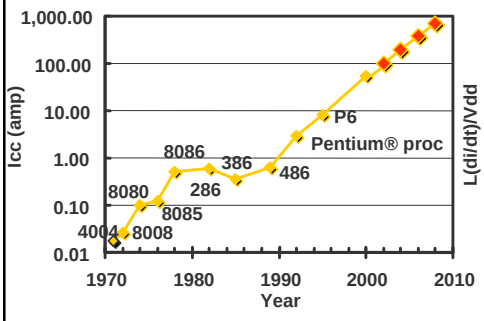
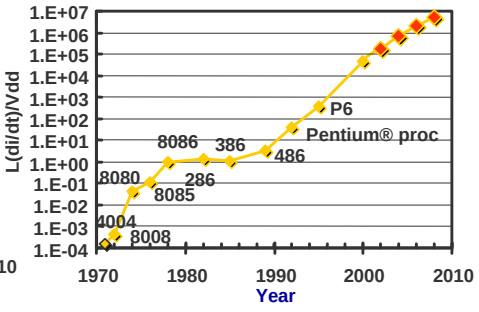
dildt Trends

- ***dildt* increases roughly as *I*f***





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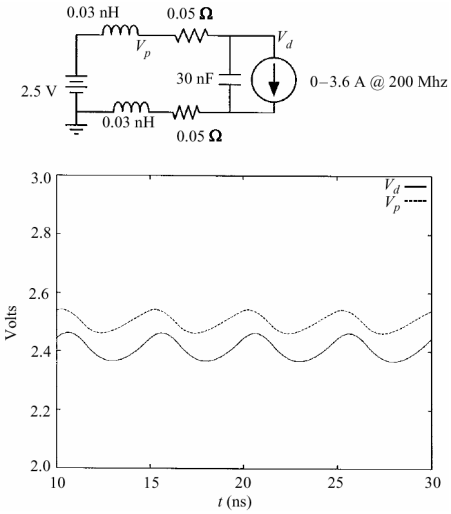
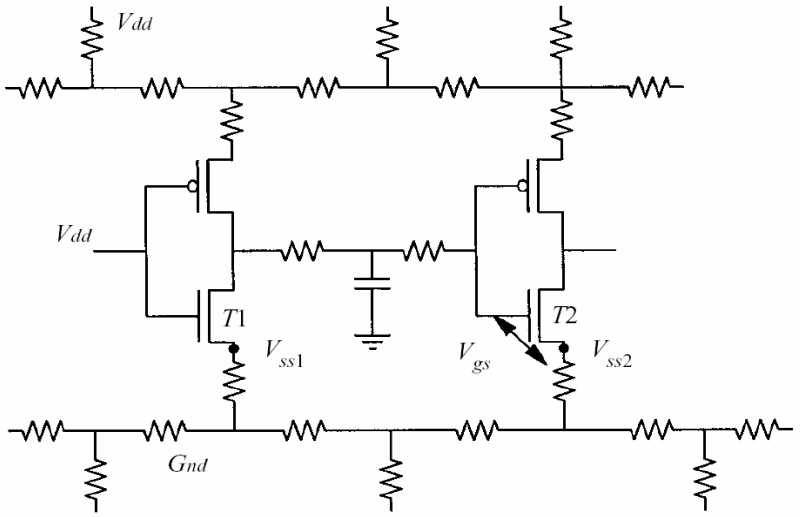
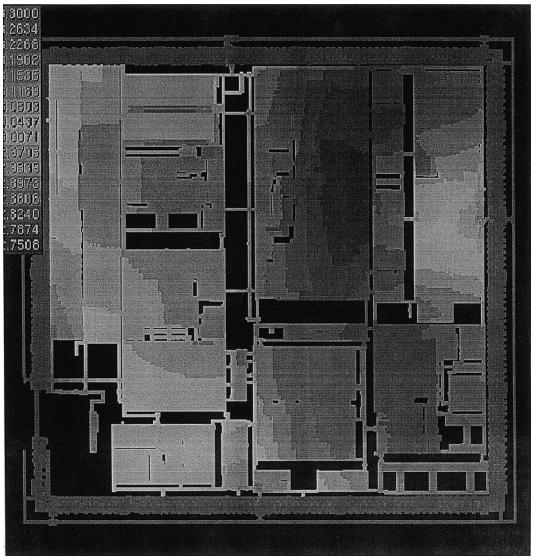
Power Distribution Network: Simplified



IR Drop

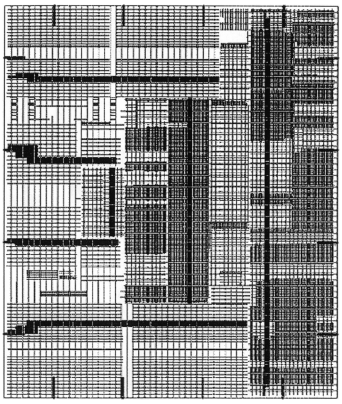


Option 1: The "Routed" Power Network (DSP Processor)



Courtesy of IEEE Press, New York. © 2000

Option 2: The Power Grid



Power grid of PPC 750

Courtesy of IEEE Press, New York. © 2000

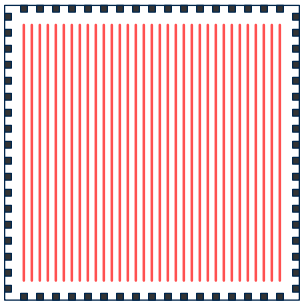
DEC EV4 - 3 Metal Layers

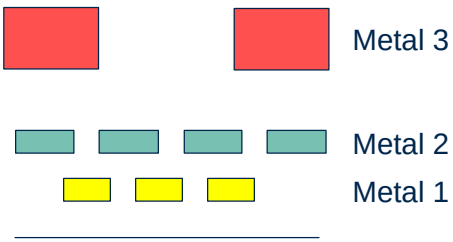
3rd "coarse and thick" metal layer added to the technology for EV4 design

Power supplied from two sides of the die via 3rd metal layer

2nd metal layer used to form power grid

90% of 3rd metal layer used for power/clock routing





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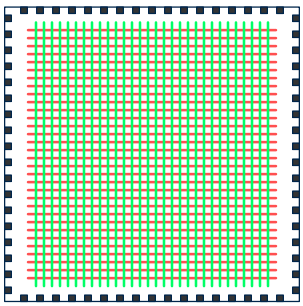
DEC EV5 - 4 Metal Layers

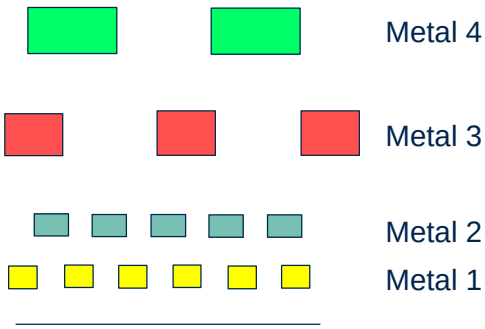
4th "coarse and thick" metal layer added to the technology for EV5 design

Power supplied from four sides of the die

Grid strapping done all in coarse metal

90% of 3rd and 4th metals used for power/clock routing





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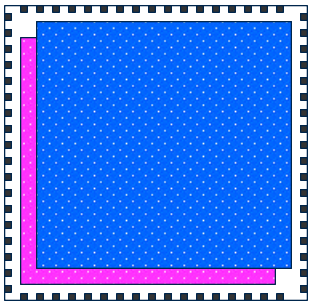
Option 3: Power Planes
DEC EV6 - 6 Metal Layers

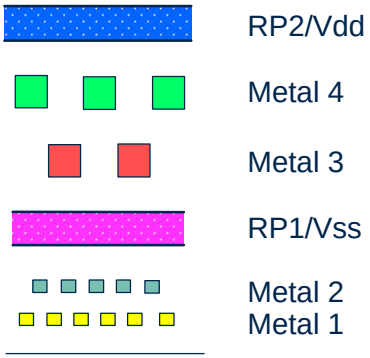
2 reference plane metal layers added to the technology for EV6 design

Solid planes dedicated to Vdd/Vss

Significantly lowers resistance of grid

Lowers on-chip inductance





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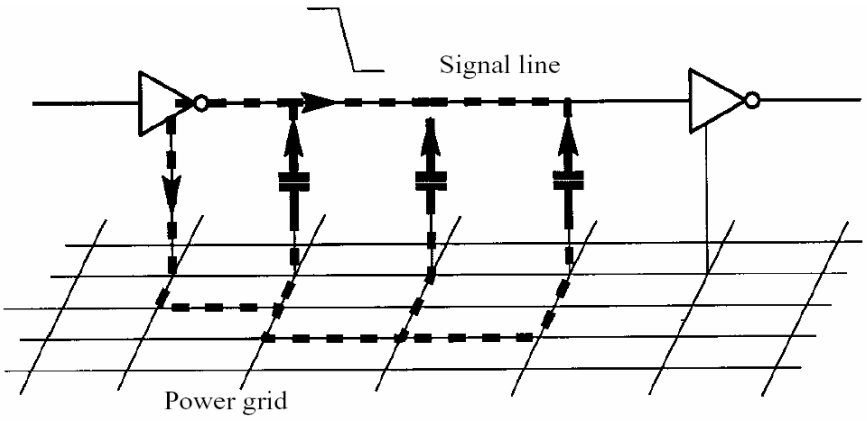
Power Distribution and Signal Net Inductance



$L = k.A$

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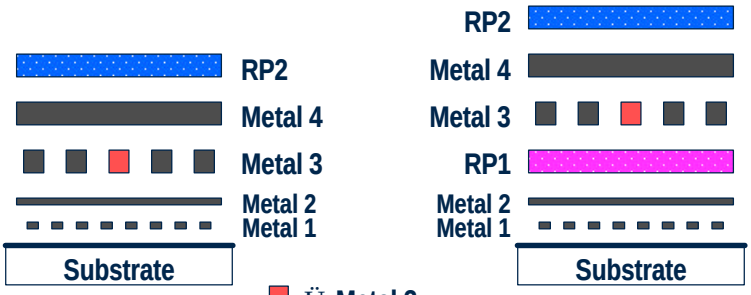
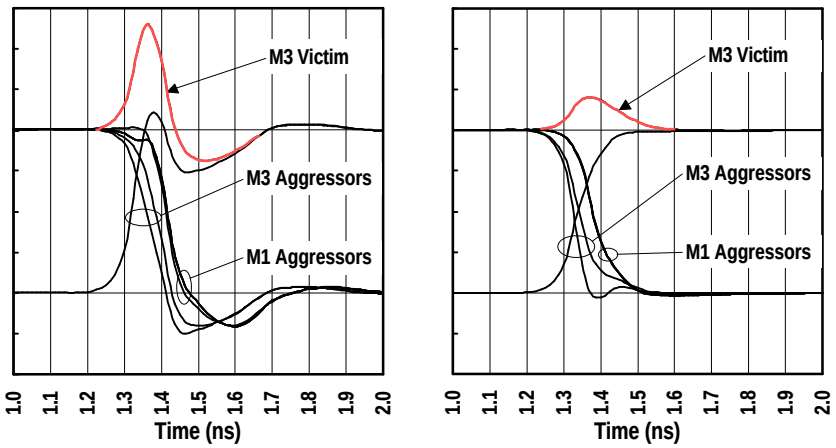
Reference Plane Example

Simulation Methodology

Extract Inductance & Resistance versus Frequency
Model Skin Effect Both Vertically and Horizontally
Construct Time-Domain SPICE Model and Simulate with SPICE
Use FF Devices, High Vdd & Low Temperature to Aggravate Inductive Effects



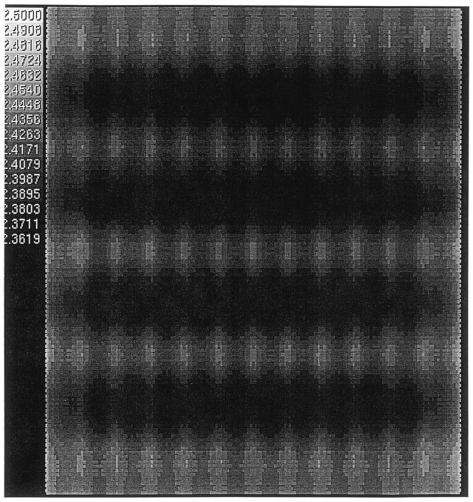
Reference Plane Example (continued)



RP2 Only

RP1 & RP2

Power Distribution Network Design Methodology



PPC 750
Early Analysis
(before actual circuit implementation)
Assumes uniform current distribution
Max drop: 156 mV

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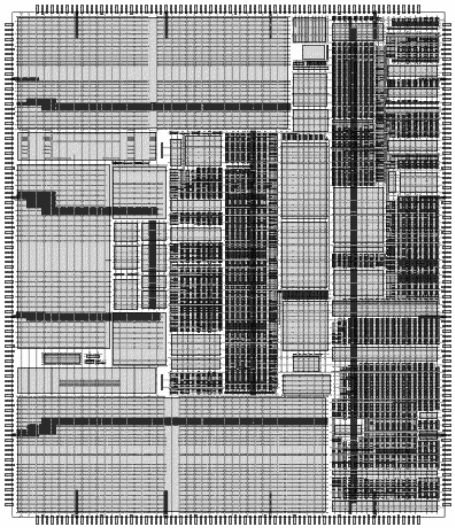
Power Distribution Network Design Methodology



PPC 750
After floorplanning.
Estimates of current of each block.
Power density uniform over block
Max drop: 172 mV

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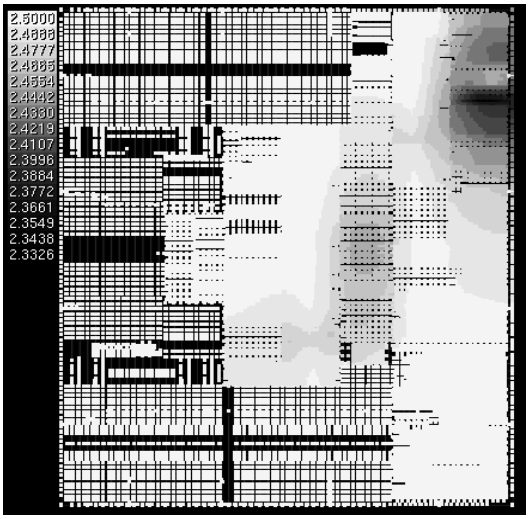
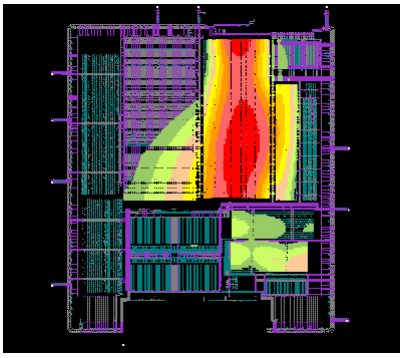
Power Distribution Network Design Methodology



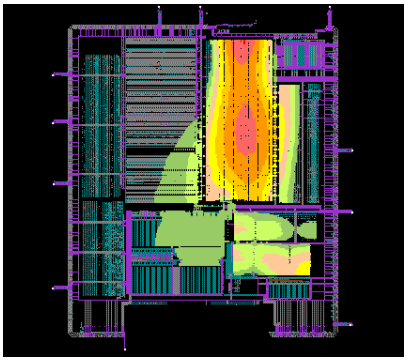
PPC 750
After layout.
RC network extracted.
Gates modeled as time-varying current sources
Max drop: 170 mV

Power Distribution Analysis Tools

Before



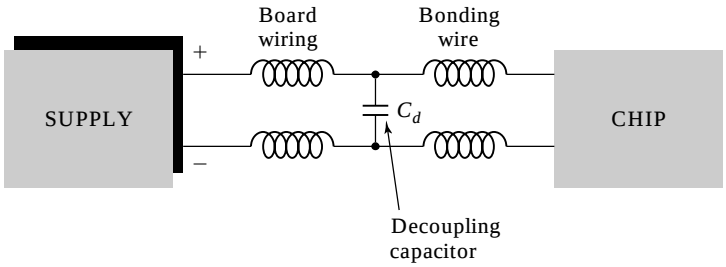
After



- **Requires fast and accurate peak current prediction**
- **Heavily influenced by packaging technology**

Source: Cadence

Dealing with Ldi/dt
Decoupling Capacitors



Decoupling capacitors are added:
- on the board (right under the supply pins)
- on the chip (under the supply straps, near large buffers)

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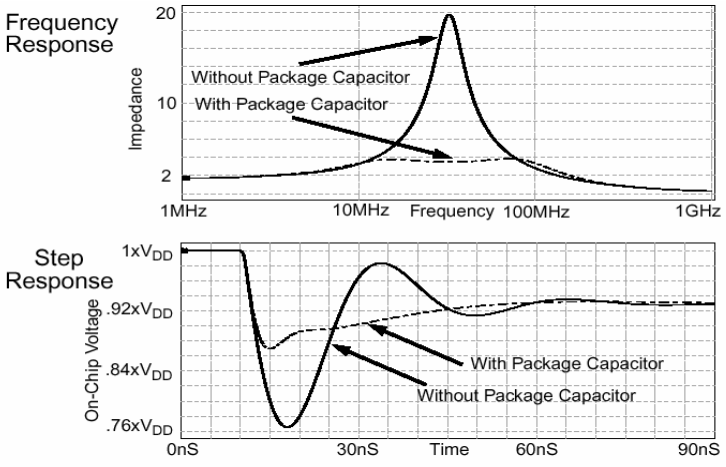
Impact of Bypass Cap



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On-Chip Bypass Capacitors

- Much of the difference between peak and average current may be supplied by local, on-chip bypass (decoupling) capacitors
- Bypass capacitors are also critical in mitigating the effects of the supply bond-wire inductance
- Decoupling is done by all the devices, N-wells, and specific capacitors
- Capacitors need fuses to prevent manufacturing shorts, sizing for limited oscillations.

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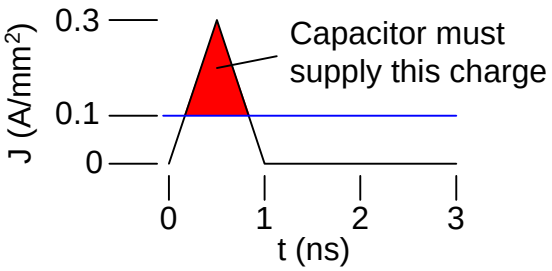
3x Reduction in Peak Current



$$Q = \left(\frac{2}{3}\right)^2 \left(0.3\text{A/mm}^2\right)\left(1\times10^{-9}\right)\left(0.5\right) = 67\text{pC/mm}^2$$

$$C = \frac{Q}{\Delta V} = \frac{67\text{pC/mm}^2}{0.25V} = 267\text{pF/mm}^2$$

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Decoupling Capacitor Ratios

- **EV4**
  - total effective switching capacitance = 12.5nF
  - 128nF of de-coupling capacitance
  - de-coupling/switching capacitance ~ 10x
- **EV5**
  - 13.9nF of switching capacitance
  - 160nF of de-coupling capacitance
- **EV6**
  - 34nF of effective switching capacitance
  - 320nF of de-coupling capacitance -- not enough!

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EV6 Decoupling Capacitance

Design for Idd= 25 A @ Vdd = 2.2 V, *f* = 600 MHz

- 0.32-µF of on-chip de-coupling capacitance was added
  - Under major busses and around major gridded clock drivers
  - Occupies 15-20% of die area
- 1-µF 2-cm^2 Wirebond Attached Chip Capacitor (WACC) significantly increases “Near-Chip” de-coupling
  - 160 Vdd/Vss bondwire pairs on the WACC minimize inductance

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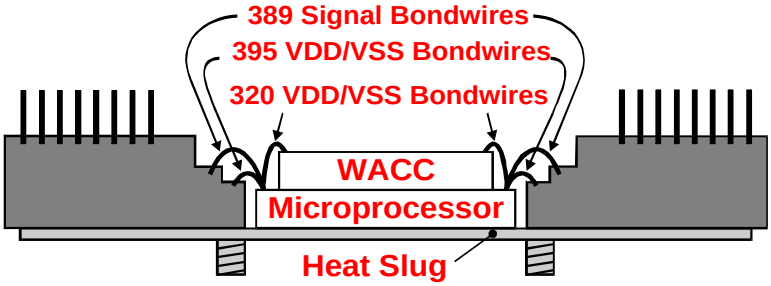
EV6 WACC

389 Signal - 198 VDD/VSS Pins



587 IPGA

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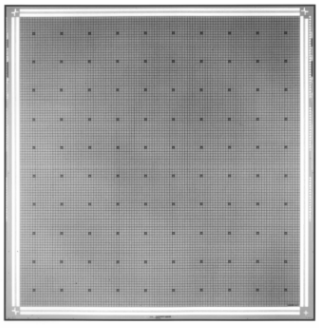
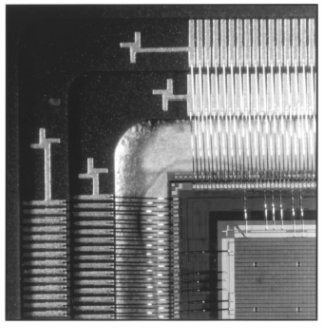
WACC Assembly



Prototype 600nF WACC (1.2cm^2)



Prototype Package Assembly

Gieseke, ISSCC'97

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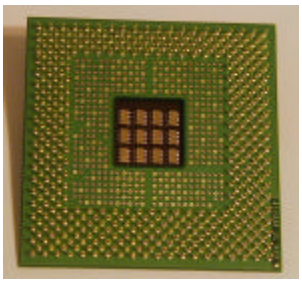
Flip-Chip Solutions

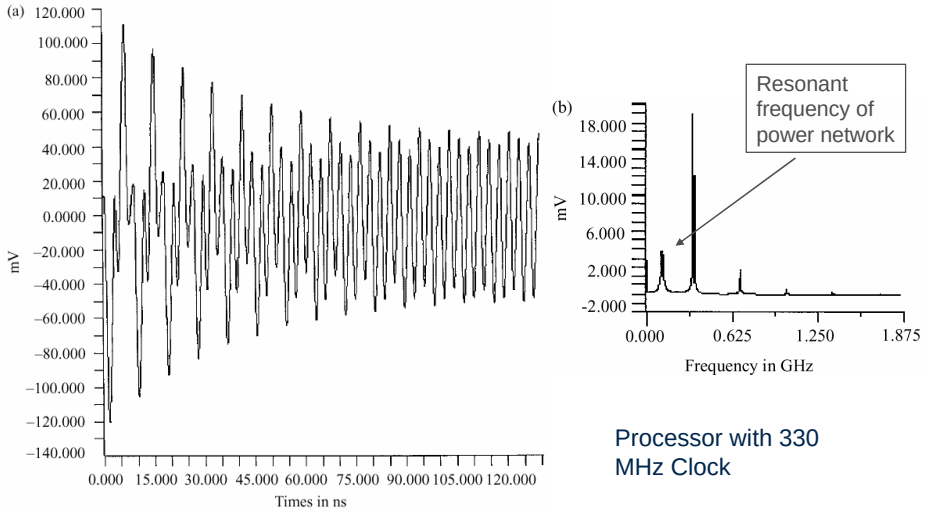


Intel Pentium 4

Challenge

- **Resonance frequency of LC power distribution network ($f = 1/(2\pi(LC)^{0.5})$) used to be above clock frequency**
- **But …**
  - LC of network is going down
  - Clock frequency going up
  - Impact of clock gating
- **Solutions …**

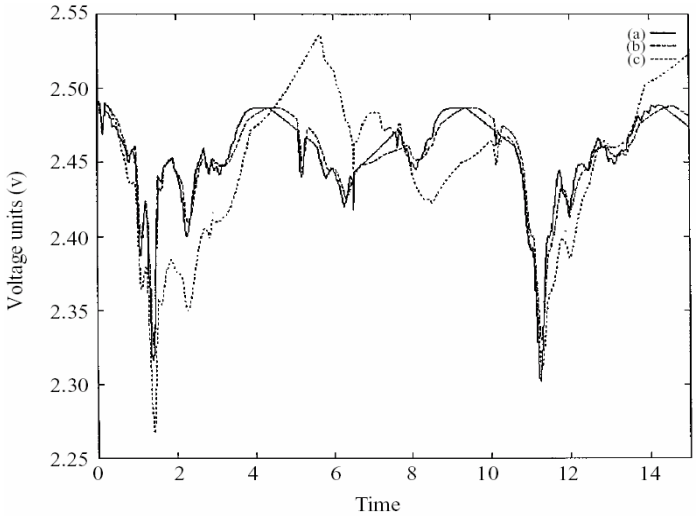
Grid Resonance



Processor with 330 MHz Clock

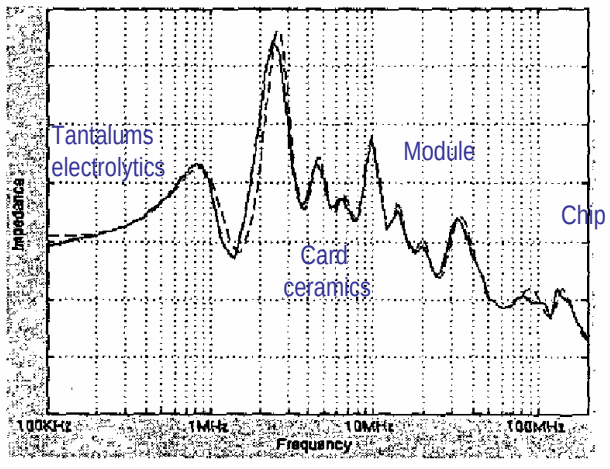
PPC750

Comparison between R, RC, and RLC analysis



AC Impedance

- IBM POWER 4 FPU



Weekly, EPEP'03