Architecture Evaluation for Power-efficient FPGAs

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Partially supported by NSF and SRC

Outline

- Introduction
- Evaluation Flow
- Architecture Model
- Power Model
- Architecture Evaluation Results
- Conclusions

Introduction

- Existing FPGAs are known to be power inefficient
  - E.g. [Kusse, ISLPED'98]

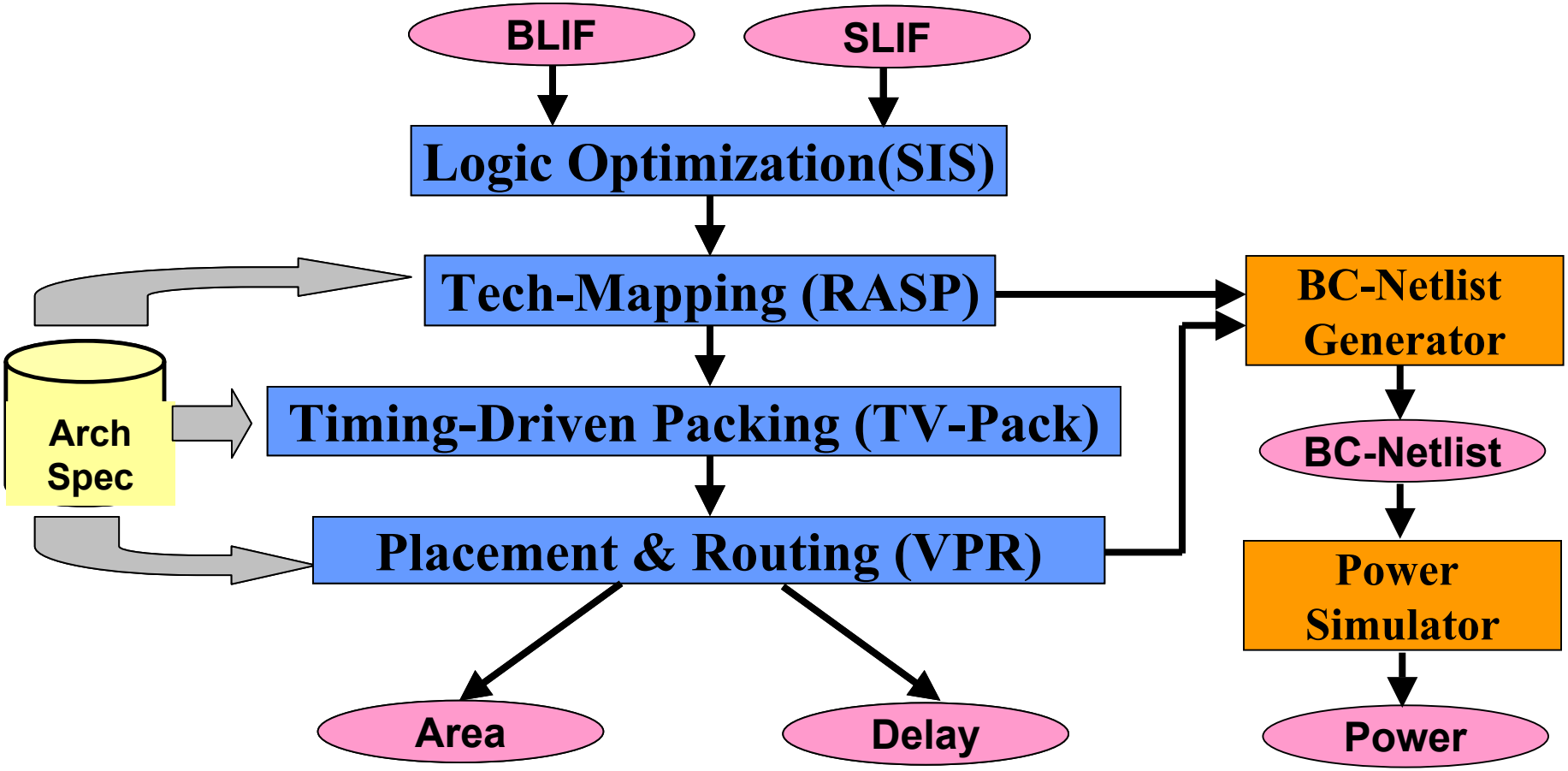
Design Example	Vdd	Energy
Xilinx XC4003A	5v	4.2mW/MHz
Static CMOS	3.3v	5.5uW/MHz

Table1 8-bit adder

  - 100X power overhead
- Need to explore power efficient FPGAs

Evaluation Framework — *fpgaEva-LP*

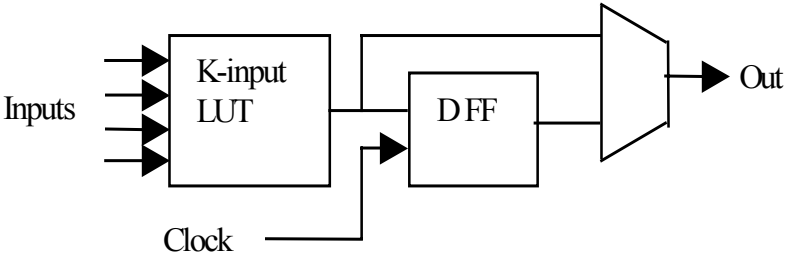
- *fpgaEva-LP* [Cong, et al, ICCD'00]



Architecture Model

- **Logic Block [Ahmed-Rose, FPGA2000]**

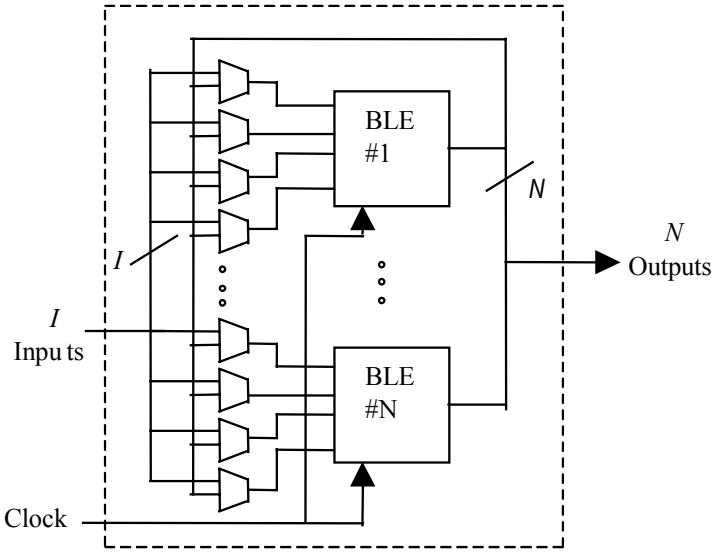
BLE:
Basic Logic Element



Parameters:

LUT Size *k*

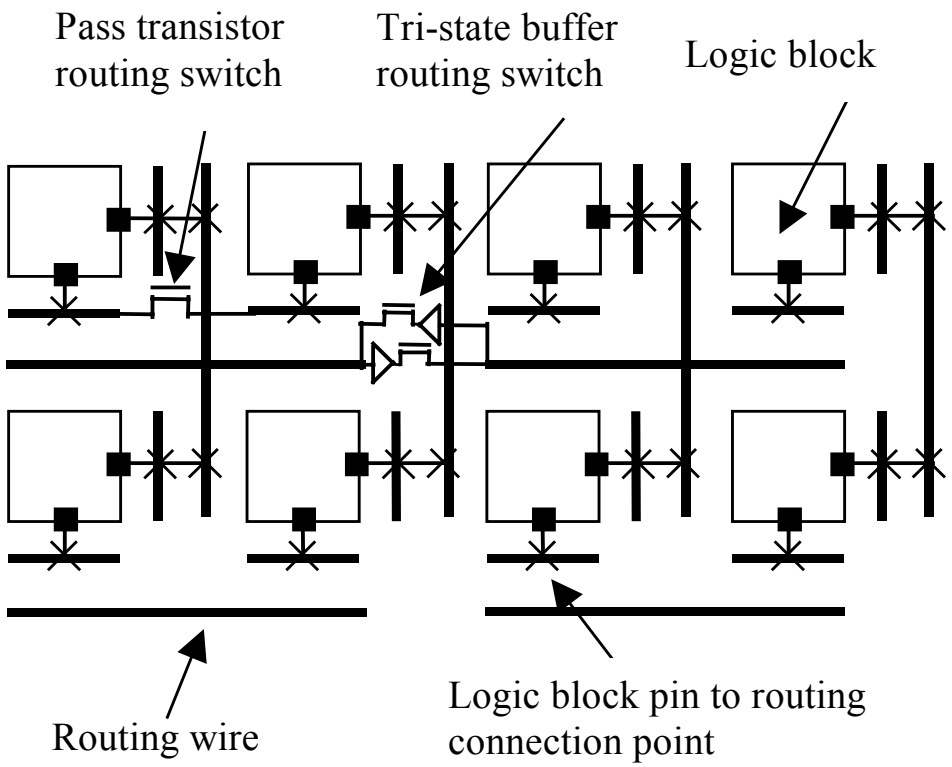
CLB:
Cluster-Based Logic Block



Cluster Size *N*

Architecture Model

- **Routing Structure [Betz-Rose, FPGA1999]**



Parameters:

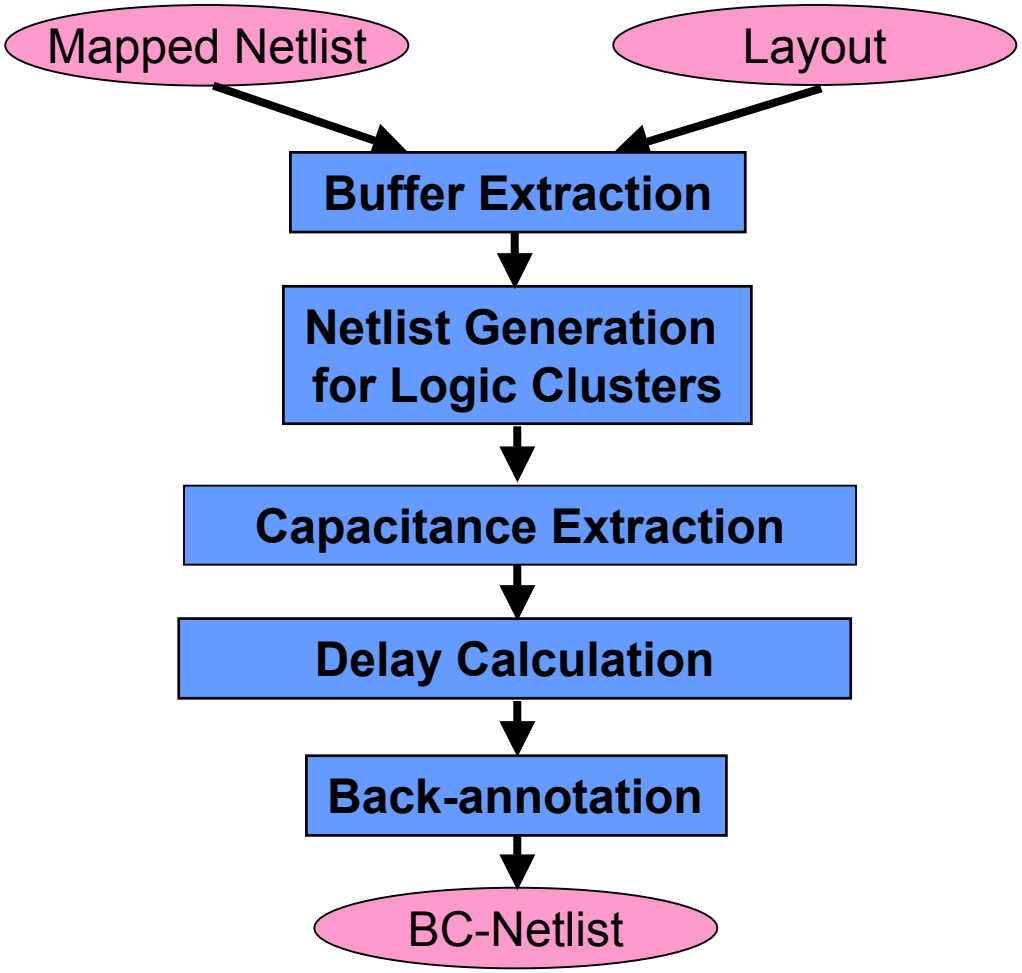
Wire segment length

Switch-box type

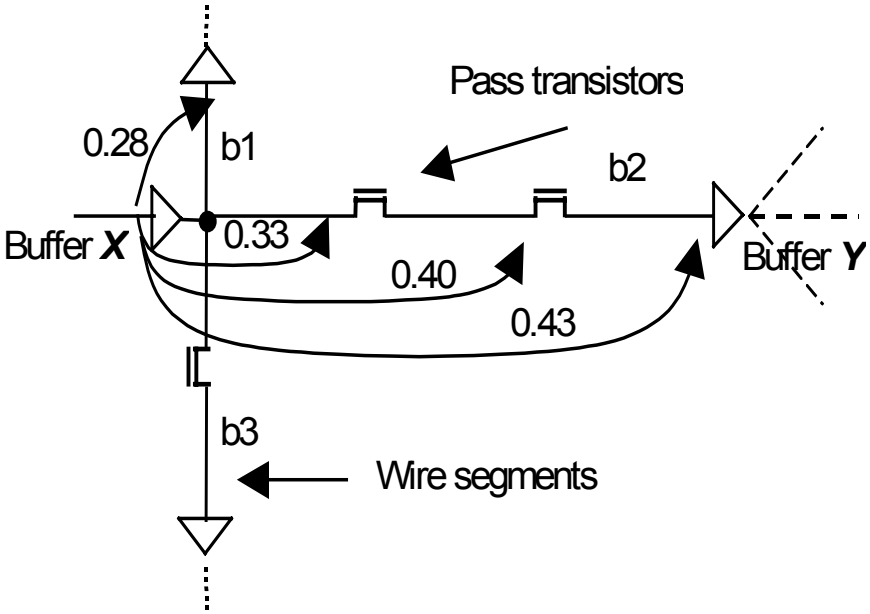
Buffer/Pass transistor distribution

Connection box configuration

BC-Netlist Generator



Capacitance Extraction and Delay Calculation

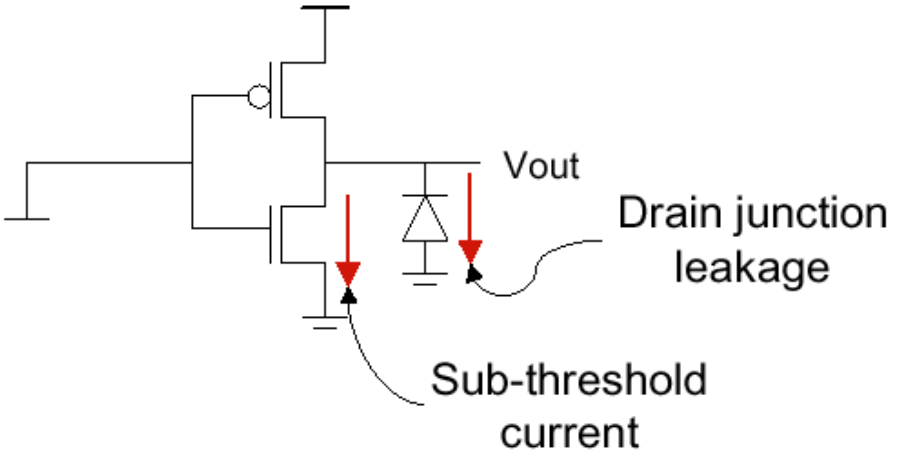


- Wires segmented by buffers and pass transistors
- Capacitance: lumped from all branches for wires, pass transistors and gates (buffers)
- Delay: Elmore Delay model

Mixed-level Power Model – Overview

- Dynamic power
  - Switching power
  - Short-circuit power
- Related to signal transitions
  - Functional switch
  - Glitch
- Static Power
  - Sub-threshold leakage
  - Reverse biased leakage
- Depending on the input vector

components / power sources	Logi	
Dynamic	Macr	
Static	Macro-model	Macro-model



Macromodeling – Dynamic Power

- Pre-characterized average power per access
  - Based SPICE simulation with random input vectors
  - Both switching power and short-circuit power
- Applied to LUTs that have the regularity of connection
- Verification

	SPICE simulation	Our Power Model	Error
Total Energy (Jourl)	1.42E-11	1.27E-11	10.56%

200 random input vectors

Macromodeling – Static Power

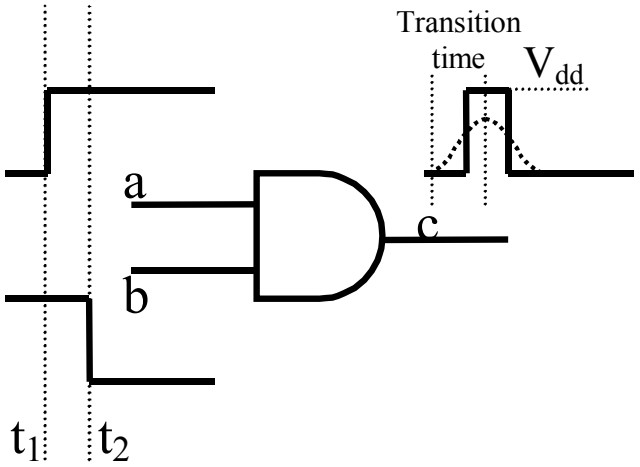
- Input pattern dependent
- Pre-characterized average static power
  - Input vectors are grouped into vector sets
  - Typical vectors are simulated in each set
  - Save SPICE simulation time
- Applied to both LUTs and Interconnect buffs

Switch-level Model – Interconnect Switching Power

- **Switching power without glitches**

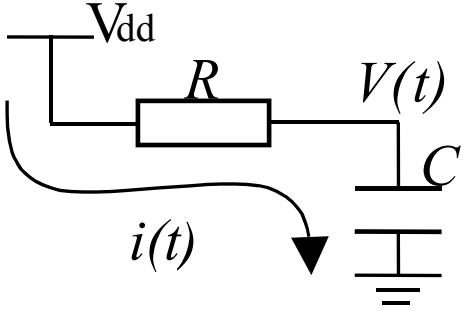
$$P_{sw} = 0.5 f \cdot V_{dd}^2 \cdot \sum_{i=1}^{n} C_i \cdot E_i$$

$$= 0.5 f \cdot V_{dd}^2 \cdot \sum_{i=1}^{n} C_i \cdot (N_i / cycles)$$



- **Effective transition number**

$$\hat{N}_i(\text{rising}) = \frac{(V_1 - V_2)(V_1 + V_2 - 2V_{dd})}{V_{dd}^2} N_i$$



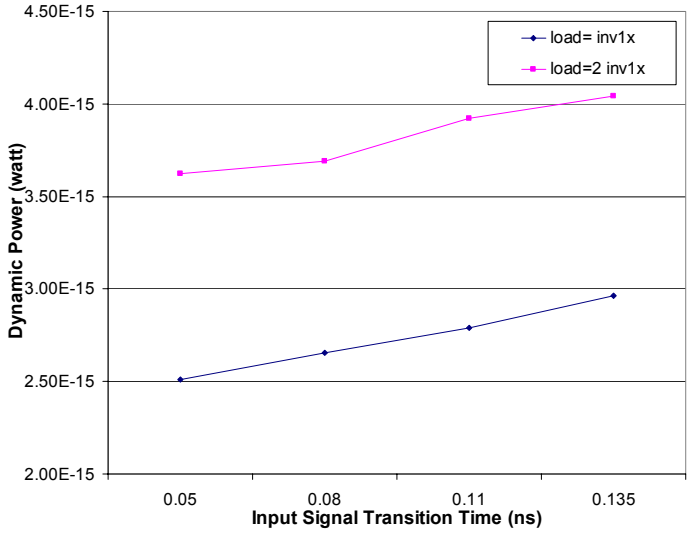
- **Switching power with glitches**

$$P_{sw} = 0.5 f \cdot V_{dd}^2 \cdot \sum_{i=1}^{n} C_i \hat{E}_i$$

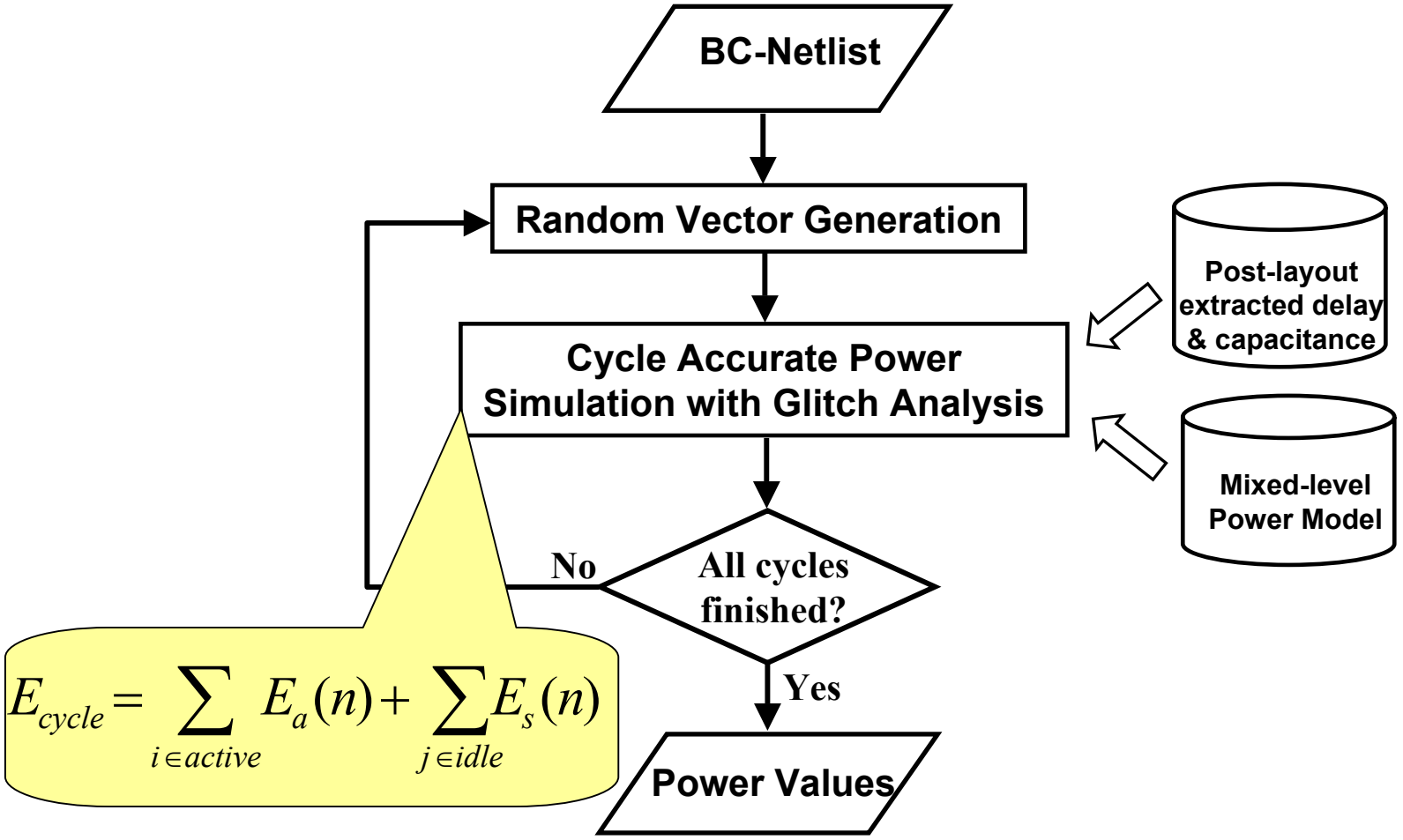
$$= 0.5 f \cdot V_{dd}^2 \cdot \sum_{i=1}^{n} C_i (\hat{N}_i / cycles)$$

Switch-level Model – Interconnect Short-Circuit Power

- Short-circuit power
  - Fixed ratio between short-circuit and switching power
  - The ratio is decided by SPICE simulation (13%)



Power Simulator

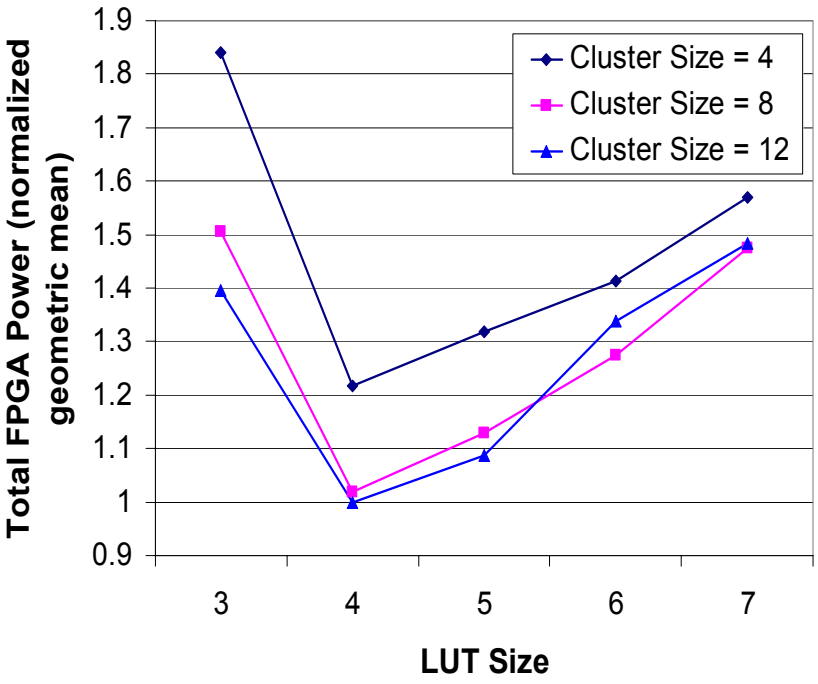


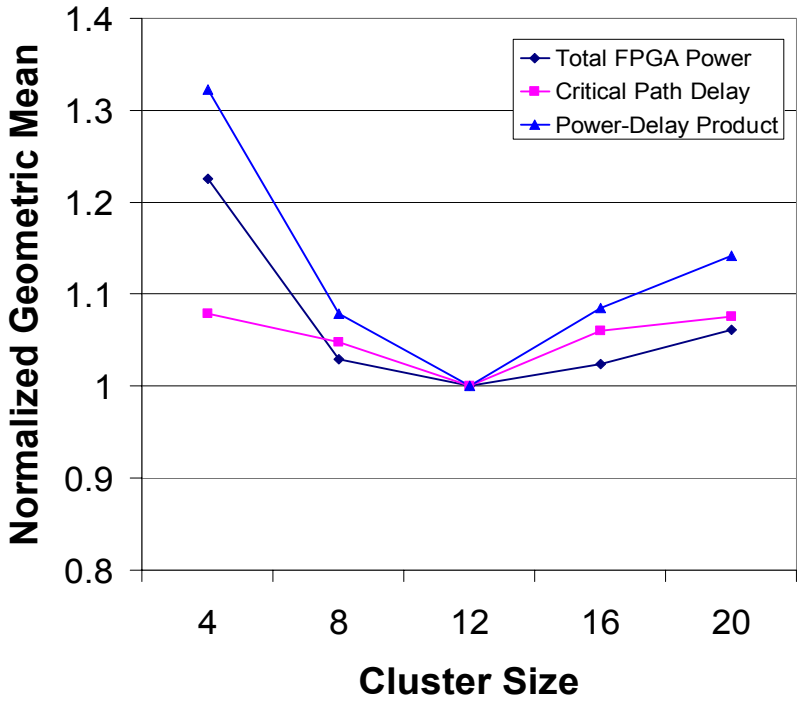
Experimental Settings

Technology	R_NMOS	R_wire	C_wire
0.1 µ	5300 Ohm	0.91667 MOhm/m	73.8 aF/um

Logic Block Architectures	
LUT Size *k*	3 – 7
Cluster Size *N*	4, 8, 12, 16, 20
Routing Architectures	
routing_default	wire length 4, 50% buffers and 50% pass transistors
routing_fullbuf1	wire length 4, 100% buffers
routing_fullbuf2	wire lengths 4 and 8, 100% buffers

Experiments on Logic Block Architectures





LUT Size = 4

- **LUT Size = 4 is also optimal for power consumption**
- **Cluster Size = 12 is the optimal cluster size**

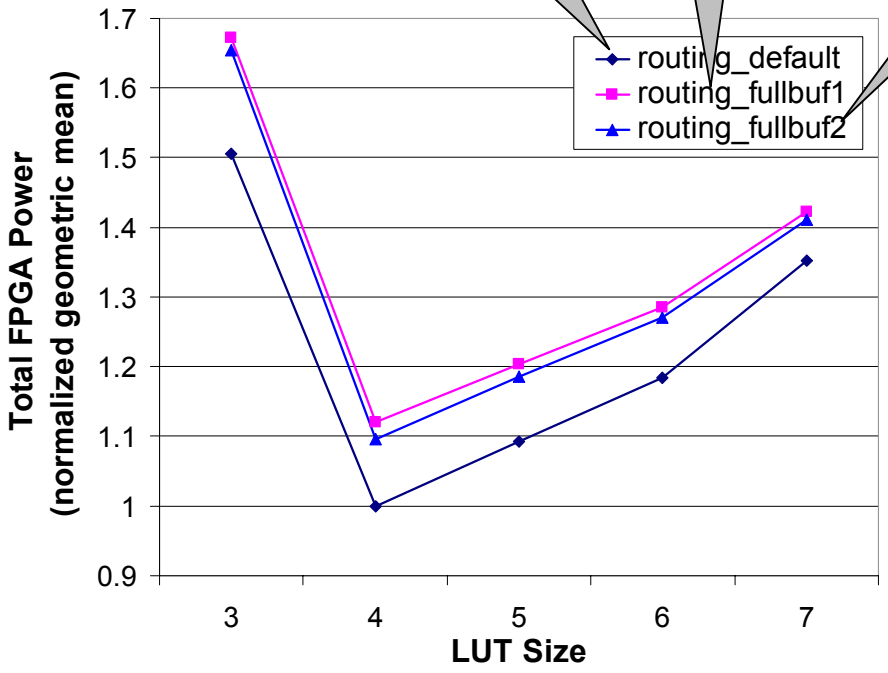
Experiments on Routing Architectures

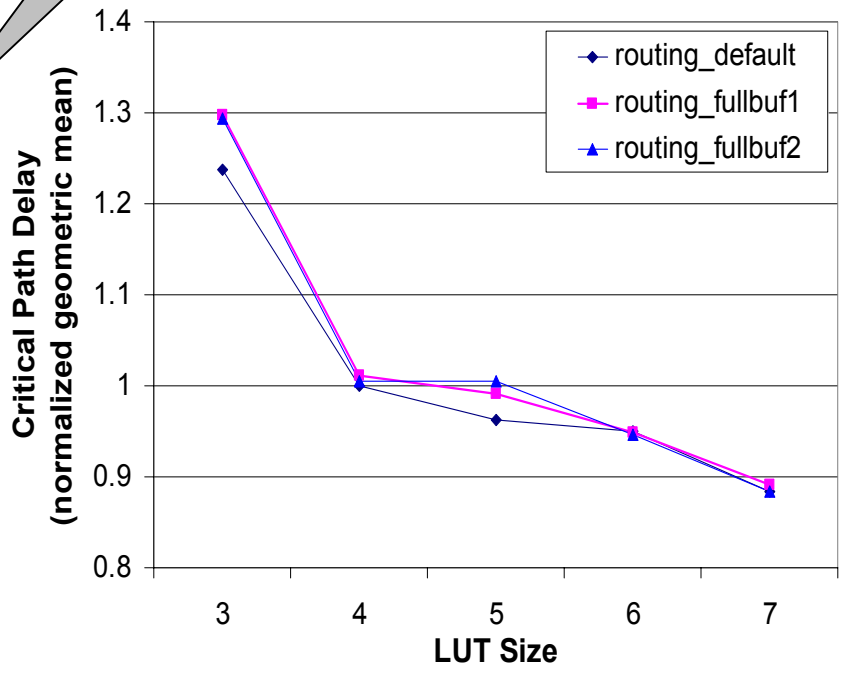
wire length 4, 50% buffers and 50% pass transistors

wire length 4, 100% buffers

wire lengths 4 and 8, 100% buffers

- *routing_default* achieves lowest power

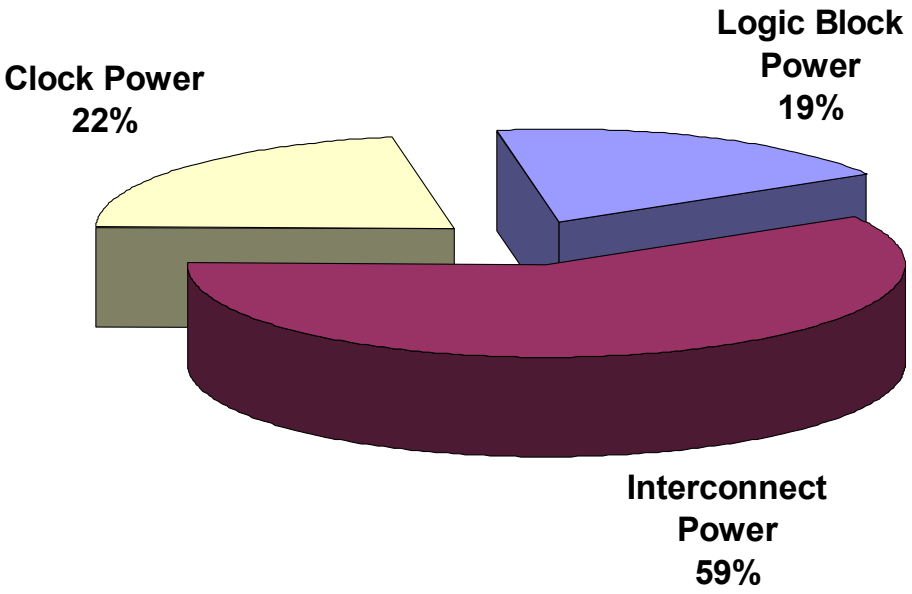




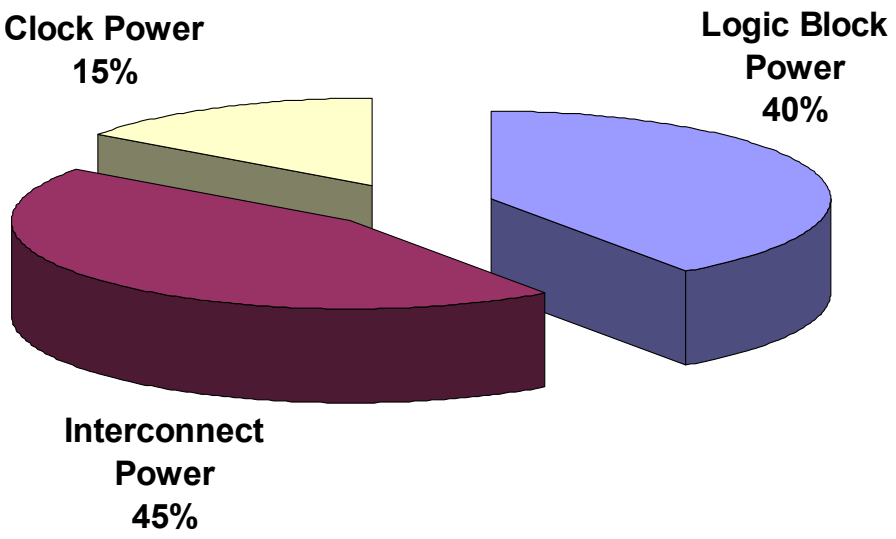
Cluster Size = 4

Power Breakdown

Cluster Size = 12, LUT Size = 4



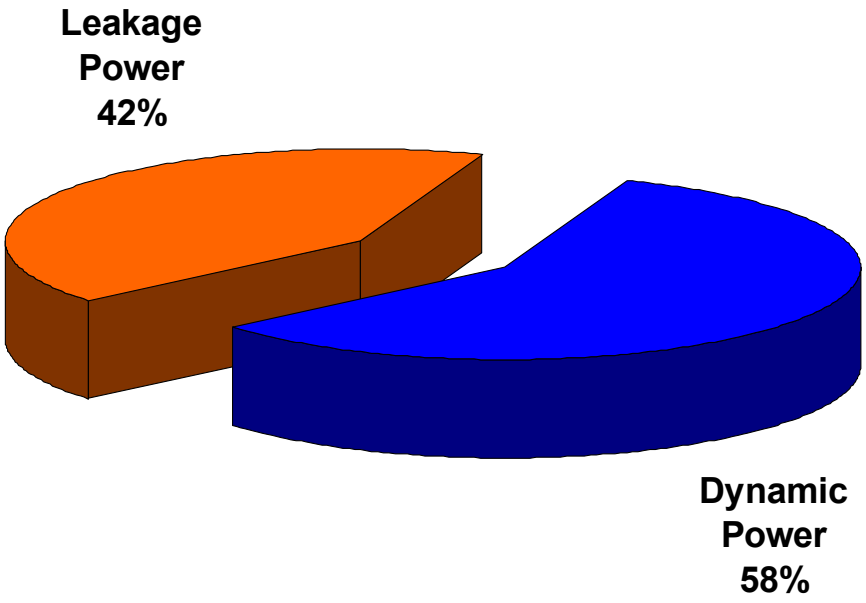
Cluster Size = 12, LUT Size = 6



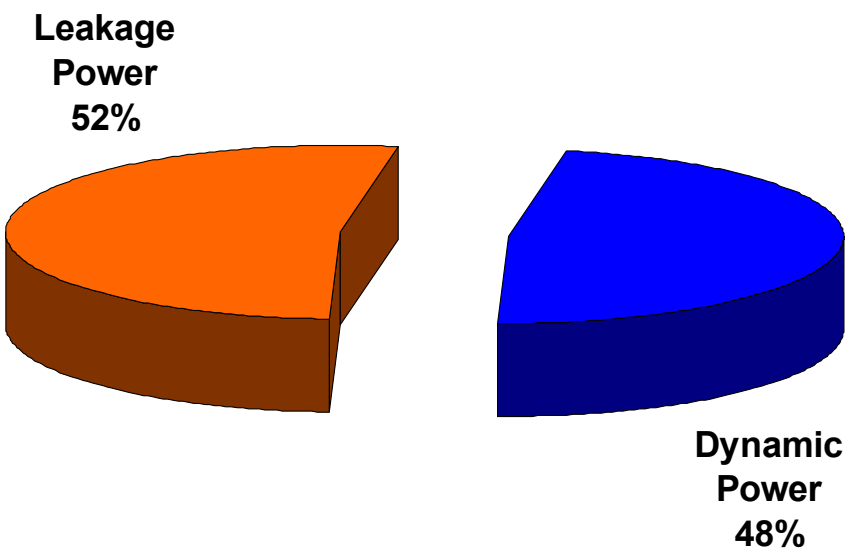
- Interconnect power is dominant

Power Breakdown

Cluster Size = 12, LUT Size = 4



Cluster Size = 12, LUT Size = 6



- Leakage power becomes increasingly important

Conclusions

- Developed an architecture evaluation framework *fpgaEVA-LP* for power efficiency
- Performed quantitative analysis for parameterized FPGA architecture
- Identified future directions for FPGA power optimization
  - Interconnect power is dominant
  - Leakage power is becoming important