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To cite this article: A. K. M. Mahfuzul Islam and Hidetoshi Onodera 2014 *Jpn. J. Appl. Phys.* **53** 04EE08

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Japanese Journal of Applied Physics 53, 04EE08 (2014) **REGULAR PAPER**
http://dx.doi.org/10.7567/JJAP.53.04EE08

Area-efficient reconfigurable ring oscillator for device and circuit level characterization of static and dynamic variations

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Received September 30, 2013; accepted January 3, 2014; published online March 7, 2014

Accurate characterization of transistor variation under dynamic switching condition has become important for reliable digital circuit design. This paper proposes a reconfigurable ring oscillator (RO) structure which enables measurement of transistor level variation. Each inverter stage in the RO can be configured into several delay modes. The delay of a particular inverting stage can be made dominant by configuring an inhomogeneous RO structure. By scanning the inhomogeneous stage, delay variation of each stage can be measured. Furthermore, pMOSFET and nMOSFET variation can be measured separately by making only rise or fall delay dominant. Specific transistor with random telegraph noise (RTN) in the inhomogeneous stage can be identified by reconfiguring the inhomogeneous stage. Thus, using a single RO, static delay variation as well as dynamic variation such as RTN can be measured. The area for a 127-staged reconfigurable RO including peripheral circuits is only 0.0085 mm^2 thus area-efficient measurement becomes possible. Measurement results from a 65-nm test chip shows the validity of the proposed circuit structure. © 2014 The Japan Society of Applied Physics

1. Introduction

With device scaling, static device variations[1] as well as dynamic variations such as negative bias temperature instability (NBTI)[2] and random telegraph noise (RTN)[3] have become serious problem. Static variation occurs during the manufacturing process of the device whereas dynamic variation occurs during the run-time. Dynamic variations are difficult to predict and therefore it is difficult to set adequate design margin. In the case of static variations, circuit performance can be predicted with statistical analysis.[4,5] In the case of dynamic variations, simple statistical analysis is not sufficient. Performance models based on variation characterization are required.[6] In order to develop effective performance models, the nature of dynamic variations and their effects on the circuit behavior needs to be understood and characterized accurately. The effects of both the static and dynamic variations need to be taken into account during the design phase to ensure correct operation.

NBTI is being considered for long as a major reliability concern.[7] NBTI degrades pMOSFET performance over time thus reduces the product lifetime. Several sensor circuits to monitor NBTI degradation and characterize its effect are reported.[8–10] Using the recovery phenomenon of NBTI, NBTI-aware design methodologies are proposed to increase product life time and reduce design margin.[11] NBTI induced device degradation can be recovered by applying body bias too.[12] Whereas, RTN is an intrinsic device variation which causes temporal fluctuation in MOSFET threshold voltage during run time. With device scaling, RTN induced device variability has become comparable to static device variability.[13] RTN is reported to be causing failures in static random access memories (SRAMs),[14] flash memories[15] and CMOS image sensors.[16] RTN can cause ring oscillator (RO) frequency fluctuation as much as 10% at low voltage in 40-nm process.[17] For finer process, RTN variability is reported to be increasing. Thus, RTN is a big concern for reliable operation of future LSI. In order to predict RTN effect on circuit behavior, modeling of RTN based on accurate characterization of devices under dynamic operation is needed. However, the effect of RTN on digital circuit performance is still not well investigated. Conventionally, device level measurement of RTN is performed where DC bias is applied.[18] Present measurement techniques for RTN effect on digital circuit behavior is performed using simple ring oscillator.[17,19,20] From large number of RO circuits, ROs with RTN are first screened out. Then detailed measurement is performed to characterize RTN effect. This method requires large area to implement large number of ROs which is very costly. Conventional ring oscillator based measurement does not give us device level variation information as the variations on each device are averaged out. Besides, the relationship between device variation and circuit behavior variation cannot be correlated with simple ring oscillator based measurement.

Static device variation can be categorized into die-to-die (D2D) and within-die (WID) variation. D2D variation is global in a chip meaning all the transistors have the same variation. WID variation can be further categorized into systematic and random components.[21] Systematic variation can be classified as across-field and layout dependent variations.[22,23] WID random variation causes device mismatch between even two adjacent devices. The impact of WID random variation is increasing with every new technology node. As both the WID random variation and RTN induced variation are statistical phenomena, large number of samples are required to characterize these variations. Conventionally, device-array based test structures,[18,24] or RO array based test structures[21,25] are used to characterize static variation. Various approaches are proposed to make the RO frequency sensitive to a particular variation source which helps to develop detailed statistical models of these variations.[26–28] An inhomogeneous structure is proposed in an attempt to characterize RTN induced variability at the device level.[29] However, the existing techniques have two fundamental problems. One is the large area required for large samples. The other is the inability of device identifications for accurate characterization and modeling. In order to overcome these problems, we propose a reconfigurable RO structure where each inverter stage can be configured to several structures. Large measurement samples can be obtained from a single RO by reconfiguring the RO.

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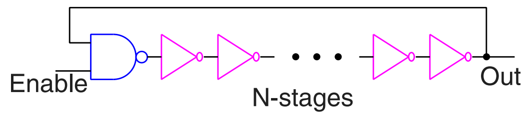

Fig. 1. (Color online) Schematic of ring oscillator circuit used for variation characterization. Conventionally, the inverter structure of each stage is fixed. Multiple ROs with different inverter structures are implemented for extracting various variation information.

The proposed structure has the following key advantages over the conventional structure.

(1) Enables large number of measurement samples from a single RO instance.

(2) Variation of each transistor can be measured which allows accurate characterization of variation.

2. Reconfigurable ring oscillator for device level characterization

2.1 Reconfigurable ring oscillator structure

RO based measurement gives us characteristics of digital circuit behavior. Conventional RO structure uses the same inverter structure for each inverter stage. Figure 1 shows a conventional RO structure. In order to extract various variation information, inverters of various structures are used.[26–28] As the inverter structure is fixed, multiple designs and implementation of ROs with various inverter structures are needed. For a conventional RO structure, variation of each transistor is averaged out and thus transistor-by-transistor level characterization is not possible. An inhomogeneous RO structure is proposed where the RO frequency can be made sensitive to a small number of transistors.[29] In this section, we describe a reconfigurable RO structure by which device identification is possible allowing accurate device level variation characterization.

Figure 2 shows our proposed reconfigurable RO structure. The inverter structure of each stage is configurable so that various structures can be obtained with a single RO instance. A controller sets the configuration signals for each inverter stage. Using the inhomogeneous structure, the RO frequency can be made sensitive to the inhomogeneous stage. By scanning the inhomogeneous stage, large measurement samples can be obtained allowing statistical evaluation of variations. We show this measurement procedure to evaluate delay variation of each stage in Fig. 3. With the same inhomogeneous configuration, by reconfiguring the inhomogeneous stage again, device identification becomes possible.

2.2 Device variation characterization

Using the measurement method shown in Fig. 3, WID random variation is measured. With an N-staged RO, N types of inhomogeneous configurations are achieved. By reconfiguring the inhomogeneous stage further to be either nMOSFET- or pMOSFET-sensitive, statistical evaluation of nMOSFET and pMOSFET becomes possible. Reference 29 shows that the sensitivity of transistors in the inhomogeneous stage can become as large as 40 times compared with other transistors at 0.8 V operation. This makes the delay variation in the inhomogeneous stage multiple times larger than the delay variation in other stages. The sensitivity is defined as the percentage change of frequency due to one mV of

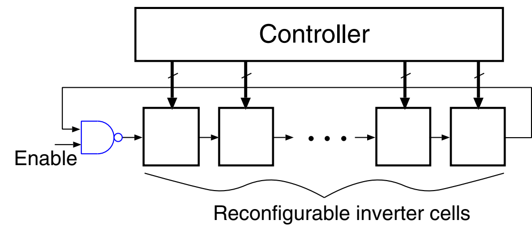

Fig. 2. (Color online) Proposed reconfigurable ring oscillator structure. Each inverter stage can be configured to several delay modes.

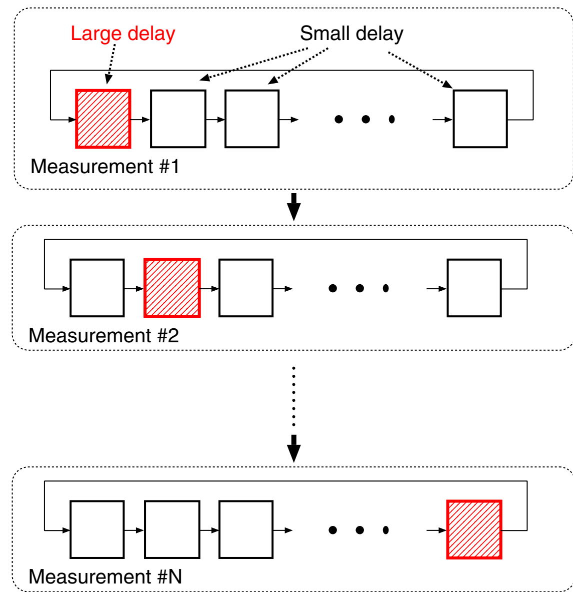

Fig. 3. (Color online) Characterization of delay variation using inhomogeneous configuration of our proposed ring oscillator. If the delay sensitivity of the inhomogeneous stage is multiple times larger than the other stages, then each measurement will reflect the delay variation of the corresponding inhomogeneous stage. Thus, by scanning the inhomogeneous stages, delay variation of each inhomogeneous stage can be measured.

threshold voltage change. Measuring the frequencies by scanning the inhomogeneous stages gives us a distribution which is a strong function of the delay variation between the inhomogeneous stages. By making the inhomogeneous stage to be either nMOSFET- or pMOSFET-sensitive, frequency distribution reflecting either nMOSFET or pMOSFET are obtained. The accuracy of the characterization depends on the sensitivity increase of transistors in the inhomogeneous stage compared with the transistors in the other stages. For example, assuming the frequency variation caused by each stage to be random and independent, frequency f_i for an inhomogeneous configuration where ith stage is the inhomogeneous stage can be expressed as follows:

$$f_i = f_0 + \sum_{j=1}^{i-1} x_j + x_i^s + \sum_{j=i+1}^{N} x_j = f_0 + x_i^s - x_i + \sum_{j=1}^{N} x_j. \quad (2.1)$$

Here, f_0 is the frequency at typical condition and x_j is the amount of frequency fluctuation caused by the jth stage. x_i^s is the amount of frequency fluctuation caused by the ith inhomogeneous stage. N is the number of stages. As the

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measurements of Fig. 3 is performed using the same circuit instance, $\sum_{j=1}^{N} x_j$ is constant. Thus, the frequency variation σ_f becomes the following:

$$\sigma_f^2 = \sigma_{x^s}^2 + \sigma_x^2, \tag{2.2}$$

$$\sigma_f = \sqrt{m^2 + 1} \cdot \sigma_x. \tag{2.3}$$

Here, σ_{x^s} and σ_x are the amounts of frequency variation caused by the inhomogeneous configuration and the default configuration which is used in the stages other than the inhomogeneous one. m is the sensitivity increase for the inhomogeneous stage compared with the other stages. Thus, variation between the inhomogeneous stages can be obtained by exploiting the sensitivity enhancement with the proposed measurement method of Fig. 3. From Eq. (2.3), larger the sensitivity increase m is, more enhancement is achieved in the measured frequency variation. In case of an 8 times increase in the sensitivity of an inhomogeneous configuration, frequency variation will be dominated by the variation caused by the inhomogeneous stages by more than 99% $(8/\sqrt{8^2 + 1})$. Statistical properties can be obtained by choosing the number of stage N to be sufficiently large.

D2D variation is measured by configuring the RO as homogeneous.[28] As the area of the circuit is very small, placing the circuit at several locations on a chip can capture systematic variations as well.

In order to identify devices with RTN effects, frequency fluctuation is observed for each inhomogeneous configuration. For an inhomogeneous configuration, the oscillation frequency is dominated by the delay of the inhomogeneous stage.[29] When a transistor inside an inhomogeneous stage is affected by RTN induced variability, the fluctuation becomes directly visible to the oscillation frequency due to its high sensitivity. By reconfiguring the pull-up or pull-down network, RTN affected devices become distinguishable. Thus, device level characterization becomes possible under switching condition. A homogeneous configuration may also show RTN-induced frequency fluctuation. Devices responsible for frequency fluctuation are distinguished by configuring the RO as inhomogeneous. This helps us to characterize device level variability as well as its effect on circuit behavior.

2.3 Reconfigurable inverter cell design

In order to realize the reconfigurable RO of Fig. 2, inverter cell with reconfigurable structure is required. In Fig. 4(a), we show a general concept of a reconfigurable inverter cell.

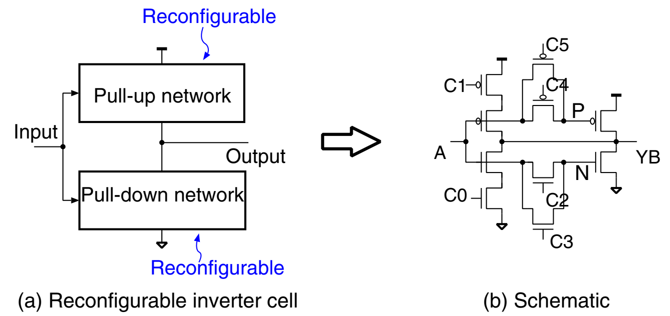

Fig. 4. (Color online) (a) Design of a reconfigurable inverter cell. Pull-up and pull-down networks are reconfigurable separately. (b) One design example of a reconfigurable inverter cell and its transistor level schematic. Various delay modes are realized.

Pull-up and pull-down networks are configurable separately to allow the measurements of pMOSFET and nMOSFET independently. Figure 4(b) shows one example of such a reconfigurable inverter cell structure. The inverter cell can be configured to several delay modes which is shown in Fig. 5. Cell configuration in Fig. 5(a) has equal rise and fall delay. Cell configuration in Fig. 5(b) has large fall delay compared to the rise/fall delays of Fig. 5(a) structure. Similarly, Fig. 5(c) has large rise delay compared with that of Fig. 5(a) structure. Each of the structures in Figs. 5(b) and 5(c) can be further reconfigured. For example, Fig. 5(b) has two pass-gates in parallel each of which can be either turned ON or OFF. We get three different configurations for the structure in Fig. 5(b) excluding both pass-gate OFF configuration.

When the pass-gates are turned off in Fig. 5 configurations, voltages of nodes “N” and “P” are determined by the charging and discharging currents during the oscillation. The charging and discharging currents depend on pass-gate off-resistances. “N” and “P” nodes have capacitances associated with the MOSFET gates and interconnect, thus form RC low pass filters. When the inverter input is “H”, nodes “N” and “P” are charged. When the inverter input is “L”, nodes “N” and “P” are discharged. For example, in case of Fig. 5(c) configuration, during the charging phase, the gate–source voltage of the nMOSFET pass-gate becomes negative with the increase of node “N” voltage. The pass-gate is also affected by reverse bias with the voltage increase. These effects lead to an exponential increase in the nMOSFET pass-gate off-resistance as the node “N” voltage increases with a

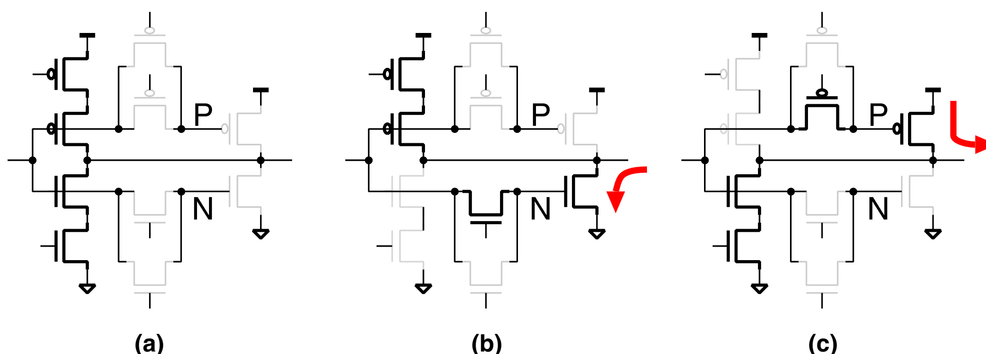

Fig. 5. (Color online) Several pull-up and pull-down network configurations to realize various delay modes: (a) standard, (b) large fall delay, and (c) large rise delay.

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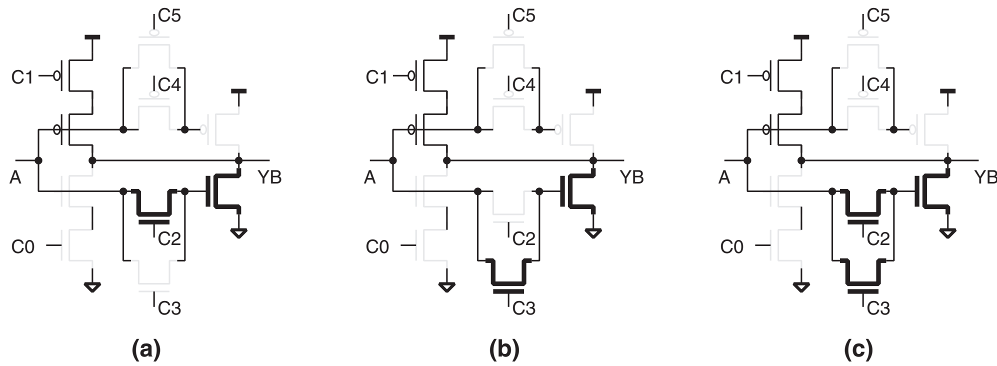

Fig. 6. Three different pass-gate configurations for the reconfigurable inverter structure: (a) C2 only ON, (b) C3 only ON, and (c) C2 and C3 ON. By swapping the pass-gate configuration, transistor with RTN can be identified. The frequency difference of (a) and (b) configurations gives the mismatch of two adjacent devices.

rate similar to the subthreshold slope factor which is typically several tens mV per decade. During the discharging phase, on the other hand, gate–source voltage remains zero thus the off-resistance does not change much. As the oscillation period is much smaller than the RC time constant, node "N" voltage is maintained to a value close to "L" which is determined by the off-resistance ratio between charging and discharging phases. Similarly, when the pMOSFET pass-gates are turned off as in Fig. 5(b) configuration, node "P" voltage is maintained to a value close to "H" making the pull-up pMOSFET off.

The three configurations for the structure Fig. 5(b) is shown in Fig. 6. Two pass-gates in parallel of the reconfigurable inverter allows us to measure device mismatch directly by taking the difference between the frequencies by turning one of the two parallel pass-gates ON and the other OFF, and vice versa. Device identification with RTN is done by observing frequency fluctuation for each of the configurations of Fig. 6. If the Fig. 6(a) configuration shows RTN induced variability and the other configurations does not, it is concluded that the RTN is occurring at the C2 device. Similarly, if Fig. 6(b) configuration only shows RTN, then the RTN is occurred at the C3 device. This way nMOSFET identification is done by reconfiguring the inhomogeneous stage of an inhomogeneous structure. pMOSFET identification is done in the same way as nMOSFET identification.

3. Test chip design and measurement results

3.1 Test chip design

A test chip is fabricated in a 65-nm process to validate our proposed structure. The process features one poly layer, 12 metal layers, copper wiring, and low-K insulating material techniques. The physical gate oxide thickness is 1.7 nm. Figure 7 shows the chip micrograph, the layout of the reconfigurable RO and the controller. The inverter cell has the structure shown in Fig. 4(b) and is designed with the same height as that of the standard cells to allow conventional cell based design. This approach reduces implementation and design cost. The proposed RO thus can be embedded in any digital circuit. The number of stages for the implemented RO is 127. The oscillation wave is divided by 4 inside the chip and then output outside the chip. Output frequency is around 750 kHz at 0.8 V supply for an inhomogeneous configuration. The frequency is counted using an external counter. The sizes of pMOSFET and nMOSFET are 360 and 240 nm, respectively. The area of our proposed RO with the controller is 0.0085 mm^2. With the proposed reconfigurable RO, 252 nMOSFET-sensitive inhomogeneous configurations and 252 pMOSFET-sensitive inhomogeneous configurations are achieved. In order to obtain the above number of samples, the conventional approach[29,31] would require 504 ROs in total. Considering 13-stage ROs, the proposed RO consumes only 5% area that of the conventional approach. Please note that only the RO area is compared here. The conventional approach puts the RO instances to several locations of the chip, thus routing and placing the ROs will increase area overhead. Besides, with small stage ROs, the oscillation frequency needs to be divided on-chip requiring additional circuitry.

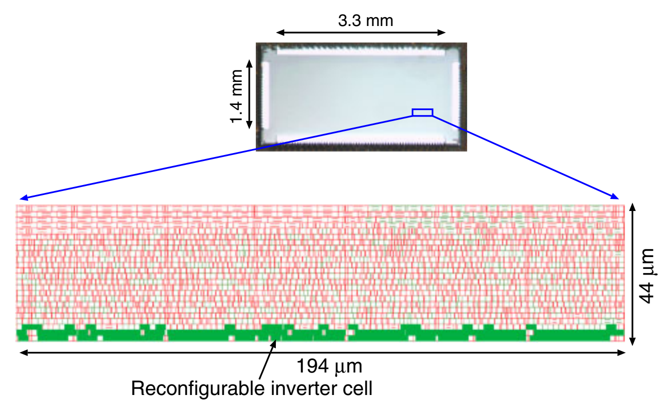

Fig. 7. (Color online) Chip micrograph and layout of the proposed reconfigurable ring oscillator.

Sensitivities are calculated for each of the configurations for the proposed RO using post-layout simulation. For an nMOSFET-sensitive inhomogeneous configuration using Fig. 5(b) structure, 18 times of sensitivity increase for the nMOSFET pass-gate and 24 times of sensitivity increase for the pull-down nMOSFET are achieved compared with the other nMOSFETs in the RO. Supply voltage of 0.8 V is used in the simulation. For pMOSFET-sensitive inhomogeneous configuration using Fig. 5(c) structure, 14 times of sensitivity increase for the pMOSFET pass-gate and 19 times of sensitivity increase for the pull-up pMOSFET are achieved compared with the other pMOSFETs.

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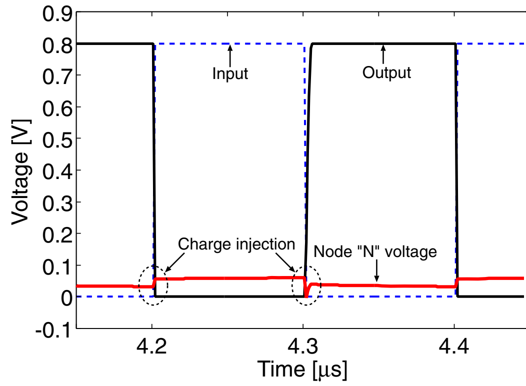

Fig. 8. (Color online) Simulated waveform of the nMOSFET pass-gate output for the inverter structure in Fig. 5(c). Input and output signals are also plotted. AC signal of 5 MHz is applied to the input.

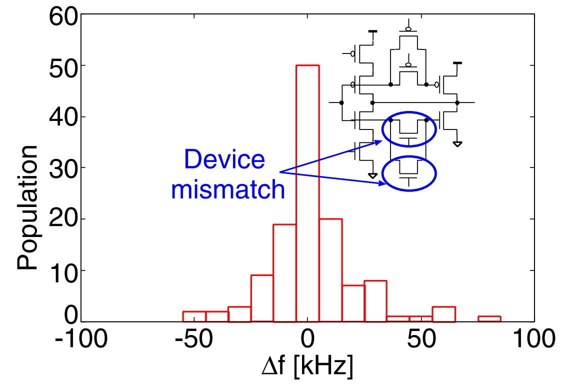

Fig. 9. (Color online) Histogram of frequency difference for two nMOSFET pass-gate configurations in the inhomogeneous stage. Frequency difference represents the device mismatch of the two nMOSFET pass-gates.

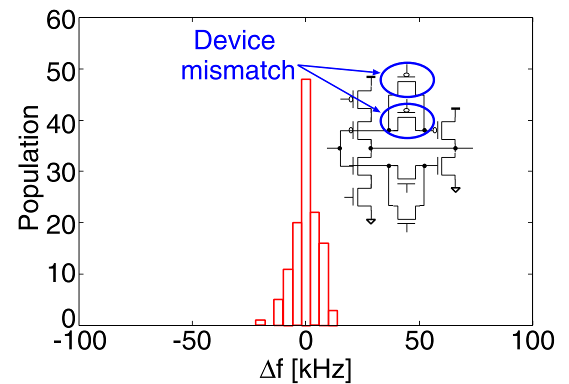

Fig. 10. (Color online) Histogram of frequency difference for two pMOSFET pass-gate configurations in the inhomogeneous stage. Frequency difference represents the device mismatch of the two pMOSFET pass-gates.

Next, voltage characteristics of nodes "N" and "P" are simulated for the reconfigurable inverter cell using RC extracted netlist. Figure 8 shows the simulation results of node "N" for Fig. 5(c) configuration under AC condition at 0.8 V operation. AC signal of 5 MHz is applied to the input. The off-resistance ratio between charging and discharging phases is around 14 times making the node "N" voltage 1/15 of the supply voltage $V_{\rm dd}$. Node "N" voltage remains around 0.05 V which is small enough compared with the nMOSFET threshold voltage. Small amount of voltage fluctuation occurs at node "N" during the switching due to the coupling capacitances between the inverter input "A" and output "YB" nodes. This voltage fluctuation is also small enough compared with the threshold voltage. Similarly, when the pMOSFET pass-gates are turned off as in Fig. 5(b), node "P" voltage fluctuates around 750 mV.

Below we show several measurement results of WID static variation and RTN induced variation at 0.8 V supply voltage to validate our proposed RO structure. By changing the supply voltage, various properties of these variations can be extracted which is our future work.

3.2 Device mismatch measurement

Figure 9 shows the histogram of frequency differences when C2 and C3 pass-gates (nMOSFET pass-gates) are ON alternately. The frequency difference is the function of the device mismatch between these two transistors. Thus, device mismatch is directly measured with our proposed structure. Figure 10 shows the histogram when C4 and C5 pass-gates (pMOSFET pass-gates) are ON alternately. Both of the distributions are Gaussian suggesting we could measure the random variation. These variations can be further analyzed to extract the underlying variation sources such as threshold voltage by sensitivity based analysis.[28,29]

Assuming threshold voltage to be the main source of static device variability, oscillation frequencies for an nMOSFET-sensitive inhomogeneous configuration can be expressed with the following linear approximations:

$$f_{n,1} = f_{n,1_0} + k_{n,1}\Delta V_{\rm thn,1} + \alpha, \quad (3.1)$$

$$f_{n,2} = f_{n,2_0} + k_{n,2}\Delta V_{\rm thn,2} + \alpha. \quad (3.2)$$

Here, $f_{n,1}$ is the frequency for the first nMOSFET pass-gate (C2 pass-gate) only being ON and $f_{n,2}$ is the frequency for the second nMOSFET pass-gate (C3 pass-gate) only being ON. $f_{n,1_0}$ and $f_{n,2_0}$ are nominal frequency values. $k_{n,1}$ and $k_{n,2}$ are sensitivity coefficients to the nMOSFET pass-gate threshold voltage variations. α is the sum of delay contributions of stages other than the inhomogeneous stage. As the delay contribution from each stage is much smaller than the inhomogeneous stage, random variation effect of other stages is expected to be canceled out because of large number of stages. Thus, α here is assumed to be constant. If we layout the two nMOSFET pass-gates to be identical, $f_{n,1_0}$ and $f_{n,2_0}$ become equal. Similarly sensitivity coefficients $k_{n,1}$ and $k_{n,2}$ are equal too. From the above two equations, the relationship between frequency mismatch and threshold voltage mismatch for the two different pass-gate inhomogeneous configurations can be obtained as follows:

$$\Delta f_n = f_{n,1} - f_{n,2} = k_n(\Delta V_{\rm thn,1} - \Delta V_{\rm thn,2}). \quad (3.3)$$

Here, Δf_n is the frequency mismatch for two pass-gate based inhomogeneous configurations, and k_n is the sensitivity coefficient to each of the pass-gate threshold voltage. Next, by scanning the inhomogeneous stage and measure each configurations frequency mismatch as shown in Fig. 3, threshold voltage variation ($\sigma_{V_{\rm thn}}$) for nMOSFET is calculated as follows:

$$\sigma^2_{\Delta f_n} = k_n^2(\sigma^2_{V_{\rm thn}} + \sigma^2_{V_{\rm thn}}), \quad (3.4)$$

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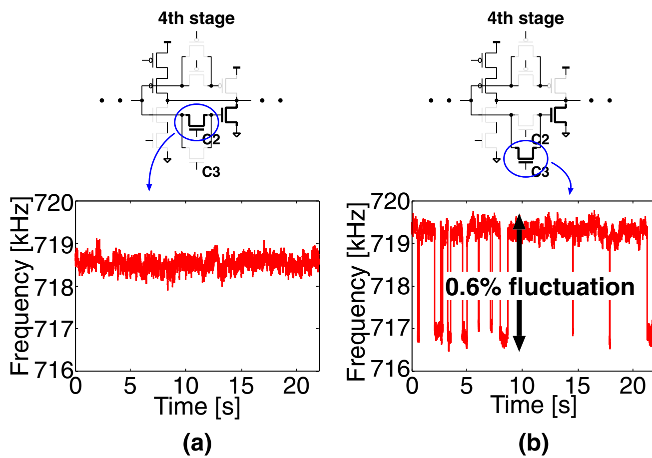

Fig. 11. (Color online) An example of nMOSFET identification with RTN: (a) C2 pass-gate ON, C3 pass-gate OFF, and (b) C2 pass-gate OFF, C3 pass-gate ON. C3 nMOSFET pass-gate of the 4th stage is identified with RTN occurring.

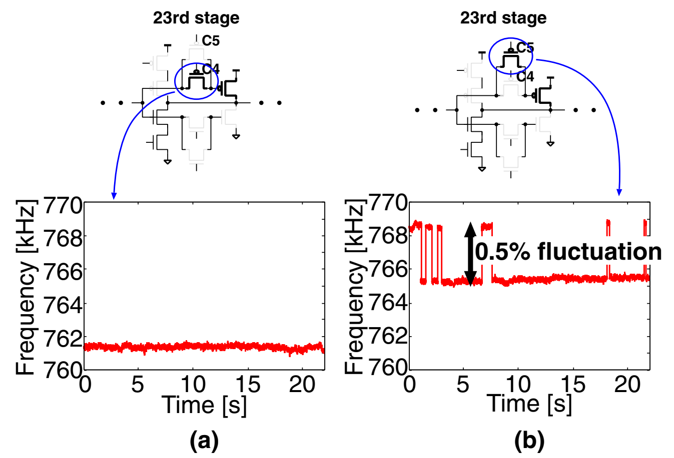

Fig. 12. (Color online) An example of pMOSFET identification with RTN: (a) C4 pass-gate ON, C5 pass-gate OFF, and (b) C4 pass-gate OFF, C5 pass-gate ON. C5 pMOSFET pass-gate of the 23rd stage is identified with RTN occurring.

$$\sigma_{V_{\text{thn}}} = \frac{\sigma_{\Delta f_n}}{\sqrt{2k_n}}. \tag{3.5}$$

pMOSFET threshold voltage variation can be calculated the same way. Calculating k_n for pass-gate using post-layout simulation, the amounts of WID variability for nMOSFET and pMOSFET threshold voltages are calculated to be 6.9 and 3.2%, respectively. nMOSFET variability is measured to be larger than that of pMOSFET which agrees with the device array based measurement results.[18,30] Thus, area-efficient device level measurement of static variation is performed with our proposed reconfigurable RO.

3.3 RTN measurement

3.3.1 Device identification In order to measure RTN effects, RO frequency for each inhomogeneous configuration is measured for 22 s with an integration time of 1 ms. In this test chip, there are 126 stages of reconfigurable inverter cells thus 252 configurations of inhomogeneous RO structure for nMOFSET and 252 configurations of inhomogeneous RO structure for pMOSFET can be measured. For each inhomogeneous configuration measurement (Fig. 3), the pass-gate configuration in the inhomogeneous stage is swapped to identify devices with RTN. 67 inhomogeneous configurations out of 252 configurations showed RTN induced frequency fluctuation for nMOSFET. For pMOSFET, the number of configurations showing RTN induced variability is 69. Figure 11 shows one example of frequency fluctuations observed over time for an nMOSFET-sensitive inhomogeneous configuration. Figure 11(a) shows the frequency fluctuation when the C2 pass-gate is turned ON and C3 pass-gate is turned OFF. Figure 11(b) shows the frequency fluctuation for an opposite configuration (C2 OFF and C3 ON). C2 pass-gate ON configuration shows no binary fluctuation whereas C3 pass-gate ON configuration shows binary fluctuation which indicates that C3 pass-gate is RTN affected. Figures 12(a) and 12(b) show two examples of frequency fluctuation for an pMOSFET-sensitive inhomogeneous configuration. RTN is observed when C4 transistor is turned OFF and C5 transistor is turned ON referring that C5 transistor is RTN affected. Thus, by changing the configuration of our reconfigurable RO, we can identify devices with RTN induced variability which will help us characterize the effects accurately.

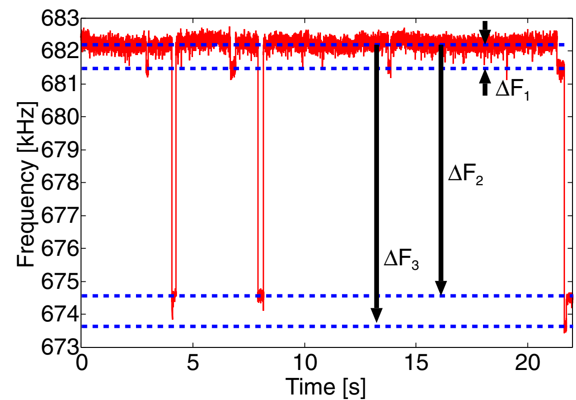

Fig. 13. (Color online) Frequency fluctuation over time showing complex RTN occurring on an nMOSFET pass-gate.

3.3.2 Multiple RTN Now that we can identify transistors with RTN occurring on it, we can further explore and investigate devices with multiple RTN, different time constants and frequency fluctuations which will help us to build accurate models. In Fig. 13, we show one example of an nMOSFET device showing multiple RTN. Several states are being observed. Relatively larger frequency fluctuation of 1.42% is observed in this case. Figure 14 shows the histogram of the frequency fluctuation of Fig. 13. Four states are clearly distinguishable. Device identification allows us accurate characterization of RTN induced variability.

3.3.3 CDF We have measured frequency over time for 252 inhomogeneous configurations for nMOSFET and pMOSFET characterization each. Figures 15 and 16 show cumulative distribution function (CDF) of frequency fluctuation for nMOSFET and pMOSFET, respectively. Frequency fluctuations for RTN and static process variation are plotted.

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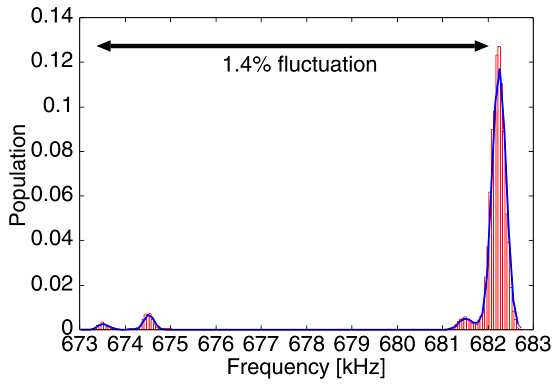

Fig. 14. (Color online) Histogram of frequency fluctuation of Fig. 13. Four states are clearly distinguishable showing possibility of two traps being involved.

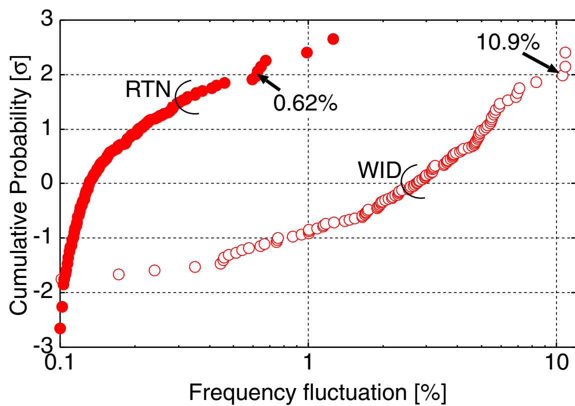

Fig. 15. (Color online) CDF of RTN induced frequency fluctuation and static process variation induced frequency fluctuation for nMOSFET-sensitive inhomogeneous configuration. Long tail exists for RTN induced fluctuation.

RTN induced frequency fluctuation is calculated by $\Delta f/f_{\max}$ where Δf is the difference between the maximum and minimum frequencies and $f_{\max}$ is the maximum frequency. Process variation induced frequency fluctuation is calculated by $(|\mu_f - f|)/\mu_f)$ where μ_f is the average value of frequency measurements. In the case of RTN induced frequency fluctuation, long tails are observed for both the nMOSFET and pMOSFET-sensitive frequency fluctuations. nMOSFET variation is larger than that of pMOSFET. For nMOSFET, maximum of 1.42% frequency fluctuation is observed. Whereas for pMOSFET, maximum of 0.53% frequency fluctuation is observed.

Next, we compare RTN induced frequency fluctuation with static process variation induced frequency fluctuation. With the proposed RO, frequency distribution for inhomogeneous configuration can be measured for nMOSFET and pMOSFET separately. Figure 15 plots the CDF of RTN induced frequency fluctuation and process variation induced frequency fluctuation for nMOSFET. At 2σ level, RTN induced fluctuation is 0.62% whereas process variation induced fluctuation is 10.9%. Thus, RTN induced fluctuation is 5.7% of process variation induced fluctuation at 2σ level. Similarly, Fig. 16 plots the CDF of RTN and process variation induced frequency fluctuation for pMOSFET. At 2σ

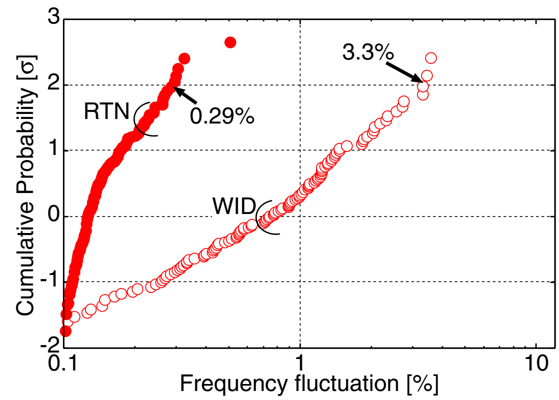

Fig. 16. (Color online) CDF of RTN-induced frequency fluctuation and static process variation induced frequency fluctuation for pMOSFET-sensitive inhomogeneous configuration. Long tail exists for RTN induced fluctuation.

level, RTN induced fluctuation is 0.29% and process variation induced fluctuation is 3.3%. RTN induced fluctuation is 8.8% of process variation induced fluctuation. Measured data from multiple ROs will give 3σ, 4σ level comparison. Implementing the proposed reconfigurable RO with various device sizes will give us more information on the relationship between device size and RTN effect. For finer process, RTN variability is reported to be increasing. Thus, RTN is a big concern for reliable operation of future LSI.

4. Conclusion and future work

An area-efficient reconfigurable ring oscillator circuit structure is proposed for characterizing static and dynamic variations at both device and circuit level. The proposed circuit consists of inverter cells whose pull-up and pull-down networks can be reconfigured. Device level variation measurement is done using an inhomogeneous structure and by reconfiguring the inhomogeneous stage. Measurement results from a 65-nm test chip confirms the validity of the proposed structure.

With the proposed circuit structure, transistor-by-transistor characteristics of both static and dynamic variations can be characterized. Thus, the proposed circuit enables to investigate and understand on the interactions between these variations under dynamic switching condition. The proposed structure can be used for transistor-by-transistor NBTI characterization too. The proposed circuit can be used to understand the complex relationships between different device phenomena which will help circuit designers to establish models and tools. Furthermore, the proposed RO can be implemented with very small area thus can be used as on-chip variation sensors.

Acknowledgments

The authors would like to express their thanks to Takashi Matsumoto for his advises in RTN measurement and analysis. The VLSI chip in this study was fabricated in the chip fabrication program of the VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with STARC. This work was partly supported by JSPS KAKENHI Grant Numbers 22300016 and 25·6432.

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