



Ralf  
Jesse

# **ARM Cortex-M3 Mikrocontroller**

## **Einstieg und Praxis**

# Stichwortverzeichnis

## Numerisch

7-Segment-Anzeige 223

## A

A/D-Wandler 54

Acorn Computers 53

Advanced RISC Machines 53

Analog Comparator Controller (ACC) 425, 442

CMSIS

ACC\_Configure() 445

ACC\_GetComparisonResult() 446

ACC\_SetComparisonPair() 445

Analog Comparator Converter Controller (ACC)

ACC Analog Control Register (ACC\_ACR) 443

ACC Control Register (ACC\_CR) 443

ACC Interrupt Disable Register (ACC\_IDR) 443

ACC Interrupt Enable Register (ACC\_IER) 443

ACC Interrupt Mask Register (ACC\_IMR) 443

ACC Interrupt Status Register (ACC\_ISR) 443

ACC Mode Register (ACC\_MR) 443

ACC Write Protect Mode Register (ACC\_WPMR) 443

ACC Write Protect Status Register (ACC\_WPSR) 443

Analog-to-Digital Converter (ADC) 425, 448

ADC Analog Control Register (ADC\_ACR) 450, 457

ADC Analog Extended Mode Register (ADC\_EMR) 451

ADC Channel Data Register (ADC\_CDR) 450

ADC Channel Data Register (ADC\_CDRx) 456

ADC Channel Disable Register (ADC\_CHDR) 450, 454

ADC Channel Enable Register (ADC\_CHER) 450, 454

ADC Channel Gain Register (ADC\_CGR) 450

ADC Channel Last Converted Data Register (ADC\_LCDR) 450

ADC Channel Offset Register (ADC\_ADC\_COR) 456

ADC Channel Offset Register (ADC\_COR) 450

ADC Channel Sequence 1 Register (ADC\_SEQR1) 450

ADC Channel Sequence 2 Register (ADC\_SEQR2) 450

ADC Channel Sequence Register 1 und 2 (ADC\_SEQR1 und ADC\_SEQR2) 453

ADC Channel Status Register (ADC\_CHSR) 450, 454

ADC Compare Window Register (ADC\_CWR) 450, 455

ADC Control Register (ADC\_CR) 449, 451

ADC Extended Mode Register (ADC\_EMR) 450

ADC Interrupt Disable Register (ADC\_IDR) 450, 455

ADC Interrupt Enable Register (ADC\_IER) 450, 455

ADC Interrupt Mask Register (ADC\_IMR) 450, 455

ADC Interrupt Status Register (ADC\_ISR) 450, 455

ADC Last Converted Data Register (ADC\_LCDR) 454

ADC Mode Register (ADC\_MR) 449, 451

ADC Overrun Status Register (ADC\_OVER) 450, 455

- ADC Write Protect Mode Register  
(ADC\_WPMR) 450, 457
- ADC Write Protect Status Register  
(ADC\_WPSR) 450, 457
- Apple Computer 53
- Application Programming Interfaces (API) 55
- Arduino 37
- ARM EABI 29
- ARM Holdings PLC 53
- As-if-Regel 312
- ATMEL Studio 6 30
- Atollic TrueSTUDIO 29
- Ausgabeformat
  - elf32-little 89
  - elf32-littlearm 89
  - ihex 89
- Ausgabeformate
  - elf32-littlearm 107
- B**
- Bare Metal System 119
- Bare-Metal-System 355
- Baudrate 483
- BCD
  - Binary Coded Decimal 226
- BCD-Code 226
- Betriebsspannung
  - maximal zulässige 147
- Bibliothek
  - libc 61
  - newlib 61
- Binary File Descriptor 107
- Binary File Descriptor (BFD) 100
- Bipolar-Transistoren 181
- Bitfeld 527
- Borland 32
- Bouncing 272
- Brown Out Detection 264
- Brown-out-Detektor 153
- Bus
  - serieller 54
- C**
- CAN siehe Serieller Bus
- Chip Identifier 158
  - Chip ID Extension Register  
(CHIPID\_EXID) 159
  - Chip ID Register (CHIPID\_CIDR) 159
- Clock Generator 239, 252
- Main Clock (MCK) 252, 253, 257
- Main Clock Oscillator Section 257
- Master Clock (MCK) 252, 253, 257
- Phase-Lock Loops (PLLA und PLLB) 257
- PLL Clock 252
- Slow Clock (SLCK) 252, 253
- CMSIS 53, 54
- CMSIS-Funktion
  - Übersicht 248
- Code::Blocks 32
- Compiler
  - Optimierungen 312
- Compiler-Toolchain 56
- CooCox CoIDE 31
- Cortex Microcontroller Software Interface  
Standard 53
- Cortex Microcontroller Software Interface  
Standard siehe CMSIS
- CPU 54
- Cross Compiling 32
- Cross-Compiling 33
- Current Sinking 150, 174
- Current Sourcing 150, 174
- D**
- D/A-Umsetzer 54
- Datenwortlänge 484
- Definition
  - Begriff 376
- Deklaration
  - Begriff 376
- Digital-to-Analog Converter Controller  
(DACC) 425
  - CMSIS
    - DACC\_Initialize() 427, 429
    - DACC\_SetConversionData() 429
    - DACC\_WriteBuffer() 430
  - DACC Channel Disable Register  
(DACC\_CHDR) 427
  - DACC Channel Enable Register  
(DACC\_CHER) 427
  - DACC Channel Status Register  
(DACC\_CHSR) 427
  - DACC Control Register (DACC\_CR) 427
  - DACC Conversion Data Register  
(DACC\_CDR) 427
  - DACC Interrupt Analog Current  
Register (DACC\_ACR) 427

DACC Interrupt Disable Register  
(DACC\_IDR) 427  
 DACC Interrupt Enable Register  
(DACC\_IER) 427  
 DACC Interrupt Mask Register  
(DACC\_IMR) 427  
 DACC Interrupt Status Register  
(DACC\_ISR) 427  
 DACC Mode Register (DACC\_MR) 427  
 DACC Write Protect Mode Register  
(DACC\_WPMR) 427  
 DACC Write Protect Status Register  
(DACC\_WPSR) 427  
 Diskrete Größe 194  
 Dokumentation  
 DOC 6500 142  
 Dot-Matrix-Anzeige 224

**E**

EABI 40  
 Eclipse 32, 56  
 Workspace 43  
 Einzelschrittmodus 550  
 Elektrische Daten  
 SAM3S 145  
 Elektrische Spannung  
 Formelzeichen 147  
 maximale 147  
 Elektronik  
 kirchhoffsches Gesetz 178  
 ohmsches Gesetz 178  
 Embedded Application Binary Interface siehe  
 EABI  
 Embedded Linux 119  
 emIDE 32  
 Enhanced Embedded Flash Controller 258  
 Entwicklungsplattform siehe IDE  
 Entwicklungsumgebung siehe IDE  
 Entwicklungsumgebungen 27  
 Ereignis  
 asynchron 240  
 Polling 240  
 synchron 240  
 Externe Referenz 84

**F**

Feldeffekt-Transistor 190  
 Firmware 119

Fortè for Java 32  
 Frontend 85

**G**

gcc 56  
 General Purpose Input/Output Mode (GPIO)  
 siehe Parallel Input/Output Controller  
 (PIO-Controller)  
 Glitch 272  
 GNU 56  
 GNU Compiler Collection 56  
 GPIO  
 General Purpose Input/Output 151  
 QTouch-Bibliothek 285  
 Größe  
 analoge siehe kontinuierliche  
 digitale siehe diskrete  
 diskrete 165, 194  
 Größen  
 diskrete bzw. analoge 425  
 physikalische 425

**H**

High Speed MultiMedia Card Interface  
 (HSMCI) 515, 538  
 HSMCI Block Completion Signal  
 Timeout Register  
 (HSMCI\_CSTOR) 543  
 HSMCI Block Register (HSMCI\_BLKCR)  
 543  
 HSMCI Command Register  
 (HSMCI\_CMDR) 542  
 HSMCI Control Register (HSMCI\_CR)  
 541  
 HSMCI Data Timeout Register  
 (HSMCI\_DTOR) 542  
 HSMCI Mode Register (HSMCI\_MR)  
 541  
 HSMCI SDCard/SDIO Register  
 (HSMCI\_SDCR) 539, 542  
 Hysterese 445

**I**

I<sup>2</sup>C siehe Serieller Bus  
 IAR Workbench 28, 55  
 IBM (International Business Machines) 32  
 IBM Visual Age 32  
 ICE 34

**I**

- IDE
  - Mac OS X 39
  - Windows 39
- IDE (Integrated Development Environment)
  - 27
- IEEE 1149.1
  - JTAG 34
- In-Circuit-Emulation siehe ICE
- In-Circuit-Emulator (ICE) 550
- Inhaltsassistent 161
- Initialisierung
  - Begriff 377
- In-System-Programmer 64
- Intellectual Property (IP) 53
- Interface
  - parallele 477
  - serielle 477
- Interface siehe Schnittstelle
- Inter-Integrated Circuit (I2C) siehe Two-wire
  - Interface (TWI)
- Interrupt 152
  - Interrupt Pending Register 246
  - Interrupt Request 240
  - Interrupt-Service-Routinen 240
  - IRQ 240
  - NMI 240
  - Non-maskable Interrupt 240
  - Program Counter 246
- Interrupt-Service-Routine (ISR) 301
- Interrupt-Service-Routine ISR
  - Erläuterung 251

**J**

- Java 31, 38
- Java Runtime Environment siehe Java
- Java-Laufzeitumgebung
  - JRE (Java Runtime Environment) 32
- Java-Laufzeitumgebung siehe Java
- Joint Test Action Group siehe JTAG
- JTAG 34
- JTAG ID 69

**K**

- Keil Microsystems 55
- Keil  $\mu$ Vision 28
- Konfigurationsdatei
  - Debugger 109

**L**

- LC-Display
  - HD44780 200
  - KS0066 200
  - KS0070 200
  - LCD 199
- Linker
  - Linkerscript 84
- Linux-Wrapper
  - Cywin 39
  - MinGW 39
- Local Loopback 486
- Loopback
  - local 486
  - remote 486

**M**

- make 59
  - Makefiles 59
  - Whitespace 59
- Maskieren 161
- MCU 141
- Mentor Sourcery Codebench 28
- Metal Oxid Semiconductor 190
- Microcontroller Unit 141
- Microsoft Visual Studio 30
- MOSFET 190

**N**

- Nested Vector Interrupt Controller (NVIC)
  - 239, 240
    - INTID 243
    - Level Detection 241
    - Level-sensitive Interrupt 243
    - Non-nested Interrupts 241
    - NVIC Interrupt Active Bit Register
      - (IABR0, IABR1) 243
    - NVIC Interrupt Clear-enable Register
      - (ICER0, ICER1) 242
    - NVIC Interrupt Clear-pending Register
      - (ICPR0, ICPR1) 242
    - NVIC Interrupt Priority Register
      - (IPR0..IPR8) 243
    - NVIC Interrupt Set Enable Register
      - (ISER0, ISER1) 242
    - NVIC Interrupt Set-pending Register
      - (ISPR0, ISPR1) 242
    - Software Interrupt 243

- Software Trigger Interrupt Register (STIR) 243
- Software-Interrupts 252
- Tail Chaining 241, 247
- NetBeans 31
- Nullmodemkabel 36
- NVIC 54
  - Interrupt Set-enable Register 275
  - Nested Vector Interrupt Controller 275
- NVIC-Register
  - Überblick 244
- O**
- Objekt-Datei 84
- Olimex-Board SAM3-P256 33
- Opto-Isolator siehe Optokoppler
- Optokoppler 191, 196
- P**
- Parallel Input/Output Controller (PIO Controller)
  - General Purpose Input/Output (GPIO) 168
  - Peripheriekomponente 168
  - PIO Output Status Register (REG\_PIO\_OSRA/B/C) 167
  - PIO Pad Pull-down Status Register (REG\_PIOA\_PPDSR, REG\_PIOB\_PPDSR, REG\_PIOC\_PPDSR) 169
  - PIO Status Register (REG\_PIO\_PSR) 167
  - REG\_PIOA\_PUSR, REG\_PIOB\_PUSR, REG\_PIOC\_PUSR) 169
- Parallel Input/Output Controller (PIO-Controller) 265
- Parallel Input/Output Controller (PIO-Controller)
  - Flankenerkennung 275
  - Glitches, Störimpulse, Prellen 272
  - GPIO-Modus 265
  - Multi-Drive Option 278
  - Multiplex-Modus 265
  - Open Drain 278
  - Parallel-Capture-Modus 286
  - PIO Additional Interrupt Mode Disable Register (REG\_PIOx\_AIMDR) 275
  - PIO Additional Interrupt Mode Enable Register (REG\_PIOx\_AIMER) 275
  - PIO Additional Interrupt Mode Mask Register (REG\_PIOx\_AIMMR) 276
  - PIO Capture Mode Register (REG\_PIOx\_PCMR) 286
  - PIO Clear Output Data Register (REG\_PIOx\_CODR) 271
  - PIO Edge Select Register (REG\_PIOx\_ESR) 276
  - PIO Edge/Level Status Register (REG\_PIOx\_ELSR) 276
  - PIO Fall/Rise – Low/High Status Register (REG\_PIOx\_FRLHSR) 276
  - PIO Falling Edge/Low Level Select Register (REG\_PIOx\_FELLSR) 276
  - PIO Input Filter Disable Register (REG\_PIOx\_IFDR) 273
  - PIO Input Filter Enable Register (REG\_PIOx\_IFER) 273
  - PIO Input Filter Slow Clock Disable Register (REG\_PIOx\_IFSCDR) 273
  - PIO Input Filter Slow Clock Enable Register (REG\_PIOx\_IFSCER) 273
  - PIO Input Filter Slow Clock Status Register (REG\_PIOx\_IFSCSR) 273
  - PIO Input Filter Status Register (REG\_PIOx\_IFSR) 273
  - PIO Interrupt Disable Register (REG\_PIOx\_IDR) 275
  - PIO Interrupt Enable Register (REG\_PIOx\_IER) 275
  - PIO Interrupt Mask Register (REG\_PIOx\_IMR) 275
  - PIO Interrupt Status Register (REG\_PIOx\_ISR) 275
  - PIO Level Select Register (REG\_PIOx\_LSR) 276
  - PIO Lock Status Register (REG\_PIOx\_LOCKSR) 284
  - PIO Multi-driver Disable Register (REG\_PIOx\_MDDR) 279

- PIO Multi-driver Enable Register  
(REG\_PIOx\_MDER) 279
- PIO Multi-driver Status Register  
(REG\_PIOx\_MDSR) 279
- PIO Output Data Status Register  
(REG\_PIOx\_ODSR) 271, 283
- PIO Output Disable Register  
(REG\_PIOx\_ODR) 270
- PIO Output Enable Register  
(REG\_PIOx\_OER) 270
- PIO Output Status Register  
(REG\_PIOx\_OSR) 270
- PIO Output Write Disable Register  
(REG\_PIOx\_OWDR) 283
- PIO Output Write Enable Register  
(REG\_PIOx\_OWER) 283
- PIO Output Write Status Register  
(REG\_PIOx\_OWSR) 284
- PIO Pad Pull-down Disable Register  
(REG\_PIOx\_PPDDR) 280
- PIO Pad Pull-down Enable Register  
(REG\_PIOx\_PPDER) 280
- PIO Pad Pull-down Status Register  
(REG\_PIOx\_PPDSR) 280
- PIO Parallel Capture Interrupt Disable Register (REG\_PIOx\_PCIDR) 288
- PIO Parallel Capture Interrupt Enable Register (REG\_PIOx\_PCIER) 288
- PIO Parallel Capture Interrupt Mask Register (REG\_PIOx\_PCIMR) 288
- PIO Parallel Capture Interrupt Status Register (REG\_PIOx\_PCISR) 287, 288
- PIO Parallel Capture Reception Holding Register (REG\_PIOx\_PCRHR) 287, 289
- PIO Peripheral ABCD Select Register 1  
(REG\_PIOx\_ABCDSR<sub>1</sub>) 281
- PIO Peripheral ABCD Select Register 2  
(REG\_PIOx\_ABCDSR<sub>2</sub>) 281
- PIO Pin Data Status Register  
(REG\_PIOx\_PDSR) 271
- PIO Pull Up Disable Register  
(REG\_PIOx\_PUDR) 279
- PIO Pull Up Enable Register  
(REG\_PIOx\_PUER) 279
- PIO Pull Up Status Register  
(REG\_PIOx\_PUSR) 279
- PIO Rising Edge/High Level Select Register  
(REG\_PIOx\_REHLSR) 276
- PIO Schmitt Trigger Register  
(REG\_PIOx\_SCHMITT) 285
- PIO Set Output Data Register  
(REG\_PIOx\_SODR) 271
- PIO Slow Clock Divider Debouncing Register (REG\_PIOx\_SCDR) 273
- PIO Write Protect Mode Register  
(REG\_PIOx\_WPMR) 282
- PIO Write Protect Status Register  
(REG\_PIOx\_WPSR) 283
- PIOA, B, C Input/Output Controller  
(PIOA, PIOB, PIOC) 265
- Spannungspiegel, Level Detection 275
- Write Protect Violation Source  
(PIO\_WPSR\_WPVSRC) 283
- Write Protect Violation Status  
(PIO\_WPSR\_WPVV) 283
- Write Protection Enable (WPEN) 270
- Parität 484
- Parser 93
- Peripheral DMA Controller (PDC) 391
- Receive Counter Register  
(PERIPH\_RCR) 394
- Receive Next Counter Register  
(PERIPH\_RNCR) 394
- Receive Next Pointer Register  
(PERIPH\_RNPR) 394
- Receive Pointer Register  
(PERIPH\_RPR) 394
- Transfer Control Register  
(PERIPH\_PTCR) 395
- Transfer Status Register  
(PERIPH\_PTSR) 395
- Transmit Counter Register  
(PERIPH\_TCR) 394
- Transmit Next Counter Register  
(PERIPH\_TNCR) 394
- Transmit Next Pointer Register  
(PERIPH\_TNPR) 394
- Transmit Pointer Register  
(PERIPH\_TPR) 394
- Phased Lock Loop siehe Power Management Controller (PMC)

- Phasenregelschleife siehe Power Management Controller (PMC)
- PIO 54
- PIO-Controller 152
- PMC Clock Generator (CKGR)
  - Main Clock Frequency Register (CKGR\_MCFR) 255
  - PLLA/PLLB (CKGR\_PLLAR und CKGR\_PLLBR) 255
  - PMC Clock Generator Main Oscillator Register (CKGR\_MOR) 255
- Power Management Controller (PMC) 239, 256
  - Clock Failure Detector Event (CFDEV) 260
  - Fast Startup 259
  - Free Running Processor Clock (FCLK) 258
  - Highspeed Clock (HCLK) 258
  - Main Clock (MCK) 259
  - Master Clock (MCK) 259
  - Peripheral Clock Controller (PCK) 258
  - Peripheral Clock Disable Register (PMC\_PCDRx) 258
  - Peripheral Clock Enable Register (PMC\_PCErX) 258
  - PLLA, PLLB 259
  - PMC Clock Generator Main Oscillator Register (CKGR\_MOR) 264
  - PMC Master Clock Register (PMC\_MCKR) 261
  - PMC Programmable Clock Register (PMC\_PCRx) 262
  - PMC Status Register (PMC\_SR) 260
  - PMC USB Clock Register (PMC\_USB) 262
  - PMC Write Protect Enable Bit (WPEN) 263
  - PMC Write Protect Mode Register (PMC\_WPMR) 263
  - PMC Write Protect Status Register (PMC\_WPSR) 263
  - Programmable Output Controller (PMC\_PCKx) 259
  - Slow Clock (SLCK) 259
  - System Clock (SysTick) 258
  - USB Clock Controller (UDPCK) 258
  - Wait for Event (WFE) 259
- Prellen 272
  - Tasten- oder Schalterprellen 125
- Pulse Width Modulation Controller (PWMC) 397
  - CMSIS
    - PWMC\_ConfigureChannel() 400
    - PWMC\_ConfigureChannelExt() 401
    - PWMC\_ConfigureClocks() 402
    - PWMC\_ConfigureComparisonUnit() 402
    - PWMC\_ConfigureEventLineMode() 402
    - PWMC\_ConfigureSyncChannel() 403
    - PWMC\_DisableChannel() 403
    - PWMC\_DisableChannelIt() 404
    - PWMC\_DisableIt() 404
    - PWMC\_DisableOverrideOutput() 404
    - PWMC\_EnableChannel() 403
    - PWMC\_EnableChannelIt() 404
    - PWMC\_EnableFaultProtection() 405
    - PWMC\_EnableIt() 404
    - PWMC\_EnableOverrideOutput() 404
    - PWMC\_FaultClear() 405
    - PWMC\_SetDeadTime() 405
    - PWMC\_SetDutyCycle() 406
    - PWMC\_SetFaultMode() 406
    - PWMC\_SetFaultProtectionValue() 407
    - PWMC\_SetOverrideValue() 407
    - PWMC\_SetPeriod() 407
    - PWMC\_SetSyncChannelUpdatePeriod() 408
    - PWMC\_SetSyncChannelUpdateUnlock() 408
    - PWMC\_WriteBuffer() 408
  - Peripheral DMA Controller (PDC) 399
    - Register
      - PWM Channel Duty Cycle Register (PWM\_CDTYx) 406
      - PWM Channel Duty Cycle Update Register (PWM\_CDTYx) 406
      - PWM Channel Period Register (PWM\_CPRDx) 407
      - PWM Channel Period Update Register (PWM\_CPRDUPDx) 407



**Q**

QNX Software Systems 32

**R**

RaspberryPi 37

Rational Software 32

Real Time Operating System 351

Real-time Clock (RTC) 314

RTC Calendar Alarm Register  
(RTC\_CALALR) 342

RTC Calendar Register (RTC\_CALR) 341

RTC Control Register (RTC\_CR) 340

RTC Interrupt Disable Register  
(RTC\_IDR) 343RTC Interrupt Enable Register  
(RTC\_IER) 343RTC Interrupt Mask Register  
(RTC\_IMR) 343RTC Status Clear Command Register  
(RTC\_SCCR) 343

RTC Status Register (RTC\_SR) 342

RTC Time Alarm Register  
(RTC\_TIMALR) 342

RTC Time Register (RTC\_TIMER) 341

RTC Valid Entry Register (RTC\_VER)  
344

Real-time Timer (RTT) 300

RTT Alarm Register (RTT\_AR) 302

RTT Status Register (RTT\_SR) 302

RTT Value Register (RTT\_VR) 302, 305

Real-timeClock (RTC)

RTC Mode Register (RTC\_MR) 340

Red Hat 32

Referenz

externe 84

REG\_PIOx\_WPMR 282

Remote Loopback 486

Reset 166

Reset Controller 152

Reset-Zustand 166

Retargeting 488, 494

Reverse Engineering 77

Rowley Associates CrossWorks for ARM 29

RTOS

Real Time Operating System 350

**S**

SAM Boot Assistant 64

SAM Boot Assistant siehe SAM-BA

SAM3S Software Package 57

SAM3S4

elektrische Daten 145

SAM3S4BA 34

SAM-BA 38

Schmitt-Trigger 284

Schnittstelle

Baudrate 483

Betriebsart Echo-Modus 486

Betriebsart Loopback 486

Datenwortlänge 484

Fehlererkennung, Framing-Fehler 488

Fehlererkennung, Kabelbruch 488

Fehlererkennung, Parität 487

Fehlererkennung, Überlauf, Overrun  
488

gerade Parität, even parity 484

Halb-Duplex 487

Hardware-Protokolle, Hardware  
Handshaking 485

Inter-Integrated Sound (I2S) 482

keine Parität, no parity 484

MARK Parity 484

parallele 477

Parität 484

Protokolle, Handshaking 485

RS-232 (EIA-232) 479

RS-485 (EIA-485) 481

Serial Peripheral Interface (SPI) 482

serielle 477

Simplex 487

Software-Protokolle, Software  
Handshaking 485

SPACE Parity 484

Start- und Stoppbits 484

Synchronous Serial Controller (SSC)  
482

Two-Wire-Interface (TWI) 482

ungerade Parität, odd parity 484

Universal Asynchronous Receiver

Transceiver (UART) 489

Universal Synchronous Asynchronous  
Receiver Transceiver (USART)

496

Voll-Duplex 486

Schreibweise

Widerstände 178

SD-Karte

Simplified Specification 515

Semihosting 494

- Semihosting siehe Retargeting
  - Serial Peripheral Interface (SPI) 515
    - SPI Chip Select Register (SPI\_CSR) 520
    - SPI Mode Register (SPI\_MR) 520
  - Serieller Bus 54
  - Single Step Tracing 550
  - Slow Clock (SLCK) 304
  - Speichersegment
    - BSS 103
    - Heap 103
    - Stack 103
  - ST Visual Developer 31
  - Standard-Compiler
    - Optionen (Übersicht) 83
  - Standardfunktion 61
  - Statemachine siehe Statusmaschine
  - Statusmaschine 320, 328
  - STMicroelectronics STVD
    - ST Visual Developer 31
  - Störimpuls 272
  - Supply Control Register
    - SUPC\_CR 253
  - Supply Controller 153
  - Supply Controller (SUPC) 239, 264, 300
  - Synchronous Serial Controller (SSC) 515, 543
    - SSC Clock Mode Register (SSC\_CMR) 545
    - SSC Control Register (SSC\_CR) 545
    - SSC Receive Clock Mode Register (SSC\_RCMR) 545
    - SSC Transmit Clock Mode Register (SSC\_TCMR) 545
  - SYSC 54
  - SysClk siehe System Clock
  - System Clock
    - Systemtakt 299
  - System Controller 152
  - System-Timer (SysTick) 353, 356
    - System Control Block (SCB) 356
    - SysTick Calibration Value Register (SysTick -> CALIB) 358
    - SysTick Current Value Registers (SysTick -> VAL) 357
    - SysTick Reload Value Register (SysTick -> LOAD) 357
  - System-Timer (Systick)
    - SysTick Control and Status Register (SysTick -> CTRL) 356
  - SysTick 350
- T**
- Taktgenerator 252
    - Fast RC-Oszillator 253
  - Tetrade
    - Nutztetraden 227
    - Pseudotetraden 227
  - Texas Instruments StellarisWare 30
  - Timer/Counter (TC) 359
    - Ausgangsfunktionalität 360
    - Block-Register 361
    - Capture Mode (CM) 360
    - Channel Mode Register (TC\_CMRx) 361
    - Clock Chaining 361
    - Eingangsfunktionalität 360
    - Gray-Down 359
    - NVIC 360
    - PIO-Controller 360
    - PMC-Controller 360
    - PWM-Controller 360
    - Quadrature Decoder Logic 359
    - RA, RB, RC 374
    - Register C Compare Match 361
    - Struktur Tc 366
    - Struktur TcChannel 366
    - TC Block Control Register (TC\_BCR) 361, 369
    - TC Block Mode Register (TC\_BMR) 369
    - TC Channel Control Register (TC\_CCRx) 361, 371
    - TC Channel Mode Register (TC\_CMR) 371, 373
    - TC Counter Value Register (TC\_CVx) 374
    - TC Fault Mode Register (TC\_FMR) 371
    - TC Interrupt Disable Register (TC\_IDR) 374
    - TC Interrupt Enable Register (TC\_IER) 374
    - TC Interrupt Mask Register (TC\_IMR) 374
    - TC Quadrature Decoder Logic Interrupt Disable Register (TC\_QDEC\_IDR) 371
    - TC Quadrature Decoder Logic Interrupt Enable Register (TC\_QDEC\_IER) 371
    - TC Quadrature Decoder Logic Interrupt Mask Register (TC\_QDEC\_IMR) 371

- TC Quadrature Decoder Logic Interrupt
  - Status Register (TC\_QDEC\_ISR) 371
- TC Register C (TC\_RCx) 361
- TC Status Register (TC\_SR) 374
- TC Stepper Motor Mode Register (TC\_SMMR) 374
- TIMER\_CLOCK<sub>1</sub> bis TIMER\_CLOCK<sub>5</sub> 361
- Timer/Counter Channel 359
- Trigger 361
- Triggern per Software 361
- Wave Mode (WM) 360
- XC<sub>0</sub> bis XC<sub>2</sub> 361
- TinkerForge 37
- Tool
  - SAM-BA 64
- Toolchain
  - arm-none-eabi-cp 39
  - arm-none-eabi-objcopy 39, 88
  - arm-none-eabi-objdump 39
  - arm-none-eabi-size 39
  - GNU-Assembler arm-none-eabi-as 39
  - GNU-Compiler arm-none-eabi-gcc 39
  - GNU-Debugger arm-none-eabi-gdb 39
  - GNU-Linker arm-none-eabi-ld 39
  - launchpad 40
  - make 39
  - Michael Fischer 39
  - MinGW, Minimal GNU Tools for Windows 42
  - rm 39
  - sh 39
  - touch 39
  - Yagarto 39
- Two-wire Interface (TWI) 507
  - Arbitration 509
  - Fast-Modus 508
  - Fast-Modus Plus 508
  - High-Speed-Modus 508
  - Standard-Modus 508
  - System Management Bus, SMBus, SMB 507
  - TWI Clock Waveform Generator Register (TWI\_CWGR) 511
  - TWI Control Register (TWI\_CR) 510
  - TWI Internal Address Register (TWI\_IADR) 511
  - TWI Interrupt Disable Register (TWI\_IDR) 514
  - TWI Interrupt Enable Register (TWI\_IER) 514
  - TWI Interrupt Mask Register (TWI\_IMR) 514
  - TWI Master Mode Register (TWI\_MMR) 511
  - TWI Receive Holding Register (TWI\_RHR) 514
  - TWI Slave Mode Register (TWI\_SMR) 511
  - TWI Status Register (TWI\_SR) 512
  - TWI Transmit Holding Register (TWI\_THR) 514
  - Ultra-Fast-Modus 508
- U**
- UEXT 35
- Universal Asynchronous Receiver Transceiver (UART)
  - UART Baud Rate Generator Register (UART\_BRGR) 493
  - UART Control Register (UART\_CR) 491
  - UART Interrupt Disable Register (UART\_IDR) 493
  - UART Interrupt Enable Register (UART\_IER) 492
  - UART Interrupt Mask Register (UART\_IMR) 493
  - UART Mode Register (UART\_MR) 491
  - UART Receiver Holding Register (UART\_RHR) 493
  - UART Status Register (UART\_SR) 493
  - UART Transmitter Holding Register (UART\_THR) 493
- Universal EXTension siehe UEXT
- Universal Synchronous Asynchronous Receiver Transceiver (USART)
  - USART Baud Rate Generator Register (US\_BRGR) 505
  - USART Channel Status Register (US\_CSR) 504
  - USART Control Register (US\_CR) 500
  - USART FI DI Ratio Register (US\_FIDI) 505
  - USART Interrupt Disable Register (US\_IDR) 504
  - USART Interrupt Enable Register (US\_IER) 504
  - USART Interrupt Mask Register (US\_IMR) 504

- USART IrDA Filter Register (US\_IF) 505
  - USART Mode Register (US\_MR) 501
  - USART Number of Errors Register (US\_NER) 505
  - USART Receive Holding Register (US\_RHR) 505
  - USART Receiver Time-out Register (US\_RTOR) 505
  - USART Transmit Holding Register (US\_THR) 505
  - USART Transmitter Timeguard Register (US\_TTGR) 505
  - Universal Synchronous Asynchronous Receiver Transceiver USART)
    - USART Manchester Configuration Register (US\_MAN) 506
  - USB Clock Controller (UDPCK) siehe Power Management Controller (PMC)
- V**
- Vektortabelle 101
  - Versionierung
    - Git 154
    - Subversion 154
    - SVN siehe Subversion
  - Versorgungsspannung 147
  - VLSI Technology 53
  - volatile 312
- W**
- Watchdog Timer 152
  - Watchdog Timer (WDT)
- Deadlock 344
  - WDT Control Register (WDT\_CR) 352
  - WDT Mode Register (REG\_WDT\_MR) 345
  - WDT Mode Register Watchdog Debug Halt (WDT\_MR\_WDDBGHLT) 348
  - WDT Mode Register Watchdog Fault Interrupt Enable (WDT\_MR\_WDFIEN) 348
  - WDT Mode Register Watchdog Idle Halt (WDT\_MR\_WDIDLEHLT) 348
  - WDT Mode Register Watchdog Reset Enable (WDT\_MR\_WDRSTEN) 348
  - Watchdog.Timer 120
  - Watchdog-Timer (WDT) 344
    - WDT Mode Register (REG\_WDT\_MR) 352
    - WDT Status Register (REG\_WDT\_SR) 353
  - Widerstand
    - dimensionieren 193
    - internationale Schreibweise 178
  - Windows CE 119
  - WPEN (Write Protection Enable) 282
  - WPMR siehe PIO Write Protect Mode Register
- Z**
- Zustandsautomat siehe Statusmaschine