ARM Processors

Lecture on Introduction to Embedded Systems

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Abstraction

Embedded Systems

SOFTWARE

HARDWARE

PROTOCOL

Abstraction

System architecture

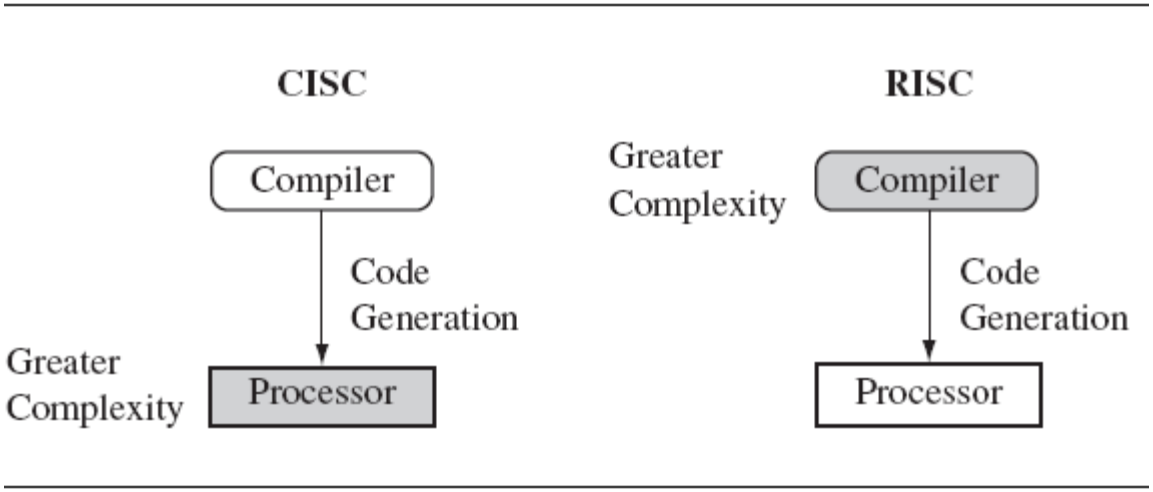
Microprocessor	Microcontroller
• CPU is stand-alone, RAM, ROM, I/O, timer are separate	• CPU, RAM, ROM, I/O and timer are all on a single chip
• Designer can decide on the amount of ROM, RAM and I/O ports.	• Fix amount of on-chip ROM, RAM, I/O ports
• Expansive	• For applications in which cost, power and space are critical
• Versatility	• Not Expansive
• General-purpose	• Single-purpose

CPU architecture

Comparison

CISC	RISC
Any instruction may reference memory	Only load/store references memory
Many instructions & addressing modes	Few instructions & addressing modes
Variable instruction formats	Fixed instruction formats
Single register set	Multiple register sets
Multi-clock cycle instructions	Single-clock cycle instructions
Micro-program interprets instructions	Hardware (FSM) executes instructions
Complexity is in the micro-program	Complexity is in the compiler
Less to no pipelining	Highly pipelined
Program code size small	Program code size large

CPU architecture



Memory architecture

von Neumann Architecture

- Memory holds data, instructions.
- Central processing unit (CPU) fetches instructions from memory.
  - Separate CPU and memory distinguishes programmable computer.
- CPU registers help out:
  - Program counter (PC),
  - Instruction register (IR),
  - General-purpose registers, etc.

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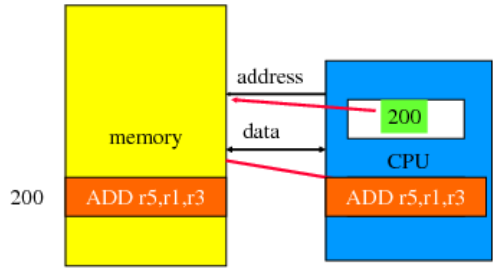
CPU + memory in von Neumann



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von Neumann vs. Harvard

- von Neumann
  - Same memory holds data, instructions.
  - A single set of address/data buses between CPU and memory
- Harvard
  - Separate memories for data and instructions.
  - Two sets of address/data buses between CPU and memory

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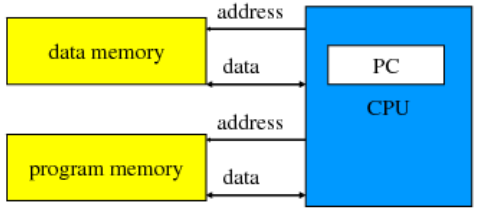
Harvard architecture



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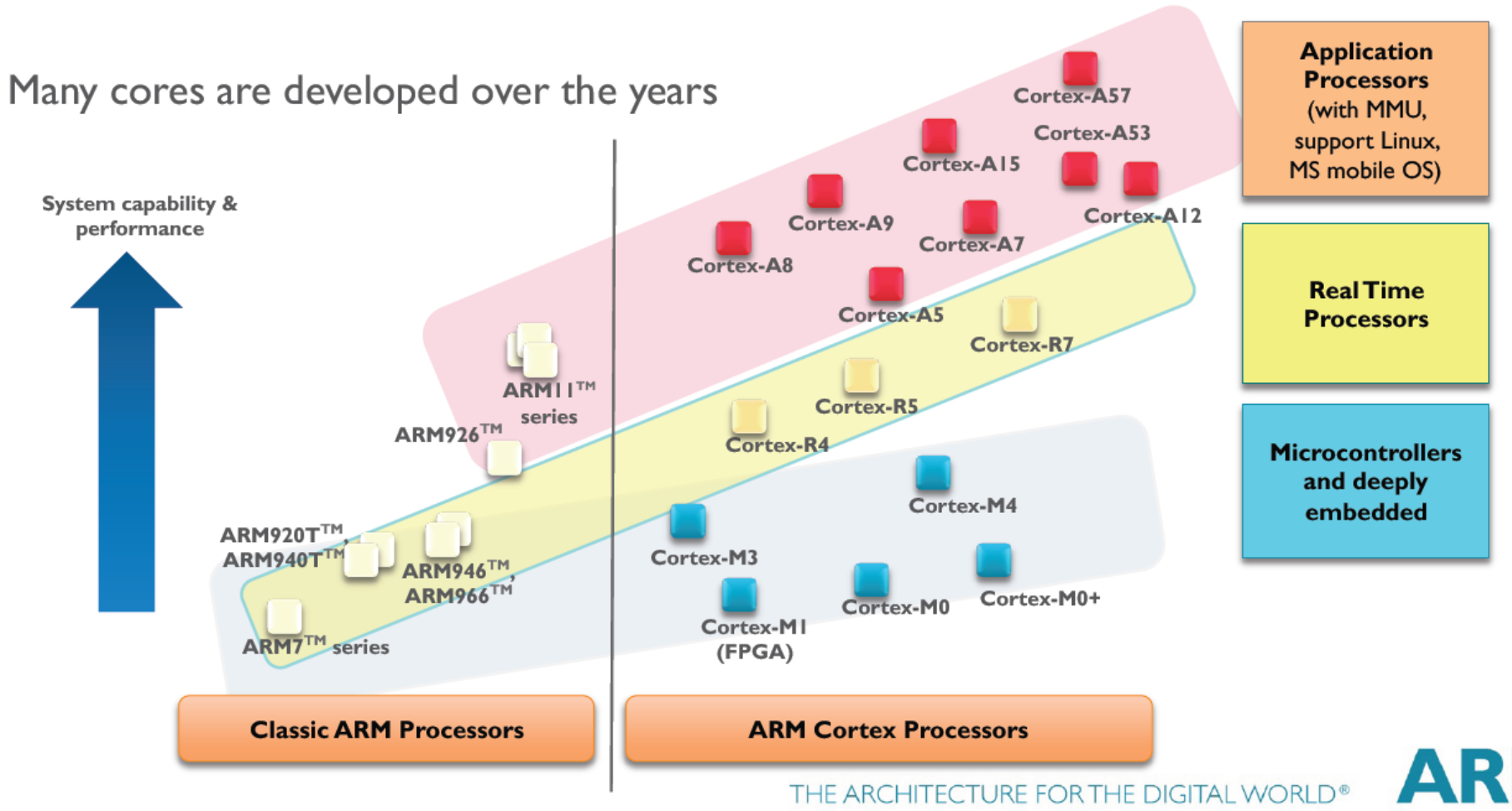
Why ARM ?

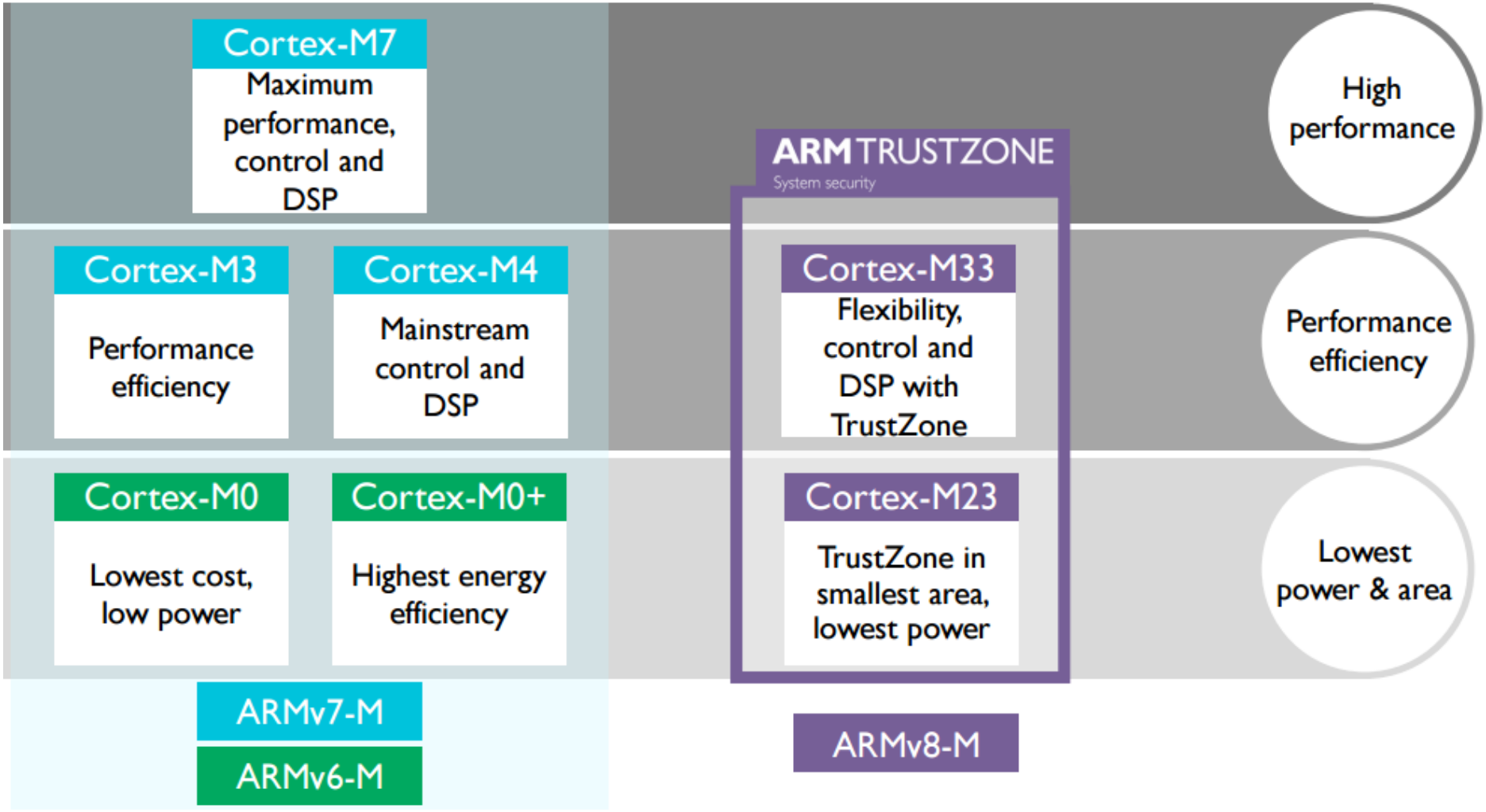
ARM Design Philosophy

- Low power
- Small size
- High code density
- Low cost
- Easy debug

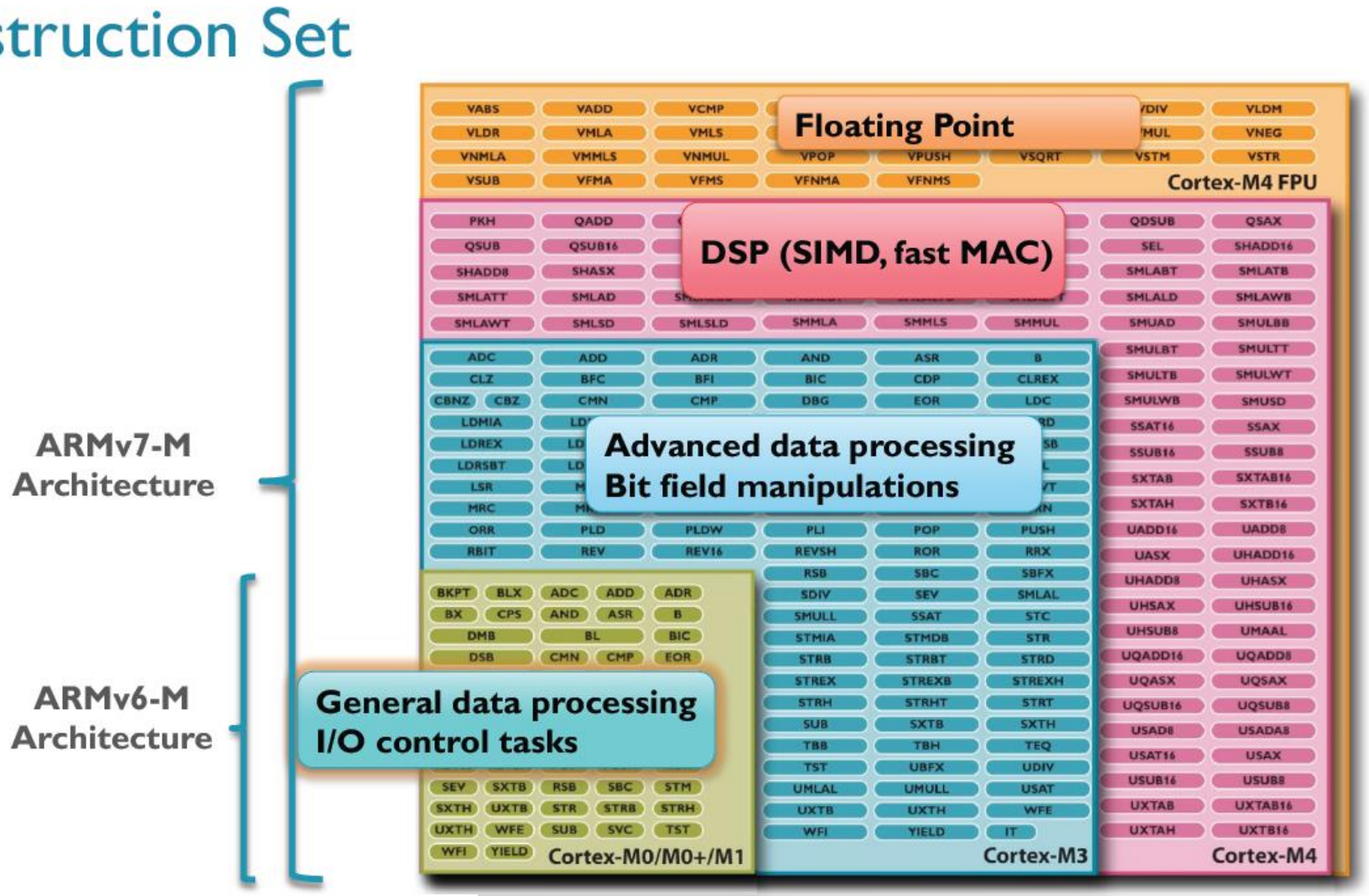
The ARM Processor Family



The ARM Processor Family



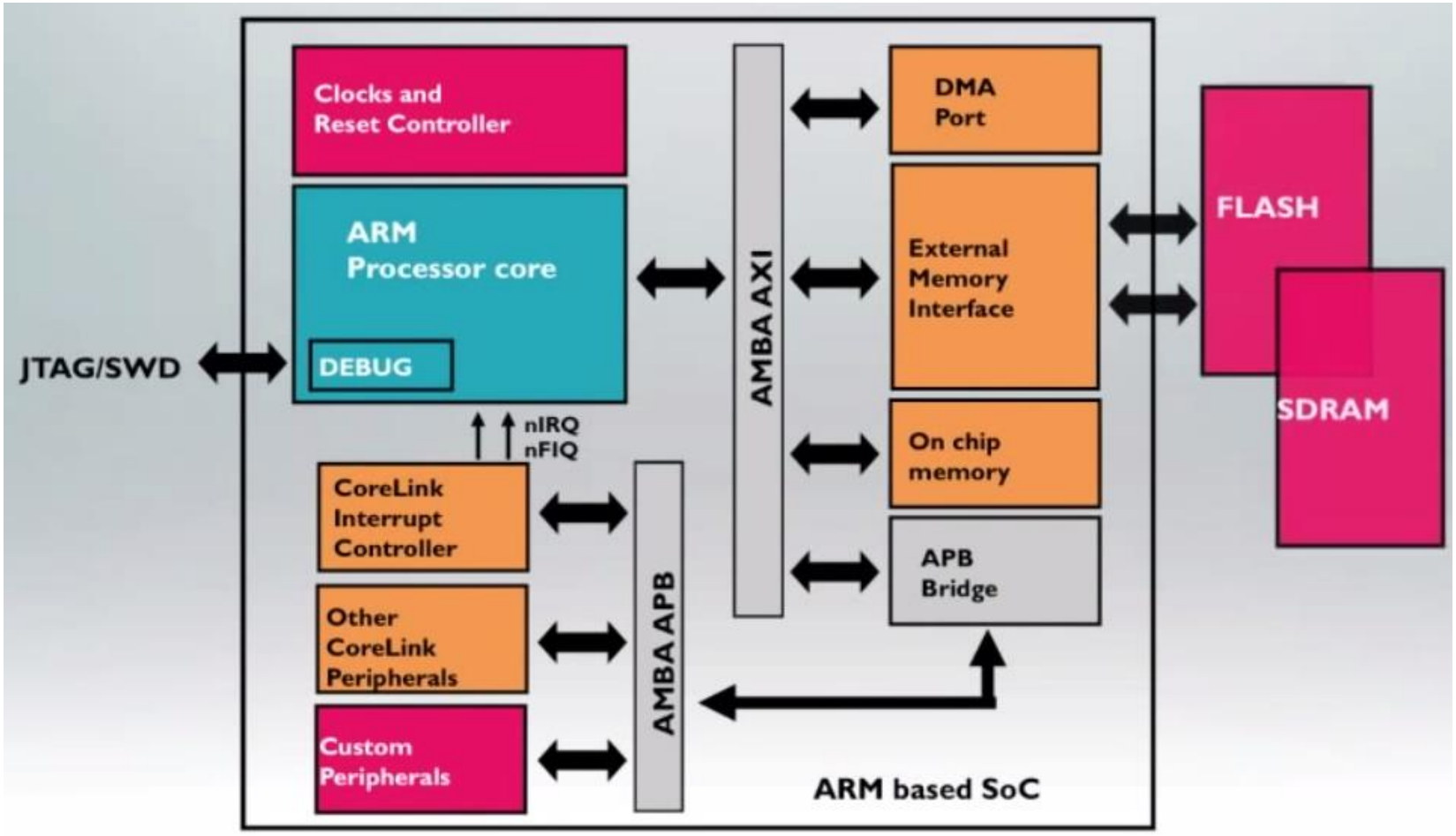
Binary Upwards Compatibility



ARM University Program

The Architecture for the Digital World® ARM

Inside ARM based System



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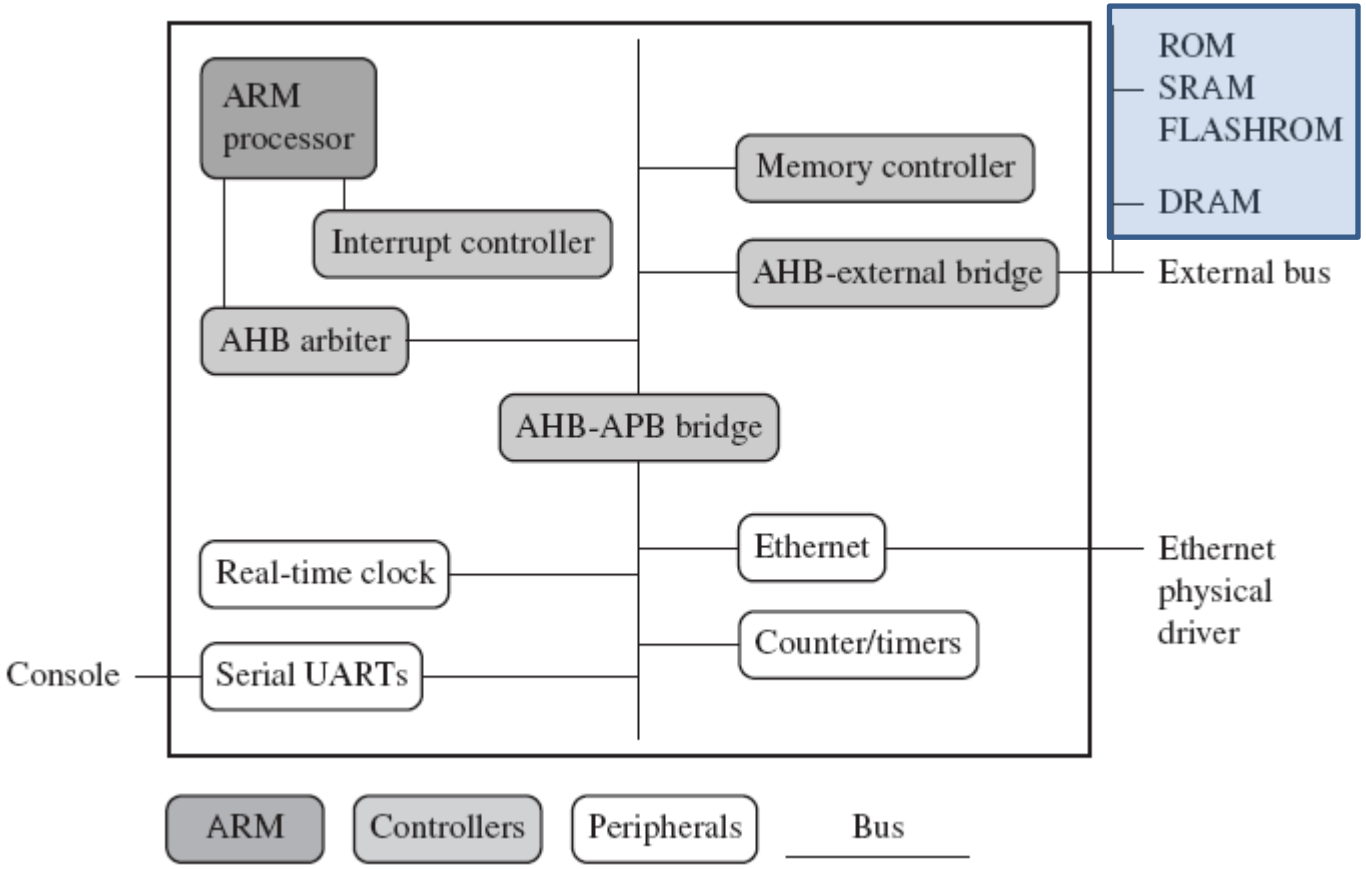


AMBA

- AMBA (**A**dvanced **M**icrocontroller **B**us **A**rchitecture)

  It is an open-standard, on-chip interconnect specification for the connection and management of functional blocks in system-on-a-chip (SoC) designs.

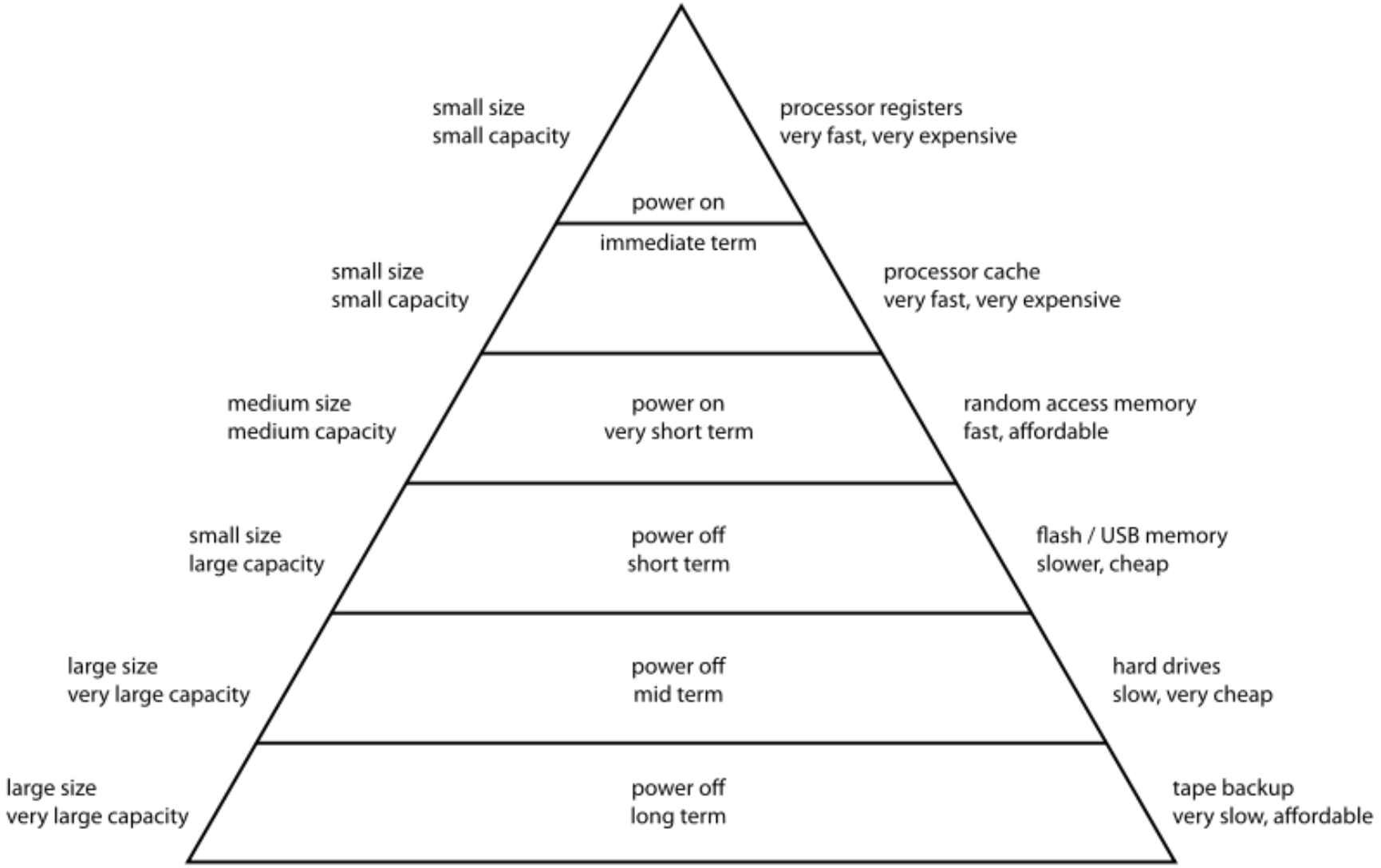
  - ASB (Advanced System Bus) : Simple bi-directional bus
  - APB (Advanced Peripheral Bus) : Low speed peripheral bus
  - AHB (Advanced High speed Bus): Centralized multilayer bus
    - AHB multi : Multi master – multi slave
    - AHB lite : Single master – multi slave

- Mostly ARM core is Bus master and Peripherals are slaves

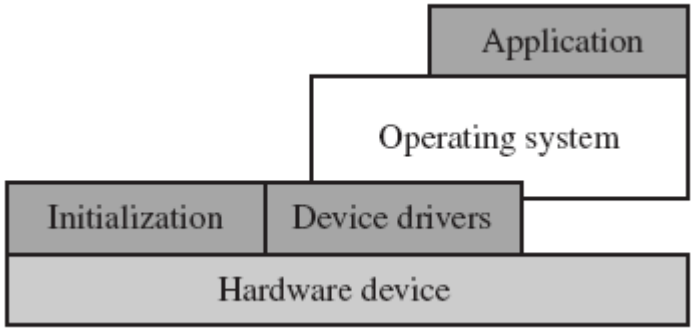
Peripherals

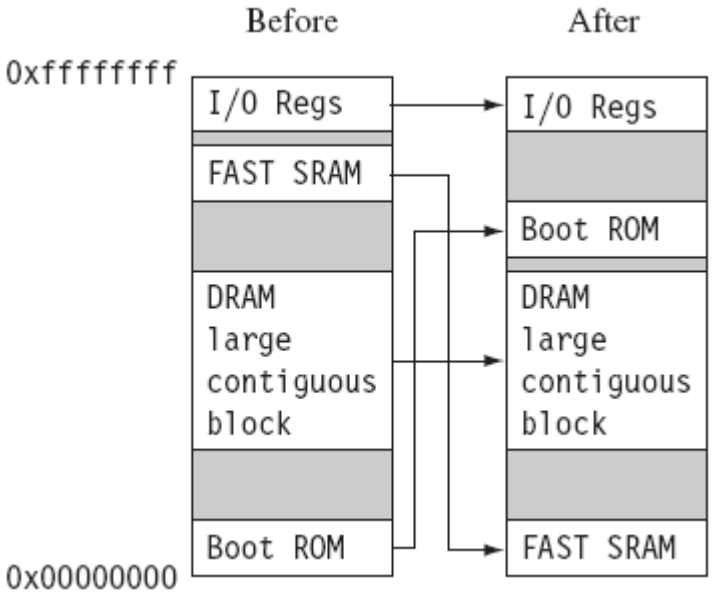
- All peripherals are Memory mapped
- **Controllers** are special types of peripherals that govern the interfacing policies
  - Interrupt controller
    - Standard Interrupt control - No Priority
    - **Vector Interrupt Control (VIC) - Priority based**
  - Memory controller
    - Memory preparation
      - Ex : DRAM requires to be configured for refresh rates and timing before it is accessed
    - Memory management
    - Memory protection

Computer Memory Hierarchy



Embedded Software





- **Boot / initialization code**
  It runs on reset and does following basic tasks
  - Initial hardware configuration like memory controllers and cache i.e., it prepares the hardware to satisfy the image to be booted
  - Diagnostics : Fault detection and isolation
  - Booting : Loading image and handing over the control to image by modifying the PC(Program Counter)

Embedded Software

- **Operating System**
  Organizes system resources like peripherals, memory and processors time

  - Two main categories
    - Real Time Operating Systems (RTOS)
      - Hard real time
      - Soft real time
    - Platform Operating Systems
      Manages large non real time applications

- **Applications**
  Code dedicated to handle a particular task

Thank you

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