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DCM Boost PFC for High Brightness LED Driver Applications

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Abstract: This paper is concerned with the derivation of a discontinuous conduction mode boost PFC rectifier as a driver for high-power LED lighting applications. The proposed driver is operated in the current mode regime while emulating a resistance towards the line, thus attaining a near unity power factor and low total harmonic distortion of the line current. Theoretical analysis is reported and conditions for the low LED flicker are derived. A method of design for minimum THD is also suggested. Simulation and experimental results are reported.

Keywords: LED driver; AC–DC conversion; boost converter; DCM; PFC

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1. Introduction

The next generation of lighting systems is hinged on high-brightness light-emitting diodes (LEDs). The high brightness LED is comprised of an array of rather small-sized basic LED devices put together to produce a significant amount of luminous flux for illumination purposes. The LED light source usually relies on high-energy blue LEDs covered by a phosphorus coating. The phosphorous coating converts the light spectra, that is, absorbs the blue light and emits a warm white light pleasant to the human eye. LEDs are very efficient, durable, maintenance-free, and have a long service life. Therefore, in the foreseeable future, LEDs are expected to replace much of the old incandescent and fluorescent light sources. By 2027, the widespread use of LED lighting in the US alone could save about 348 TWh—a total savings of more than $30 billion in today's electricity prices [1,2].

LEDs are direct current devices that require a suitable and reliable AC/DC converter, aka LED driver, to connect to the grid. The expected popularity of LED lighting also implies that their prospective drivers are about to be manufactured and applied in great numbers. To prevent massive utility pollution, the emerging off-line LED drivers must comply with the existing harmonic regulations [1,2]. Therefore, the LED drivers of any significant power are expected to perform high-quality rectification, also referred to as power factor correction (PFC). At the output, due to their steep current–voltage characteristics, LEDs should be energized by a current source, whereas the input is a voltage source, which calls for driver circuits with gyrator characteristics [3–6].

In the past, power factor correction (PFC) rectifiers' technology was intensely developed for industry, consumer, and military markets, and nowadays has reached maturity. The boost converter is frequently used in single-phase PFC applications due to its simplicity, robustness, high efficiency, and low part count [7]. At a higher power (>250 W), continuous current mode (CCM) operation is preferred due to its low-ripple input current that is easier to filter, whereas at the low power level (~100 W), the boost converter is usually operated in discontinuous conduction mode (DCM) with the advantage of attaining natural zero-current turn-off, and so alleviating the reverse recovery problems of the boost diode. Operation at a constant switching frequency also makes the EMI filter design

easier [3]. However, unlike the popular DCM flyback PFC, which can provide a near unity power factor just by operating at a constant duty cycle [8,9], the DCM boost PFC rectifier tends to generate a much higher total harmonic distortion (THD) [10,11]. Therefore, to attain an acceptable THD performance, the DCM boost PFC requires a feedback control scheme to actively shape the line current.

Several control methods of boost PFC can be found in the literature [12]. The constant frequency peak current mode (PCM) [13] and the average current mode (ACM) controllers [14] are, perhaps, the most popular. These methods require the application of both an inner feedback loop to shape the line current (which includes current reference and error amplifier circuits) and an outer loop to regulate the output voltage. Thus, a substantial design effort is needed to attain proper compensator design. Two related approaches that offer simplified controller implementation of the boost rectifier belong to a class of "PFC with no input voltage sensing". These are the non-linear carrier (NLC) [15,16] and the one cycle control (OCC) [17–19] techniques. Both methods can provide inherent line current shaping. Therefore, only the outer loop needs the designer's attention.

The application of OCC to power factor correction is advantageous. The OCC controller for the CCM boost rectifier is simpler when compared with the traditional approach and can be easily implemented. Furthermore, OCC has the advantages of inherent stability and robustness. The ACM and OCC control methods for a bridgeless boost PFC were investigated by [20], who confirmed the superiority of the OCC approach. However, at light loading or near zero-crossing of the line voltage, the PFC stage usually undergoes CCM to DCM mode changes. This necessitates control law adjustments to avoid distortion in the input current. Improved boost PFC analog OCC controllers that can regulate the switch turn-on time or frequency according to the AC input line voltage and reduce the distortion in the vicinity of the line voltage zero-crossing have been suggested [21]. A Digital version of [21] was suggested in [18]. To overcome the CCM–DCM transition problem, [22] suggested increasing the switching frequency at the dips of the line, whereas a control strategy for bidirectional boost rectifiers based on the OCC of charge was proposed in [23]. A discrete-time OCC PWM modulator, implemented in FPGA, was proposed to a single-phase PFC boost converter by [24]. Digital systems are flexible and can implement complex control strategies. However, when PFC enters DCM, the limited numeric resolution and, consequently, duty cycle errors of the digital controller appear as additional sources of instability. The problem of mode transition was resolved in [25] by though a mixed conduction mode (MCM) digital controller with a DCM detection technique to realize boost PFC operating in both CCM and DCM during AC line half-cycle, and resulted in an improved THD performance. Yet, the above solutions for the mode transition problem complicate the OCC controllers and so diminish its key advantage.

A straightforward solution to the problem of mode changes is designing the power stage to operate exclusively in DCM. Thus, no mode changes can be expected and the same control law can be effectively employed throughout the entire line cycle. An earlier OCC-controlled DCM boost PFC rectifier [19] relied on sensing both the rectified input and the output voltages to generate the required duty cycle (see Figure 1a). However, the analysis revealed that the OCC modulator in Figure 1a has the disadvantage of having the output power, P_{out}, reciprocal to the modulation voltage, V_m: $P_{out} = k/V_m$, where k is a system's constant [19]. As a result, the increment of the PFC's average output current, $\hat{\imath}_D$, as function of the small signal variation of the modulation voltage, $\hat{v}_m$, strongly depends on its power level: $\hat{\imath}_D = -\frac{P_{out}^2}{kV_o}\hat{v}_m$. The non-linear and negative small signal loop-gain poses design difficulties and operational limitations, and, therefore, is a hindrance.

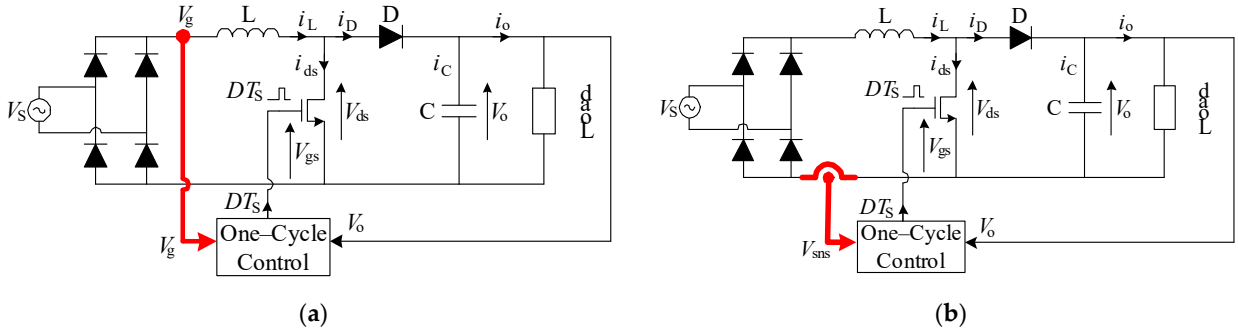


Figure 1. DCM boost PFC rectifiers with: (**a**) an earlier feed-forward OCC controller and (**b**) proposed current mode OCC controller.

The rest of the paper is organized as follows. Section 2 presents a review of the basic quantities of the DCM boost power stage that are used in the next sections. Section 3 is concerned with the derivation of an alternative OCC control scheme for the DCM boost PFC rectifier with the aim of improving its dynamic characteristics. Unlike the earlier voltage feed-forward DCM OCC approach in Figure 1a, the proposed OCC controller in Figure 1b relies on sensing the inductor current to generate the duty cycle for the DCM boost PFC power stage. Thus, the proposed scheme is referred to as the current mode DCM OCC. In the past, the current mode OCC modulator was successively employed to control the CCM PFC rectifiers [17]; however, the CCM OCC control law is incompatible with the DCM operation. Therefore, in this paper, the current mode OCC is further investigated to formulate the required control law that suits the DCM boost PFC in Figure 1b. This is indeed derived and its key features are studied. The proposed controller has the advantage of having a linear relationship between the power and the control voltage, $P_{out} = kv_m$. As a result, the small signal gain is also linear and of a positive sign. This greatly alleviates the outer feedback loop design. Section 4 of the paper describes the static design considerations to help choose the storage capacitor to limit the light flicker to an acceptable level. Section 5 of the paper presents the small-signal model of the outer current loop and reports on the analytical results. In Section 6, a design example is given demonstrating the design of the OCC DCM boost PFC/LED driver to provide the preferred operational conditions for the LED string load. Lastly, in Sections 7 and 8, the simulation and experimental results are reported.

2. Review of the Basic Relationships of DCM Boost PFC

To introduce the nomenclature and facilitate the analysis approach, the basic relationship of DCM boost PFC are reviewed first.

The topology of the boost PFC rectifier / LED driver is shown in Figure 2a. The peak inductor current, I_p, of the boost converter operating in the DCM mode, see Figure 2b, is given by

$$I_p = \frac{1}{L} V_s d T_s = \frac{1}{L}(V_o - V_s) d_1 T_s \tag{1}$$

here, L is the boost inductor, $T_s = 1/f_s$ is the switching period, f_s is the switching frequency, V_s is the source voltage, V_o is the output voltage, d is the on (switch) duty cycle, and d_1 is the off (diode) duty cycle.

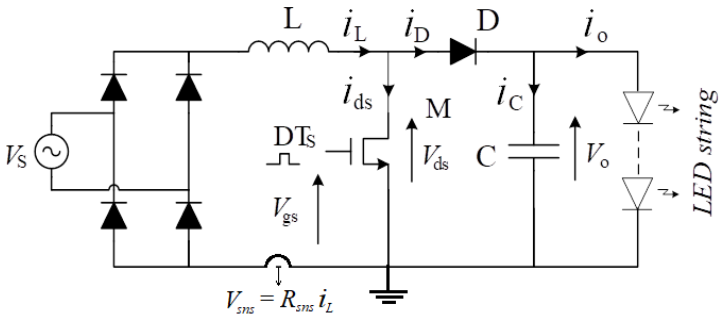
The ratio of the switch to diode duty cycle can be obtained from (1) as a function of the source and output voltages

$$\frac{d_1}{d} = \frac{V_s}{V_o - V_s} \tag{2}$$

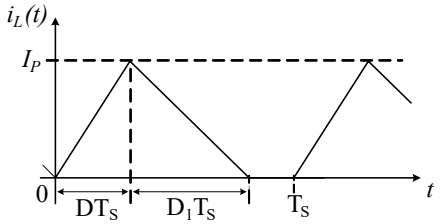
Then, applying geometrical considerations and using (1) and (2), the average inductor current can be expressed as

$$i_{av} = \frac{1}{T_s}\left[\frac{1}{2} I_p (d + d_1) T_s\right] = \frac{1}{2} I_p d \left(\frac{V_o}{V_o - V_s}\right) = \frac{1}{2}\frac{V_s}{L f_s} d^2 \left(\frac{V_o}{V_o - V_s}\right) \quad (3)$$

The above relationship will be useful in the following derivation of the DCM OCC control law.



(**a**)



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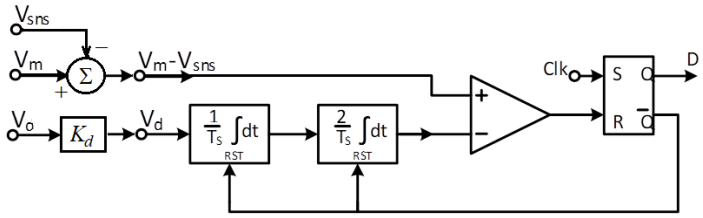


(**c**)

Figure 2. The topology of the boost PFC rectifier / LED driver (**a**), illustration of the boost inductor current in DCM (**b**), and improved OCC PWM modulator scheme for the current mode DCM boost PFC rectifiers (**c**).

3. The Proposed Line Current Shaping Method

3.1. Derivation of the Current Mode DCM Boost OCC Control Law

The control objective of the PFC is shaping the average current, i_{av}, proportionally to the source voltage V_s, so that

$$i_{av} = \frac{V_s}{R_e} \quad (4)$$

here, R_e is the emulated resistance presented by the PFC towards the line, which can be evaluated in terms of the RMS source voltage, V_{RMS}, and the average power, P_{av}, drawn throughout the line cycle

$$R_e = \frac{V_{rms}^2}{P_{av}} \quad (5)$$

Combining (3), (4) and (3) leads to

$$i_{av} = \frac{V_s}{R_e} = \frac{1}{2}\frac{V_s}{Lf_s}d^2\left(\frac{V_o}{V_o - V_s}\right) \quad (6)$$

Rearranging (6) and applying (4) results in

$$\frac{V_o}{R_e} - i_{av} = \frac{1}{2}\frac{V_o}{Lf_s}d^2 \quad (7)$$

The sensed voltage, v_{sns}, at the output of the input current sensing network (see Figure 2a) is defined as

$$v_{sns} = i_{av}R_{sns} \quad (8)$$

here, R_{sns} is the low-frequency trans-resistance gain of the input current sensing network.

Furthermore, defining the modulation voltage, V_m, as

$$V_m = V_0\frac{R_{sns}}{R_e} = V_0R_{sns}\frac{P_{av}}{V_{RMS}^2} \quad (9)$$

and the sensed output voltage, V_d, as

$$V_d = \frac{R_{sns}}{2Lf_s}V_o \quad (10)$$

and applying the definitions (8–10) to (7) yields the current mode OCC control law of the DCM boost PFC

$$V_m - v_{sns} = V_d d^2 \quad (11)$$

The control law (11) can be realized by applying double integration as follows

$$V_m - v_{sns} = \frac{2}{T_s^2}\int_0^{dT_s}\left(\int_0^t V_d d\,\tau\right)dt \quad (12)$$

This can be implemented in the hardware, as shown in Figure 2c.

With the proposed OCC controller, the DCM boost rectifier can attain the desired resistive input characteristic (4).

3.2. The Emulated Resistance

Further examination of (9) reveals that the average power is given by

$$P_{\mathrm{av}} = \frac{1}{R_{\mathrm{sns}}}\frac{V_{\mathrm{RMS}}^2}{V_o}V_m \quad (13)$$

Note that the average power is linear with the modulation signal V_m. Thus, the latter can be used in control purposes to regulate (modulate) the load power. Note again that the advantage of the proposed approach stems from the above linear relationship.

Further substituting (13) into (5) yields the emulated resistance, R_e, as a function of the modulation voltage, Vm, and the output voltage, V_o

$$R_e = R_{sns}\frac{V_o}{V_m} \quad (14)$$

The emulated resistance, R_e, is a function of the current sensor gain, R_{sns}, but also depends on the ratio between the output voltage, V_o, and the modulation voltage, V_m.

4. Static Design of DCM Boost PFC/LED Driver

Static design of a boost converter involves properly choosing the values of the inductor, *L*, and the capacitor, *C*, of the power stage. Inductor design is well documented in the literature; however, in the case of LED driver application, selecting the capacitor value requires deeper consideration, as described below.

4.1. Output Ripple of a PFC with LED-String Load

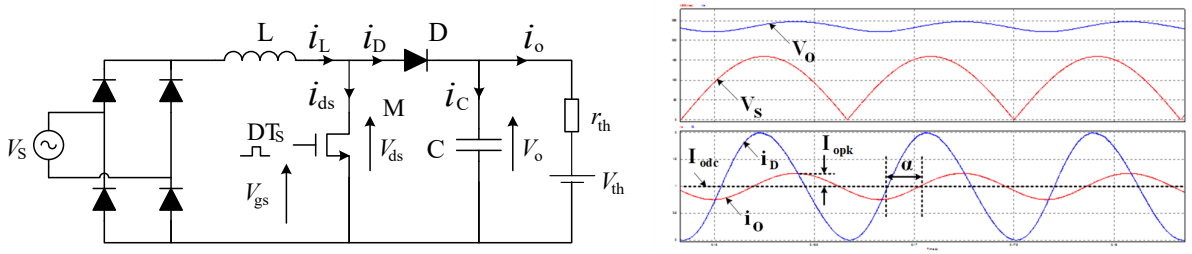
Assuming the control circuit attains its goal of unity PF so that its average line current is a pure sinusoid, and considering the AC–DC power balance, the average diode current, supplied to the output filter and the LED load is

$$\langle i_D(t)\rangle = I_{odc}\left(1 - Cos(2\omega_L t)\right) \tag{15}$$

Here ω_L is the line's angular frequency.

The LED string can be modeled by its Thevenin equivalent circuit. The simplified model is shown in Figure 3a. Here, V_{th} and r_{th} are the Thevenin equivalent voltage and Thevenin equivalent resistance of the LED string respectively. According to Figure 3a, the LED current, i_o, is simply

$$i_o = \frac{1}{r_{th}}(v_o - V_{th}) \tag{16}$$



(**a**) (**b**)

Figure 3. (**a**) DCM Boost PFC/ LED driver with the LED string represented by its Thevenin equivalent circuit; (**b**) simulated voltage and average current waveforms.

Applying KCL to the output node, $\langle i_D(t)\rangle = i_C + i_o$, and using, $i_c = C\frac{dv_o}{dt}$, yields the differential equation for the output voltage

$$C\frac{dv_o}{dt} + \frac{v_{o-V_{th}}}{r_{th}} = I_{odc}\left(1 - Cos(2\omega_L t)\right) \tag{17}$$

whence the output voltage is derived as

$$v_o(t) = V_{th} + r_{th}I_{odc}\left(1 - \frac{1}{\sqrt{1+C_n^2}}\cos(2\omega_L t - \alpha)\right) \tag{18}$$

Here, the normalized output capacitor is defined as $C_n = C/C_b$, the base capacitance is defined as $C_b = \frac{1}{2\omega_L r_{th}}$ and the phase shift is $\alpha = \tan^{-1}(C_n)$, see 3b. Using (16) and (18) the LED string current can be obtained as

$$i_o(t) = I_{odc}\left(1 - \gamma Cos(2\omega_L t - \alpha)\right) \tag{19}$$

where the peak LED string current ripple is defined as

$$\gamma = \frac{I_{opk}}{I_{odc}} = \frac{1}{\sqrt{1+C_n^2}} \tag{20}$$

The LED string current is illustrated in Figure 3b as having an average value of I_{odc} with a superimposed second harmonic ripple component of amplitude I_{opk}. The unwanted second harmonic current causes LED flickering.

Figure 4 presents a plot of the LED current ripple, γ, as a function of the normalized output capacitor C_n. Equation (19) predicts that the LED current ripple, γ, is constant depending on the system parameters. This also means that the LED flicker is constant. The flicker is also independent of the power level, which is an advantage. The flicker can be reduced by a proper choice of the filter capacitor, C, given by

$$C_n = \frac{C}{C_b} = \sqrt{\left(\frac{1}{\gamma}\right)^2 - 1} \tag{21}$$

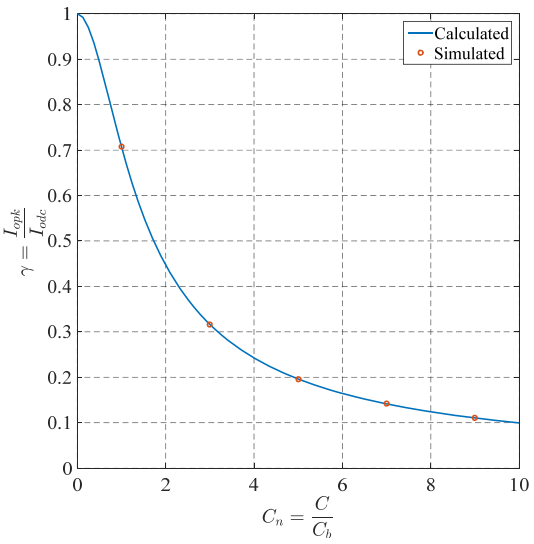


Figure 4. Peak LED string current ripple as a function of the normalized output capacitance.

4.2. Flicker Considerations

According to [26], the percent of flicker is defined as follows:

$$Mod\% = 100\frac{Max - Min}{Max + Min} \tag{22}$$

where Max and Min are the levels of the LED's light intensity over a single period of the LED current.

As the LED light intensity is proportional to the LED current, the modulation is

$$\text{Mod\%} = 100\frac{\left(I_{odc} + I_{opk}\right) - \left(I_{odc} - I_{opk}\right)}{\left(I_{odc} + I_{opk}\right) + \left(I_{odc} - I_{opk}\right)} = 100\frac{I_{opk}}{I_{odc}} = 100\gamma \tag{23}$$

Reportedly, flickering light can adversely affect human wellbeing. The percent of a flicker threshold level for no noticeable harm, where the flicker might only cause discomfort to some people but photosensitive seizures would not occur, is

$$Mod\% \le 0.08 \cdot f_{Flicker} \tag{24}$$

where $f_{Flicker}$ is the flicker frequency, which is the frequency that corresponds to the periodic change in the light intensity level [26].

The flicker of a single-phase LED driver is due to the output ripple, which is at the second harmonic of the line frequency $f_{Flicker} = 2f_L$, where f_L is the line frequency. From (23), (24) complies with the "no noticeable harm" condition and the allowable ripple at the output of the LED driver has to be restricted to

$$\gamma \le \frac{0.08}{100} \cdot f_{Flicker} \tag{25}$$

Applying (25) and (20) to (24), the "no noticeable harm" criteria for C_n can be formulated as follows:

$$C_n \ge \sqrt{\left(\frac{100}{0.16 \cdot f_L}\right)^2 - 1} \tag{26}$$

5. Modelling the Control Loop

The OCC DCM boost PFC operates under two feedback loops. The OCC modulator, boost power stage, and inductor current sensing network comprise the inner current loop. The inner current loop shapes the line current according to (12), and thus responds within a switching cycle. As shown in Figure 5a, the outer current loop is comprised of the output current shunt network, H_{sh}; the current reference, V_{ref}; and the current error amplifier, CEA, which generates the modulation voltage, V_m, for the OCC modulator. The objective of the outer current loop is to regulate the average LED current component, I_{odc}, while attenuating the second harmonic of the line frequency. To reject the second harmonic of the line frequency, the outer current loop bandwidth has to be severely restricted. For this reason, the outer current loop regards the fast inner loop just as a constant gain system. For the same reason, the slow outer current loop disregards the LED string dynamics. Hence, the low-frequency dynamic model of the LED string is merely a pure resistive term, r_{th}.

The small-signal model of the OCC modulator and the power stage can be derived following the general principles of PFC analysis [27]. First, the large-signal model of the boost diode current is formulated applying power balance considerations

$$\langle i_D(t)\rangle = \frac{\langle P(t)\rangle}{\langle V_o(t)\rangle} = \frac{V_{RMS}^2(t)}{R_e\big(V_m(t)\big)\langle V_o(t)\rangle} = \frac{V_{RMS}^2(t)}{V_o^2(t)R_{sns}}\, v_m(t) \tag{27}$$

here, (9) was used.

Next, perturbation and linearization of the large-signal model (27) are performed. This yields the following:

$$\hat{\imath}_D = g_s\hat{v}_{RMS}(t) + g_m\hat{v}_m(t) + g_o\hat{v}_o(t) \tag{28}$$

here, $\hat{\imath}_D, \hat{v}_{RMS}, \hat{v}_m, and\ \hat{v}_o$ are the small-signal perturbations in the boost diode current, the line RMS voltage, the modulating voltage, and the output voltage, respectively. The corresponding gain coefficients are as follows:

$$g_s = \left.\frac{\partial\langle i_D(t)\rangle}{\partial v_{RMS}}\right|_{v_{RMS}=V_{RMS}} = \frac{2V_{RMS}V_m}{V_o^2R_{sns}} = \frac{2P_{av}}{V_oV_{RMS}} \tag{29}$$

$$g_m = \left.\frac{\partial\langle i_D(t)\rangle}{\partial v_m}\right|_{v_m=V_m} = \frac{V_{RMS}^2}{V_o^2R_{sns}} = \frac{P_{av}}{V_oV_m} \tag{30}$$

$$g_o = -\frac{1}{r_o} = \left.\frac{\partial\langle i_D(t)\rangle}{\partial v_o}\right|_{v_o=V_o} = \frac{-3\cdot V_{RMS}^2V_m}{V_o^3R_{sns}} = -\frac{3P_{av}}{V_o^2} \tag{31}$$

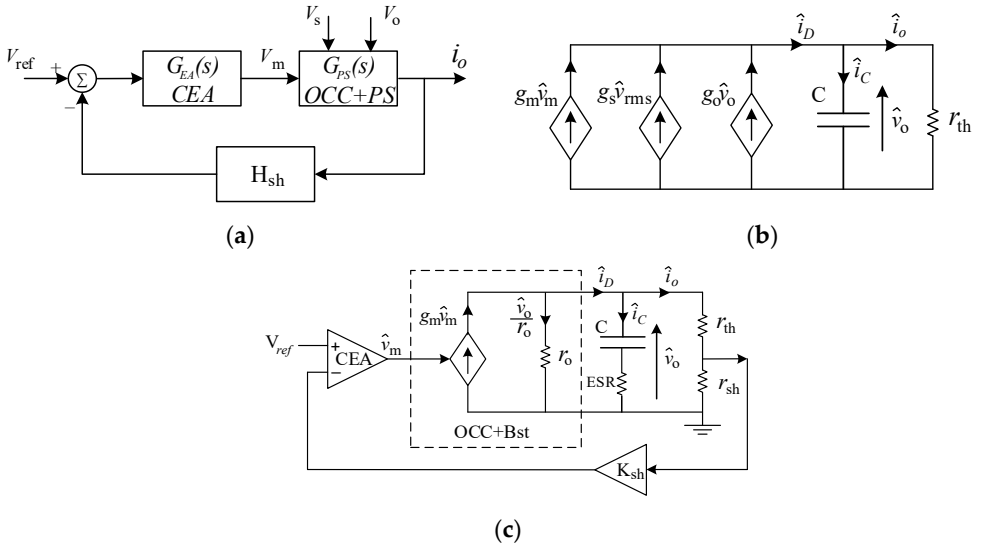


Figure 5. Simplified low frequency dynamic models of the outer current loop of the OCC DCM boost PFC with LED string load: (**a**) conceptual model; (**b**) combined modulator and power stage model; (**c**) small-signal model used for stability analysis of the output current mode operation of the LED-string load.

Table 1 summarizes the combined small-signal gains of the OCC modulator and the DCM boost PFC operating with an LED string load under a regulated output voltage mode (OVM) as a function of the average output voltage, V_o, and under a regulated output current mode (OCM) as a function of the average output current, I_o. The model is shown in Figure 5b. The low-frequency small-signal model of the OCC DCM boost PFC with LED string load can be constructed as shown in Figure 5c, from which the modulating voltage to LED string current transfer function is found.

$$\frac{\hat{\imath}_o}{\hat{v}_m} = \frac{g_m r_o}{r_{th} + r_o} \cdot \frac{1 + sC \cdot ESR}{1 + sC(r_{th} || r_o + ESR)} \tag{32}$$

Table 1. Outer loop gain coefficients.

	OVM	**OCM**
g_s	$\frac{2P_{av}}{V_o V_{RMS}}$	$\frac{2I_o}{V_{RMS}}$
g_m	$\frac{P_{av}}{V_o V_m}$	$\frac{V_{RMS}^2}{R_{sns}(V_{th} + r_{th} I_o)^2}$
$r_o = -\frac{1}{g_o}$	$\frac{V_o^2}{3P_{av}}$	$\frac{1}{3}\left(r_{th} + \frac{V_{th}}{I_o}\right)$

6. Design Example

The OCC DCM boost PFC can be designed to meet the following specifications: line voltage $V_{rms} = 115$ Vac ($V_{pk} = 160$ V); LED load with $V_{th} = 183$ Vdc, $r_{th} = 52.5$ Ω; nominal output current $I_o = 1$ A; nominal power $P_{av} = 235.5$ W. The PFC's switching frequency is $f_s = 50$ kHz.

6.1. Static Design

As the first step, the power stage parameters are determined. To keep the boost converter running in DCM, the boost inductor value shall not exceed the critical inductance value given by

$$L_{cr} = \frac{1}{4f_s} \cdot \frac{V_{pk}^2}{P} \cdot \left(1 - \frac{V_{pk}}{Vo}\right) \tag{33}$$

The given specifications yield $L_{cr} = 173.83$ μH. Leaving room for component tolerances and transient conditions, the boost inductor is chosen as $L = 0.7L_{cr} = 120$ μH.

The normalized output capacitor value that satisfies the "no noticeable harm" condition can be estimated according to (26) as

$$C_n \geq \sqrt{\left(\frac{100}{0.08 \cdot 2 \cdot 60}\right)^2 - 1} \approx 10.37 \tag{34}$$

As the base capacitance is $C_b = \frac{1}{2\omega_L r_{th}} = \frac{1}{2 \cdot 2\pi \cdot 60 \cdot 52.5} \approx 25.26$ μF, the minimum required value of the output capacitance is $C = C_n \cdot C_b \geq 10.37 \cdot 25.26$ μF $= 262$ μF. In practice, $C = 270$ μF is selected.

Applying (34), the inductor's RMS current is $I_{L,RMS} = 2.78$ [A], the switch RMS current is $I_{T,RMS} = 1.82$ [A], and the diode RMS current is $I_{D,RMS} = 2.1$ [A]. These were found for the nominal power level.

The input current sensing network is implemented with a cascading a sensing resistor, R_s, a current sensing amplifier, K_{sns}, and a low pass filter, $H_{sns}(s)$, which is needed to attenuate the current ripple and to provide the averaged sense signal. Thus, the combined gain of the current sensing network is

$$R_{sns}(s) = \frac{v_{sns}}{i_L}(s) = R_s K_{sns} H_{sns}(s) \tag{35}$$

The components of the current sensing network can be evaluated by applying the following considerations. The practical dynamic range of the modulating voltage, V_m, is limited by the saturation level of the error amplifier voltage, V_{ea_sat}. Assuming $V_{ea\_sat} = 12$ V, and leaving some room for transient conditions, the modulation voltage needed to attain the nominal power is about $V_m = 0.8V_{ea\_sat} \approx 10$ V. Therefore, the overall low-frequency gain of the sensing network Rsns can be derived from (9) and as a function of the output current, I_o:

$$R_{sns} = V_m \frac{V_{RMS}^2 \cdot I_o}{P_{av}^2} \approx 2.31 \tag{36}$$

It is suggested that at full power, the power dissipation in the load current sensing resistor, R_s, be limited to 0.2% of the nominal power, P_{av}. Hence,

$$R_s = 0.002 \frac{P_{av}}{I_{Lrms}^2} = 0.061\ \Omega \tag{37}$$

as the RMS current through the sensing resistor equals the inductor current, $I_{L,RMS}$. A standard value $R_s = 0.05\ \Omega$ was chosen, which also resulted in a bit of a lower power dissipation.

To attain the required value of R_{sns}, an input current sensing amplifier is needed with a voltage gain of

$$K_{sns} = \frac{R_{sns}}{R_s} = 46.2 \tag{38}$$

In practice, the low pass function, $H_{sns}(s)$, can be realized with the current sensing amplifier. The bandwidth of the filter affects the THD performance of the PFC. Reference [28] suggests that a corner frequency just above 1 kHz is adequate.

A voltage divider can be used to provide the voltage V_d needed for the OCC modulator of the output voltage (see Figure 2c). The required divider ratio can be found from (10)

$$K_d = \frac{R_{sns}}{2Lf_s} \approx 0.193 \tag{39}$$

Another issue to consider is evaluating the output current shunt network (see Figure 5c). Here, the overall current feedback gain is $H_{sh} = r_{sh}K_{sh}$. To prevent unnecessary power losses, the shunt resistor value, r_{sh}, is chosen, such that its power dissipation is about 0.1% of the power consumption of r_{th} at full load. This consideration leads to

$$r_{sh} = r_{th} \cdot 0.001 = 52.5 \cdot 0.001 = 0.0525 \tag{40}$$

A standard value of $r_{sh} = 0.05\ \Omega$ was chosen.

Choosing a comfortable value of $V_{ref} = 2.5$ V, the desired level of $I_o = 1$ A can be obtained with the shunt voltage gain, K_{sh}, of

$$K_{sh} = \frac{V_{ref}}{I_o \cdot r_{sh}} = \frac{2.5}{1 \cdot 0.05} = 50 \tag{41}$$

6.2. Calculation of the Outer Loop Small-Signal Parameters

The outer current loop design is done referring to Figure 5c. The design objectives are to establish the parameters of the shunt amplifier and the current error amplifier for the given (and the derived above) parameters: $C_o = 100\ \mu$F ; $ESR = 4.7\ \mu\Omega$; $V_{th} = 183$ Vdc; $r_{th} = 52.5\ \Omega$; $I_o = 1$ A; $P_{av} = 235.5$ W; $V_m = 10$.

The open-loop small-signal transfer function of the outer loop can be obtained from Figure 5a as

$$G_L(s) = H_{sh}G_{PS}(s)G_{EA}(s) \tag{42}$$

Now the gain coefficients of the combined small-signal modulator and power stage transfer function, $G_{PS}(s)$, are established. The small-signal gain g_m is

$$g_m = \frac{V_{sRMS}^2}{R_{sns}(V_{th} + r_{th}I_o)^2} = \frac{115^2}{2.31(183 + 52.5 \cdot 1)^2} = 0.1\left[\frac{1}{\Omega}\right] \tag{43}$$

whereas the small-signal output resistance r_o is

$$r_o = \frac{1}{3}\left(\frac{V_{th}}{I_o} + r_{th}\right) = \frac{1}{3}\left(\frac{183}{1} + 52.5\right) = 78.5[\Omega] \tag{44}$$

As the outer current loop bandwidth is rather low, the effect of the output filter capacitor's ESR on the outer loop dynamics can be neglected. Hence, according to (32), and using the parameters above, the combined small-signal modulator and power stage transfer function is:

$$G_{PS}(s) = \frac{\hat{\imath}_o}{\hat{v}_m} = \frac{0.1 \cdot 78.5}{52.5 + 78.5} \cdot \frac{1}{1 + s \cdot 270\mu \cdot \frac{78.5 \cdot 52.5}{78.5 + 52.5}} \approx 0.06 \cdot \frac{1}{1 + s \cdot \frac{1}{2\pi \cdot 18.7}} \tag{45}$$

Next, the parameters of the error amplifier are established. A simple outer loop current error amplifier having the following transfer function is sufficient to stabilize the loop

$$G_{EA}(s) = \frac{\omega_0}{s} \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \tag{46}$$

The error amplifier's zero $\omega_z \approx 2\pi 18.7\ \left[\frac{rad}{s}\right]$ is placed to cancel the power stage pole, (see (45)). To suppress the second line harmonic ripple propagating through the current loop, the loop crossover frequency is set to about a decade below the second harmonic frequency: $\omega_c = 2\pi(10)\left[\frac{rad}{s}\right] \ll 2\pi 120\left[\frac{rad}{s}\right] = 4\pi f_L$. In order to limit the output current overshoot, the error amplifier's pole will be set such that $PM(G_L(\omega_c)) = 65°$.

Note that with the pole-zero cancellation, the open-loop transfer function has only an integrator and a single simple pole, so that its phase margin is

$$PM\big(G_L(\omega_c)\big) = 180° - 90° - \tan^{-1}\left(\frac{\omega_c}{\omega_p}\right) = 65° \tag{47}$$

Hence, the desired crossover frequency is $\omega_c = 2\pi \cdot 10$ and the pole angular frequency is $\omega_p \approx 2\pi \cdot 21.45$.

Using (42) and (45), the outer loop gain at the crossover frequency can be approximated by

$$G_L(\omega_c) = H_{sh}G_{PS}(\omega_c)G_{EA}(\omega_c) \approx \frac{15 \cdot 10^{-3}}{2\pi}\omega_o = 1 \quad (48)$$

hence $\omega_o \approx 418.88$. Thus, the desired current error amplifier transfer function is as follows:

$$G_{EA}(s) = \frac{418.88}{s} \cdot \frac{1 + \frac{s}{2\pi 18.7}}{1 + \frac{s}{2\pi \cdot 21.45}} \quad (49)$$

The resulting frequency responses of the outer current loop gain components are shown in Figure 6.

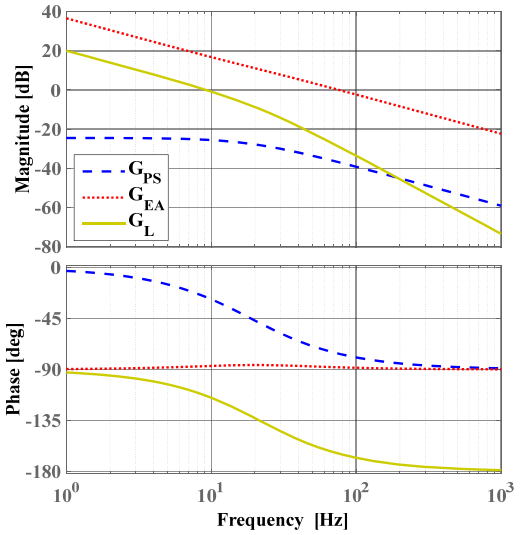


Figure 6. Frequency response of the outer current loop components (OCCs): modulator and power stage (GPS); error amplifier (GEA); the loop gain (GL).

7. Simulation Results

The OCC DCM boost PFC LED driver design was confirmed by simulation. PSIM simulation software was used. The parameters derived in the design example above were introduced into the program (line voltage $V_{RMS} = 115$ Vac, $V_{pk} = 160$ V; LED load with $V_{th} = 183$ Vdc, $r_{th} = 52.5\ \Omega$; nominal output current $I_o = 1$ A; nominal power $P_{av} = 235.5$ W. The PFC's switching frequency $f_s = 50$ kHz). The simulation diagram of the DCM boost PFC with the proposed control circuit is shown in Figure 7.

A simulation was run to confirm the design and to evaluate the performance of the DCM boost PFC with the modified OCC algorithm. Figure 8a illustrates the steady-state key variables of the improved OCC controller at full load. Simulated waveforms of the line voltage, the average power, the output voltage, and the line current are given in Figure 8b. Both the power and the output voltage ripple specifications were reached. The steady-state line current is of a good quality with about 3% THD.

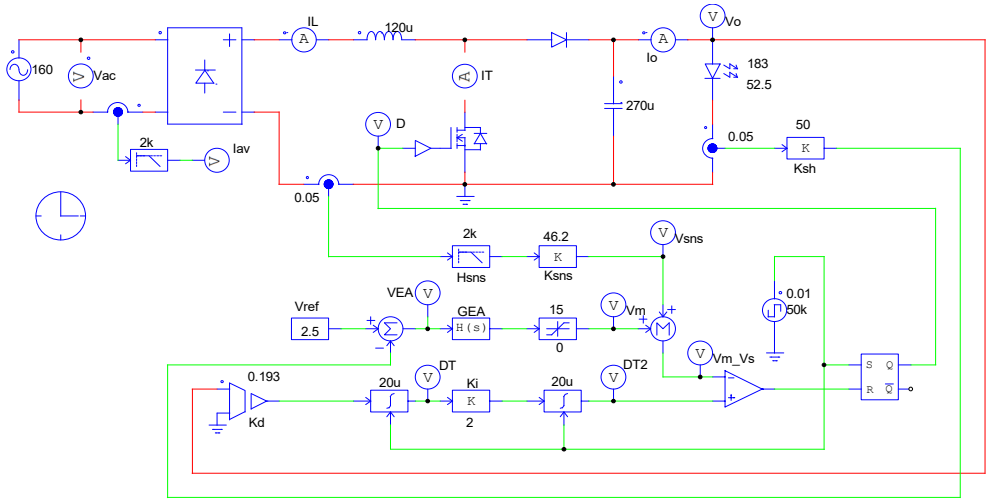
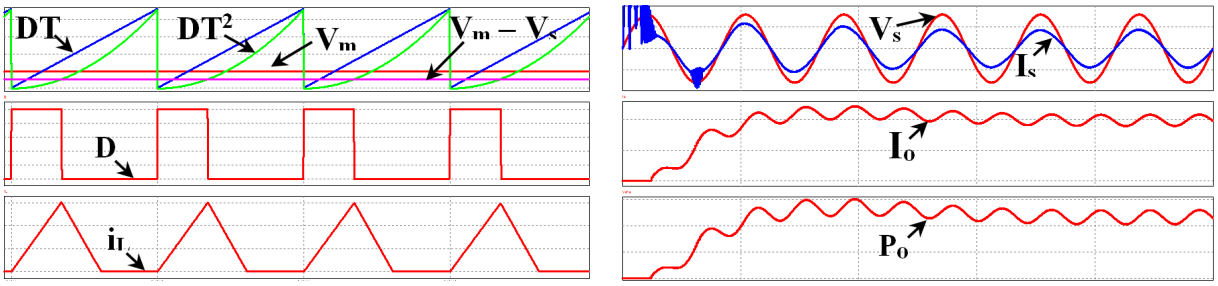


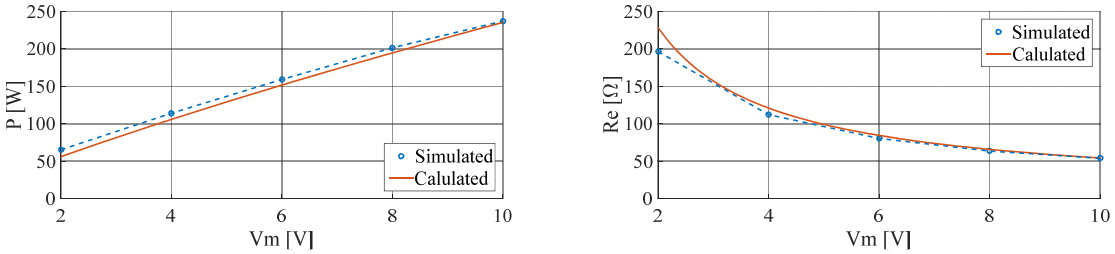
Figure 7. PSIM simulation diagram of the DCM boost PFC with the improved OCC control circuit (design example).



(**a**) (**b**)

Figure 8. Simulated waveforms of the OCC DCM boost PFC (design example): (**a**) key OCC modulator variables; (**b**) the line voltage, the average power, the output voltage, and the line current at full power.

The power relationship (13) and the emulated resistance (5) were compared with the simulated results and are plotted in Figure 9a and Figure 9b, respectively. Excellent agreement between the theoretical predictions and simulation results was found in both cases.



(**a**) (**b**)

Figure 9. Comparison of the theoretically predicted and simulated results for: (**a**) power level $P_{out}(V_m)$; (**b**) emulated resistance $R_e(V_m)$ as a function of modulated voltage, V_m.

8. Experimental Verification

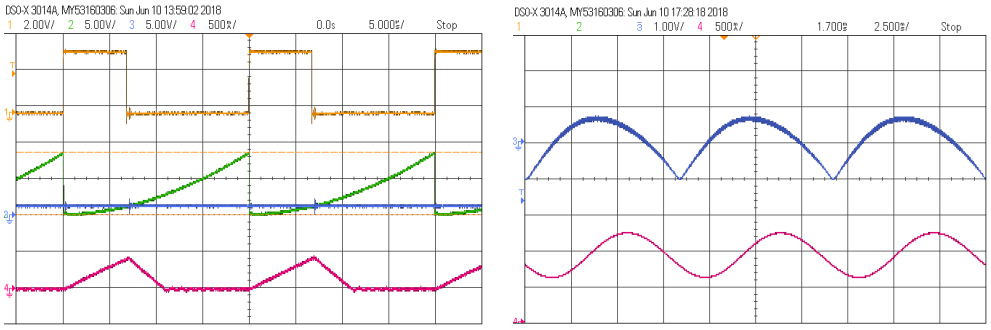
Experimental DCM boost PFC was designed, built, and tested. The prototype had the following parameters: line voltage *Vac* = 110 VRMS (60 Hz), output voltage *Vo* = 230 V dc;

and nominal output power Po = 250 W. The boost stage was implemented with L = 120 μH and C = 100 μF, and operated at a switching frequency of fs = 50 kHz. The semiconductors used were: MOSFET switch IPP65R190C7; boost diode DPG10I400PM; rectifier bridge GBU607; bypass diode 6A40G. Series connection of three CXA3590 LED units were used for high power. The non-inverting double integrator within the OCC controller was implemented using trans-conduction amplifier NE5517.

Key experimental waveforms of the DCM boost PFC on the switching frequency scale and the line frequency scale are illustrated in Figures 10 and 11 which show the line voltage and the average line current drawn by the DCM boost PFC, respectively. Testing conditions were line voltage Vac = 110 VRMS; average AC power Po = 250 W; Po=190 W; Po = 125 W. The measured total harmonic distortion in the line current was THD_I = 4.3%, and the measured power factor (PF) = 0.995.

THD performance of the proposed PFC rectifier/LED driver depends primarily on three factors: the accuracy of the current sensing network averaging performance (because of the limited switching noise filtering and its inherent phase shift), the accuracy of duty cycle generation by the OCC modulator, and the propagation of the second harmonic ripple within the control loop (which appears as v_2 term superimposed on the true modulation voltage, V_m). As a result, in practice, somewhat corrupted modulation voltages are presented to the OCC modulator and generate distortion. Accordingly, 3% THD was predicted by simulation, whereas the measured experimental value was just a bit higher at 4.5%.

As the experimental work was aimed at verifying the OCC control law (11) and its implementation, little consideration was given to the efficiency issues. The experimental prototype relied on hard switching and used no snubbers. Yet, an acceptable performance was obtained. The efficiency plot of the experimental prototype at nominal voltage and full power is presented in Figure 12**.**



(**a**) (**b**)

Figure 10. Experimental waveforms of the modified OCC DCM boost PFC rectifier. (**a**) At the switching frequency scale (horizontal scale 5 uS/div): blue—the control voltage, Vc; green—the quadratic ramp; yellow—the gating voltage, Vgs; red—the inductor current; (**b**) at the line frequency scale (horizontal scale–2.5 mS/div): blue–the sensed (and filtered) input current signal, Vsns; red—the LED current. (Vertical scale of each trace is found in the upper left corner).

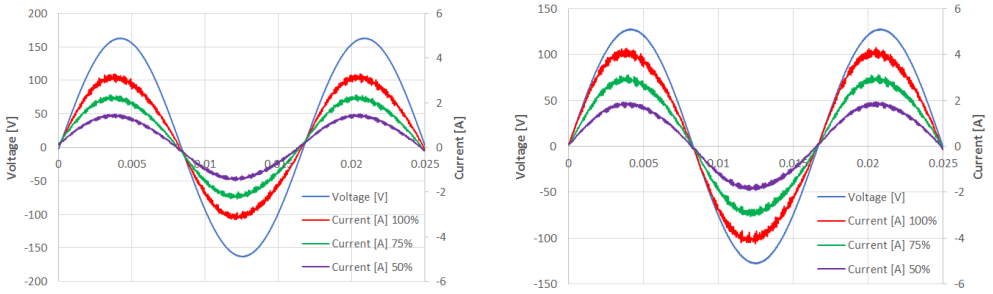


Figure 11. Line voltage, V_{ac}, and the average line current, I_{ac}, of the experimental prototype at different line voltages: (**a**) V_{ac} rms = 115 v; (**b**) V_{ac} rms = 90 v; Po = 250 W; Po = 190 W; Po = 125 W.

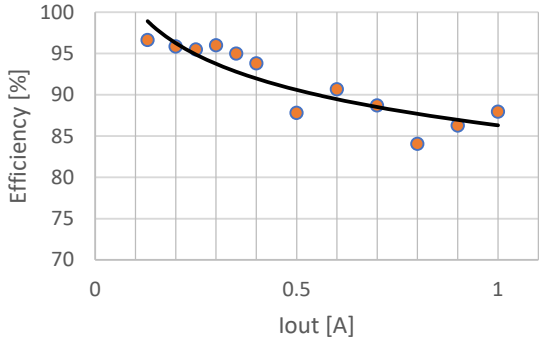


Figure 12. The efficiency of the experimental prototype DCM boost PFC.

9. Conclusions

This work was inspired by an earlier counterpart [19], which suggested a feedforward type of an OCC modulation scheme for a DCM boost PFC rectifier. This paper is aimed to improve the small-signal characteristics of the original circuit. Here, a current feedback OCC scheme was investigated to control the DCM boost PFC rectifier. As an application example, the improved PFC rectifier was employed as a high brightness high power LED driver; however, it could also be used for other applications. In the paper, the improved control law and other key theoretical considerations of the current mode OCC DCM boost PFC were derived, analyzed, and successively applied to the design of an experimental prototype. A method of design for minimum THD was also suggested. The reported theoretical predictions stand in good agreement with the simulation and the experimental results. The experimental prototype was proven to be rather robust.

The primary advantage of the proposed scheme over the earlier counterpart [19] is in the linear dependence of power on modulating voltage. As a result, the average small-signal gains of the average model are linear. Hence, the system is robust and easier to design. Furthermore, in comparison with recently reported work of [29,30], the proposed controller is simple to implement.

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