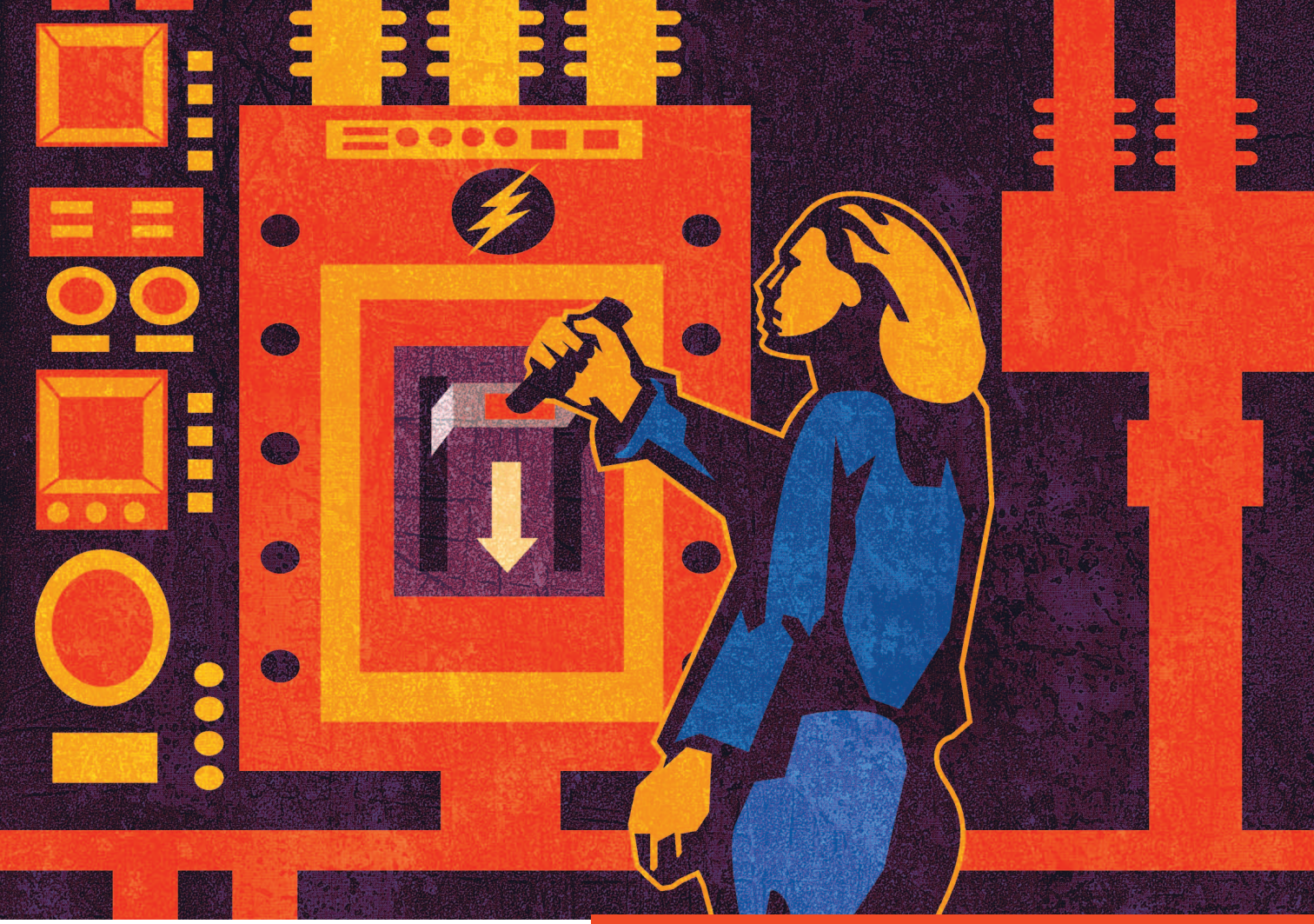

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Flipping the CMOS Switch

Xue Jun Li and Yue Ping Zhang

Wireless communication has become increasingly popular due to its accessibility by anyone at anytime, anywhere. To a great extent, the success of wireless communications has been achieved through the rapid progress in semiconductor technologies, particularly in complementary metal oxide semiconductor (CMOS) technology. Indeed, CMOS has made it possible to integrate radio-frequency (RF), intermediate-frequency (IF) and baseband blocks on the same die at low cost for wireless communication applications. Consequently, this attracts more subscribers to enjoy affordable wireless communication services.

The transmit/receive (T/R) switch is an important function block in an RF transceiver front-end, which

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generally consists of one transmission branch and one reception branch [1]. Along the reception branch, the received RF signals will be passed through a bandpass filter (BPF) and then switched by a T/R switch to a low-noise amplifier (LNA); while in the transmission branch, the transmitted RF signals will be amplified by a power amplifier (PA), and then switched by the T/R switch to the antenna. In particular, a T/R switch can be found in any time-division duplexing (TDD)-based radio front-end [1], and it connects radio transmitter (TX) and receiver (RX) alternatively to a shared antenna (ANT). A TDD radio system can inherently offer a number of advantages and flexibilities that a frequency-division duplexing (FDD) radio system cannot. These advantages include channel reciprocity, dynamic bandwidth allocation, and higher frequency diversity [2]. As shown in Table 1, TDD is dominant in area-network radio systems and is expanding its share in cellular radio systems.

TABLE 1. Summary of wireless technologies.

	System Characteristics			
Technology	**Frequency (GHz)**	**Date Rate (Mb/s)**	**Peak Power Level (dBm)**	**Duplexing Features**
2G	0.9/1.8/1.9	<0.1	30	FDD
3G	1.8~2.2	<2	30	FDD/TDD
4G LTE	2.0~2.6	>50	30	FDD/TDD
4G WiMAX	2.3~3.5	<75	30	FDD/TDD
Bluetooth	2.4	<54	20	TDD
WLAN	2.4 or 5.8	<54	20	TDD
UWB	3.1~10.6	>110	−15	TDD
60-GHz	57~66	>1500	10	TDD

The difficulty of integrating various RF components in a single chip is dependent on the wireless technology requirements. For example, wireless communications are mainly realized with cellular and area-network radio systems [3]. First generation (1G) cellular radio systems began operation in 1979, using analog signals, FDD, and frequency division multiple access (FDMA) [4]. In the early 1990s, second generation (2G) cellular radio systems arrived, which employ digital signals, FDD, and time division multiple access (TDMA) or code division multiple access (CDMA) to provide telephony plus text messaging and limited circuit-switched data communications [5]. 2G systems achieved unexpected success, brought the niche 1G to the mass market, and revolutionized the world communications. In 2001, following the phenomenal success of 2G, third generation (3G) cellular radio systems debuted. Since then, 3G systems have been deployed in many countries, using FDD or TDD and wideband W-CDMA or time division-synchronous CDMA (TD-SCDMA) to allow mobile multimedia applications [6], [7]. The fourth generation (4G) work started in 2005 and offers a high degree of commonality of functionality worldwide, while retaining the flexibility to support a wide range of services and applications (100 Mb/s for high mobility and 1 Gb/s for low mobility), and does so in a cost-efficient manner. It is expected that 4G candidate technologies can be approved in October 2010. The two most likely 4G candidate technologies are mobile worldwide interoperability for microwave access (WiMAX) and long-term evolution (LTE) [8]. Both 4G candidate technologies feature multi-input/multi-output (MIMO) antennae to improve spectral efficiency and transmission quality.

Meanwhile, various area-network radio systems, such as wireless local area network (WLAN), are based on the IEEE 802.11 standard [9]. Wireless personal area networks (WPAN) are based on Bluetooth [10], and ultra-wide band (UWB) [11] and 60-GHz standards [12] have been developed for short-range, high-speed personal wireless communications [3]. Table 1 lists some data on these radio systems related to design of T/R switches. It is interesting to note that, as these radio systems evolve, their operating frequencies get higher and bandwidths get wider due to the congestion in lower frequency bands and the increase in data rates. It is more important to note that the maximal transmit power levels are 30 dBm and 20 dBm for cellular and WLAN radio terminals, respectively.

From Table 1, we notice that the operating frequency increases as the wireless technology advances. Consequently, it is desirable to have a high level of integration using CMOS technology so that we can squeeze more functions onto the same wireless communication device. However, CMOS has not yet realized complete cellular radio integration because of challenges in PA and T/R switches. These challenges become even tougher as CMOS scales. Nevertheless, many techniques have been proposed to mitigate the difficulty on the PA integration [13]. In this article, we focus on design of T/R switches in CMOS and review their recent advances. The following section describes typical T/R switch topologies, key performance parameters, and n-channel MOS (NMOS) field-effect transistor (FET) device circuit models. That is followed by a discussion of the important circuit techniques and concepts developed specifically for improving the performance of CMOS T/R switches. Finally, the reported CMOS T/R switches and identification of the important work for future development is summarized.

T/R Switch Topologies and Device Circuit Models

The aforementioned T/R switch, whose function is to alternately connect between the antenna and the TX

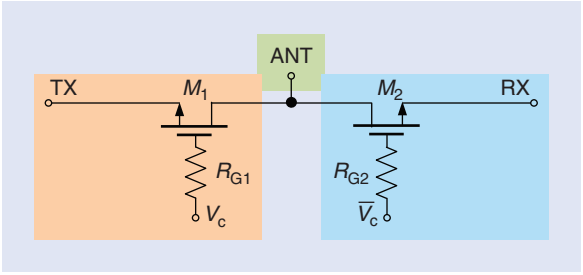

Figure 1. *Series single-pole double-throw transmit/receive switch topology.*

or RX, can be implemented using mechanical switches or solid-state switches. However, as compared with mechanical switches, solid-state switches have the following advantages: 1) faster switching speed or lower switching time, 2) higher reliability, and, most importantly, 3) more compact size and, therefore, easier use in large-scale integration/fabrication. Micromachining provides new technologies, such as RF microelectromechanical systems (MEMS) [14] to implement T/R switches, but integration and reliability challenges have prevented these solutions from being adopted. Solid-state switches can be implemented using positive intrinsic negative (PIN) diodes [15], FETs/high electromobility transistors (HEMTs) [16] and CMOS transistors, where PIN diodes and FETs/HEMTs are fabricated using gallium arsenide (GaAs) technology.

As compared to other technologies used for RF and microwave control functions (e.g., GaAs), CMOS technology is superior due to its low-cost structure and its integration potential of IF and baseband blocks on the same die [17]. In particular, CMOS transceivers can provide lower power consumption, lower component cost, and stability in manufacturing, comparable to other digital CMOS products. Investigation into the design of T/R switches in CMOS started in the late 1990s. Caverly reported a CMOS T/R switch design with less than 1-dB insertion loss and isolation of greater than 50 dB [17]. Madihian et al. presented a CMOS RF IC design for 900 MHz–2.4 GHz band wireless communication networks in [18]. Following that, many design techniques for CMOS RF switches have been reported. This article focuses on the design of T/R switches using CMOS technology.

The performance of a T/R switch is quantified by the following [19]:

- *Insertion loss*: the signal power loss introduced by the T/R switch between the input port and the output port
- *Isolation:* how well a T/R switch is able to prevent power leakage from the input port to ports other than the desired output port
- *Linearity:* the property of an active circuit device that its output power linearly increases with its input power; in practice, nonlinearity is usually measured by checking the third-order intercept point (IP3), which relates nonlinear products caused by the third-order nonlinear term to the linear term
- *Power handling capacity:* usually measured by the 1-dB compression point (P_{1dB}), which is defined as the input power that causes a 1 dB drop in the linear gain due to device saturation. P_{1dB} can also be considered as an indicator of nonlinearity; however, it is not as useful as IP3 because a T/R switch is designed to have insertion loss less than 1 dB. In addition, the inband third-order (and sometimes higher-order) intermodulation distortion is the important issue, because these nonlinearities can severely affects performance even before compression occurs
- *Offset:* measures the nonzero output voltage of a device when its input port is grounded
- *Switching time:* the delay between the signal at the output port and that at the input port, which is introduced by a T/R switch.

Generally, a T/R switch should be designed to have low insertion loss, high isolation, large P_{1dB}, low offset, short switching time, and good reliability. For a mobile cellular radio, the T/R switch should achieve an insertion loss of less than 1.5 dB, an isolation of more than 30 dB, and a P_{1dB} of more than 33 dBm. For a WLAN radio, the specifications for the switch are typically an insertion loss of less than 1 dB, an isolation of more than 20 dB, and a P_{1dB} of more than 23 dBm. Usually, switching time is not a limiting factor for mobile cellular and WLAN radios because the typical value of switching time requirements for WLAN radios is 10 μs and the typical value of CMOS T/R switching time is 0.1 μs [20].

Another important issue related to CMOS T/R switches is electrostatic discharge. As CMOS scales, gate oxide thickness continues to decrease and CMOS circuits become more vulnerable to the ubiquitous electrostatic discharge, especially due to the fact that a static charge transfer occurs upon static electricity discharge between a human and a chip. The standard human-body model assumes a static charge transfer of about 0.1 μC upon static electricity discharge between a human and a chip. Such charge may result in a tremendous electric field in the gate oxide on the order of 10^{15} V/m because the gate oxide thickness is only about 10^{-8} m. The T/R switch is conventionally connected to the outside world through the antenna and can therefore be exposed to electrostatic discharge stress events. It is thus desirable to incorporate a sufficient level of on-chip electrostatic discharge protection on a given T/R switch circuit. For example, an on-chip inductor shunt between the input/output and ground can provide electrostatic discharge protection, tune out

the parasitic capacitance so as to further decrease insertion loss, and serve as one part of the impedance matching network for further integration with other RF components, such as LNA and PA. In particular, as the gate control pins for integrated T/R switches are connected on-chip, electrostatic discharge is usually implemented at the port of the antenna. On the contrary, if the T/R switch is fabricated on a separate chip apart from other RF components, the gate-control pins are usually connected off-chip and electrostatic discharge should be implemented for the T/R switch chip.

The gate resistance R_G improves dc bias isolation and NMOS transistor reliability. If R_G is not present, the fluctuations of V_{GD} and V_{GS} of the NMOS transistor due to the voltage swing at its drain and source will be higher, which not only affects the NMOS transistor channel resistance, but also may result in excessive voltage across the gate dielectric and cause breakdown. In addition, R_G also affects power handling and frequency response of the T/R switch. Higher R_G values provide better dc isolation on the gate and improve low-end frequency response, but at the expense of slower switching times because the gate capacitance must be charged/discharged through higher R_G values [21]. Thus, a typical range of values for R_G is 5–15 kΩ. It is worth pointing out that the gate resistance R_G is typically implemented using an on-chip resistor.

Topologies

A survey of literature reveals that various CMOS T/R switch topologies have been proposed. They are described in the following sections.

Series SPDT T/R Switch Topology

Figure 1 shows a series T/R switch topology. It adopts transistor M_1 for the TX path and another transistor M_2 for the RX path. A control signal is applied to the gate of a transistor to alternate its ON/OFF state. For example, during a transmitting period, V_c is high and M1 is turned ON; at the same time, $\overline{V_c}$ is low and M_2 is turned OFF. In this way, the ANT is connected to the TX path. On the contrary, M_1 is turned OFF and M_2 is turned ON during a receiving period, letting the ANT connected to the RX path. Therefore, this T/R switch illustrates a typical single-pole double-throw (SPDT) configuration. Note that $\overline{V_c}$ and V_c are below and above, respectively, the device threshold voltage V_{th}, which is generally determined by many factors, such as gate width, oxide thickness, and temperature. Table 2 lists the typical values of V_{th} (~0.5 V) versus values of gate width for NMOS.

Series-Shunt SPDT T/R Switch Topology

Figure 2 shows a series-shunt T/R switch topology. The series transistors, M_1 and M_2, perform the switch function while the shunt transistors, M_3 and M_4, are used to pull the undesired signal in each mode to ground as M_3 and M_4 are turned ON when M_1 and M_2 are turned OFF, respectively. As compared with the series topology, the series-shunt topology improves isolation but increases insertion loss, especially at high frequencies.

TABLE 2. Typical values of V_{th} versus gate width for NMOS.

Gate Width (μm)	0.25	0.18	0.13	0.09	0.065
V_{th} (V)	0.47	0.445	0.44	0.43	0.422

Modified SPDT T/R Switch Topologies

Figure 3 shows a differential SPDT T/R switch topology [22], [23], which is mirrored from the single-ended series SPDT T/R switch topology shown in Figure 1. Theoretically, differential topology has 3-dB higher power-handling capability than single-ended topology. As the power-handling capability is a bottleneck of CMOS T/R switches, differential topology is of great advantage in current CMOS technology. Furthermore, the differential nature permits higher linearity and lower offset and makes it immune to power supply variations and substrate noise. Therefore, differential

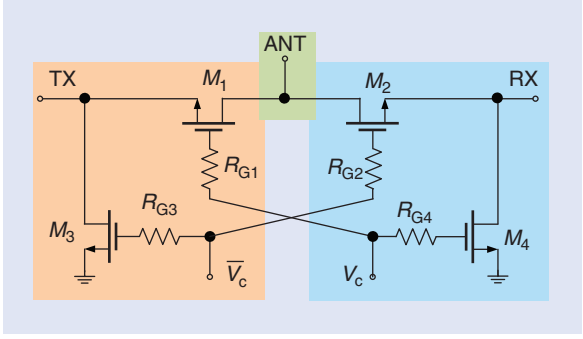

Figure 2. *Series-shunt single-pole double-throw transmit/receive switch topology.*

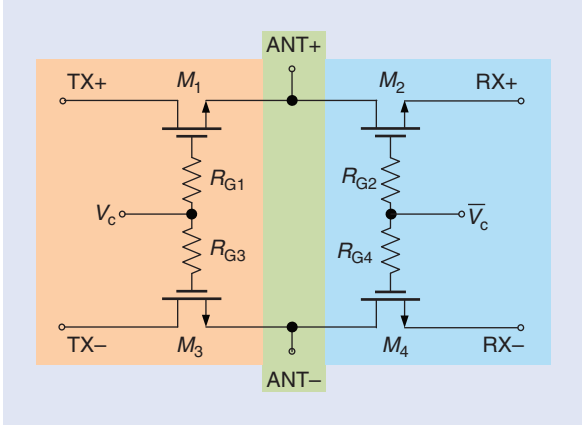

Figure 3. *Differential single-pole double-throw transmit/receive switch topology [23].*

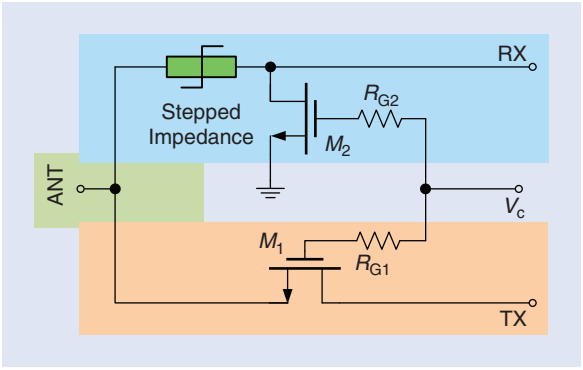

Figure 4. *Asymmetric single-pole double-throw transmit/receive switch topology.*

topology is normally preferred in applications requiring higher signal quality.

Figure 4 shows an asymmetric SPDT T/R switch topology, which can be considered as a modification to the symmetric series-shunt T/R switch topology shown in Figure 2 by replacing transistor M2 in the RX path with a stepped impedance block (see the "Stepped Impedance" section for more details) and deleting transistor M3 in the TX side. The stepped impedance block exhibits high impedance in the TX mode but low impedance in the RX mode. The asymmetric T/R switch topology meets the different requirements in the TX and RX modes. For instance, a large power-handling capability is more critical for the TX mode than for the RX mode because the signal power level applied to the T/R switch from the TX can be as high as 33 dBm while the received signal from the antenna is typically less than −30 dBm [2], [24]–[27].

4P4T T/R Switch Topology

MIMO technology has emerged as a promising solution to challenges in 4G systems [28]. MIMO technology, however, shifts the paradigm in which the T/R switch functions. It utilizes multiple antennae to attain true full duplexing and, therefore, does not require the switch to specify the transmitting or receiving operations. The role of a T/R switch is to link data streams to their corresponding antennae. The number of antenna elements used in a MIMO radio dictates the configuration of the T/R switch. The antenna elements for a base station should be limited to a moderate number such as four, because large RF output powers can pose environmental concerns and may be a public health threat [29], [30]. In addition, a maximum of four dual polarized patch antennae with half-wavelength spacing can be exploited for terminal operations. However, there are concerns that space constraints in handsets may pose a challenge to the use of more than one antenna. Nevertheless, we believe that four antenna elements are proper for most MIMO radios.

A four-pole and four-throw (4P4T) T/R switch topology has been proposed for MIMO radios with four antenna elements [31]. Figure 5 shows the 4P4T topology, which exhibits a total of 16 states determined by four bias controls, V_{c1}–V_{c4}, as each bias control has two input signals—below and above the device threshold voltage. As the topology features four antenna ports, it allows a full range of switching states and can support both a one-uplink–three-downlink and a two-uplink–two-downlink antenna operation. However, the 4P4T T/R switch suffers larger insertion loss as compared with the SPDT T/R switch because the signal needs to pass through an additional transistor between ANT and TX/RX. Furthermore, both 4P4T and SPDT T/R switches show similar isolation because added switches are not helpful in improving isolation.

A brief comparison of T/R switch topologies is summarized in Table 3. Our intention is to provide researchers/designers some general information on how to select an appropriate T/R switch topology.

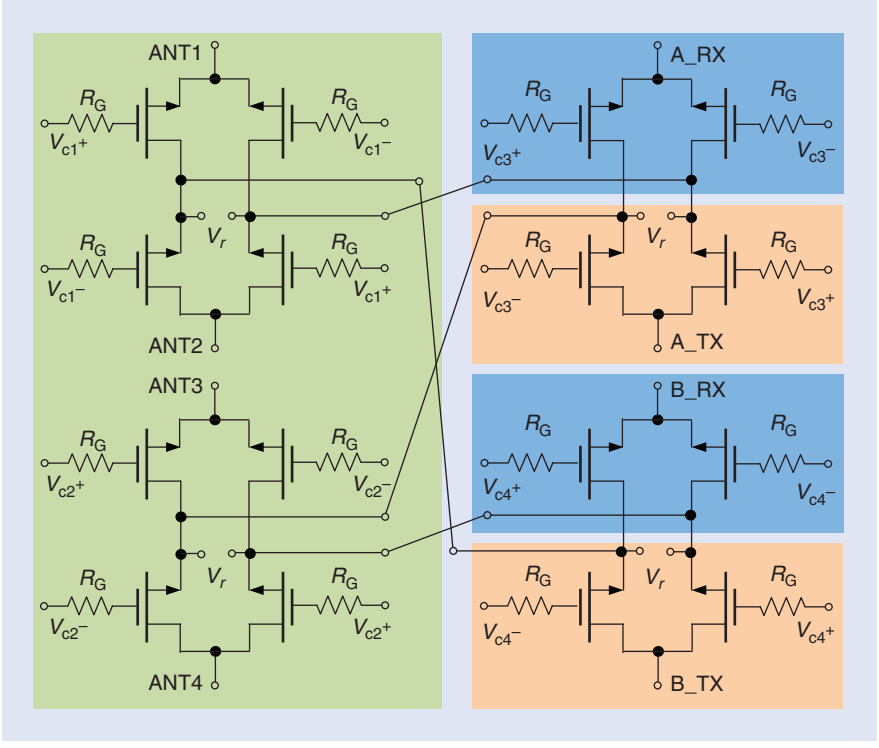

Figure 5. *Four-pole four-throw transmit/receive switch topology [31].*

Device Circuit Models

Bulk NMOS

Figure 6(a) shows the cross-sectional view of a typical bulk NMOS transistor. Note there are two parasitic diodes between the substrate and source and drain. The substrate is typically biased to 0 V. Thus, if no dc bias (greater than 0 V) is applied, as the signal amplitude approaches 0.6 V, these diodes start to become forward biased and limit the power-handling capability P_{1dB} at about 6 dBm in a 50-Ω system. Figure 6(b) shows a small-signal circuit model for the ON state of the NMOS transistor [19], [32]. At low frequencies, the on-resistance R_{on} determines insertion loss. As the operating frequency increases, insertion loss will increase due to an increase of capacitive coupling of the signal through the ON-state parasitic capacitances C_{db}, C_{sb}, C_{gd}, C_{gs}, and C_{gb} to the substrate resistance R_B. Figure 6(c) shows a small-signal circuit model for the OFF state of the NMOS transistor [19], [32]. Similarly, at low frequencies, the off-resistance R_{off} determines isolation. R_{off} is typically more than 100 kΩ, leading to very good isolation at low frequencies. However, at high frequencies, isolation deteriorates greatly due to OFF-state parasitic capacitances C_{db}, C_{sb}, C_{gd}, C_{gs}, and C_{gb} and channel capacitance C_{off}.

TABLE 3. Summary of T/R switch topologies.

	System Characteristics			
Topology	**Frequency Response**	**Insertion Loss**	**Isolation**	**Power Handling**
Series	Good	Excellent	Poor	Good
Series-shunt	Good	Poor	Good	Good
Differential	Good	Excellent	Good	Excellent
Asymmetric	Poor	Good	Good	Excellent

Triple-Well NMOS

Figure 7(a) shows the cross-sectional view of a typical triple-well NMOS transistor, which consists of a P-well embedded within a deep N-well to create an isolated body for the NMOS from the P-substrate (P_{sub}). Note there are four parasitic diodes, i.e., P-well-source, P-well-drain, P-well-deep-N-well, and P_{sub}-deep-N-well [22]. The triple-well NMOS has better performance than bulk NMOS in terms of noise isolation and body bias control. For CMOS technology at nodes below 130 nm, the incremental cost of the triple-well option is becoming insignificant. Hence, triple-well NMOS has become a popular choice to improve design robustness [26]. Figure 7(b) shows a small-signal circuit model for the ON state of the triple-well NMOS transistor. The on-state resistance R_{on} determines the insertion loss. Figure 7(c) shows a small-signal circuit model for the OFF state of the triple-well NMOS transistor. Off-state capacitances C_{db}, C_{sb}, C_{gd}, C_{gs}, and C_{ds} deteriorate isolation.

T/R Switch Circuit Techniques and Concepts

CMOS T/R switches suffer from substrate loss due to the low resistivity of the silicon substrate. The loading of parasitic diodes makes T/R switch design challenging when trying to achieve low insertion loss

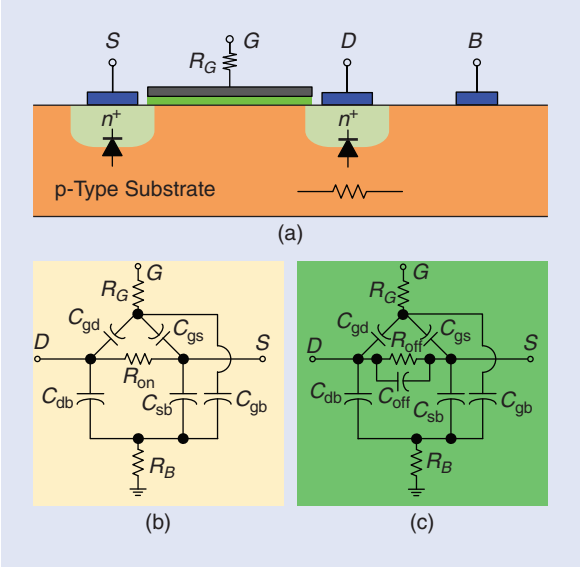

Figure 6. *(a) Cross-sectional view of an NMOS transistor, (b) ON-state model, and (c) OFF-state model with the gate floated and the body grounded. (Figure in (b) taken from [19].)*

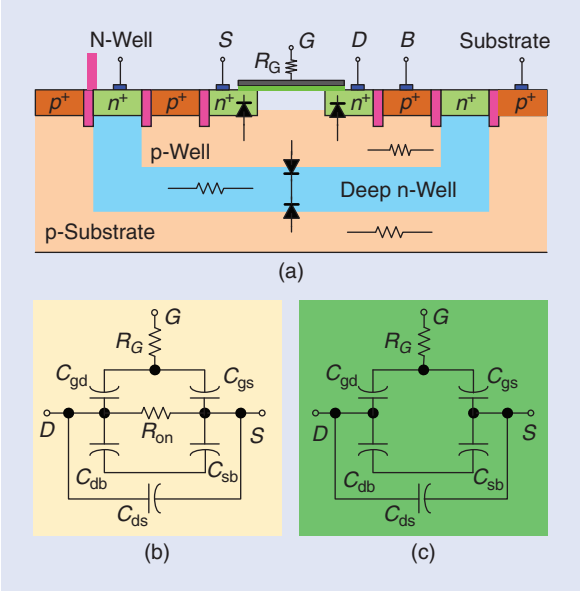

Figure 7. *(a) Cross-sectional view of a triple-well NMOS transistor, (b) ON-state model and (c) OFF-state model with both the gate and body floated. (Figure in (a) taken from [30].)*

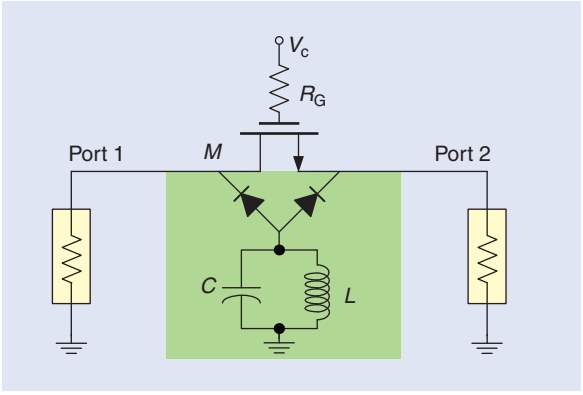

Figure 8. *Switch design using bulk NMOS and LC-tuned body-floating technique [24].*

and high P_{1dB}. To address this problem, several circuit techniques and concepts have been developed recently that have greatly improved the performance of CMOS T/R switches for P_{1dB} 11–30 dBm, insertion loss 1.5–0.1 dB, and isolation 24–30 dB at 2.4 GHz [32], [33]. For simplicity, we have purposely used single-pole-single-throw (SPST) topology in Figures 8–14 to illustrate the key characteristics of various techniques.

Optimizing Device Dimensions

Optimizing device dimensions is a fundamental technique in designing any CMOS circuit. The size of a switch transistor is optimized to obtain the minimum insertion loss. To achieve lower insertion loss, one needs to reduce the on-resistance by enlarging the transistor gate width. However, a larger transistor gate width will lead to larger parasitic capacitance in the substrate, which results in more signal loss in the substrate as well as degradation of isolation. Furthermore, this phenomenon is magnified as the frequency increases. Therefore, the trade-off between the on-resistance and parasitic capacitance yields an optimum value for the transistor gate width at a given frequency. Yamamoto et al. derived the optimum value [32] as

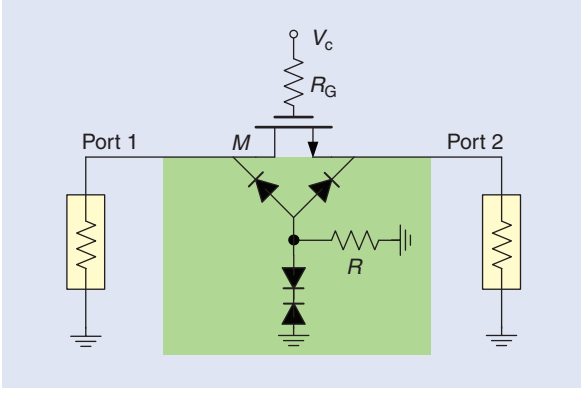

Figure 9. *Switch design using triple-well NMOS and resistive body floating.*

$$W_m = \sqrt{\frac{K_1K_2\{(1-Q_s^2)[2(1-Q_s^2)+3K]+2Q_s^2(3K+4)\}}{Z_0^2\{(2K+3)[2(1-Q_s^2)+3K]+3Q_s(3K+4)\}}}, \quad (1)$$

where K_1 and K_2 are constants and $K = K_1/K_2$; $Q_s = 1/\omega C_s R_s$; R_s and C_s represent parasitic resistances and capacitances resulting from a low-resistivity substrate. It should be mentioned that on-chip inductance can be used to tune out parasitic capacitance so that a larger transistor width can be allowed [34]. Furthermore, the customized layout with asymmetric drain and source may be used [35]. The customized layout increases the distance between the drain and source by stretching one side. As a result, only the drain or the source area is enlarged. The distance between them is fixed at four times the p-cell default, which is to ensure the minimized drain-source coupling due to metal interconnections. This reduction of drain-source coupling will improve both insertion loss and isolation performance.

Minimizing or Maximizing Substrate Resistances

The substrate resistance R_B increases insertion loss more at higher frequencies. Huang and O studied the dependence of insertion loss on the substrate resistance and parasitic capacitances and found there is a value of substrate resistance, $R_{B(MAX)}$, for which insertion loss is maximum [19]

$$R_{B(MAX)} = \frac{-\omega^2 C_T^2(R_{ON}Z_0 + Z_0^2)}{2\omega^2 C_T^2(R_{ON}+2Z_0)} + \frac{\sqrt{\omega^4 C_T^4(R_{ON}Z_0+Z_0^2)^2 + 4\omega^2 C_T^2(R_{ON}+2Z_0)^2}}{2\omega^2 C_T^2(R_{ON}+2Z_0)}, \quad (2)$$

where Z0 is the characteristic impedance and $C_T = C_{DB} + C_{SB} + [(C_{GD}+C_{GS})C_{GB}/(C_{GD}+C_{GS}+C_{GB})]$. As a result, one needs to either minimize or maximize the substrate resistance to avoid the value of $R_{B(MAX)}$ in order to achieve low insertion loss in CMOS bulk T/R switches. This can be done by reducing R_B to near zero or increasing R_B to a very large value. The small R_B can be achieved by fully surrounding the transistors with large area P^+ substrate contacts and filling in any open spaces with substrate contacts [19]. The large R_B can be realized by blocking the P implants close to the switch NMOS transistors and placing the substrate connections far from them [25], [36].

Body-Floating

Body-floating is probably the most important circuit technique that improves all the performance parameters of CMOS T/R switches. Talwalkar et al. reported the LC-tuned body-floating technique for bulk NMOS in [24]. As shown in Figure 8, by using an on-chip

inductor and capacitor, one can tune the bulk of the switching transistor to be floating at certain frequencies. This technique, however, increases the design complexity and consumes large silicon area. Furthermore, the effect of internal capacitive loss cannot be reduced.

The resistive body-floating technique is not viable with bulk NMOS because it involves manipulation to the substrate conditions. Taking advantage of the modern triple-well CMOS process, Yeh et al. realized the resistive body floating simply by using a large resistor to bias the bulk as shown in Figure 9 [33]. As resistors are intrinsically wideband, the P_{1dB} improvement is also wideband. The area is saved as compared with the LC-tuned approach; however, the linearity improvement to 21 dBm is not comparable to the LC-tuned technique [24], where more than 28 dBm was achieved.

Li and Zhang introduced the double-well body-floating technique in [22] to overcome the resistive body-floating limitation presented previously. As shown in Figure 10, in addition to both the P-well and deep-N-well biased through large resistors to make them RF floating, the deep-N-well should also be floated. With both terminals floated, the P-well-deep-N-well diode is then made safe. In a similar manner, the P_{sub}- deep-N-well diode is then unprotected and may be turned on by large signals. However, as the bootstrapped effect is digressive, the signals that can turn on this diode need to be very high.

The switched body floating technique is presented in [35]. As shown in Figure 11, the body floating is controlled by an additional switch, S, connected in parallel with the biasing transistor to provide controllable impedance between the body and its dc-biasing voltage. When the switch transistor, M, is turned ON, its body switch transistor, e.g., S, is turned OFF. The body of the ON switch transistor becomes RF floating, and vice versa. Consequently, the body of the OFF switch transistor becomes RF grounded, and the drain-source coupling through the body is significantly reduced [35]. A drawback of the switched body floating technique is that the insertion loss is degraded. This is due to extra loss caused by the parasitic to the body when the OFF switch transistor is RF grounded. Naturally, the insertion loss of a T/R switch with switched body floating technique is inferior to that of T/R switch with its body always floating.

Transistor Stacking

The stacked transistor technique, as shown in Figure 12, improves P1dB but degrades insertion loss. Ohnakado et al. proposed using depletion-layer-extended transistors and Poh and Zhang proposed using triple-well NMOS to compensate such a drawback [30], [37]–[39]. Triple-well NMOS, with the resistive body-floating technique can prevent losses through the body, thereby facilitating an equal voltage division, as well as manageable insertion loss. It was highlighted that the stacked transistors result in different impedance

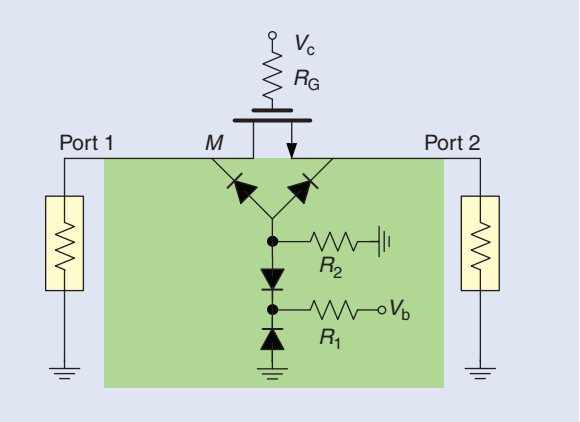

Figure 10. *Switch design using triple-well NMOS and double-well body floating.*

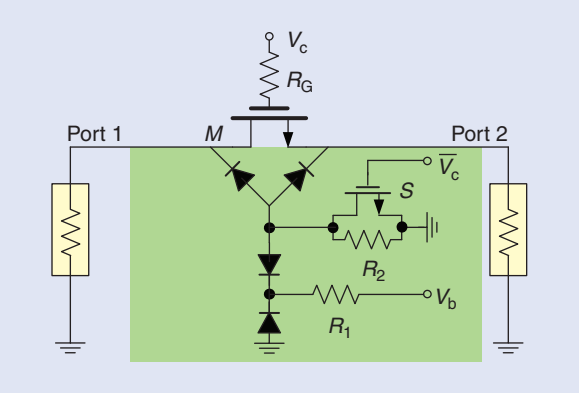

Figure 11. *Switch design using triple-well NMOS and switched body floating.*

to ground at each successive drain/source node [37]. The asymmetry produces an unequal splitting of the RF voltage causing the transistor nearest to the signal source to experience the largest voltage and breakdown first. Again, the concern is unwarranted with triple-well NMOS as the body is floated at RF and isolated from the substrate. Increasing the number of stacked transistors effectively improves the power handling and isolation, while compromising the insertion loss. Therefore, it is expected that there exists an optimum number of stacked transistors for which the switch performance is optimized, and the reasonable range for the number of stacked transistor is from two to five.

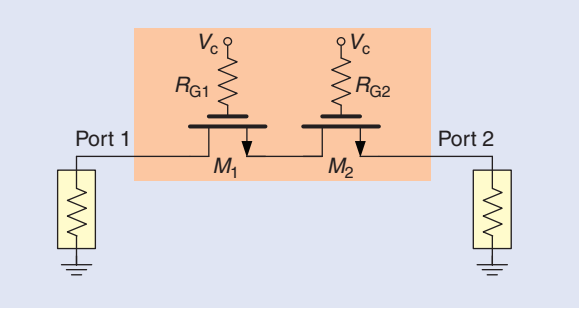

Figure 12. *Switch design with stacked transistors.*

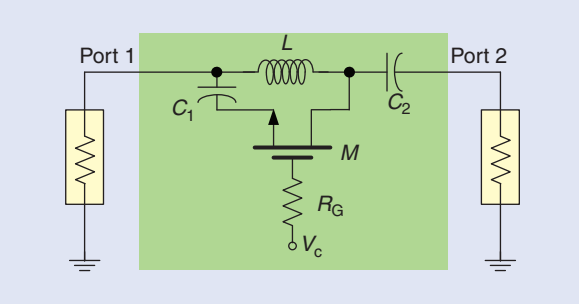

Figure 13. *Switch design with stepped impedance concept.*

Stepped Impedance

The stepped impedance concept plays an important role in a T/R switch having an asymmetric topology. The stepped impedance concept is based on LC resonance [25], i.e., the impedance of an LC circuit becomes zero at the series resonance but is infinitely large at the parallel resonance. Figure 13 illustrates the implementation. When V_c is low, M is turned OFF and L-C_2 forms a series resonator. On the other hand, when V_c is high, M_1 is turned ON and L-C_1 forms a parallel resonator. Obviously, the quality factor of L affects the performance and bandwidth of stepped impedance.

Travelling Wave

There have been a few attempts to design T/R switches in CMOS for millimeter-wave applications [40]–[43]. The switch parasitics and voltage stress severely degrade the switch performance at millimeter-wave frequencies. The traveling-wave concept has been adopted to guide the design [42]. As shown in Figure 14, the inductive line is periodically loaded by shunt transistors. In the ON state, the inductive line with loaded off-state capacitances functions as a transmission line to pass the millimeter-wave signals, while in the OFF state, the shunt on-resistance shorts the millimeter-wave signal to ground. There exists an optimum number of shunt transistors for which the switch performance is a compromise between insertion loss and isolation. It is worth pointing out that the traveling-wave concept is similar to the artificial transmission line technique [44]. Both are intended to reduce/eliminate signal reflections and allow the load port to absorb the desired signal. One minor difference between them might be that the traveling-wave switch adopts a periodic structure with inductive lines and shunt transistors, while the artificial-transmission-line switch uses a structure with on-chip inductors and the parasitic capacitance of transistors to synthesize artificial transmission lines [42], [44].

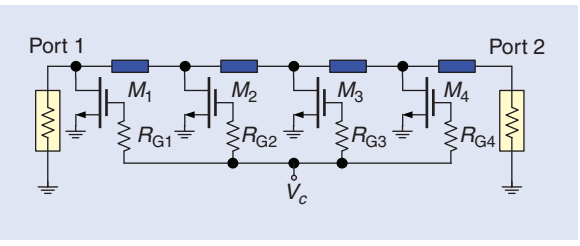

Figure 14. *Switch design with travelling-wave concept.*

Summary and Further Development

As CMOS technology is scaled down and adopted for many RF and millimeter-wave radio systems, design of T/R switches in CMOS has received considerable attention. Many T/R switches designed in 0.5 μm–65 nm CMOS processes have been reported. Table 4 summarizes these T/R switches. Some of them have become great candidates for WLAN and UWB radios. However, none of them met the requirements of mobile cellular and WPAN 60-GHz radios. Hence, performance enhancement of CMOS T/R switches for mobile cellular and 60-GHz radios is needed and can be sought from the following aspects.

First and foremost, methodologies for codesigning the T/R switch with the LNA and PA and the antenna in the radio package must be developed. A full differential architecture from the antenna through the T/R switch to such circuits as the LNA and PA with low interface impedance is preferable for such a radio [45]. The advantages of the differential architecture are well known. Lower interface impedance not only improves the T/R switch power handling capability but also enables the PA to deliver the required power at a lower voltage swing, reducing reliability issues for T/R switch devices and PA output devices. Furthermore, a lower interface impedance facilitates impedance matching from the antenna through the T/R switch to the LNA. The RX side switch can be part of the LNA matching network, which reduces die area and insertion loss compared to the conventional noncodesign. Moreover, impedance matching can be used to improve the power handling capacity of a T/R switch [46], [47].

Second, electromagnetic simulation and circuit modeling of switch transistors and their layouts need to be made to provide deep physical insight into the coupling mechanisms so as to find way to improve isolation between the TX and RX. For example, artificial transmission line techniques could be adopted [44].

Third, the T/R switch can be treated as a bandpass filter in the ON state and a bandstop filter in the OFF state. Filter theory can be drawn upon to synthesize and guide the T/R switch design.

Finally, CMOS device innovations and novel ideas such as artificial dielectric strips and bandgap structures may provide a comprehensive solution to the challenges of design of T/R switches for mobile cellular and 60-GHz radios.

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TABLE 4. Summary of T/R Switch design.

Ref.	Frequency (GHz)	Insertion Loss (dB)	Isolation (dB)	P_{1dB} (dBm)	Technology	Die Area	Topology	Techniques
[2]	5.2	2.02	31	29.6	0.18-μm	650 × 900 μm^2	Asymmetric	Stepped impedance
[19]	0.9	0.7	42	17	0.5-μm	560 × 560 μm^2	Series-shunt	Minimizing R_B
[22]	2.4–20	0.9–2.0	43–21	30	0.13-μm TW	415 × 415 μm^2	Series-shunt	DW resistive floating
[23]	<6	<2	>15	15	0.18-μm	60 × 40 μm^2	Differential architecture	Optimizing dimensions
[24]	2.4/5.2	1.5	30	28	0.18-μm	~0.56 mm^2	Asymmetric	LC-tuned body-floating
[25]	2.4	0.4	30	30	0.09-μm	~0.02 mm^2	Asymmetric	Stepped impedance
[26]	24	3.5	10	28.7	0.09-μm TW	110 × 160 μm^2	Asymmetric	Stepped impedance
[27]	2.4	0.8	28	29	0.065-μm TW	0.2 mm^2	Asymmetric	Stepped impedance
[32]	2.4	1.5	>24	11	0.18-μm	450 × 1000 μm^2	Series-shunt	Optimizing dimensions
[33]	2.4 5.8	0.7 1.1	35 27	21.3 20	0.18-μm	530 × 370 μm^2	Series-shunt	Resistive body-floating
[34]	3.1–4.8	0.78–0.99	30.8	8	0.13-μm	550 × 250 μm^2	Series	Switched body floating
[35]	16.6 28	0.8 1.3	20 23	26.5 25.5	0.13-μm TW	150 × 100 μm^2	Series, asymmetric drain/source	Switched body floating
[36]	5.8	0.8 1	>29 27	17 18	0.18-μm p-Substrate	473 × 451 μm^2	Series-shunt	Minimizing R_B, maximizing R_B
[37]	5	1.44	>22	21.5	0.18-μm DET	<0.1 mm^2	Series-shunt	Transistor stacking
[38]	0.9 2.4	0.5 0.8	29 24	31.3 28	0.13-μm	300 × 380 μm^2	Series-shunt	Transistor stacking
[39]	1.9	1.6	20	33.5	0.18-μm TW	0.4 mm^2	Series-shunt	Transistor stacking; resistive body floating
[40]	57–66	4.5–5.8	24.1–26	4.1	0.13-μm	680 × 325 μm^2	Series-shunt	Traveling wave
[41]	35	2.2	32	23	0.13-μm	180 × 90 μm^2	Series-shunt	Maximizing R_B
[42]	50–94GHz	<3.3 dB	>27 dB	15	0.09-μm	570 × 420 μm^2	Series	Travelling wave
[43]	50–70GHz	2.0	32	13–14	0.13-μm	390 × 320 μm^2	Shunt-shunt	Maximizing R_B
[44]	dc–20GHz	0.7–2.5	25–60	26.2	0.18-μm TW	230 × 250 μm^2	Series-shunt	Artificial transmission line
[45]	5.425	1.8	15	15	0.18-μm	60 × 40 μm^2	Differential architecture	Optimizing dimensions
[46]	0.9 2.4	0.97 1.1	>39 >24	24.3 20.6	0.18-μm p-Substrate	531 × 531 μm^2	Series-shunt	Impedance matching
[47]	15	1.8	17.8	21.5	0.13-μm	400 × 500 μm^2	Series-shunt	Impedance matching

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