*This document summarizes major features of the device. The contents of this document are preliminary. A formal specification is separately provided by "DATA SHEET".

FUJITSU	Analog LSI Design & Product Support Dept. System Solution LSI Division **FUJITSU LIMITED**	**Version 2.0** **Date: Nov/2001**

ASSP For Power Management Applications

2-Channel DC/DC Converter IC with Overcurrent Protection

MB39A104

■DESCRIPTION

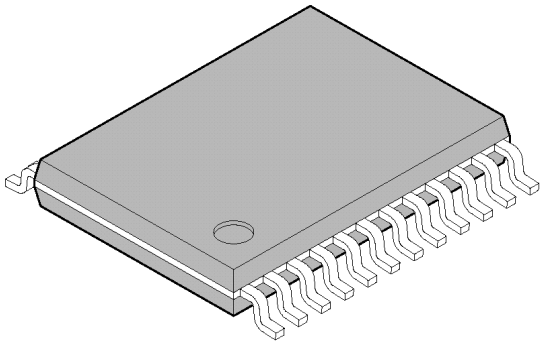
The MB39A104 is a 2-channel pulse width modulation (PWM) DC/DC converter IC with over current protection. This IC corresponds to the operation of wide range (7V to 19V) of the power supply voltage. This IC can be operated by high frequency, therefore the value of the coil can be reduced.
In addition, the DC/DC converter can be few external parts, and various application of the LCD monitor etc. can be achieved by a low cost.

■FEATURES

Wide input voltage operating range :7V to 19V
High frequency operation :1MHz (Max)
High precision reference voltage : 5.0V ± 1%
Built-in over current protection
Built-in standby current function: 0μA(typ)
Built-in circuit for load-independent soft-start
Built-in totem-pole output stage supporting P-channel MOS FETs devices.

■PACKAGE

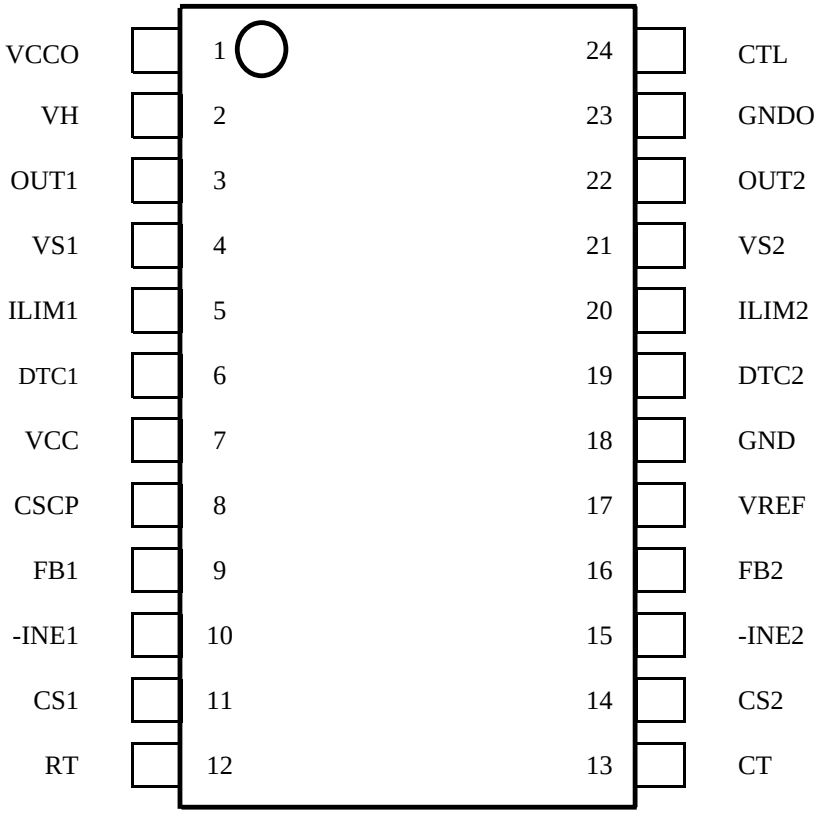
24-pin plastic SSOP



(FPT-24P-M03)

■PIN ASSIGHNMENT

(TOP VIEW)

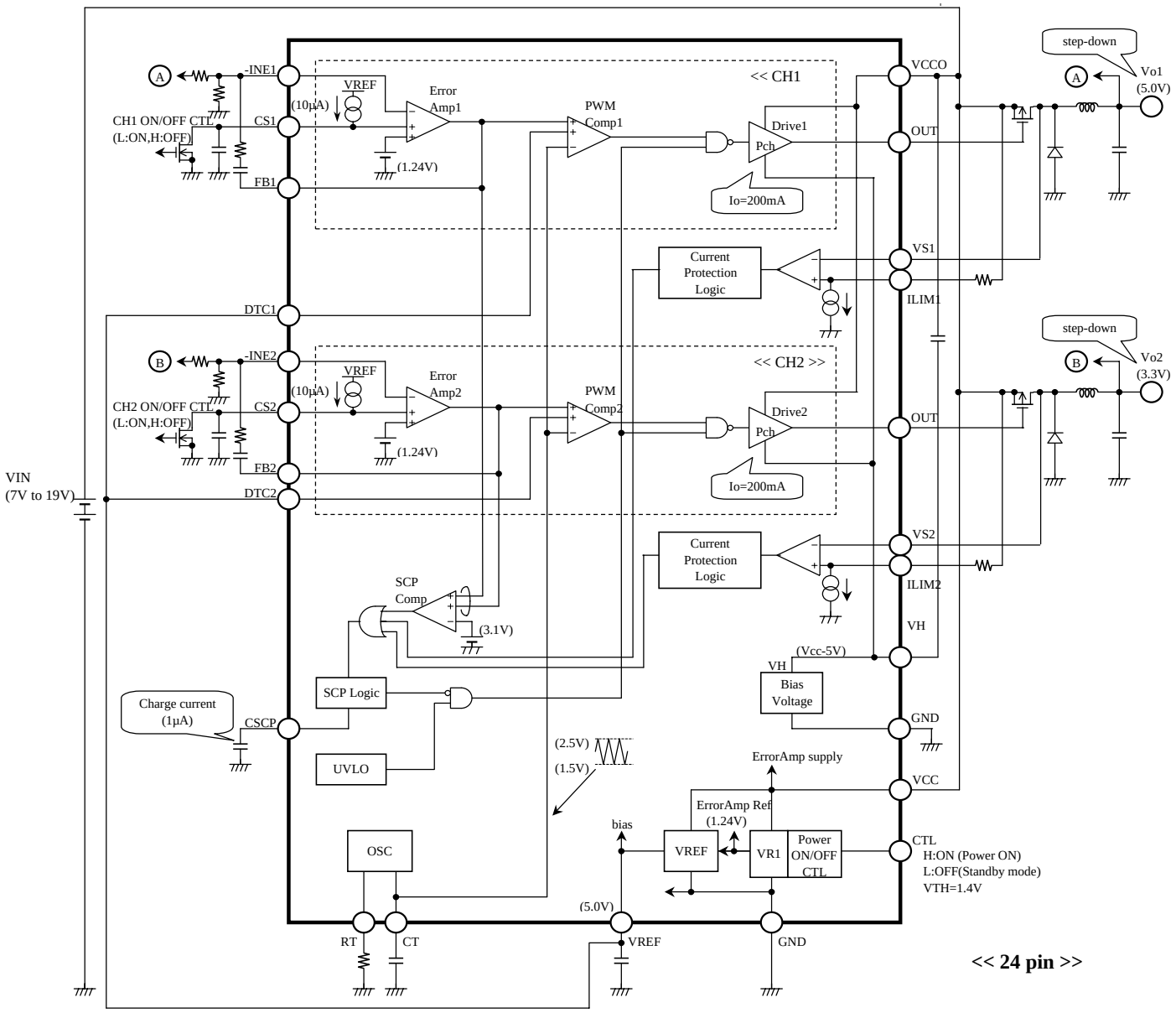


(FPT-24P-M03)

■PIN DESCRIPTION

Pin no.	Symbol	I/O	Descriptions
1	VCCO	-	Output circuit power supply terminal.
2	VH	O	Power supply terminal for FET drive circuit (VH = VCC - 5 V)
3	OUT1	O	CH1 external Pch FET gate drive terminal.
4	VS1	I	CH1 overcurrent protection circuit input terminal.
5	ILIM1	I	CH1 overcurrent detection resistor connection terminal.The overcurrent detection reference voltage is set by external resistance and the internal current source(110μA at RT=24kΩ).
6	DTC1	I	CH1 PWM comparator input terminal.The output is controlled by the lowest voltages in FB1 and the DTC1 terminal voltage.
7	VCC	-	Power supply terminal for reference voltage and control circuit.
8	CSCP	-	Timer-latch short-circuit protection capacitor connection terminal.
9	FB1	O	CH1 Error amplifier (Error Amp 1) output terminal.
10	-INE1	I	CH1 Error amplifier (Error Amp 1)inverted input terminal.
11	CS1	-	CH1 Soft-start capacitor connection terminal.
12	RT	-	Triangular-wave oscillation frequency setting resistor connection terminal.
13	CT	-	Triangular-wave oscillation frequency setting capacitor connection terminal.
14	CS2	-	CH2 Soft-start capacitor connection terminal.
15	-INE2	I	CH2 Error amplifier (Error Amp 2)inverted input terminal.
16	FB2	O	CH2 Error amplifier (Error Amp 2) output terminal.
17	VREF	O	Reference voltage output terminal.
18	GND	-	Output circuit ground terminal.
19	DTC2	I	CH2 PWM comparator input terminal.The output is controlled by the lowest voltages in FB2 the DTC2 terminal voltage.
20	ILIM2	I	CH2 overcurrent detection resistor connection terminal.The overcurrent detection reference voltage is set by external resistance and the internal current source (110μA at RT=24kΩ).
21	VS2	I	CH2 overcurrent protection circuit input terminal.
22	OUT2	O	CH2 external FET gate drive terminal.
23	GNDO	-	Output circuit ground terminal.
24	CTL	I	Power supply control terminal “H” level : IC operating mode “L” level : IC standby mode

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{CC}	VCC, VCCO	20	V
Output current	I_{OUT}	-	60	mA
Peak output current	I_{OUT}	Duty ≤ 5 % (t = 1 / fosc × Duty)	700	mA
Power dissipation	P_D	Ta ≤ +25 °C	740*	mW
Storage temperature	Tstg	-	-55 to +125	°C

*: The package is mounted on the dual-sided epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	VCC, VCCO	7	-	19	V
Reference voltage output current	I_{REF}	-	-1	-	0	mA
VH pin output current	I_{VH}	-	0	-	(30)	mA
Input voltage	V_{INE}	-INE1, +INE2	0	-	V_{CC} - 0.9	V
	V_{DTC}	DTC1,DTC2	(0.3)	-	(V_{CC} - 0.9)	V
CTL pin input voltage	V_{CTL}	-	0	-	19	V
Output current	I_{OUT}	-	-45	-	45	mA
Peak Output current	I_{OUT}	Duty ≤ 5%(t = 1 / fosc × Duty)	-450	-	450	mA
Oscillation frequency	f_{OSC}	-	100	500	(1000)	kHz
Timing capacitor	C_T	-	(47)	(100)	(560)	pF
Timing resistor	R_T	-	(12)	(24)	(120)	kΩ
VH pin capacitor	C_{VH}	-	-	0.1	1.0	µF
Soft-start capacitor	C_S	CS1,CS2	-	(0.1)	(1.0)	µF
Short-circuit protection capacitor	C_{SCP}	-	-	(0.1)	(1.0)	µF
Reference voltage output capacitor	C_{REF}	-	-	0.1	1.0	µF
Operating ambient temperature	Ta	-	-30	+25	+85	°C

WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ELECTRICAL CHARACTERISTICS

(Ta=25ºC,VCC=12V,VCCO=12V,VREF=0mA)

Parameter	Symbol	Pin No.	Conditions	Min.	Typ.	Max.	Unit
1.Reference voltage block (REF)							
Output voltage	VREF	17	-	(4.95)	(5.00)	(5.05)	V
Input stability	Line	17	VCC = 7V to 19V	-	3	10	mV
Load stability	Load	17	VREF = 0 mA to -1 mA	-	1	10	mV
Short-circuit output current	IOS	17	VREF = 1 V	(-50)	(-25)	(-12)	mA
2.Under voltage lockout protection circuit (UVLO)							
Threshold voltage	VTLH	17	VREF ↗	(2.6)	2.8	(3.0)	V
	VTHL	17	VREF ↘	(2.4)	2.6	(2.8)	V
Hysteresis width	VH	17	*	-	(0.2)	-	V
3.Short-circuit protection Logic block (SCP Logic)							
Threshold voltage	VTH	8	-	0.68	0.73	0.78	V
Input source current	ICSCP	8	-	-1.4	-1.0	-0.6	µA
Reset voltage	VRST	17	VREF ↘	(2.4)	(2.6)	(2.8)	V
4.Short-circuit protection Comparator block (SCP Com.)							
Threshold voltage	VTH	8	-	(2.8)	3.1	(3.4)	V
5.Triangular wave form oscillator block (OSC)							
Oscillation frequency	fOSC	13	(CT=100pF,RT= 24 kΩ)	450	500	550	kHz
6.Soft-start block (CS1,CS2)							
Charge current	ICS	11,14	CS1=0V,CS2=0V	-14	-10	-6	µA
7.Error amplifier block (Error Amp 1, Error Amp 2)							
Threshold voltage	VIO	9,16	FB1=2V,FB2=2V	(1.227)	(1.240)	(1.253)	V
Input bias current	IB	10,15	-INE1=0V,-INE2=0V	(-120)	(-30)	-	nA
Voltage gain	AV	9,16	DC	-	100	-	dB
Frequency bandwidth	BW	9,16	AV = 0dB	-	(1.6)	-	MHz
Output voltage	VOH	9,16	-	4.7	4.9	-	V
	VOL	9,16	-	-	40	200	mV
Output source current	ISOURCE	9,16	FB1=2V,FB2=2V	-	-2	-1	mA
Output sink current	ISINK	9,16	FB1=2V,FB2=2V	150	200	-	µA

* : Standard design value

(Ta=25ºC,VCC=12V,VCCO=12V,VREF=0mA)

Parameter	Symbol	Pin No.	Conditions	Min.	Typ.	Max.	Unit
8.PWM comparator block (PWM Comp.1,PWM Comp.2)							
Threshold voltage	V_{T0}	6,19	Duty cycle = 0 %	(1.4)	(1.5)	-	V
	V_{T100}	6,19	Duty cycle = 100 %	-	(2.5)	(2.6)	V
Input bias current	I_{DTC}	6,19	DTC1=0.4V,DTC2=0.4V	(-2.0)	(-0.6)	-	µA
9.Overcurrent protection circuit block (OCP1,OCP2)							
ILIM terminal input current	I_{ILIM}	5,20	R_T=24kΩ	(99)	(110)	(121)	µA
Offset voltage	V_{IO}	5,20	*	-	1	-	mV
10.Bias voltage (VH)							
Output voltage	VH	2	VCC=VCCO=7V to 19V , VH=0 to 30mA	(Vcc-5.5)	(Vcc-5.0)	(vcc-4.5)	V
11.Output block (Drive1,Drive2)							
Output source current	I_{SOURCE}	3,22	OUT1 = 7V,OUT2 = 7V,Duty ≤ 5%	-	(-200)	(-100)	mA
Output sink current	I_{SINK}	3,22	OUT1 = 12V,OUT2 = 12V,Duty ≤ 5%	(100)	(200)	-	mA
Output ON resistor	R_{OH}	3,22	OUT1 = -45 mA OUT2 = -45 mA	-	(8.0)	(12.0)	Ω
	R_{OL}	3,22	OUT1 = 45 mA OUT2 = 45 mA	-	(6.5)	(9.7)	Ω
12.Control block (CTL)							
CTL input voltage	V_{IH}	24	Operating mode	2	-	19	V
	V_{IL}	24	Standby mode	0	-	0.8	V
Input current	I_{CTLH}	24	CTL = 5 V	-	(50)	(100)	µA
	I_{CTLL}	24	CTL = 0 V	-	-	1	µA
13.General							
Standby current	I_{CCS}	1,7	CTL = 0V	-	(0)	(10)	µA
Power supply current	I_{CC}	1,7	CTL = 5V	-	(5.0)	(7.5)	mA

* : Standard design value

■FUNCTIONAL DESCRIPTION

Control block (CTL)

As CTL terminal is setting "L" level,IC is the standby mode.The supply current in the standby mode is 10μA maximum.

Functional matrix by the control circuit operating

CTL	IC
L	OFF(Standby)
H	ON(Operating)

Protection circuit

Functional matrix by the protection circuit operating

Operation circuit	CS1	CS2	OUT1	OUT2
Short-circuit protection circuit	L	L	H	H
Under voltage lockout protction circiut	L	L	H	H
Overcurrent protection circuit	L	L	H	H

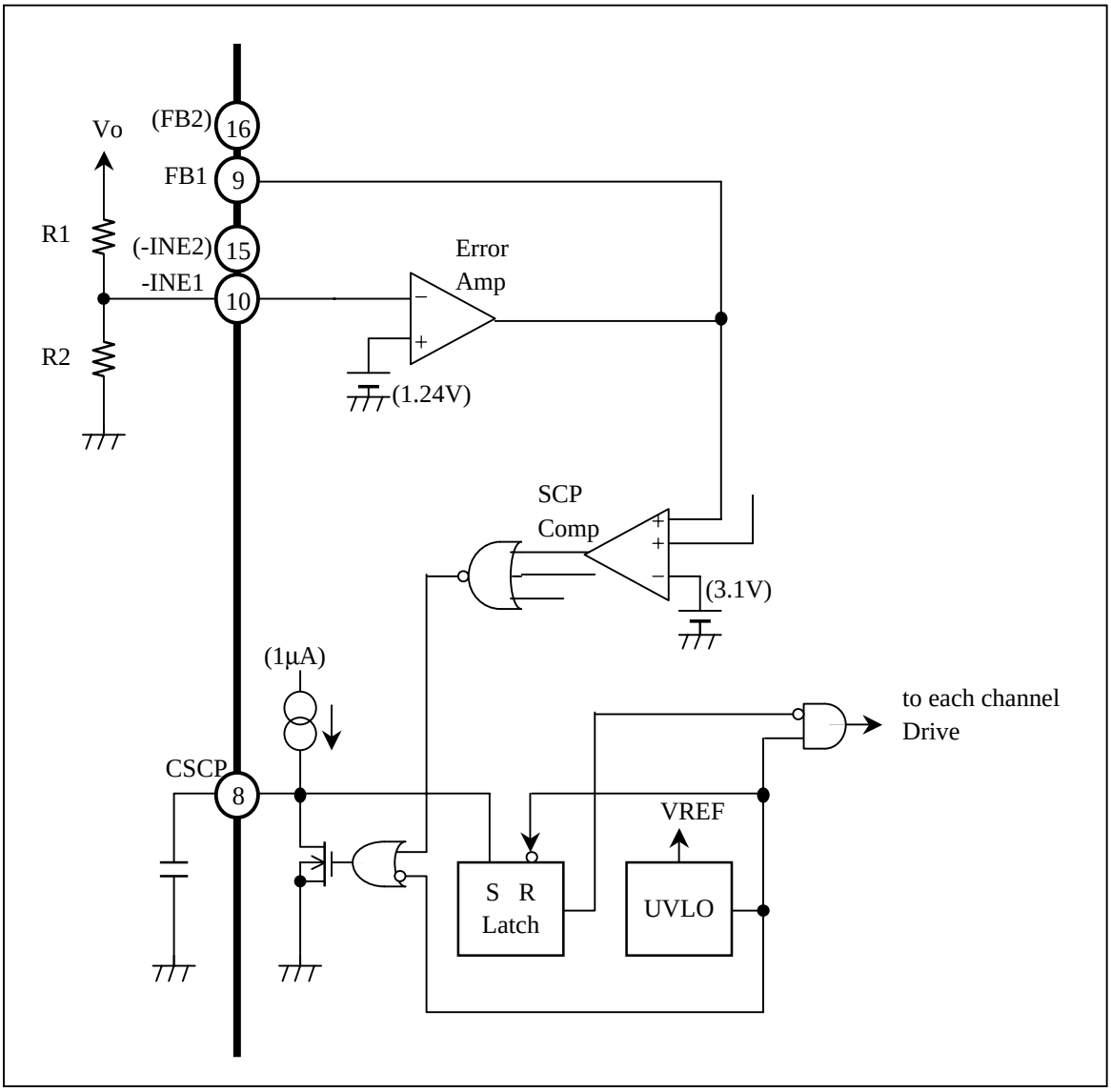
■SETTING THE TIMER-LATCH SHORT-CIRCUIT PROTECTION

Each channel uses the short-circuit detection comparator (SCP Comp.) to always compare the error amp's output level to the reference voltage.
While the DC/DC converter load conditions are stable on both channels, the short-circuit detection comparator keeps its output at the "L" level and the CSCP terminal (pin 8) remains at the "L" level.
If a load condition changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the short-circuit detection comparator changes its output to the "H" level. This causes the external short-circuit protection capacitor Cscp connected to the CSCP terminal to be charged at 1μA.

Short-circuit detection time : tscp

$$tscp\ (s) \cong 0.73 \times Cscp\ (\mu F)$$

When the capacitor Cscp is charged to the threshold voltage (VTH ≅ 0.73V), the protection circuit sets the latch and turns off the external FET (setting the dead time to 100%). At this time, the latch input is closed and the CSCP terminal (pin 8) is held at the "L" level.



<Timer-latch short-circuit protection circuit>

■SETTING THE OVERCURRENT DETECTION CURRENT

The overcurrent protection circuit is actuated upon completion of the soft-start period.

If an overcurrent flows,the circuit detects the increase in the voltage between the main side FET's drain and source by the main sideFET ON resistor (RON). When the state of overcurrent continues more than time set by capacitor connected with CSCP terminal (pin 3 ,pin 22), output is fixed at "H" level.

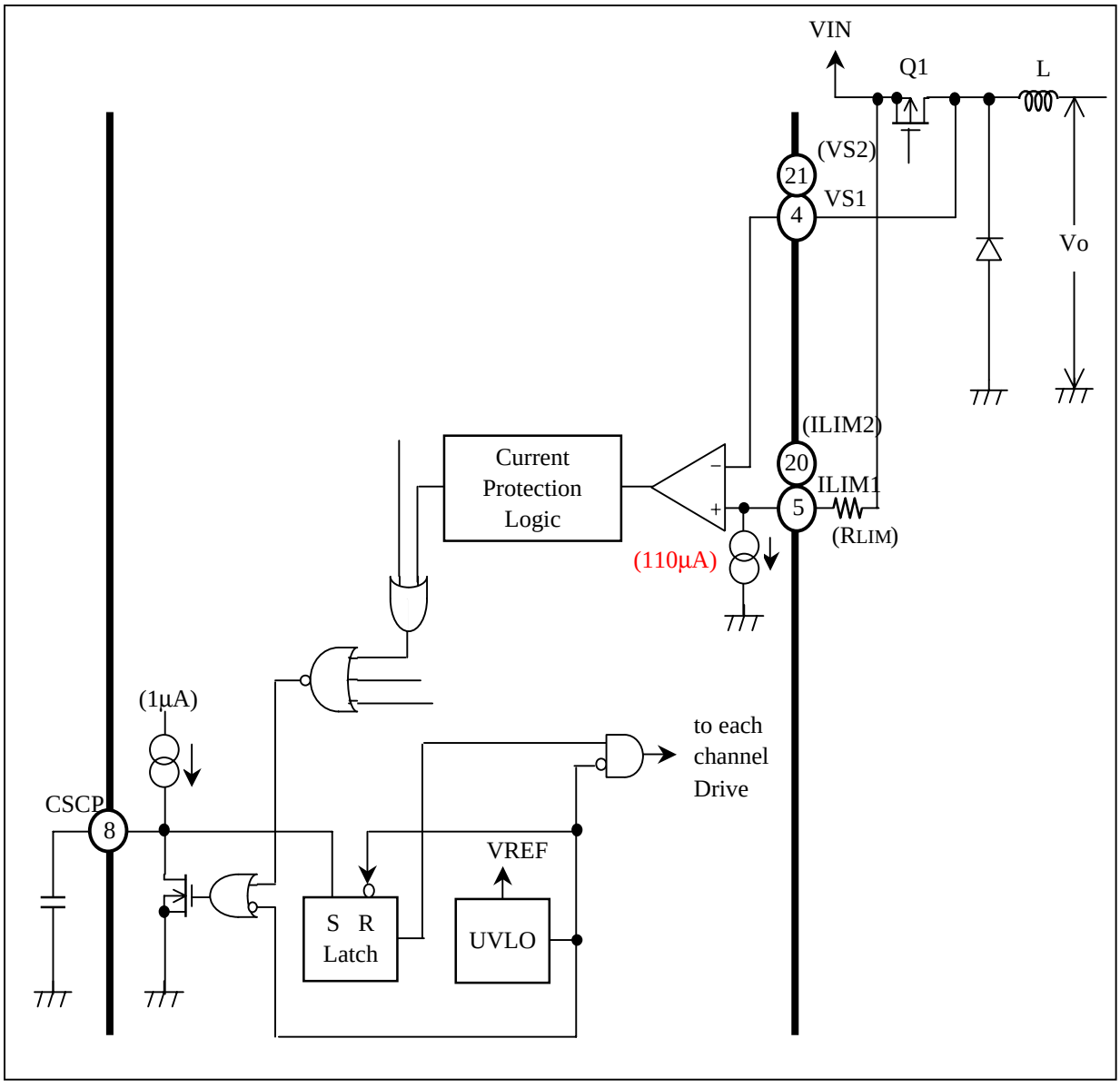
The detection current value can be set by the resistors (RLIM) connected between the drain of FET (Q1) and ILIM 1,2 terminal (pin 5, pin 20) .

Detection current value : IOCP

$$IOCP(A) \cong \frac{ILIM \times RLIM}{Ron} - \frac{(VIN-Vo) \times Vo}{2 \times VIN \times fosc \times L}$$

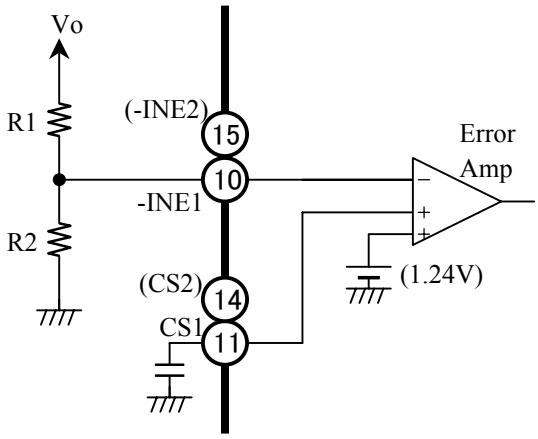
$$ILIM(A) \cong \frac{2.7}{RT}$$

Note) The detection current value is influenced by ON resistor (RON) difference (contains the temperature characteristic) on the external FET(Q1) and the board pattern. Therefore, please confirm current value with the board actually used when you set the detection current value.



<Overcurrent detection circuit>

■SETTING THE OUTPUT VOLTAGE



$$Vo(V) = \frac{1.24}{R2}(R1+R2)$$

■SETTING THE TRIANGULAR WAVE OSCILLATROR FREQUENCY

The triangular wave oscillation frequency can be set by the timing resistor (R_T) connected the RT terminal (pin 12) and the timing capacitor (C_T) conneccted the CT terminal (pin 13).

Triangular wave oscillation frequency : fosc

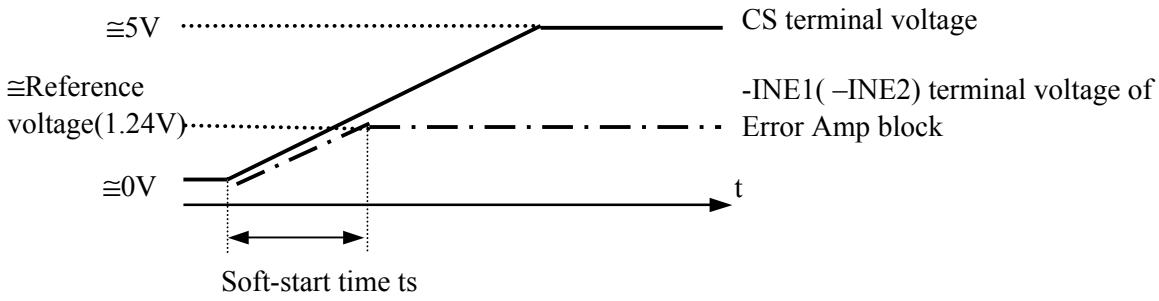
$$fosc(kHz) \cong \frac{1200000}{C_T(pF)\times R_T(k\Omega)}$$

■SETTING THE SOFT START TIME

The soft-start function prevents rush current events when the IC power is turned on , by connecting soft-start capacitor(C_S1,C_S2) to the CS terminal(pin 11,pin 14). The CTL terminal (pin 24) becomes "H" level, and when the IC is activated (more than UVLO threshold voltage), IC charges to external soft start capacitor (C_S1,C_S2) of the CS1,CS2 terminal at 10μA. Because the error amp Output terminal (FB1 (pin 9) (FB2 (pin 16))) is determined by the comparison to the lower of the two non-inverted input terminals (Reference voltage(1.24V), CS1 terminal voltage (CS2 terminal voltage)) to the inverted input terminal (-INE1 (pin 10) ,-INE2 (pin15)) voltage, the FB1 (FB2) of the soft start interval is determined by the comparison to the Reference voltage(1.24V) and CS1 terminal voltage. Thus the DC/DC converter output voltage rises in proportion to the CS1 (CS2) terminal voltage as the external soft-start capacitor connected to the CS1 (CS2) terminal charges. The soft start time is determined by the following formula.

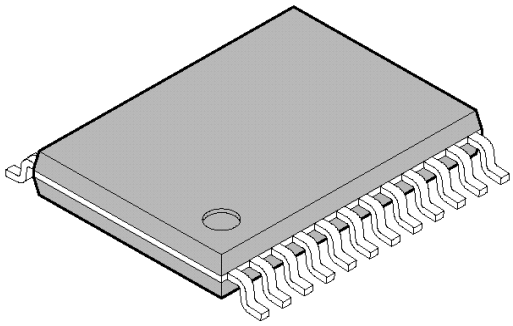
Soft-start time : ts(time to output 100%)

$$ts\ (s) \cong 0.124\times Cs\ (\mu F)$$



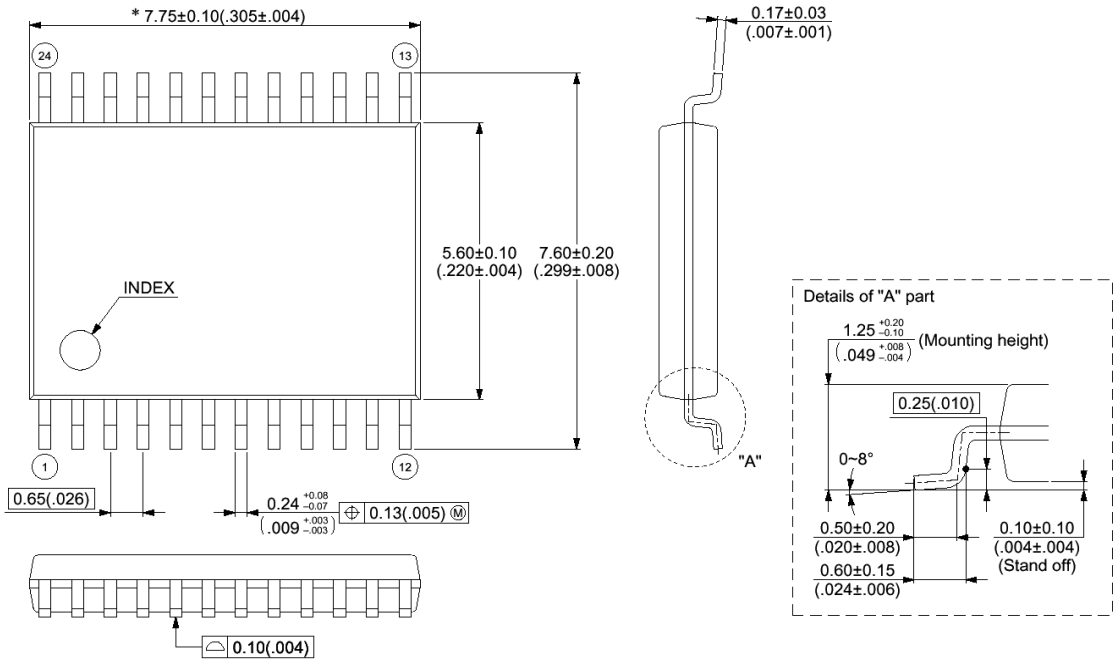
■PACKAGE DIMENSION

FPT-24P-M03

24-pin plastic SSOP		
 (FPT-24P-M03)	Lead pitch	0.65 mm
	Package width × package length	5.6 × 7.75 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.45 mm MAX
	Weight	0.12 g
	Code (Reference)	P-SSOP24-5.6×7.75-0.65

24-pin plastic SSOP
(FPT-24P-M03)

Note1: Pins width and pins thickness include plating thickness.
Note2: * This dimension does not include resin protrusion.



Dimensions in mm (inches).

■ USAGE PRECAUTIONS

1. Printed circuit board ground lines should be set up with consideration for common impedance.

2. Take appropriate static electricity measures.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kW to 1 MW between body and ground.

3. Do not apply negative voltages.

The use of negative voltages below -0.3V may create parasitic transistors on LSI lines, which can cause abnormal operation.

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