The Rise of Automotive Grade, AEC-Q100 Clock Generators

By Kyle Beckmeyer, Senior Marketing Manager, Timing, Silicon Labs

There have been an abundance of technological breakthroughs in automotive electronics in recent years. More than ever, manufacturers are motivated to bring feature-rich infotainment systems and advanced driver assistance systems (ADAS) to their product lines as they pursue the development of fully autonomous vehicles. Advanced semiconductor technologies are the key reasons behind the swift development and deployment of new vehicle systems. Semiconductor manufacturers are bringing automotive grade products such as higher bandwidth processors, GPUs, high speed PCI-Express (PCIe) switches, Ethernet switch SoC/PHYs, and FPGAs to market more frequently. The adoption of the latest generation of automotive grade IC platforms and connectivity is expected to significantly advance system capabilities, features, performance, and reduce cost. On the other hand, these improvements also create new design complexity challenges for system designers.

One challenge to explore in particular is how to fulfill the growing need for high precision, low-jitter reference clocks that are required for the high speed SerDes in processors, FPGAs, switch SoCs, Ethernet PHYs, USB PHYs, and PCIe Gen3/4 endpoints. These solutions are being used in automotive networking gateway, infotainment, digital cockpit, ADAS, Lidar, and automated driving control units. As these new applications evolve, the number of precision reference clocks needed is steadily increasing, requiring a combination of both single-ended and differential clock formats, of varying frequencies, with RMS phase jitter requirements as low as 300 fs.

Learn How

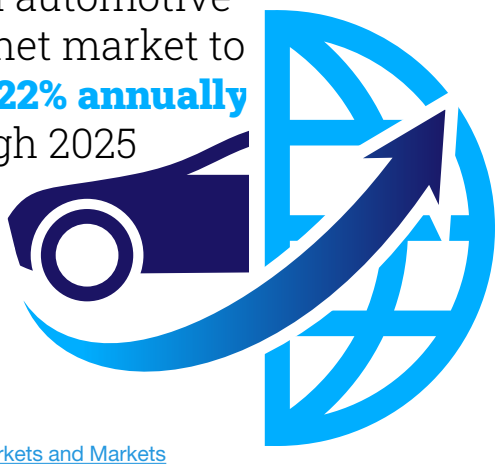
- Ethernet, PCI-Express, and high-speed SerDes are driving next-generation automotive timing requirements
- To define a clock tree leveraging feature-rich clock generators to simplify your design
- Innovative clock generator output driver design and new layout techniques help overcome CISPR emissions challenges
- Silicon-based timing solutions increase system reliability over legacy quartz crystals and oscillators

Timing Growth in Modern Automotive Electronics

Historically, automotive system designs have used lower bandwidth processors and microcontrollers, which only required one or two single-ended reference clock frequencies for each board design. Fulfilling these timing requirements was straightforward because they simply used one or two quartz crystals or crystal oscillators. As the number of reference clocks increases in modern automotive electronics design, the easiest way to satisfy the timing requirements is to simply add more quartz crystals or oscillators; however, scaling the number of quartz-based components has numerous drawbacks and limitations. In addition to increasing board space and cost, quartz crystals and oscillators are inherently susceptible to shock and vibration failure with high failure-in-time (FIT) rates. Increasing the number of quartz crystals and oscillators also increases the number of points of failure in a system design. This type of failure can trigger long-term reliability risk as well.

For many years, the communications, computing, industrial, and consumer markets have used silicon-based integrated clock generator solutions instead of quartz crystals and oscillators to fulfill their precision reference clock timing requirements. Precision, low-jitter reference clocks are critically important in high-speed designs to ensure proper system operation and minimize bit error rates. As processor speed and SerDes bandwidth level increase, the jitter requirements on the reference clock become more difficult to meet. The latest generation of automotive networking gateways, ADAS sensors, and automated driving platforms are using high bandwidth processors, FPGAs, 1G/10GbE connectivity, and PCIe Gen3/4/5 data buses, which require differential clocks with less than 500 fs RMS phase jitter. Clock generators can consolidate the functionality of up to eight quartz crystals or oscillators into a single IC and provide excellent RMS phase jitter performance (<300 fs RMS) on clock outputs while offering numerous additional features that help simplify system reference clock design.

Global automotive Ethernet market to grow **22% annually** through 2025



Source: Markets and Markets

Simplifying Clock Tree Design

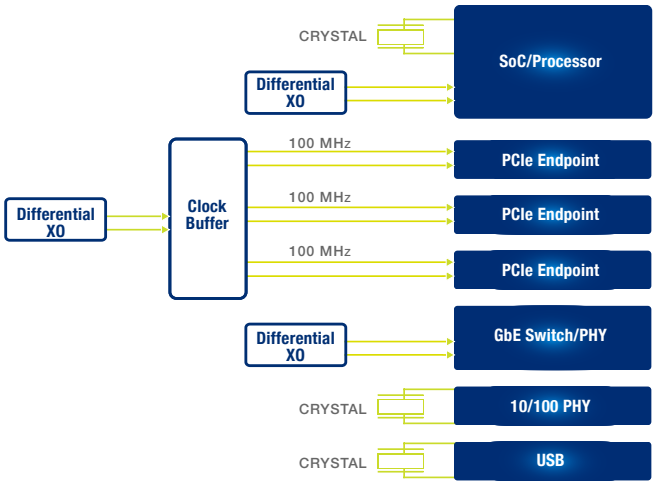
Selecting and defining an optimal timing solution can be simplified by summarizing the set of reference clocks needed in a system design. A set of reference clocks is often referred to as a 'clock tree'. A clock tree usually includes the input reference frequencies, output clock frequencies needed by endpoints, the clock output format levels, and the maximum jitter performance level for each reference clock, which is typically specified by each endpoint device manufacturer.

Clock Tree Design Guidelines

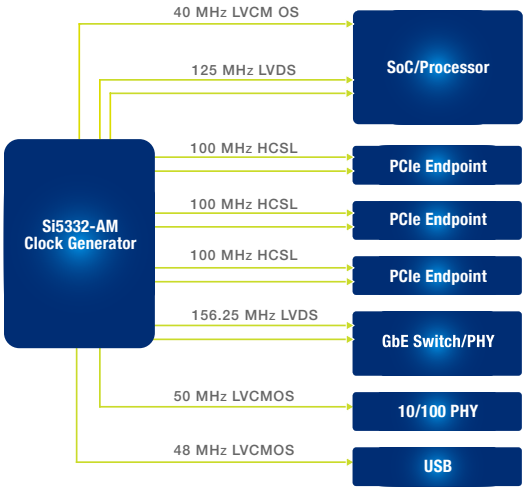
Frequency	Format	Copies Needed	Jitter	Endpoint
100 MHz	HCSL	3	500 fs RMS	PCIe Gen4 endpoints
100/125 MHz	LVDS	1	500 fs RMS	SoC/Processor
40 MHz	LVCMOS	1	1 ps	SoC/Processor
125 MHz	LVDS	1	700 fs RMS	1GbE Switch/PHY
25 MHz	LVCMOS	1	2 ps	10/100 PHY
48 MHz	LVCMOS	1	2 ps	USB

In addition to the new automotive processor, FPGA, connectivity and data bus semiconductor solutions being released into the market, AEC-Q100 qualified silicon-based timing solutions are now available to simplify the growing complexity of clock tree design in automotive applications. By consolidating reference clocks into an integrated clock generator, system designers can reduce points of failure, increase system reliability, and realize notable advantages in jitter performance and frequency flexibility. Additional benefits include a reduction in board space area and reduced total solution cost over legacy quartz-based devices.

Legacy Approach Using Quartz Components



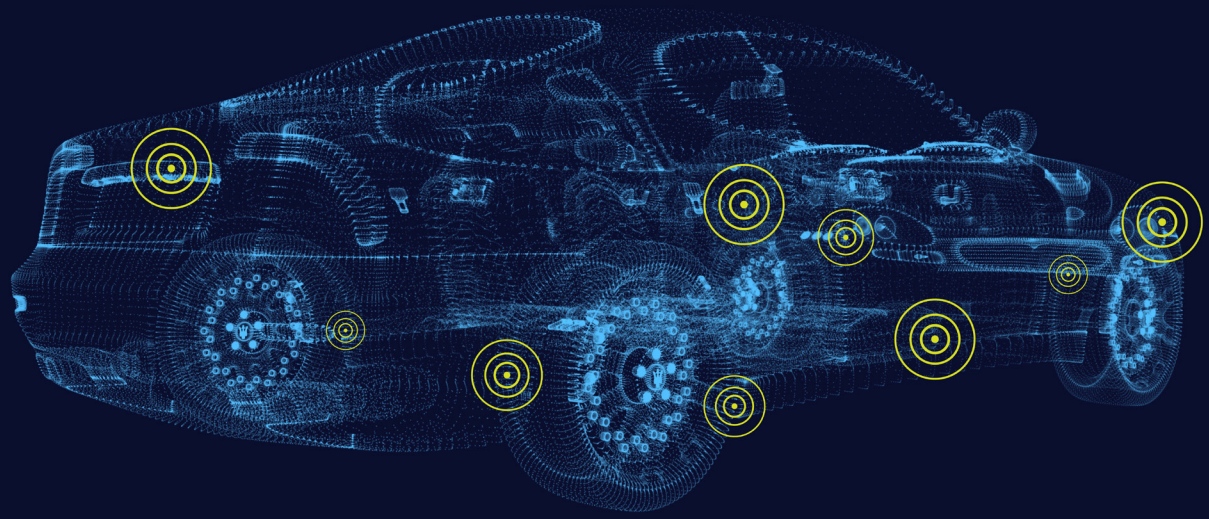
Optimal Solution Using Clock Generator



Automotive Timing Solutions Reinvented

Silicon Labs recently introduced the Si5332-AM products, a family AEC-Q100 qualified programmable clock generators capable of consolidating the functionality of up to 8 quartz crystals and/or oscillators into a single-IC. These devices provide a unique combination of frequency-flexibility and industry leading RMS phase jitter performance, in a programmable platform leveraging the ClockBuilder Pro software utility. Si5332-AM features two MultiSynth fractional output dividers capable of synthesizing output frequencies with ppb accuracy, while at the same time, synthesizing integer related output frequencies. Numerous additional features are also included: spread spectrum modulation for EMI reduction, output enable control, output frequency selection, in-system programmability, multi-profile selection, and input reference clock redundancy. Fault detection and health monitoring indicators are included as well for safety critical applications.

Industry adoption of the new ISO26262 standard and ASIL requirements present addition design complexity challenges. The Si5332-AM is the only AEC-Q100 qualified clock generator available with features to assist system designers in achieving system safety goals. The devices feature primary and backup input reference capability, and fault detection and health monitoring status indicators, which can actively communicate with a system safety manager. If a fault is detected, the system safety manager can take action to migrate from primary source to backup source, ensuring the output clocks maintain the correct frequencies to the endpoints. In the event the backup reference also faults, the Si5332-AM can enter into AlwaysOn mode, defaulting all output clocks to the on-chip VCO frequency.



Until recently, system designers have been reluctant to adopt clock generators because of the emissions that single-ended clocks and long clock traces cause, potentially resulting in CISPR25 Class4 or Class5 testing failures. Spread spectrum has been a common feature to reduce emissions but there are a limited number of frequencies and endpoints that can tolerate a reference clock with spread spectrum applied. To overcome this challenge, Silicon Labs has employed the use of complementary LVCMOS output buffer technology in the Si5332-AM devices. Combined with newly developed layout guidelines, Silicon Labs has demonstrated that driving a pair of complementary single-ended clocks 180 degrees out of phase in a differential trace effectively cancels the emissions field generated. Further details of the design techniques and CISPR25 Class4 and Class5 testing results are provided in AN1237.

Use of automotive Ethernet and the PCIe data bus are rapidly expanding within automotive electronics. As bandwidth levels and data rates increase, RMS phase jitter performance on the single-ended and differential reference clocks being supplied to the SerDes within Ethernet switches, PHYs, and PCIe endpoints become increasingly important design parameters. The Si5332-AM provides the ability to synthesize all of the frequencies needed for 1GbE/2.5GbE/5Gbe/10GbE devices, as well as PCIe Gen1/2/3/4/5 endpoints commonly used in automotive gateways and ADAS applications. The PCI-SIG specifies unique filters that must be used to properly measure RMS Phase jitter on PCIe reference clocks. To prevent confusion and simplify the process, system designers and signal integrity specialists can use the Silicon Labs' PCIe Clock Jitter Tool.

Silicon Labs gives systems designers the power to quickly and easily create a customized configuration specific to each design's unique clock tree through the ClockBuilder Pro software utility. ClockBuilder Pro guides users through a series of steps to enter information about their clock tree requirements, enable a multitude of features available, all while providing feedback to help optimize the configuration file for performance and power consumption. After a configuration file is complete, the tool also provides the ability to generate a datasheet addendum and/or custom part number.

Learn about the entire family of Silicon Labs' AEC-Q100 qualified timing solutions and automotive applications.

Si5335x Clock Buffers

Si5332- AM Clock Generators

Si5225x PCIe Gen1/2/3/4/5 Buffers

Si5325x PCIe Gen1/2/3/4/5 Clocks

Find out more details about timing requirements in networking gateways, ADAS, Lidar and Camera systems, digital cockpit, and automated driving platforms here: https://www.silabs.com/timing/automotive-timing-solutions.

Kyle Beckmeyer serves as a senior marketing manager for Silicon Labs' timing products, responsible for managing product strategy, new production introductions, and business development in data center and automotive markets. Kyle has over 15 years of timing product experience, and holds a Bachelor of Science degree in electrical engineering from the University of California, Davis and a master's degree in business adminstration from Santa Clara University.

Interested in learning more about how Silicon Labs' automotive solutions can help your business?

Contact us today.

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