

Book of Knowledge (BOK) for NASA Electronic Packaging Roadmap

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
Pasadena, California

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

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Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
Pasadena, California

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Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

<http://nepp.nasa.gov>

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OBJECTIVES AND PRODUCTS

The objective of this document is to update the NASA roadmap on packaging technologies (initially released in 2007) and to present the current trends toward further reducing size and increasing functionality. Due to the breadth of work being performed in the area of microelectronics packaging, this report presents only a number of key packaging technologies detailed in three industry roadmaps for conventional microelectronics and a more recently introduced roadmap for organic and printed electronics applications. The topics for each category were down-selected by reviewing the 2012 reports of the International Technology Roadmap for Semiconductor (ITRS), the 2013 roadmap reports of the International Electronics Manufacturing Initiative (iNEMI), the 2013 roadmap of association connecting electronics industry (IPC), the Organic Printed Electronics Association (OE-A). The report also summarizes the results of numerous articles and websites specifically discussing the trends in microelectronics packaging technologies.

Key Words: packaging technologies, roadmap, ITRS, iNEMI, IPC, FBGA, BGA, CGA, CSP, 3D, printed electronics, large area electronics, and packaging hierarchy

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1.0 EXECUTIVE SUMMARY

As with many advancements in the electronics industry, consumer electronics is driving the trends for electronic packaging technologies toward reducing size and increasing functionality. In the past, there was always a ceramic version of a plastic package, including the plastic ball-grid-array (PBGA) which has the analogous ceramic ball-grid-array (CBGA) and ceramic column-grid-array (CCGA or CGA). Today, there are few, if any, ceramic (high reliability) versions of the latest technologies. In fact, as with the BGA packages, ceramic packaging may not always be the most reliable choice when taking into account the board mounting process. Solder joint reliability has become an integral part of the electronic packaging equation for overall reliability. NASA has worked in that arena with industry in the past and will need to continue to do so in the future as most high density packaging utilizes both high I/O single chip with finer pitches and stacking of single chip packages for lower I/O— most with solder balls (or bumps).

Microelectronics meeting the technology needs for higher performance (faster), reduced power consumption and size (better), and commercial-off-the-shelf (COTS) availability (cheaper). Due to the breadth of work being performed in the area of microelectronics packaging, this report presents only a number of key packaging technologies detailed in three industry roadmaps for conventional microelectronics (Figure 1-1) and a more recently introduced roadmap for organic and printed electronics applications (Figure 1-2). The topics for each category were down-selected by reviewing the 2012 reports of the international technology roadmap for semiconductor (ITRS) [1], the 2013 roadmap reports of the International Electronics Manufacturing Initiative (iNEMI) [2], the 2013 roadmap of association connecting electronics industry (IPC) [3], the Organic Printed Electronics Association (OE-A) [4], as well as review of numerous articles and websites discussing the trends in microelectronics packaging technologies.

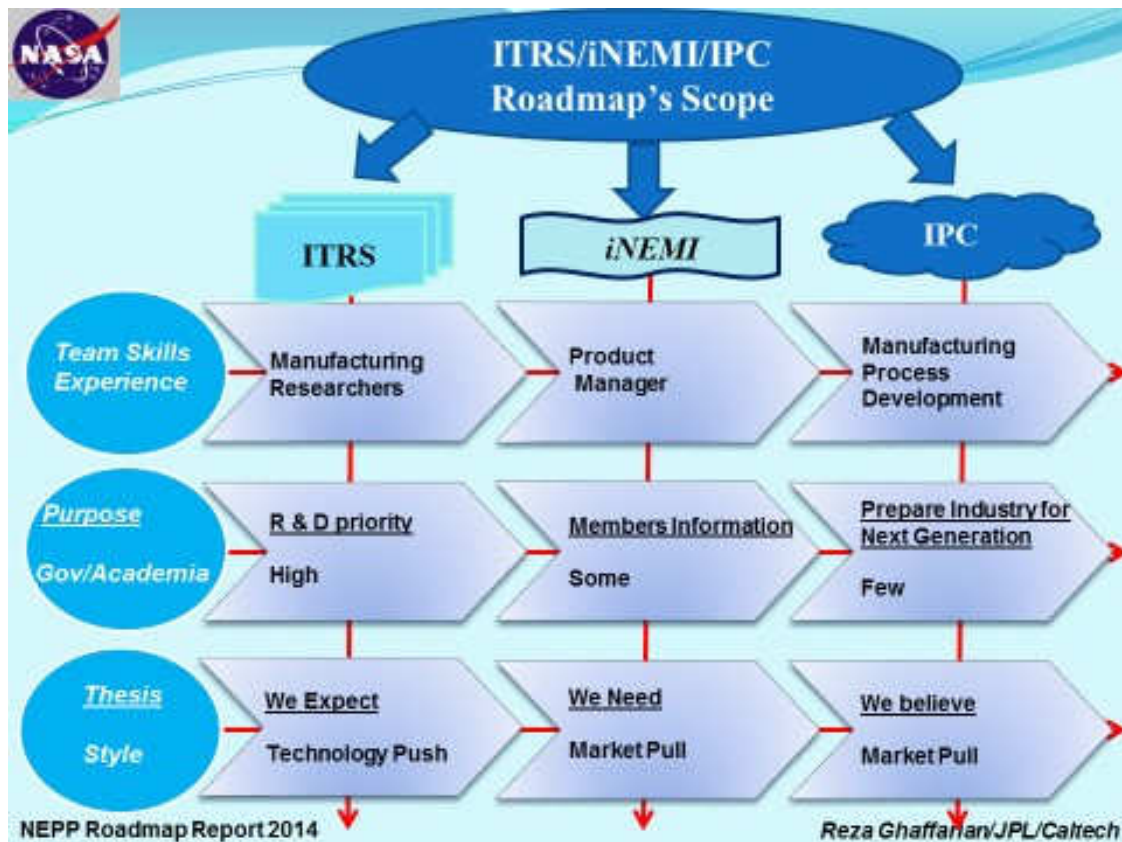


Figure 1-1. ITRI, iNEMI, and IPC roadmap focus and development styles.



Figure 1-2. OE-A roadmap showing key technology and application coverage [4].

From among numerous packaging technologies, four key areas were selected (see Figure 1-3) for further detail discussion. These technologies are presented in detail in the following chapters with potential use for high-reliability applications were identified and discussed. The key findings regarding the four packaging technologies are as follows:

- **Single chip area array packages:** Single chip packages including BGAs and CSPs (chip-scale packages) are now widely used for many electronic applications including portable and telecommunication products. More than 1000 I/O ceramic column grid arrays (CGAs) are now offered by package suppliers. The finer pitch wafer level package (WLP) became popular because of size and cost reduction as well as their wider applications. Package growths projected by iNEMI predicts a moderate growth for quad flat pack/ leadless chip carrier (QFP/LCC) and chip-on-board (COB) whereas significant growth both for QFN and WLP.
- **2.5 D/3D Packaging:** For high density packaging, the migration to three dimensional (3D) using conventional interconnection method has become mainstream. Currently, 3D packaging consists of stacking of packaged devices, called package-on-package (PoP), stacking of die within a package called package-in-package (PiP) or stacked wire bonded die (primarily memory). Both technologies are used today with the promise of stacking die (without wire bonds)—yet to be fully field tested—using through-silicon-via (TSV) technology with active on active stacking. In the meantime, the 2.5D technology – active on passive-with only the interposer TSV is being implemented. Xilinx transitioned die with 28 nm technology to 65 nm technology. iNEMI projects a decline in conventional DIP leaded package as well wire bonded die BGA with conventional pitch, whereas a moderate increase for wire bonded die of finer pitch BGAs. Significant increases are projected for flip chip FPGA as well as stack packaging technology.

- **Embedded Passive and Active Die:** Integrated resistors and capacitors within a PCB as a thin film layer is a matured technology, but the trend is now towards implementation of insertion of passive and active components. Embedded components are defined as a passive/active discrete/devices that are placed on or on inner layers of substrate/board. Embedded passive discret es is near maturing whereas much work is needed for wider implementation of active devices. A rapid growth is projected for automobile/medical, consumer and mobile/wireless industry sectors.
- **Printed Electronics:** Printed electronic technology (PET) is complementary to silicon chip technology, which industry continues to find special applications for, with significant cost per area and throughput benefits. PET's key applications are briefly presented.

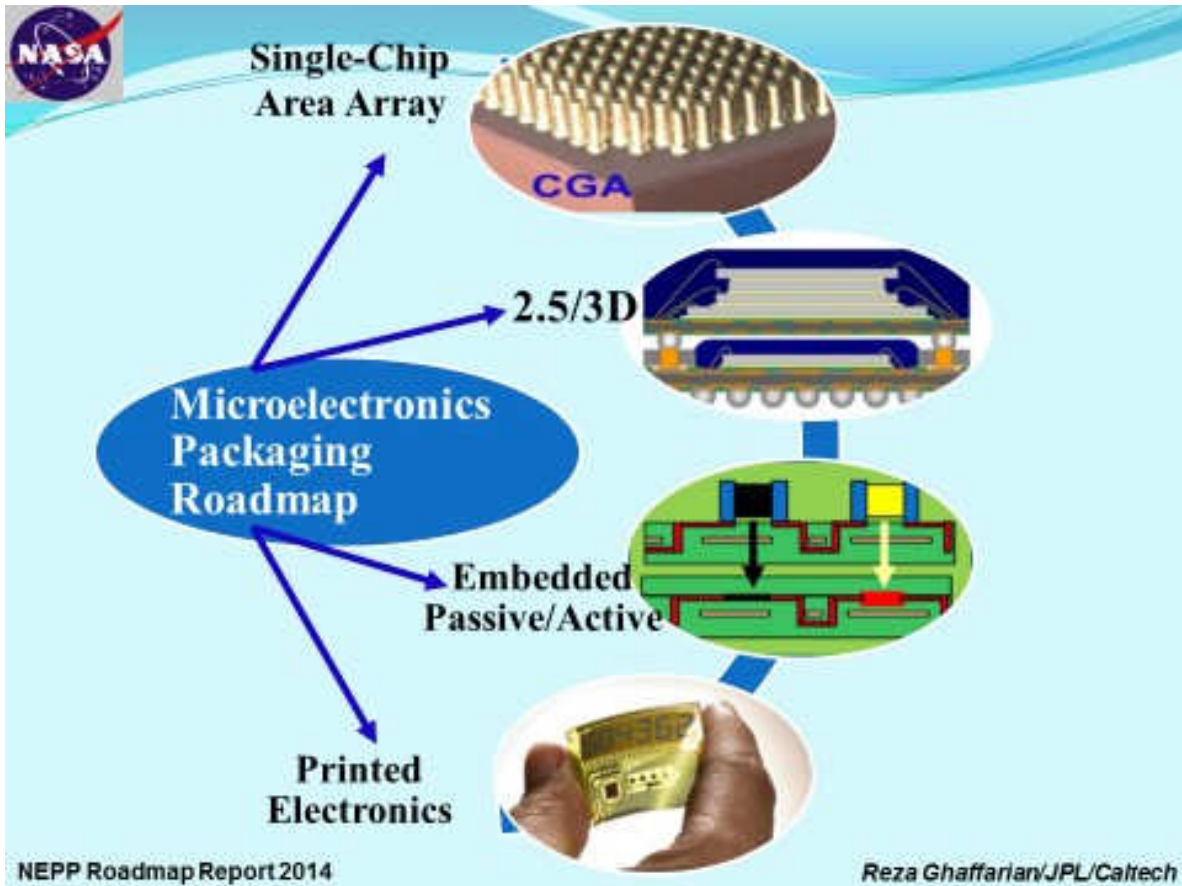


Figure 1-3. Microelectronics packaging roadmap covering single chip, 2.5/3D stack, embedded active/passive, and printed electronics technologies.

2.0 KEY ROADMAP ORGANIZATIONS

2.1 Introduction

Industry roadmap organizations have been created to address trends in numerous technologies including microelectronic, optics, and printed electronics. Figure 2-1 compares key attributes and overlap areas of three industry roadmaps discussed in the following, i.e., ITRS, iNEMI, and IPC. The ITRS roadmap emphasis is on the front-end conventional microelectronics field, and it is sponsored by the world’s five leading chip manufacturers. The objective of the ITRS is to ensure cost-effective advancements in the performance of integrated circuits and the products that employ such devices; thereby supporting the health and success of this industry.

Table 2-1. Team member make up and skills as well technology focus and development for ITRS iNEMI, and IPC —the key roadmap development industries for microelectronics sectors [3].

	ITRS	iNEMI	IPC
Team Makeup	Senior Techs. -Management -Engineers	Senior Techs. -Management -Engineers	Senior Techs. -Management -Engineers
Team Skills/Experience	Manufacturing Researchers	Product Managers	Manufacturing Process Develop.
Industry R&D Invest.	<10%	4-5%	>1%
Government and Academia Participation	High	Some	Few
Roadmap Purpose	R&D priority	Members' Information	Prepare Industry for Next Generation
Thesis	We Expect	We Need	We Believe
Style	Technology Push	Market Pull	Market Pull

iNEMI, a consortium of approximately 100 leading electronics manufacturers, suppliers, associations, government agencies and universities, is another industry roadmap provider. iNEMI roadmaps cover the future technology requirements of the global electronics industry by identifying and prioritizing gaps in technology and infrastructure. With the support of participant companies, iNEMI generates timely, high-impact deployment projects to address or eliminate those gaps.

The IPC electronic interconnection roadmap covers three basic elements: (1) the design and fabrication of semiconductors and their associated packaging; (2) the fabrication of the interconnecting substrate for both the semiconductor package and the product printed board; and (3) multiple levels of assembly and test. The IPC roadmap encounters challenges in covering increasingly fluid business relationships for the original equipment manufacturers (OEMs) and electronics manufacturing services (EMS’s) who may be anywhere on the planet rather than previously a predominantly simple model of vertically integrated the OEM markets. Teams of experts from many organizations around the world have cooperated to ensure that the IPC roadmap presents the recommendations based on the vision and needs assessments of OEM, ODM, and EMS companies.

The OE-A, a working group within the German engineering federation (VDMA) was organized a few years ago to create a communication and development interface for various fields of research. It represents the entire value chain of organic electronics, from the materials supplier and equipment and product manufacturer through to the user. The OE-A’s goal is to issue roadmaps that serve as a guide to the multitude of technical developments and help to define possible applications. While many of the developments of OE-A members are still in the test phase in the lab, a whole series of practical applications is already in use. The OE-A has published four roadmaps.

2.2 ITRS Roadmap

For five decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products-based miniaturization level. This is usually expressed as Moore’s Law, but is also sometime called scaling. The most significant trend is the decreasing cost-per-function, which has led to substantial improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics. To help guide these R&D programs in scaling, the Semiconductor Industry Association (SIA) met with corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of its roadmap and to begin work toward the first ITRS, published in 1999. Since then, the ITRS has been updated in even years and fully revised in between years. The latest 2012 update is available on the ITRS website. Figure 2-1 shows the ITRS roadmap for printed CMOS Moore’s Law and beyond, which more recently has been called “More than Moore” or its abbreviation, MtM.

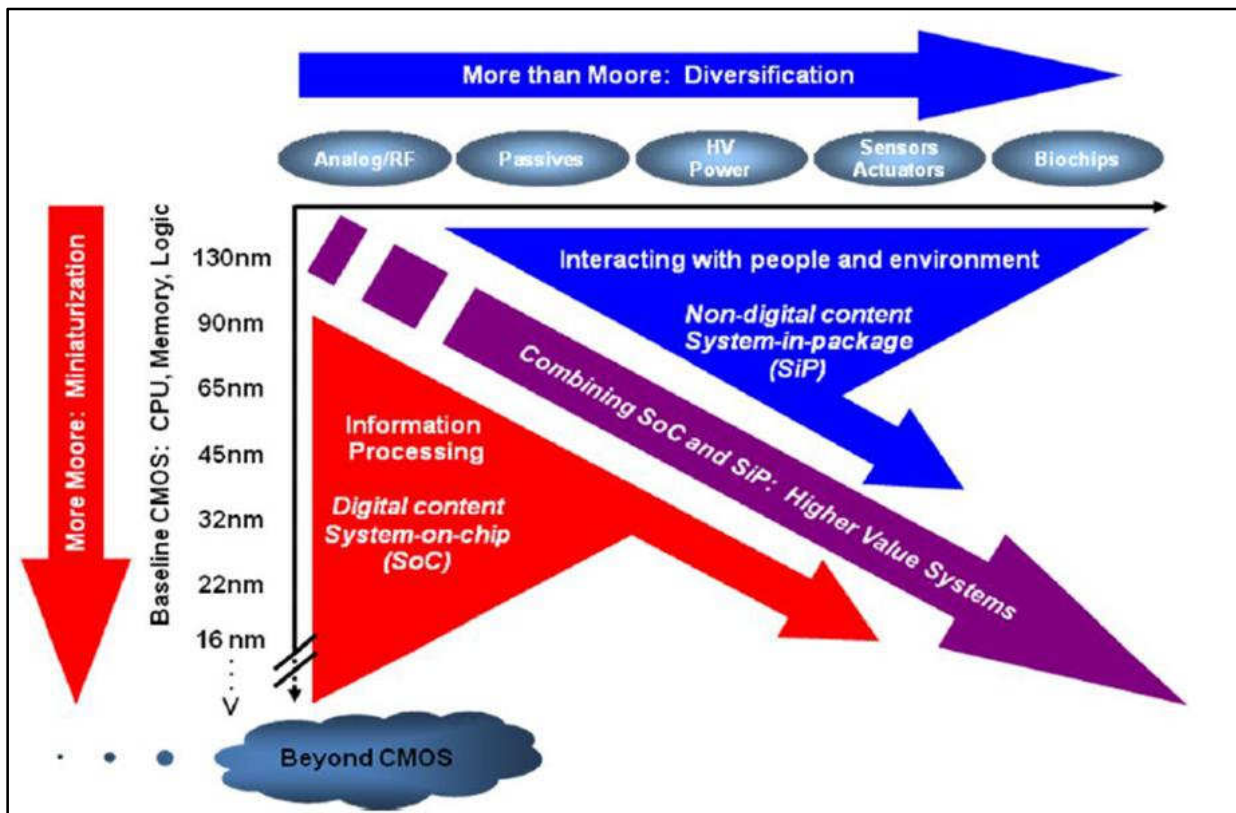


Figure 2-1. Microelectronics packaging roadmap covering single chip, 2.5/3D stack, embedded active/passive, and printed electronics technologies.

The ITRS projects that by 2020–2025, many physical dimensions are expected to be crossing the 10 nm threshold. It is expected that as dimensions approach the 5–7 nm range it will be difficult to operate any transistor structure that is utilizing CMOS physics as its basic principle of operation. It is also expected that new devices, like the very promising tunnel transistors, will allow a smooth transition from traditional CMOS to this new class of devices to reach these new levels of miniaturization. However, it is becoming clear that fundamental geometrical limits will be reached in the above timeframe. By fully utilizing the vertical dimension, it will be possible to stack layers of transistors on top of each other. This 3D approach will continue to increase the number of components per square millimeter even when horizontal physical dimensions will no longer be amenable to any further reduction.

ITRS recognized the limitations of Moore’s law (i.e., linear scaling) and proposed a methodology to identify those MtM technologies for which a roadmapping effort is feasible and desirable. The semiconductor community needs to depart from the traditional scaling “technology push” approach and involve new constituencies in its activities. ITRS materialized this new approach in 2011, when it added a MEMS chapter to the roadmap, and also aligned it with the iNEMI roadmap. The micro-electro-mechanical systems (MEMS) chapter aligns its effort towards those MEMS technologies associated with “mobile internet devices,” a driving application broad enough to incorporate many existing and emerging MEMS technologies.

2.3 iNEMI Roadmap

iNEMI has been creating and exploiting technology roadmaps for the electronics industry for 20 years. It projects trends for future opportunities and challenges for the electronics manufacturing industry. The roadmap is updated every two years, covering technology development and deployment by predicting future packaging, component and infrastructure challenges as well as describing critical technical and business elements required to support industry growth. The projects deliver solutions to identified gaps that allow the industry to continue on its fast paced speed. Figure 2-2 illustrates iNEMI methodology in addressing the gaps by forming technology working groups (TWGs).

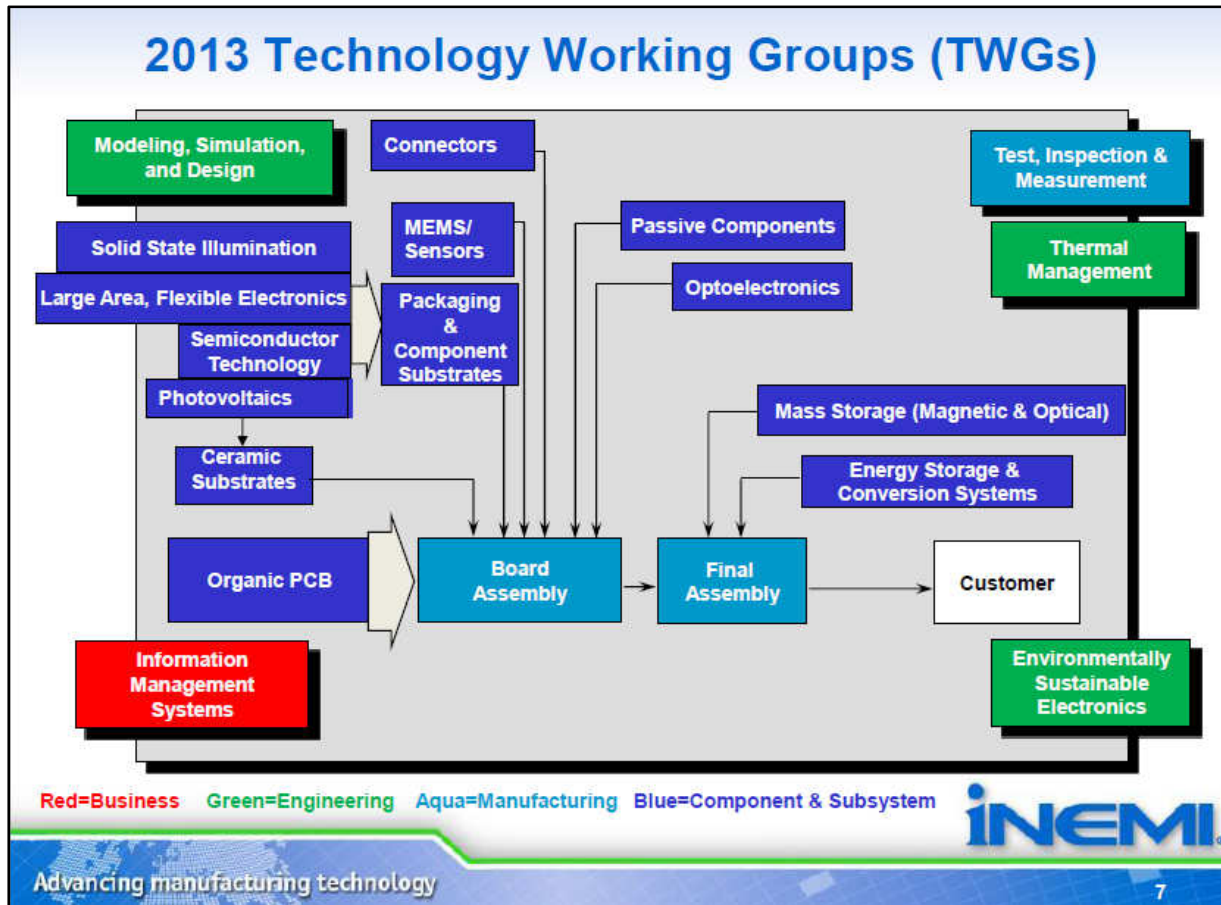
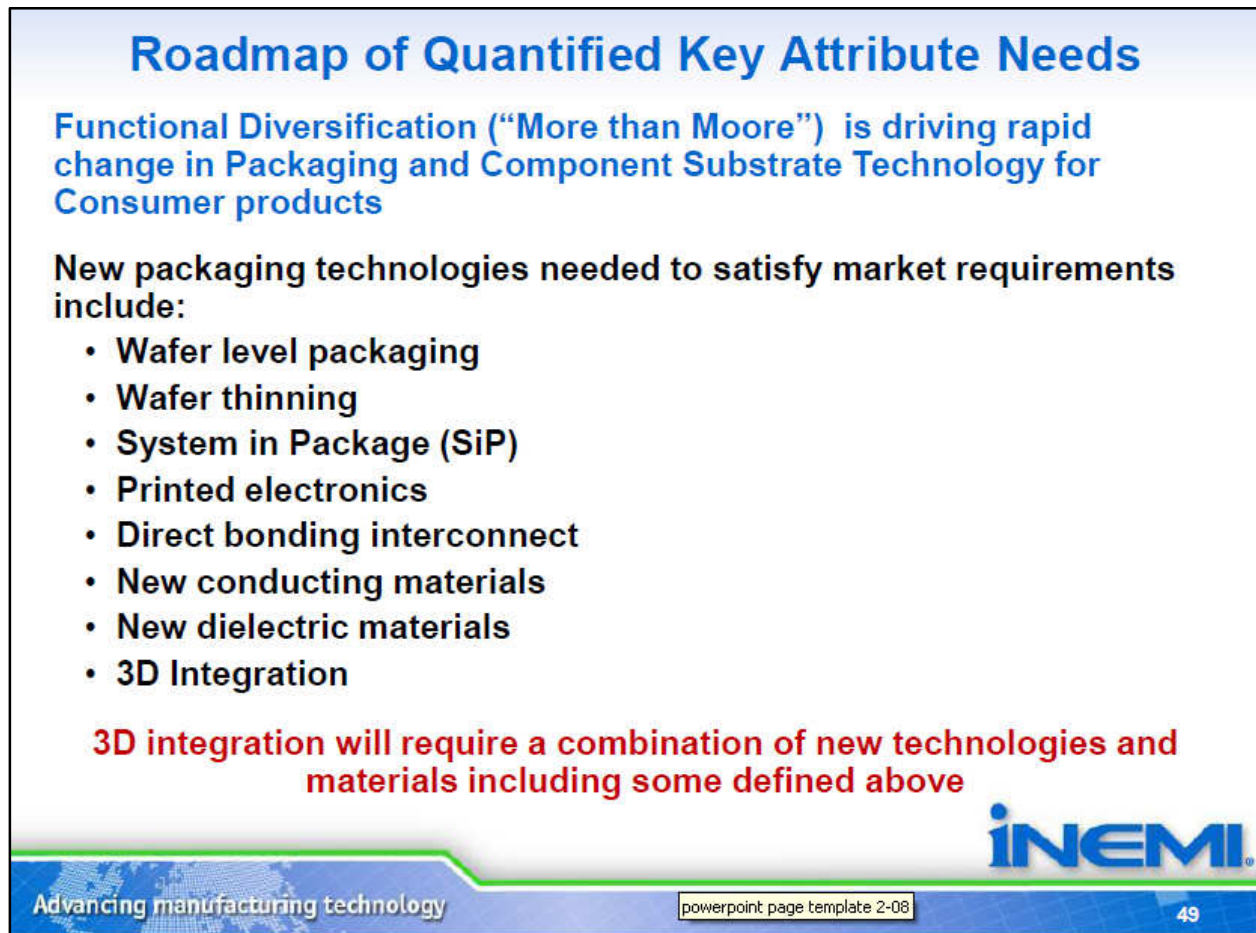


Figure 2-2. iNEMI technology working groups (TWGs) addressing various electronic technologies [2].

The pace of change in packaging technology today has accelerated to the highest rate in history. Communication, transportation, education, agriculture, entertainment, health care, environmental controls (heating and cooling), defense, and research all rely heavily upon electronics today. This diversity of

application and the never ending demand for both lower cost and higher performance cannot be achieved without major changes in architecture, materials and manufacturing processes. These new technologies include SiP, wafer level packaging (WLP), wafer thinning, and through silicon vias (TSVs) today. In the near future, we will see additional changes with the incorporation of nano-materials (See **Figure 2-3**).



Roadmap of Quantified Key Attribute Needs

Functional Diversification (“More than Moore”) is driving rapid change in Packaging and Component Substrate Technology for Consumer products

New packaging technologies needed to satisfy market requirements include:

- **Wafer level packaging**
- **Wafer thinning**
- **System in Package (SiP)**
- **Printed electronics**
- **Direct bonding interconnect**
- **New conducting materials**
- **New dielectric materials**
- **3D Integration**

3D integration will require a combination of new technologies and materials including some defined above

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Figure 2-3. iNEMI technology working groups (TWGs) addressing various electronic technologies [2].

Multi-core processors are now the norm for most computing applications. A consequence of the expected demise of the traditional scaling of semiconductors is the increased need for improved cooling and operating junction temperature reduction due to large leakage currents. The consumer's demand for thin multifunctional products has led to increased pressure on alternative high density packaging technologies. High-density three-dimensional (3D) packaging of complete functional blocks has become the major challenge in the industry.

- RF System-in-Package (SiP) applications have become the technology driver for small components, packaging, assembly processes, and high density substrates.
- The use of motion-gesture sensors in various consumer and portable devices has expanded the MEMS
- Gyroscope enables portrait-landscape mode (both 2D-axis and 3D-axis) is expected to see an exponential growth.
- Performance requirements such as increased bandwidth and lower power are driving 3D integrated circuits (ICs) designed with through silicon vias (TSV).

The need for continuous introduction of complex, multifunctional new products to address the converging markets (first identified in 2004) has continued to favor the development of functional, modular components or SiP (both 2D and 3D structures). This paradigm shift in the design approach increases the flexibility, shortens the product design cycle, and places the test burden on the producers of the modules. Major paradigm shifts identified this year include:

- Cloud-connected digital devices with sensors
- Optical interconnect by 2016
- Revolutionary transition in packaging technology
- How to develop supply-chain infrastructure while minimizing risk
- Next generations of fiber technology to keep up with capacity
- Wafer level packaging has come of age

In addition to the conventional packaging technology trend, iNEMI add printed electronic technology in its forecasting. The 2013 iNEMI’s “Large Area, Flexible Electronics Roadmap” chapter is building upon the 2011 first edition [2]. It added a comprehensive update based on a number of announcements made by industry since the previous publication. In addition, the iNEMI team identified paradigm shifts, enablers, and show stoppers (see **Figure 2-4**). One key paradigm is the transition from the beginning of the 21st Century vision for completely printed electronic products to ‘hybrid’ products, where traditional electronic components are used in combination with printed components.

Other paradigm shifts include cost per area of functionality versus cost per function for silicon chip and integration of electronics in non-traditional objects and locations – ubiquitous electronics. A few gaps and show stoppers are also identified and presented. For example, it states that the rate of commercialization of materials and manufacturing/processing equipment is occurring too slowly to meet the cost/performance/utility demands to enable near-term product launches. Additionally, the rate of development of systems must accelerate—otherwise a window of opportunity may be lost for a disruptor to commercialize a new competitive product.

- **Paradigm Shifts**
 - All PE to “hybrid” products
 - Cost per area rather than cost for function
 - Non-traditional integration- Ubiquitous electronics
 - Scalable and high volume production
 - Novel form factor and low-cost electronics
- **Enablers**
 - Establish best-in-class manufacturing
 - Develop low temp interconnect materials
 - Improve materials/processes
 - Develop high performance/stable organic/inorganic/hybrid
 - Advance design and layout products

Figure 2-4. iNEMI 2013 roadmap identification of paradigm shifts and enablers on printed electronics (PE) [2].

Seven areas of opportunity were identified by an industry survey performed by the iNEMI team. Those surveyed further predicted that the near-term commercialization opportunities will continue to be lighting, power (battery), and sensors (biological, chemical, and touch) followed later by the introduction of radio

frequency (RF) devices (anti-tampering and authentication), photovoltaics, and displays. As with silicon-based component/subsystem technologies, it is envisioned that the technology and applications will mature over time, offering additional opportunities for integration into product emulators. As an example, as these technologies become more robust, it is possible that memory products may be developed for the aerospace and defense industries.

Near-term opportunities are classified as either (1) non-hybrid—an application that is comprised of only the emerging technology or (2) hybrid—an application that is manufactured using traditional electronics and devices, circuits, or components based on the new technology, e.g., a product with a printed display module and a silicon IC RF front-end. For non-hybrid application, one technical barrier concerns the development of in-line manufacturing quality control equipment. To benefit from the economies of scale that roll-to-roll (R2R) and printing offers, systems must be developed and qualified for testing of the fabricated devices, circuits, and components.

Conversely, hybrid flexible electronics systems comprised of printed electronics-based components (sensors, power, indicators, signage) integrated with traditional electronics (surface mount technology for passive devices and silicon based ICs) continue to receive greater attention for near-term commercialization opportunities. In order to achieve further commercialization, a dedicated, hybrid manufacturing platform must be developed. iNEMI envisions that an R2R manufacturing platform combining several printing technologies (e.g., flexography, gravure, and micro dispensing) is required to enable realization of the market potential.

2.4 IPC Roadmap

The IPC has been creating and exploiting technology roadmaps for the electronics industry for the last 20 years; the first roadmap was published in 1993 and updated in 1994. Even though these documents did not follow the traditional roadmap format, but were more or less a compendium of needs of the industry looking ahead 4 years. The 1995 IPC roadmap was designed using classic timeline models with eight emulator OEM products. The 2000–2001 roadmap included 11 emulator products. The emulators were reconfigured to include information on four different topics: design issues, board fabrication issues, assembly issues, and purchasing trends. For the first time components and component substrate technology was incorporated. The 2013 roadmap becomes a departure by selecting emulators from the end-use application matrix, even though it attempted to match the definition by the OEM in the iNEMI roadmap.

The 2013 IPC *International Technology Roadmap for Electronic Interconnections* roadmap [3] is a resource for companies throughout the global electronics manufacturing industry who are embarking on business, technology, and strategic planning for the near and long term. The recent IPC roadmap concentrates on the “operational” segment of the electronic interconnect market, only reporting the very broad (overall major corporate strategic plan, i.e. iNEMI and Prismark) and very narrow (Japanese consumer electronics needs, i.e. JISSO) as much as needed for their constituents planning purposes.

IPC always recommends that users consider the input from other roadmaps where it may pertain to their specific situation. New features of the IPC roadmap include a “stewardship” section that provides expanded content and scope, with an emphasis on true sustainability; explanation of new business models an expanded coverage of the printed electronics industry as it matures into a viable technology. The IPC roadmap consists of five sections:

- Part A – provides information on how to use the roadmap;
- Part B – covers technology trends;
- Part C – addresses design considerations;
- Part D – tackles interconnections and substrates; and
- Part E covers assembly technology.

The challenge for many is the different focus of much of the roadmapping efforts—ITRS, iNEMI, and IPC. The ITRS is an emerging technology roadmap; it looks at a “technology push” covering the progress of

technology and question as what products can be developed. This roadmap lacks the broader product context provided by the product technology roadmap. The product-technology roadmap is driven by product/process needs. This is the most common type of roadmap. A product-technology roadmap can be linked to “technology push” or “market pull.” IPC and iNEMI are “market pull” roadmaps, which define desired products and asks what technologies are needed to support them.

2.5 OE-A Roadmap

The OE-A, a working group within VDMA, was organized a few years ago to create a communication and development interface for various fields of research. It represents the entire value chain of organic electronics, from the materials supplier and equipment and product manufacturer through to the user. The OE-A's goal is to issue roadmaps that serve as guides to the multitude of technical developments and help to define possible applications. While many of the developments of OE-A members are still in the test phase in the lab, a whole series of practical applications are already in use. The OE-A has published four roadmaps. An adapted summary version of the 4th map, which projects near-term to long-term growth and applications, is schematically shown in Figure 2-5. Here, the technology related to lighting and display are bundle together rather shown separately.

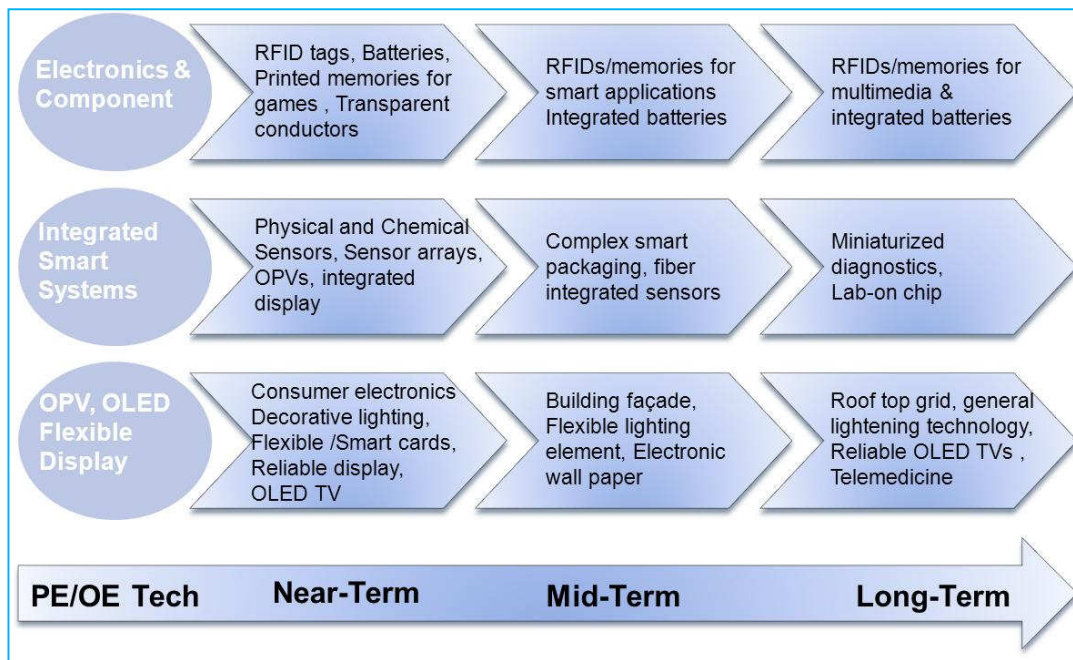


Figure 2-5. iNEMI 2013 roadmap identification of paradigm shifts and enablers [2].

The three key areas defined are:

1. Electronics and components covering radio frequency identification, batteries, printed memory for games, and transparent conductors
2. Integrated smart systems including physical and chemical sensors, sensor arrays, and integrated displays
3. Organic photovoltaic (OPV), organic light emitting diode (OLED), and flexible displays, which encompass a large number of applications in consumer electronics, lighting, and flexible/smart cards.

3.0 SINGLE-CHIP PACKAGES

3.1 Introduction

Figure 3-1 categorizes single-chip microelectronic packaging technologies into three key technologies: (1) plastic ball grid arrays (PBGAs), (2) ceramic column grid arrays (CGAs), and (3) and smaller foot print wafer level packages. There are numerous variation of packages in each category that will be discussed in the following section.

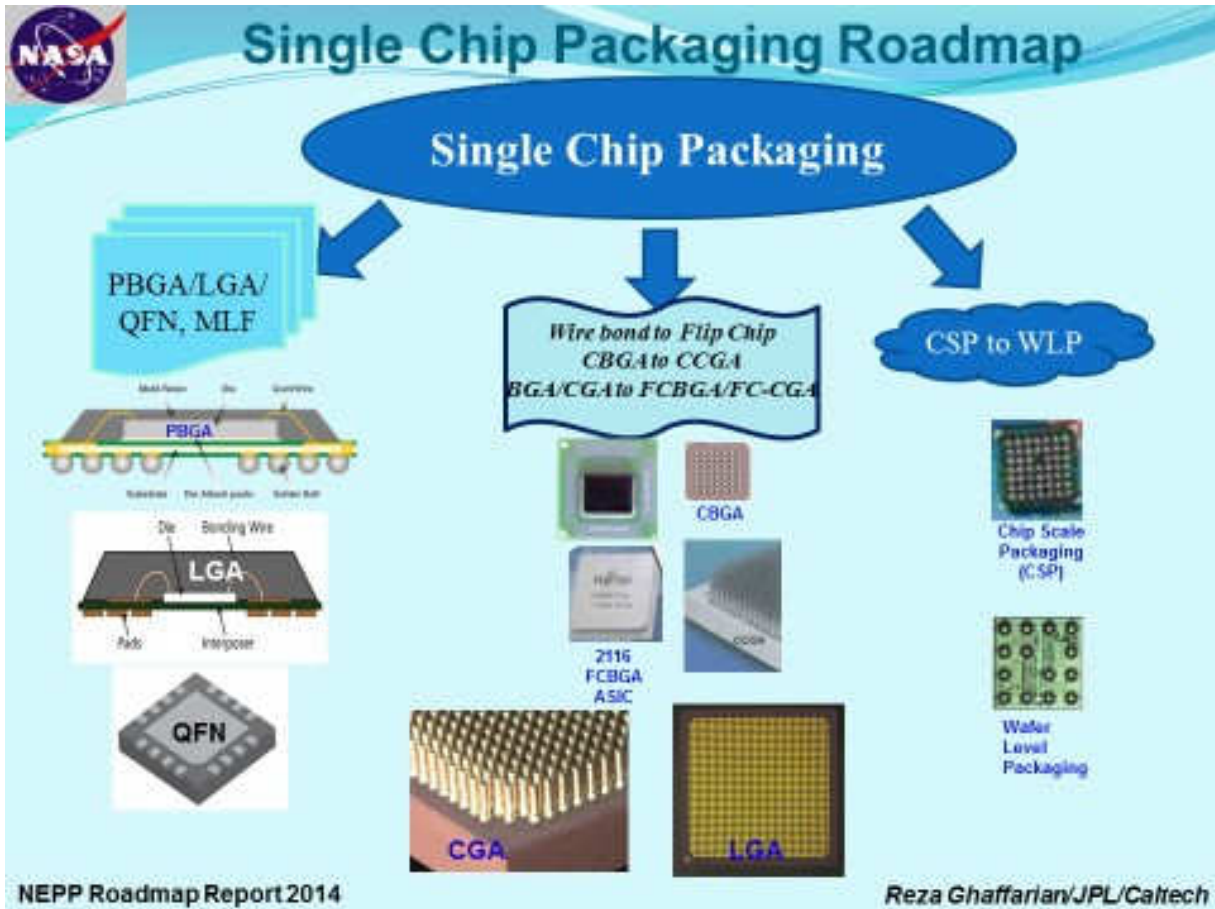


Figure 3-1. iNEMI 2013 roadmap identification of paradigm shifts and enablers [2].

PBGAs and chip scale packages (CSPs) are now widely used for many commercial electronic applications, including portable and telecommunication products. BGAs with 0.8-1.27-mm pitches are implemented for high reliability applications, generally demanding more stringent thermal and mechanical cycling requirements. The plastic BGAs introduced in the late 1980s and implemented with great caution in the early 1990s, further evolved in the mid-1990s to the CSP (also known as a fine-pitch BGA) having a much finer pitch from 0.4 mm down to 0.3 mm.

To accommodate higher I/O single-chip die, the flip-chip BGA (FCBGA) was developed. The FCBGA is similar to the PBGA, except that internally a flip-chip die rather than a wire-bonded die is used. Because of these developments, it has become even more difficult to distinguish different area array packages by size and pitch; its internal die attachment configuration also to be considered. The ultimate size reduction can be achieved by protecting single die at the wafer level, hence introduction of wafer level package (WLP). WLPs also addresses the key issues of using single bare die, and it improves ease of handling and functional testing.

For high reliability applications, ceramic and hermetic packages of area array packages were implemented. The ceramic BGA (CBGA) package uses a higher melting ball (Pb90Sn10) with eutectic attachment to the die and board. Contrary to the PBGA version, the high-melt ball does not collapse during solder interconnection reflow, hence, a control standoff height for improved reliability. The column grid array (CGA) or ceramic column grid array (CCGA) is similar to a CBGA except that it uses column interconnects instead of balls; hence it has higher flexibility for improved reliability. The lead-free CGA uses copper instead of high melting lead/tin the column. The flip-chip BGA (FCBGA) is similar to the BGA, except that internally a flip-chip die rather than a wire-bonded die is used.

Extensive work has been carried out to understand technology implementation of area array packages for high reliability applications. The work [5–12] included process optimization, assembly reliability characterization, and the use of inspection tools (including x-ray and optical microscopy) for quality control and damage detection due to environmental exposures. The following sections summarize these packaging technologies.

A new category of packages—leadless—is emerging. It has no ball or columns for interconnection, only solder. The leadless packages are generally near die size. This is similar to array CSPs, which have hidden terminations pads but are also different. They do not have solder ball spheres but rather metallized terminations or pads and a large heat-dissipation pad under the package. Leadless packages are also known as bottom-termination components (BTCs) and numerous other nomenclatures. The terms include quad flat no-lead (QFN) [13], dual-row/multi-row QFN (DRQFN/MRQFN), dual flat no-lead (DFN) [14], and land grid array (LGA) packages [15].

In addition, new terms were added for the more recently introduced improved versions. These include the advanced QFN (aQFN) [16] and array QFN [17] packages, which generally have multiple row terminals accommodating a higher number of inputs/outputs (I/Os). The number of aQFN I/Os is approaching that of CSP/FBGA packages with the advantage of lower cost for portable and telecommunication applications. The report also presents a literature survey some aspects of leadless packaging technologies

3.2 Ball Grid Array (BGA)

Ball grid arrays (see Figure 3-2), with 1.27-mm pitch (distance between adjacent ball centers) and finer pitch versions with 1- and 0.8-mm pitches, are the only choice for packages with higher than 300 I/O counts, replacing leaded packages such as the quad flat pack (QFP). BGAs provide improved electrical and thermal performance, more effective manufacturing, and ease-of-handling compared to conventional surface mount (SMT) leaded parts. Finer pitch area array packages (FPBGA), also known as CSPs, are further miniaturized versions of BGAs, or smaller configurations of leaded and leadless packages with pitches generally less than 0.8 mm.

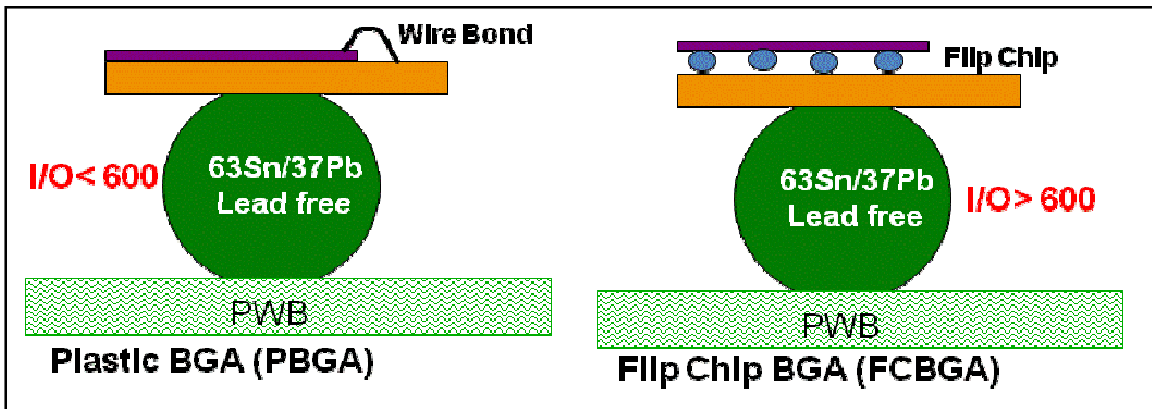


Figure 3-2. Typical plastic ball grid array with internal wire-bond and flip-chip die for low and high-I/O package configurations, respectively.

3.3 Column Grid Array (CGA)

For high reliability applications, surface mount leaded packages, such as ceramic quad flat packs (CQFPs), are now being replaced with CGAs with a 1.27-mm pitch (distance between adjacent ball centers) or less. Replacement is especially appropriate for packages with greater than 300 I/O counts where CQFP pitches become fine, making them extremely difficult to handle and assemble. In addition to size reduction, CGAs also provide improved electrical and thermal performance; however, their solder columns are prone to damage, and it is almost impossible to rework defective solder joints. Rework, re-column, and reassembly may be required to address solder defects due to processing or column damage prior to assembly due to shipping and mishandling.

CGA packages are preferred to CBGA (see Figure 3-3) since they show better thermal solder joint reliability than their CBGA counterparts. Superior reliability is achieved for larger packages and for greater than 300 I/Os when resistance to thermal cycling is further reduced with increasing package size. All ceramic packages with more than about 1,000 I/Os come in the CCGA style with 1-mm pitch or lower in order to limit growth of the package size.

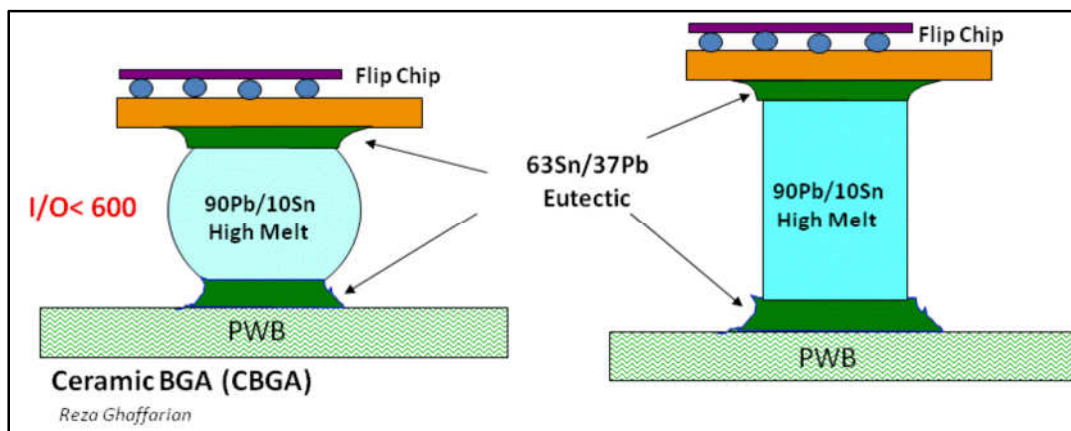


Figure 3-3. Typical plastic ball grid array with internal wire-bond and flip-chip die for low and high-I/O package configurations, respectively.

Key recent trends in electronic packages for high reliability applications are as follows:

- Ceramic quad flat pack (CQFP) to area array packages
- CBGA to CCGA/CGA (>500 I/Os) and land grid array (LGA)
- Wire-bond to flip-chip die within a package
- Hermetic to non-hermetic packages (>1000 I/Os)
- High-lead solder columns to columns with Cu wrap
- Pb-Sn to Pb-free, including potential use of a Cu column
- Land grid with conductive interconnects rather than Pb-free solder

3.4 Class Y- Non-hermetic Flip-chip CGA (FC-CGA)

Significant activities were carried out (see Figure 3-4) within the last few years to address the nonhermetic flip chip CGA for use in high reliability applications [18]. The specification was updated to ensure that new requirements be added to cover all aspects of the packaging configuration including flip-chips, underfills, adhesives, and column attaches as well as introduction of the new test methods.

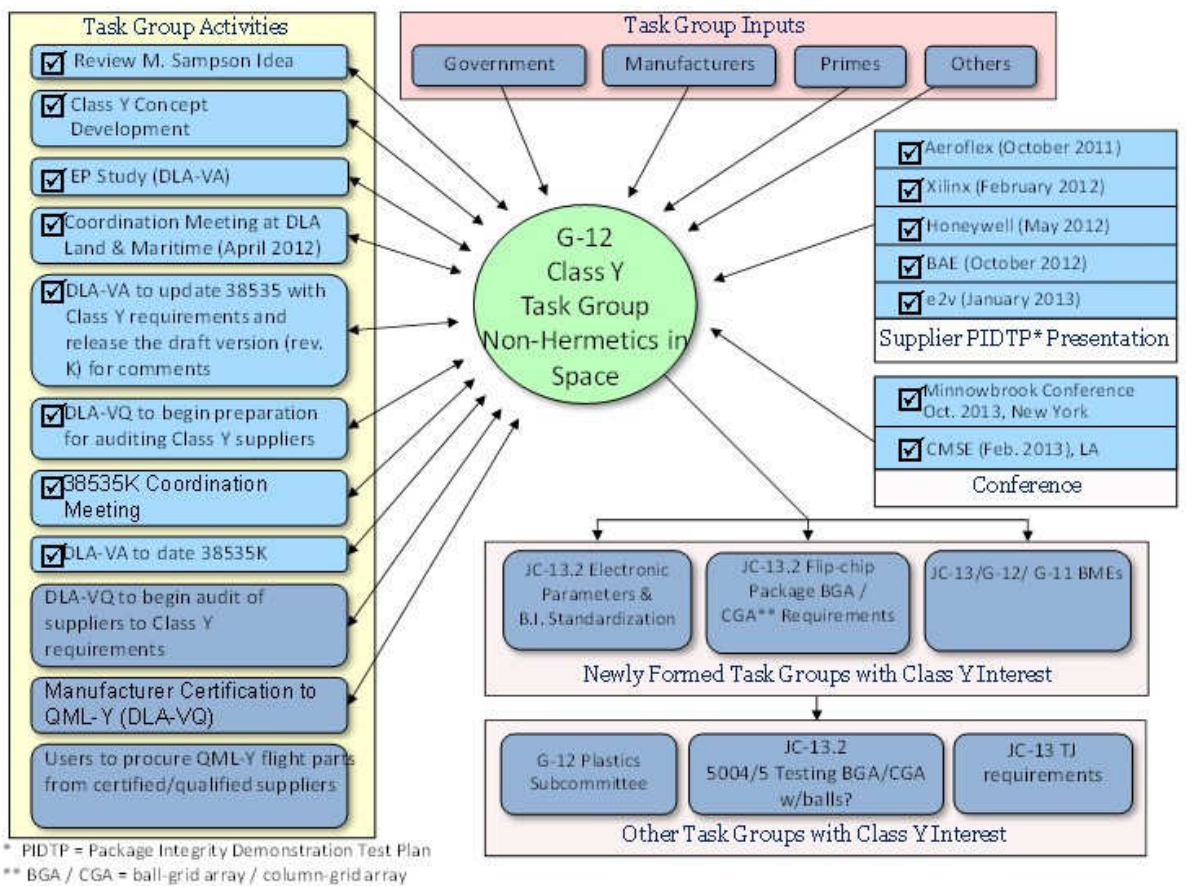


Figure 3-4. Infusion of New Technology into the QML System G12 Class Y Effort at a Glance.

3.5 Flip Chip in package (FCIP)

Flip-chip assembly is fast becoming the assembly method of choice over wirebond to connect a chip to a substrate (or package). The flip chip in package technology has been widely used in high performance FCIP applications for more than a decade. Elements of its success can be attributed to the establishment of high yield assembly processes and formulation of advanced underfill materials systems for high reliability. It is widely known that underfills help to mitigate the effects of large coefficient of thermal expansion (CTE) mismatches between silicon chips and organic substrates. To meet the demand for high I/O counts in high performance and high-bandwidth applications, flip-chip I/O pitch needs to be reduced continuously.

Reduction of I/O bump dimension also raises significant challenges to package substrate technologies. Compared to other types of substrates, a silicon package has the advantages of excellent planarity, fine-pitch wiring, and matched CTE for Si chips. The key elements of an Si carrier include ultra-fine pitch interconnection capability, known-good die testability, as well as reworkability. Micro C4s can be fabricated through various methods, such as micro screen printing, Molten Solder Ejection Method (MSEM), or photolithographic electroplating. Figure 3-5 shows a photomicrographs of a reflowed micro C4s.

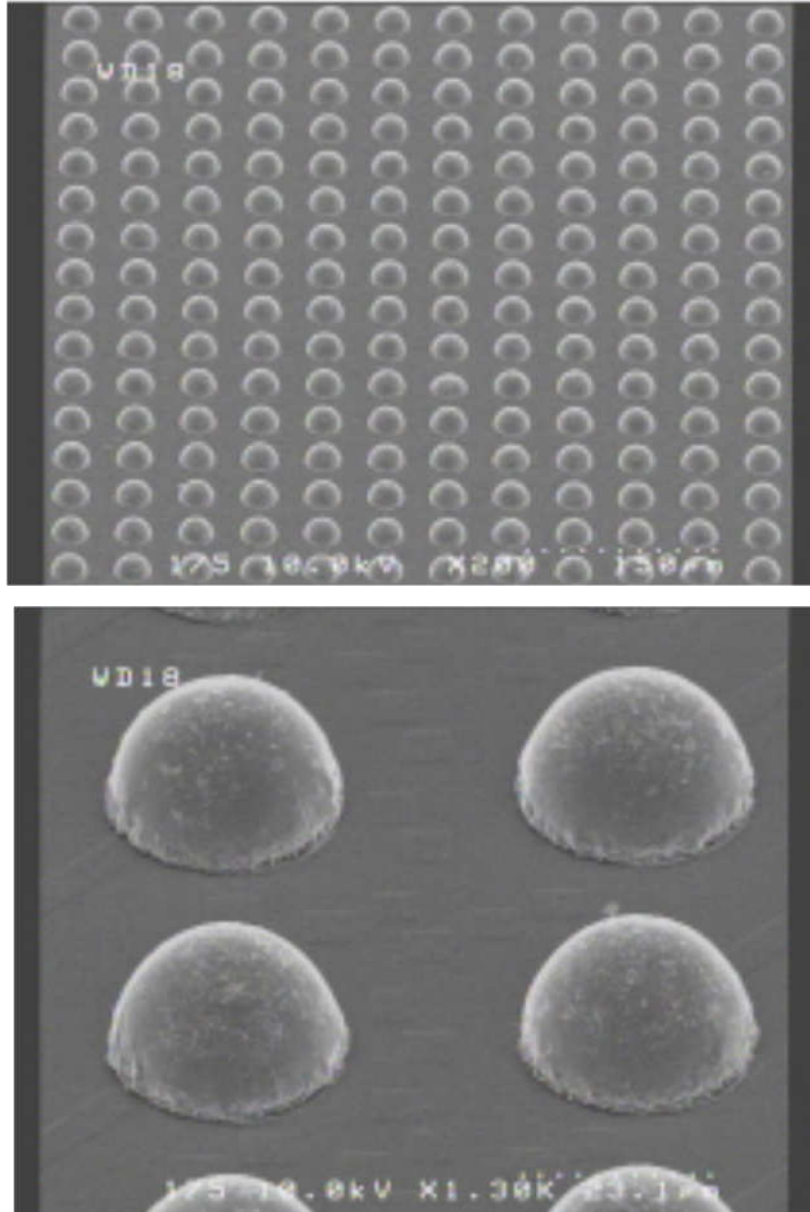


Figure 3-5. SEM photomicrographs of the as-reflowed Pb-free micro C4s in area array. The average height of the micro C4s is around $\sim 15 \mu\text{m}$ with diameter of $\sim 25 \mu\text{m}$.

3.6 Chip Scale Package (CSP)

The trend in microelectronics has been toward ever increasing numbers of I/Os on packages, which is, in turn, driving the packaging configuration of semiconductors. Key advantages and disadvantages of CSPs compared to bare die are listed in Table 3-1. Chip scale packaging can combine the strengths of various packaging technologies, such as the size and performance advantage of bare die assembly and the reliability of encapsulated devices.

The advantages offered by chip scale packages include smaller size (reduced footprint and thickness), lesser weight, a relatively easier assembly process, lower overall production costs, and improvement in electrical performance. CSPs are also tolerant of die size changes, since a reduced die size can still be accommodated by the interposer design without changing the CSP's footprint.

CSPs have already made a wide appearance in commercial industry as a result of these advantages, and now, even their three-dimensional (3D) packages are being widely implemented. Unlike conventional BGA technology at typically 0.8–1.27 mm pitch, CSPs utilize lower pitches (e.g., currently, 0.8 to 0.3 mm) and hence, will have smaller sizes and their own challenges.

Table 3-1. Pros and cons of chip scale package (CSP).

Pros	Cons
Near chip size	Moisture sensitivity
Widely used	Thermal management <ul style="list-style-type: none"> Limits package to low I/Os
Testability for known good die (KGD)	Electrical performance
Ease of package handling	Routability <ul style="list-style-type: none"> Microvia needed for high I/Os Pitch limited to use standard PWB
Robust assembly process <ul style="list-style-type: none"> Only for an area-array version 	Reliability is poor in most cases
Accommodates die shrinking or expanding	Underfill required in most cases to improve reliability.
Standards	Array version <ul style="list-style-type: none"> Inspectability Reworkability of individual balls
Infrastructure	
Rework/package as whole	

3.7 Flip Chip on board [FCOB]

Flip-chip assembly is fast becoming the assembly method of choice over wirebond to connect a chip.

Direct attachment of flip chips on board (FCOBs) with fine-pitch solder bumps are being increasingly used to address performance, power, size, and I/O requirements. FCOBs require underfills to ensure solder bump reliability. However, added processing costs associated with underfill dispensing and curing, add challenges especially for fine-pitch assemblies as well as reliability concerns due to underfill delamination make FCOBs a less likely option for future generations of microelectronic packaging. Furthermore, when low-K dielectric material (ultra low-K dielectric in the future) is used in the IC and when such ICs are assembled on organic substrates, the stiff solder bumps could crack or delaminate the low-K dielectric material under thermal excursions.

3.8 Wafer Level Packages (WLP) or Wafer Level Chip Scale Package (WLCSP)

Microelectronic packaging continues the migration from wire bond to flip chip first level interconnect (FLI) to meet aggressive requirements for improved electrical performance, reduced size and weight. For wafer bumping, solder electroplating is commonly employed, especially for fine pitch applications. Wafer level chip scale packaging (WLCSP) typically utilizes solder sphere placement technology to manufacture the bumps. In WLCSP, pitch and solder ball size are usually much higher and the number of I/O much lower than for Flip Chip in Package (FCiP) applications. However, many companies plan to use WLPs for higher pin count applications, including analog parts with larger die sizes. This will increase the number of wafers to be processed, as well as the unit volumes. The memory die is one example of a large die whose adoption significantly increases the number of wafers.

One of the major drivers for the adoption of WLPs in portable products is form factor, and mobile phones increasingly contain WLPs, representing the largest single product application. Demands for greater

functionality in smaller spaces is driving the adoption of WLPs in mobile phones faster than in any other segment of the market.

3.9 Land-Grid-Array (LGA) Packaging Trend

Land-grid array (LGA) packages have been increasingly used in portable electronics and wireless products because of its low profile on the printed wiring/circuit boards (PWB/PCB) and direct Pb-free assembly process compatibility. Since LGA has lower standoff height and different material properties compared with the conventional BGA package; its reliability behavior become of concern. A major concern is the board-level solder-joint reliability of the LGA packages under thermal loading. For high-reliability applications, this approach may become a popular approach with a much wider commercial industry implementation of restriction of hazardous substances (ROHS).

LGA in plastic package version with low I/O and sizes has been available for thinner consumer products because of lower cost and lower assembly standoff compared to ball-grid-array versions. In some cases, the LGAs are optimized for improved radio-frequency (RF) performance for wireless applications.

3.10 Conventional Leadless Packaging Trends

In a 2003 paper [13], the authors state that within the last few years, the QFN package has taken industry by storm and that the industry had already shipped one billion parts. Figure 3-6 shows a number of early generation of leadless packaging configurations including the MicroLeadFrame® package (MLF®), which were introduced more than a decade ago.

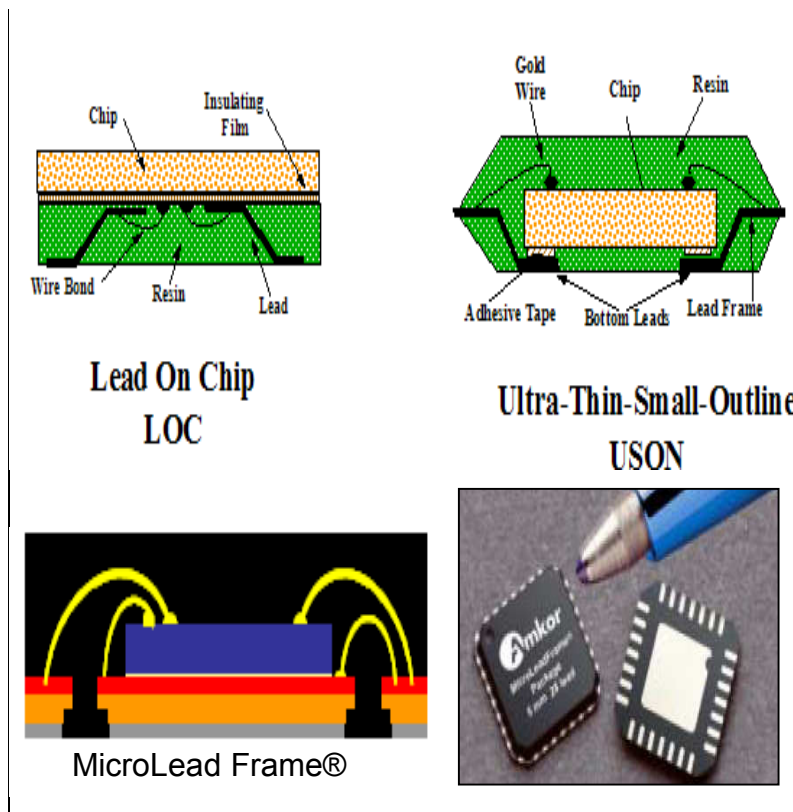


Figure 3-6. Infusion of New Technology into the QML System G12 Class Y Effort at a Glance.

3.11 Advanced Leadless Packaging Trends

IPC, the Association Connecting Electronics Industries [3] recently released the IPC 7093 specification, “Guidelines for Design and Assembly Process Implementation for Bottom Termination Components,” covering the rapidly growing leadless packaging categories. The BTC is a generic term for packaging technologies which their external connections consist of metallized terminals that are an integral part of the package body and intended for surface mounting. This class of components includes quad flat no-lead (QFN), dual-row/multi-row QFN (DRQFN/MRQFN), dual flat no lead (DFN), and land grid array (LGA). The standard describes the critical design, assembly, inspection, and reliability issues associated with BTCs.

Figure 3-7 shows an example of advanced QFN (aQFN) package [16]. The aQFN is an improved version of conventional QFN with multiple row terminals accommodating higher number of I/Os. The number of I/Os become similar to that of CSP/FBGA packages with the advantage of lower cost for portable and telecommunication applications. The multiple-row QFNs; however, are more difficult to assemble, there are more opportunities for solder-joint bridging especially when pitch is smaller, and there are higher potential for risk due to thermo-mechanical environmental exposures. The thermo-mechanical solder-joint reliability of aQFN was improved by modifying packaging processes including double-sided etching of copper lead frame to create isolated copper posts with higher standoff.

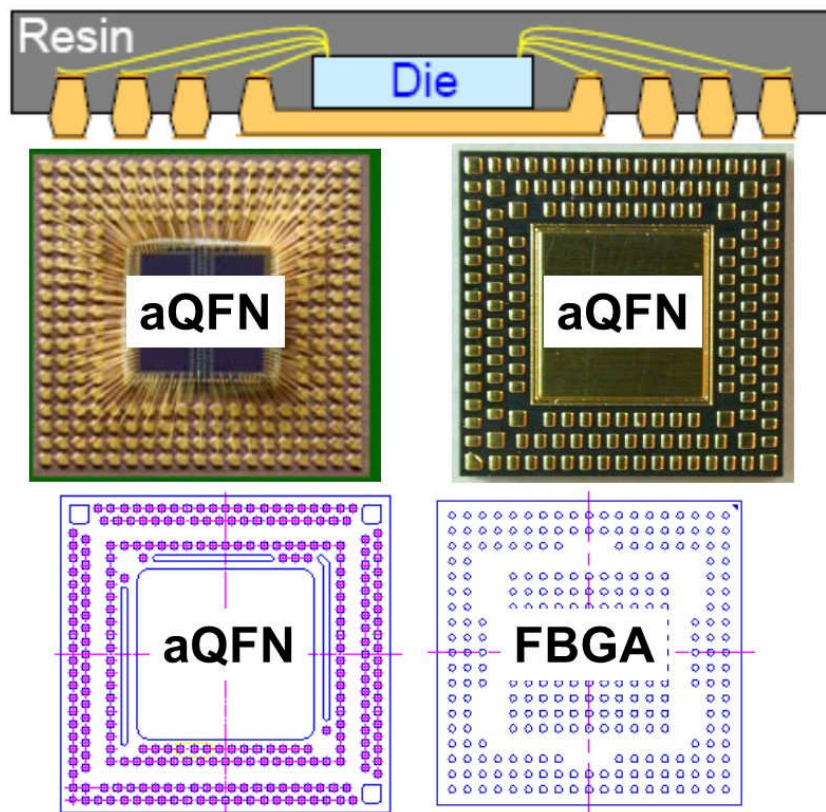


Figure 3-7. The advanced QFN (aQFN) package configuration and re-design of FBGA to aQFN for thermal and electrical characterization [16].

4.0 STACK PACKAGING TECHNOLOGIES

4.1 Introduction

The demand for high-frequency operation, high-input/output (I/O) density, and low parasitics, as well as the need for package-level integration with small form factors and extreme miniaturization, have led to numerous 2.5D and 3D packaging technologies [see Figure 4-1]. The vertically integrated 3D packages combine conventional flip-chip and wire-bond interconnection, build-up, and laminate substrates, and bring about package-level integration of disparate die and device functions through die or package stacking.

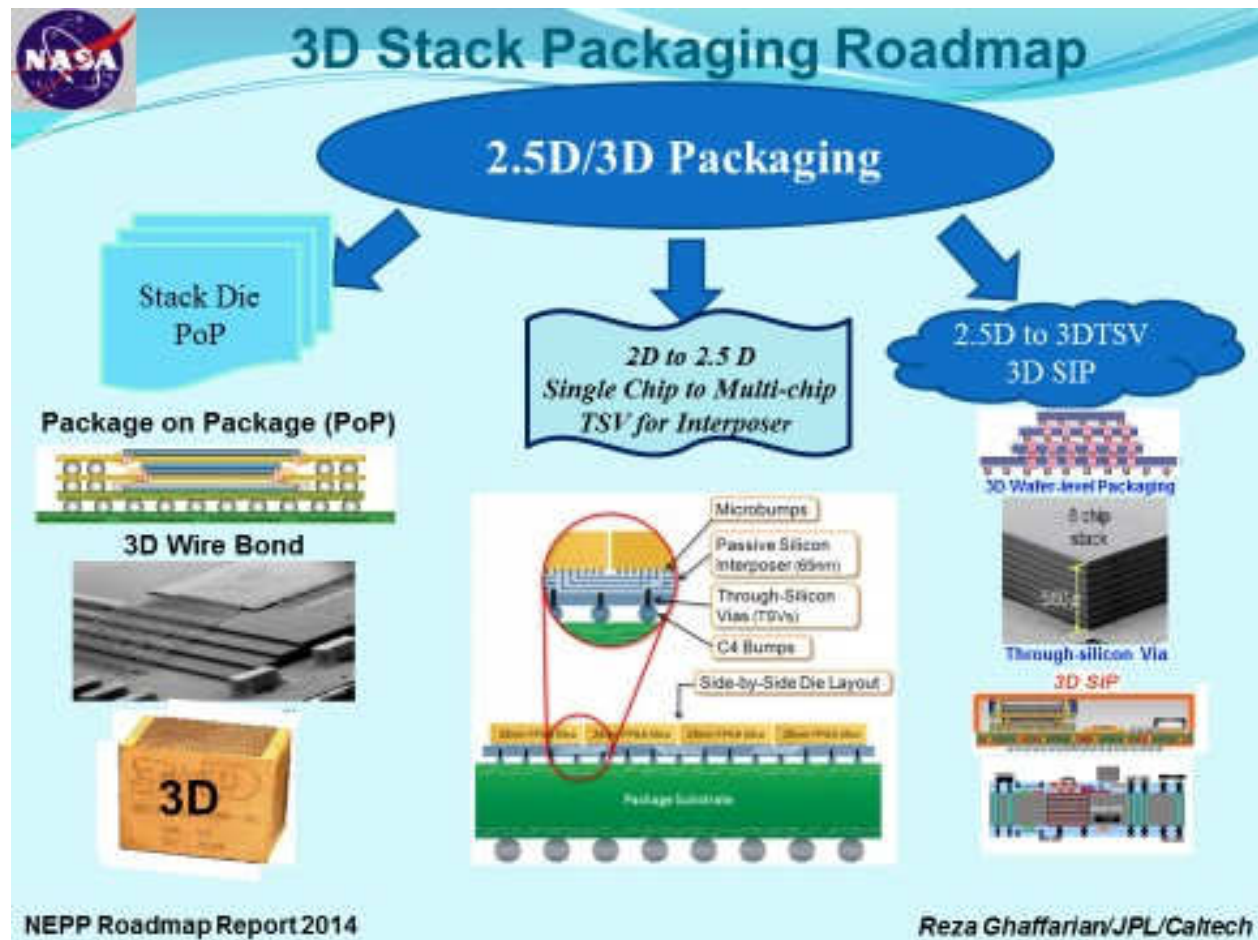


Figure 4-1. 2.5/3D packaging technologies showing conventional to advanced configurations.

From the existing 3D packaging technology options, wire-bonding is well developed for use in low-density connections of less than 200 I/Os per chip. This technology has limitations in meeting the increasing frequency requirements and increasing demands for higher interconnection due to limitation of peripheral wire-bonding. In order to overcome such wiring connectivity issues, multiple flip-chip die with passive redistribution interposed have been introduced by industry for high-end applications. Ultimately the 3D chip stacking technology using through-silicon vias (TSVs) is being pursued by industry since it offers the possibility of solving serious interconnection problems while offering integrated functions for higher performance.

4.2 3D Conventional Packaging Trends

For high-density packaging, the migration to conventional interconnection 3D, more than “Moore”, has become mainstream. Even though initially conventional 3D packaging included leaded stack configuration, the trend is more towards area array interconnections. The conventional 3D packaging (see Figure 4-2) consists of stacking of packaged-devices, known as package-on-package (PoP), and stacking of die within a package, known as package-in-package (PiP) or system-in-package (SiP). Numerous variation of PoP and PiP technologies are in use today including staking of packages by using through mold via (TMV™) interconnection technology. The following sections provide further discussions on specific conventional 3D packaging technology.



Figure 4-2. 2.5/3D packaging technologies showing conventional to advanced configurations.

4.2.1 Package-on-Package (PoP)

PoP is a packaging technology placing one package on top of another to integrate different functionalities while still remaining compact in size. This packaging technology offers procurement flexibility, lower cost of ownership, better total system costs, and faster time to market. Normally, designers use the top package for memory application and the bottom package for application-specific integrated circuits (ASICs), baseband, or processor applications. By using this technology, the memory known-good-die (KGD) issue can be mitigated since the memory to be integrated with the bottom package can be burned-in and tested before integration. PoP also answers issues with wafer thinning, die attach, wire bond, and thermal

dissipation. Three categories of the stack technologies are: (1) PoP with center mold and flip chip, (2) PoP with partial cavity structure, and (3) through-mold via (TMV™).

The TMV™ uses a matrix-molded platform for bottom PoP construction and creates through-via interconnections to the top surface via a laser ablation process [19] (Amkor TMV]. Figure 4-3 illustrates the key elements of the bottom TMV™ PoP developed by the package supplier for their internal qualification and joint SMT studies. The 14 × 14 mm daisy chain package incorporates a 200 I/O, 0.5 mm pitch top side interface, and 620 bottom BGAs at 0.4-mm pitch.

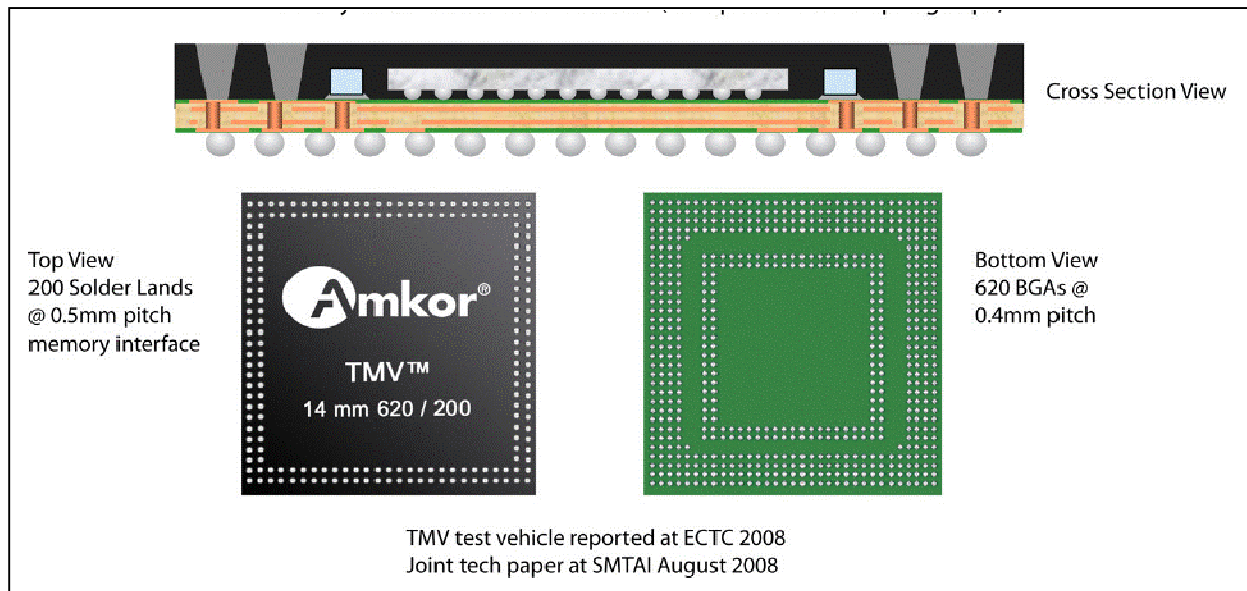


Figure 4-3. Cross-section top and bottom view of a new TMV™ PoP package [19].

The benefits of TMV™ technology include the following:

- Removes the pitch vs. package clearance bottlenecks to support future memory interface density requirements enabling the memory interface to scale with CSP pitch reduction.
- Improves warpage control and bottom package thickness reduction requirements by utilizing a balanced fully molded structure.
- Provides an increased die-to-package size ratio.
- Supports wire bond, flip chip, stacked die, and passive integration requirements.
- Leverages strong technology roadmaps and high-volume scale, from fine-pitch ball grid array (FBGA), stacked die, flip-chip CSP, and SiP platforms.
- Integrates proven laser ablation technology available from a host of laser process equipment suppliers.
- Expected to improve board-level reliability of the stacked memory interface using rules developed by package supplier.

4.2.2 Package-in-Package (PiP)

Handsets and other mobile handheld products are defining a new application for packaging technology that goes beyond the realm of traditional packaging. The optimum solution often lies in a judicious combination or hybridization of these seemingly dissimilar technologies and approaches. One such package is often called PiP. PiP with wire-bonded stack die is well established. Vertical chip stacking can be performed as chip-to-chip, chip-to-wafer, or wafer-to-wafer processes. Stacked die products inside a package results in the thinnest package with the highest board-level reliability and lowest assembly cost. Most of the time,

stacked die are multiple memory chips and rarely mixed device types, such as stacked memory with logic devices added. Special low-profile wire bonding has been developed and is a critical process for this technology.

Stacked die concepts utilizing silicon spacers or epoxy filled with spherical spacers have been used. In the silicon-spacer concept, a thin piece of silicon is used to separate the active dies in the stack. In the glue-spacer concept, this is accomplished with a spherical-filled die-attach. Adding silicon into the package increases the bending resistance. Associated with this is the increased risk and/or propensity for cracks during assembly and/or reliability / qualification testing, either in the package body (molding compound) or in the die itself.

Flip-chip bonding is also used in PiP interconnection, either on its own or as a complement to wire bonding as shown in Figure 4-4. Flip-chip configuration may be applied to either the upper die or the lower ones, depending on the intent of the design. Flip chipping a bottom die directly onto the substrate enables that die to operate at a high speed. On the other hand, flip chipping a top die eliminates the use of long wires for connection to the substrate.

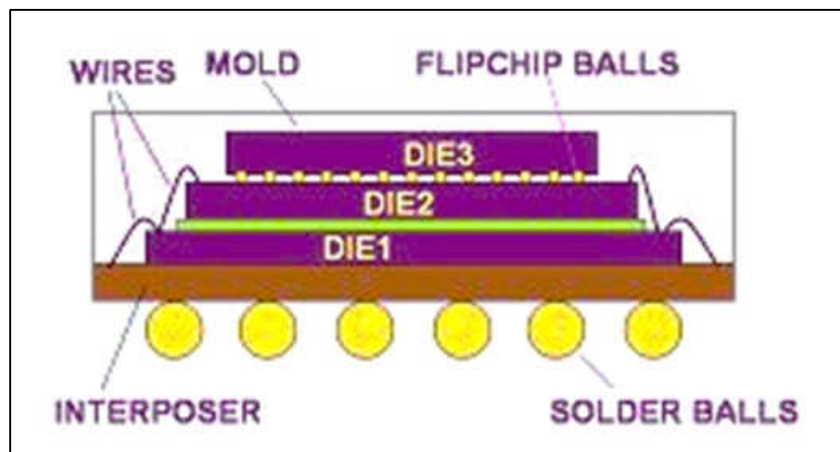


Figure 4-4. Example of a three-die PiP configuration employing both wire bonding and flip-chip bonding.

4.3 2.5D/3D TSV Packaging Trends

Conventional 3D packaging and processes have limitation in meeting system performance, throughput and power requirements. Although PiP and PoP packaging technologies allow for two or more chips and packages to be interconnected, they do not offer enough density, bandwidth or power to meet the requirements of next generation product roadmaps. The trade-offs between placing more functions on a chip (system-on-chip, SoC) versus placing more functions within a package (multi-chip package, MCP, or system-in-package, SiP) must be fully evaluated. Optimizing overall performance as well as total cost-of ownership are equally important. And perhaps one of the most significant issues is accelerating time-to-market, as it is a strategic enabler to the end users.

Figure 4-5 compares the performance advantages of 2.5D/3D ICs to standard packages on a PCB; their relative interconnect density, thermal resistance, and power usage. A 2.5D IC package is an effective cost- and functional-effective interim solution instead of full 3D through silicon via (TSV) 3D packaging. The 2.5D packaging is defined by the use of a multilayer passive silicon interposer—contrary to active interposer in 3D TSV—as a substrate to interconnect multiple active die or die stacks in a side-by-side configuration. In a 3D IC TSV stack, solder bumps are used to join one die on top of another die (active) to allow the signals to travel between the die.

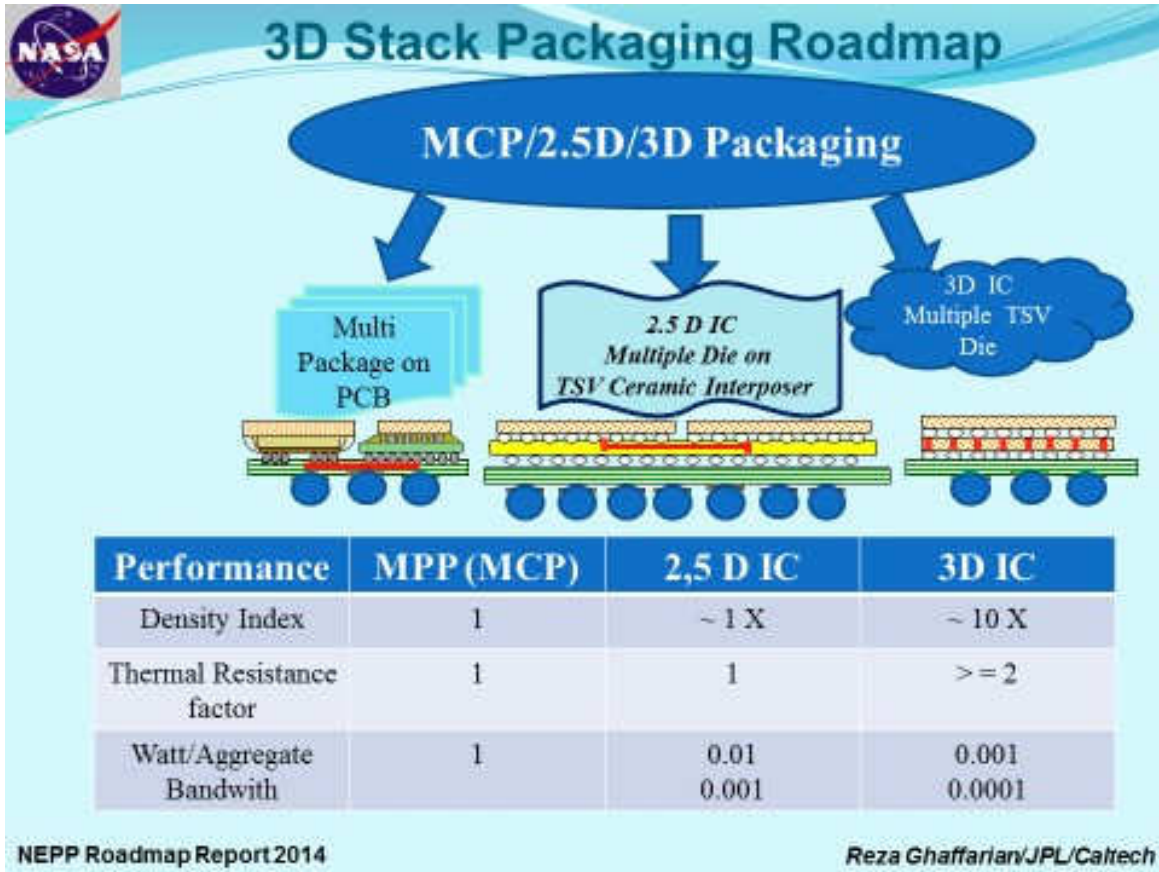


Figure 4-5. 2.5/3D packaging technologies showing conventional to advanced configurations.

4.3.1 2.5D (Passive TSV Interposer) Packaging Trends

The use of TSV interposer is key in 2.5D technology. In production of high I/O implementation, e.g., 2.5D TSV approach for Virtex-7 FPGAs [20], TSVs are used to route the signals through the silicon interposer down to flip-chip solder bumps located on the interposer's bottom side. This device has four FPGA chips attached to a silicon interposer, which supports ~10,000 silicon-speed connections between adjacent chips. The ICs themselves use much smaller copper (Cu) pillar micro-bumps for assembly onto the silicon interposer. For example, the 2.5D FPGA with a passive TSV addresses two key requirements of the programmable die and packaging challenges. Stacked silicon interconnect (SSI) technology interposer breaks the limitations of Moore's law by using multiple smaller die rather one large die. It also enables reducing the time required to deliver the largest FPGAs with the highest bandwidth in the quantities needed to satisfy end-customer volume production requirements.

System-on-chip (SoC) design is unable; however, to address these key technological challenges. An SoC comprises millions of gates connected by complex networks of wires in the form of multiple buses, complicated clock distribution networks, and multitudes of control signals. Successfully partitioning an SoC design across multiple FPGAs requires an abundance of I/Os to implement the nets spanning the gap between FPGAs. With SoC designs including buses as wide as 1,024 bits, even when targeting the highest available pin count FPGA packages, engineers must use data buffering and other design optimizations that are less efficient for implementing the thousands of one-to-one connections needed for high-performance buses and other critical paths.

Packaging technology is one of the key factors to this I/O limitation. The most advanced packages currently offer approximately 1,200 I/O pins, far short of the total number of I/Os required. At the die level, I/O

technology presents another limitation because I/O resources do not scale at the same pace as interconnect logic resources with each new process node. When compared to transistors used to build the programmable logic resources in the heart of the FPGA, the transistors comprising device I/O structures must be much larger to deliver the currents and withstand the voltages required for chip-to-chip I/O standards. Thus, increasing the number of standard I/Os on a die is not a viable solution for providing the connections for combining multiple FPGA die. SSI technology solves the following key challenges:

- The amount of available I/O is insufficient for connecting the complex networks of signals that must pass between FPGAs in a partitioned design as well as connecting the FPGAs to the rest of the system.
- The latency of signals passing between FPGAs limits performance.
- Using standard device I/Os to create logical connections between multiple FPGAs increases power consumption.

The current state of interposer substrates were compared as shown in Table 4-1[21]. It was stated that the advancement of silicon performance is becoming more challenging as scaling is becoming more costly for technology solutions beyond CMOS. Integrated co-development of silicon and packaging solutions are needed to achieve new technologies with superior cost/performance metrics. Volumetric scaling also will be critical to future performance enablement and achieved by (1) tightly coupled modules and components and (2) 3D stacking and interposer integration.

Table 4-1. Key characteristics of ceramic, glass, and organic interposers for 2.5D packaging technology [21].

	Ceramic MCM	Organic MCM	Si Interposer	Glass Interposer	Organic Interposer
Dielectric Properties	Adequate	Good	Lossy	Excellent	Very good
Feature Dimensions	Mechanically defined	Down to ~10 μm L/S	Si-like lithography	Display like	Down to 5 μm L/S
CTE Induced Stress	Very good	Moderately high	Excellent	Tailorable	Moderately high
Cost	High	Moderate	Moderate	TBD	Low–moderate
Availability	Available	Available	Available	Development	Development

Figure 4-6 shows the product application for these interposers identified in another presentation [22]. The silicon interposer will dominate in the high end use; whereas in the mid-end, silicon will be key technology while organic/glass may also play a role. In the low end, organic, low cost glass or even low cost silicon if they exist will play a role. Specific production application are:

- (1) Gaming, high definition television (HDTV), mobile tablets, computing, and servers,
- (2) High end graphics cards will be the initial focus of high bandwidth memory (HBM) memory integration, and
- (3) Mobile space has the potential to follow based on availability of low cost solutions.

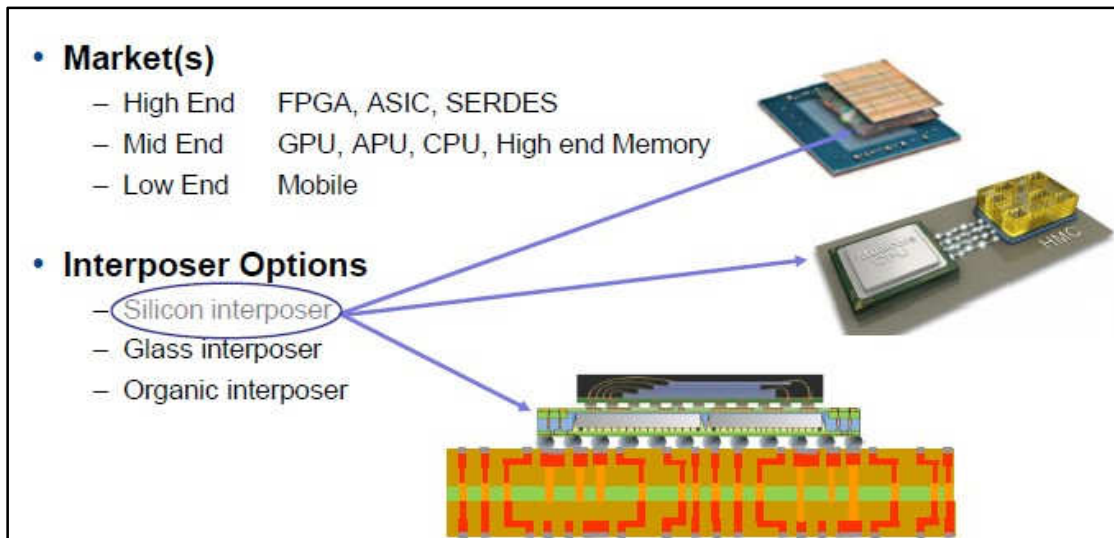


Figure 4-6. Market for 2.5D interposer options including silicon, glass, and organic materials.

In a recent paper [23], the authors discussed the options for 2.5D technologies with emphasis on assembling micro-bumped die (MBD) to a Si-interposer and then the interposer to an organic substrate. To achieve a high assembly yield and reliability, the key controls should be in place to minimize warpage, allow handling of extremely thin Si wafer, and to ensure integrity of micro-bump interconnects with fine pitch (typically can be < 45 um pitch). The high density of pads and the large die size make it extremely challenging to ensure that all of the micro-bump interconnects are attached to a thin Si-interposer. The authors concluded that semiconductor fabrication facilities can produce robust and reliable devices with TSVs and that the manufacturing infrastructure exists to assemble the 2.5D packages in high volume.

In a recent paper [24], the authors summarized the impact of 3D IC integration on various industry sectors: (1) it has impacted a large number of industries including the chip suppliers, fab-less design houses, electronic manufacturing service, material and equipment suppliers, universities, and research institutes; (2) it has attracted the researchers and engineers to attend conferences, and workshops to present their findings and look for solutions of the latest technologies; and (3) it has forced industry to build standards, infrastructures, and ecosystems for 3D IC integration

The author presented a “very low-cost interposer” using through-silicon holes (TSHs) with ability to build flip-chip die on both sides of the interposer for a 3D IC integration (see Figure 4-7). The key feature of TSH interposers is that the holes are not metallized; thus, it eliminates several processing TSV steps including dielectric layer, barrier and seed layers, via filling, and Cu revealing. The TSH interposers requires formation of with either laser or deep reactive ion etching (DRIE) on a piece of silicon wafer and redistribution layers (RDL). The top-side chip is interconnected through RDLs, whereas to the bottom-side is interconnected through copper pillars and solder.

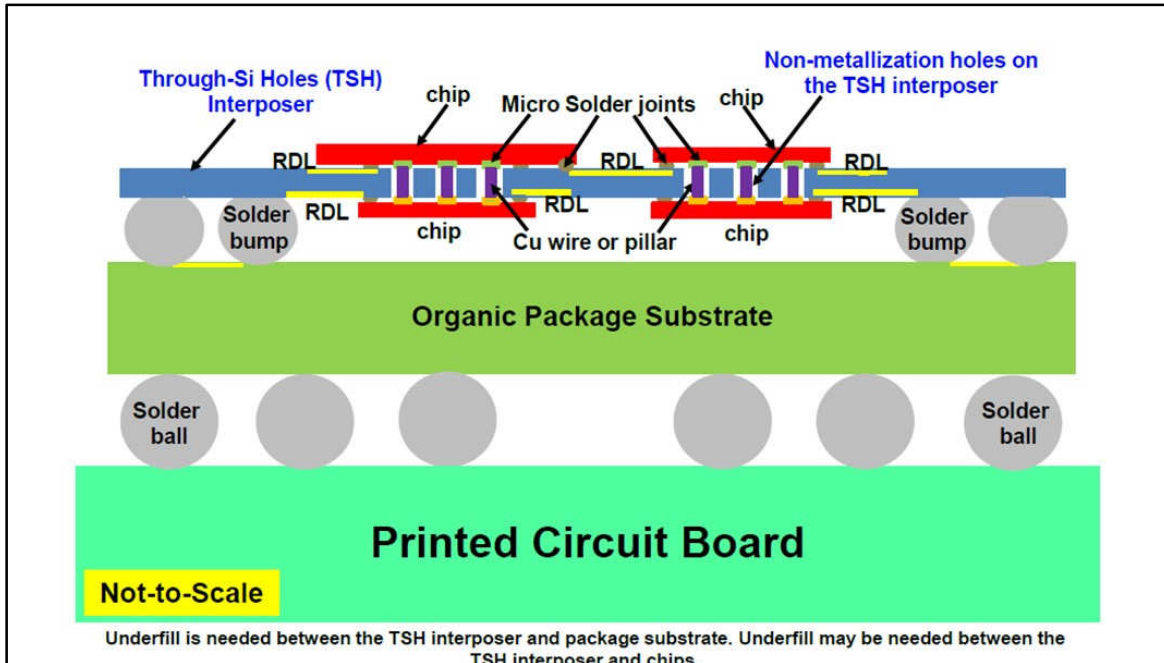


Figure 4-7. A SiP which consists of a TSH interposer supporting chips with Cu pillars on its top-side and chips with solder bumps on its bottom-side.

Use of the glass interposer technology allows for a better system solution by increasing performance and improving reliability [25]. A glass display consists of glass interposer display, low stressed drilled holes, and copper vias CTE matched to the display glass. The via diameters are approaching 40 μm in 300 μm thick glass wafers. The glass hole in this technology uses a funnel-like shape where the top side (entry) of the glass hole is 60 μm and the bottom (exit side) is 40 μm . The hole is then filled with copper material, thus creating a copper-based via. The authors claim that the technology is disruptive to the supply chain since the final via size is <50 μm and the copper is matched to the CTE of the glass, creating a true hermetic seal. The authors added that glass 2.5D and 3D packaging technologies solve hermetic problems by the integration of electronics directly into the glass.

The authors demonstrated [25] the ability to generate well-formed through and blind vias and fully populated test vehicles using glass interposers. Existing metallization technology was leveraged to generate very good Cu filling performance in glass in both wafer and panel formats. The electrical performance of glass, and tunability of material properties such as CTE and the ability to form in thin large sheets of high quality allowing cost effective processes, generates tremendous incentive for using glass as a TGV substrate for 2.5D and 3D applications.

Through-package vias (TPVs) and re-distribution layers (RDLs) are two key building block technologies for glass interposer. The TPV technology was presented covering detailed electrical modeling, design, and characterization using 3D glass interposers [27]. High frequency characterization, up to 30 GHz, was presented for high aspect-ratio 55- μm diameter TPVs in 300- μm thin glass, formed by a novel focused electrical discharge method that is capable of greater than 1000 vias per second throughput. Such a glass interposer is ideal for 2.5D and 3D package integrations for high performance digital systems with high logic-memory. Glass has been proposed as a superior alternative to silicon because of its excellent electrical property and its scalability to large panel sizes leading to lower cost.

4.3.2 3D (Active TSV Interposer) Packaging Trends

This category of packages with TSV stack die is often called “3D integration” in order to distinguish them from 3D packaging. Stacked memory die is a perfect choice for using TSV technology as all

interconnections of each die align with the corresponding die located above and below. However, this is merely a building block for future designs as mobile terminals to supercomputers, which require maximum computing power using limited resources such as power consumption and volume for the next-generation of information processing devices. A 3D-integrated logic device with stacked memory matches this objective because the shortest and highly parallel connection between logic and high-capacity memory reduces the power consumption due to long-distance and high-frequency signal transmission, and realizes the highest device density.

Therefore, TSVs refer to a 3D package that contains two or more chips (integrated circuits) stacked vertically so that they occupy less space on a printed circuit board (PCB) (usually the same footprint as the bottom chip). TSVs replace edge wiring by creating vertical connections through the body of the chips. The resulting package has no added length or width. Because no interposer is required, a TSV 3D package can also be flatter than an edge-wired 3D or 2.5D package. Not all TSVs are the same. There are many variations of this technology.

The key on use of TSV technology is to address when it is advantageous to go vertical and when it is not. Stacking two wafers and integration with vertical vias is costly. This cost must be justified through performance gains, functional gains, or cost savings elsewhere in the system. The market for TSVs will be established when the benefits justify the cost. There is a growing consensus that several mainstream circumstances exist that justify the 3D integration.

Use of TSV 3D integration is rarely justified for form-factor miniaturization alone since in most circumstances, it is much more cost-effective to meet the form-factor needs by stack and wire bond, or otherwise vertically integrate, at the package level. However, when identical memories are considered, use of TSV technology is advantageous since edge wire bonding cannot easily be used. In addition, there are system advantages to thinning and stacking multiple memory die such that the aggregate memory has the same end form factor as one memory package.

The most explored advantage of 3D is its reduction of the interconnect distances between chip functions. Many researchers justify 3D from interconnect delay and interconnect power perspectives. From a theoretical viewpoint, the advantages can be substantial. Several studies have presented a Rent's Rule style of analysis supporting this premise [28,29]. The basic argument relies on the fact that with each additional layer of transistors, there is a similar increase in the number of circuit functions that can be interconnected within a fixed wire length. This leads to a 25 percent or greater decrease in worst-case wire length [30], a similar decrease in interconnect power [31], and a modest decrease in chip area. However, experience shows that many designs do not realize the large theoretical advantages in practice. Fortunately, with careful choice, appropriate design applications can be found. For example, field programmable gate arrays (FPGAs) are very interconnect-bound and can achieve substantial performance and power improvements when recast in 3D [32].

Stacking memory die to create a new "super-memory" chip is not the only 3D application involving memory [33, 34]. An interesting area of application is targeting logic-on-memory, which creates a high-bandwidth memory interface to the logic. For many end applications, the demand for memory bandwidth is growing rapidly. In many cases, this is due to the increased use of multi-core processors. With the addition of each processor comes a similar requirement for increasing memory bandwidth. Similar bandwidths will be beneficial in other applications, including digital signal processing, graphics processing, and networking. This, by itself, gives a fairly natural case for 3D, one that has been only lightly explored, and then mainly in the context of general-purpose computer micro-architecture. For example, 3D caches can lead to 10 to 50 percent reductions in cache latency, depending on the benchmark used.

In summary, while the drivers for 3D ICs remain constant, the time line for its adoption continues to shift due to technical challenges and infrastructure issues. Progress has been made in via formation and filling, but process steps such as debonding during wafer thinning still remain problematic. Progress has been made in design tools and methodology, but low-power design of 3D IC stacks remains in the early stages. Test,

inspection, and reliability are yet to be fully implemented. Improvements in process yield and thermal solutions that lower cost are necessary. Key remaining technology gaps in 3D IC readiness are summarized in the following [35].

- Availability of commercial 3Delectronic design automation (EDA) tools
- Micro bumping and assembly for stacked die
- Assembly of die on interposers
- The debond step in temporary bond/debond
- Thermal design and dissipation when logic is part of the stack
- Test methodology and solution
- Reliability data including drop test data
- Yield improvements that lower cost
- Infrastructure related issues such as hand-off point

5.0 EMBEDDED COMPONENT TECHNOLOGIES

Passives usually refers to resistors, capacitors, and inductors; but it can also include thermistors, varistors, transformers, temperature sensors, and almost any non-switching analog device. The discrete passive component is a single passive element in its own leaded or surface mount technology (SMT) package. An on-chip passive is a passive element that is fabricated along with the active elements as part of the semiconductor wafer (die) where an on-package version uses passives on the package substrate using SMT.

For example, decoupling capacitors can be placed on either the top or bottom of the package. Each of these locations has its associated advantages and disadvantages. Top side decoupling capacitors (see Figure 5-1) have the advantage of efficient space utilization, but overall system equivalent series inductance (ESL) can be compromised because of the larger distance between the capacitors and the power and ground pins of the microprocessor. On the other hand, path length is decreased for bottom-side decoupling, but valuable real estate that could be used for I/Os is taken up.

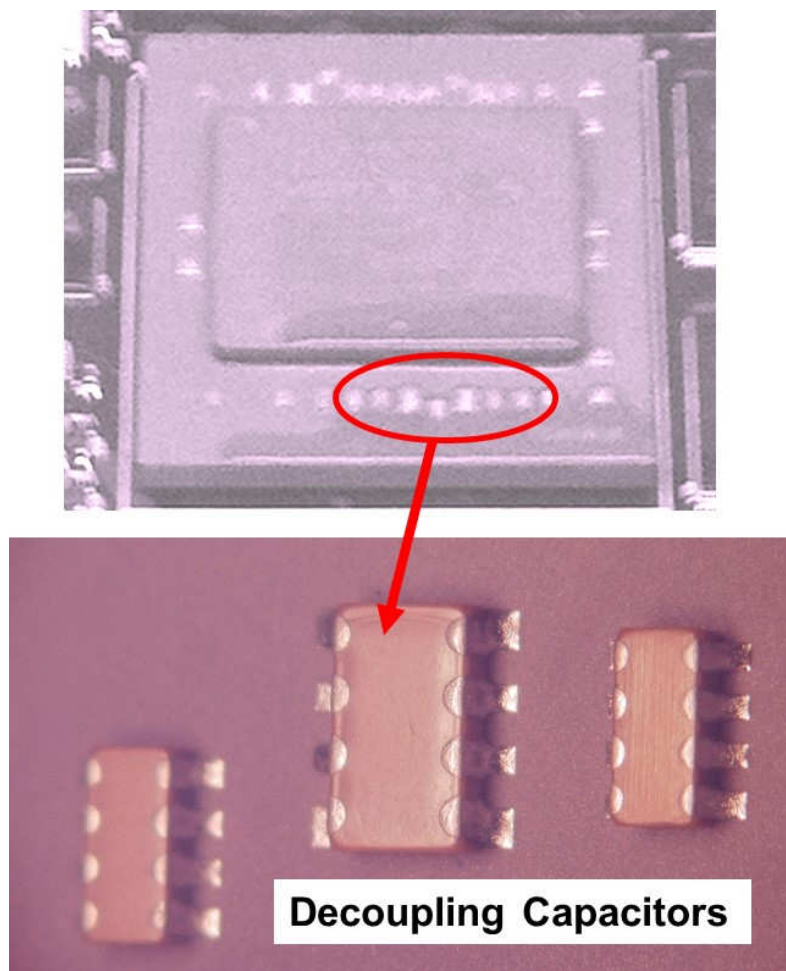


Figure 5-1. Flip-chip column grid array (CGA) with exposed decoupling capacitors.

The concept of embedded, integrated, integral, arrayed, or networked passives involves manufacturing them as a group in or on a common substrate instead of discrete packages. In general, embedded components are defined as passive or an active device that is placed or formed on an inner layer of an organic circuit board, module or chip package such that it is buried inside the completed structure, rather than on top or bottom

surface. The drivers are similar to SiP. Primary market segments using embedded components today include defense/aerospace, network infrastructure, and mobile communications. The key advantages are:

- Reduced product cost
- Added features
- Reduced size
- Improved performance
- Accelerated time to market

ITRS defines two types of passive/active devices for embedded applications (see Figure 5-2). Embedded passive devices in PCB are categorized into either chip devices or formed devices. Also, there are two types of active devices: (1) wafer level package and (2) flip-chip die. The wafer level uses die with no copper post to enhance mechanical strength whereas the flip-chip uses die with stud bump or copper posts which are embedded in an organic laminates substrate.

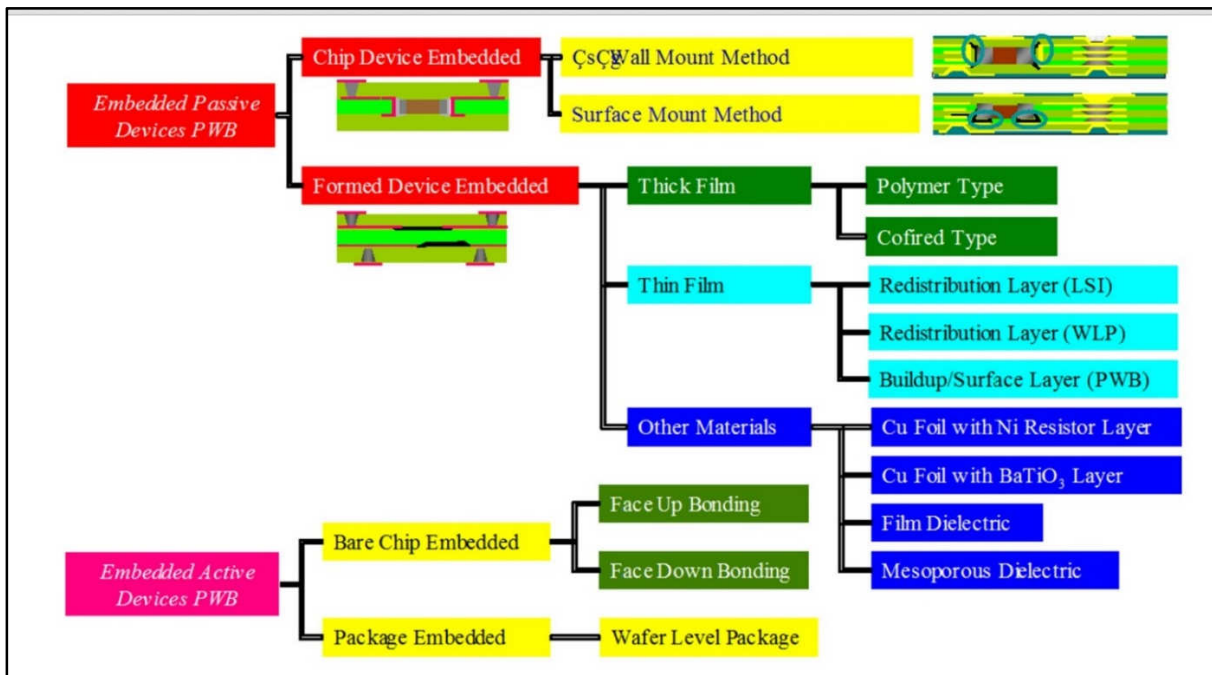


Figure 5-2. Overview of Embedded Active Devices and Passive Devices [1].

5.1 Integrated Passive Devices (IPD)

Integrated passive devices (IPDs) are subcomponents that exclusively contain passive components. The IPDs play a crucial role in the packaging technology because the passive components often occupy more than 80% of the real estate in the board, while the assembly cost accounts for around 70% of a product assembly cost. The embedded-passive technology makes an overall board size smaller, leading to the higher throughput. It also helps improve the electrical performance because it eliminates soldering, which in turn improves system reliability while achieving a cost reduction and a faster time to market by removing surface-mounted devices (SMDs). Advantages such as lower cost, compactness, reliability, and higher performance make the IPD technology a suitable package solution for the systems as well as a key technology for the higher integration.

The IPD may contain all three types of passives (R, L and C, resistor, inductor, and capacitor, respectively) in any combination. The elements can be connected to each other in order to form a certain network, matching or filter functions, or stand-alone elements to serve their function. The introduction of new materials like thin oxides or filled polymers as dielectrics as well (as the introduction of deep silicon vias) is extending the value range of capacitors into the microfarad realm. Besides standard redistribution wiring systems, it is also possible to form ground planes and transmission lines to create impedance-controlled RF-signal transmission.

IPD packaging can be categorized as either stand-alone chip scale package IPD devices or integrated IPD modules. Chip-scale IPD packages contain the entire IPD network in a single system in package (SiP) structure. This single package is designed to replace a surface mount passive component network. It is common to see these single packaged networks in ball grid arrays (BGAs), quad flat no leads (QFNs), and flip-chip packages. The area array packages help take full advantage of the size reduction achieved by using IPD technology.

Figure 5-3 shows an example of a wafer-level chip scale module package (WLCSMP) [36]. This category of module package is the advanced modular architecture that integrates mixed IC technologies with a wide variety of passive devices such as resistors, capacitors, inductors, filters, baluns, transceivers, receivers, and interconnects directly onto a silicon substrate. The result is a set of high performance system level solutions that provide a significant reduction in die size and weight.

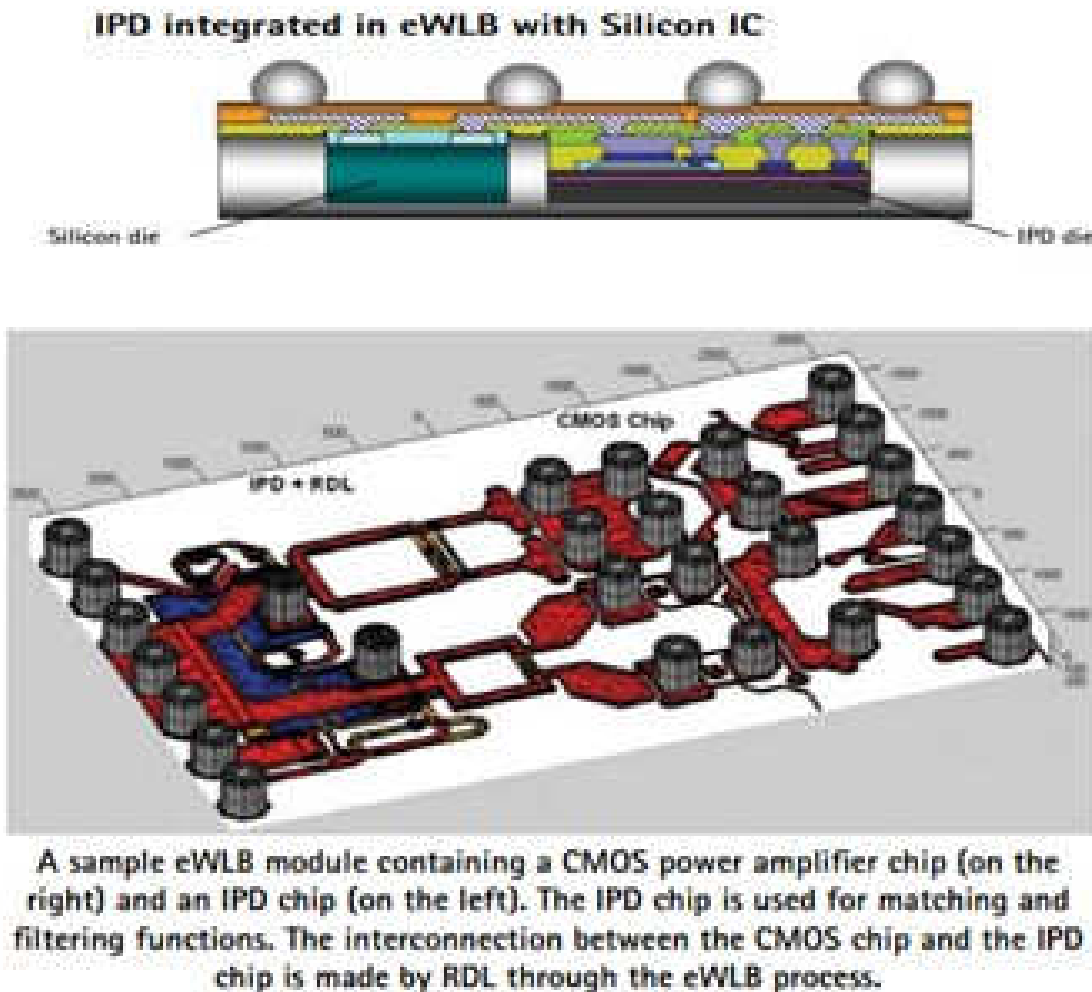


Figure 5-3. Configuration of wafer level chip scale module package (WLCSMP) [36].

In order to reduce the board surface area and system cost associated with passive components, recent movements in the industry are focusing on alternative mounting methods. Alternative mounting include on-chip, multiple value discrete passive components (arrays) mounted onto boards or substrates, passives fabricated within the board (embedded), and combinations of all of the above. One emerging method is the array or network approach known as "integrated passive devices" or IPDs. Integrated passives are simply collections of passive devices made using semiconductor or thin-film methods, packaged as an integrated circuit (IC).

In a recent presentation at the evolving technology symposium at SMTA2014, an expert author presented the key advances and hurdles in implementation of passive and active technologies [37]. The key findings are listed in the following.

- Embedded circuits are being produced successfully in very high volume worldwide.
- Embedding the semiconductor is where many companies may find a significant roadblock-
 - Procurement of semiconductors in a wafer format
 - Outsourcing metallization and thinning
 - Confidence in semiconductor quality (KGD)
 - Sequential electrical testing during PCB Fab.
 - Testing embedded mixed function assemblies
- The PCB fabricator will be expected to perform board-level functional electrical testing.
- When outsourcing embedded component PC boards, the originating company will likely bring together the two primary disciplines; the circuit board fabrication specialist and the assembly service provider.
 - These partnerships must be willing to adjust their portion of the generated revenue against the overall process yield (includes the sharing of losses from fabrication process defects and damaged components).

5.2 Embedded Active

Recently, in addition to embedding passive components, attempts are being made to embed active chips. For the embedded active structure, thinned active chips are directly buried into a core or high-density interconnect layers rather than placed onto the surface. Currently, active chips can be embedded in many different ways within the categories of chip-first, chip-middle, and chip-last. Embedding is expected to reduce the parasitic effects of interconnects (reduced interconnect length) resulting in lower power dissipation, and providing better electromagnetic shielding. They also offer smaller and thinner package profiles.

In general, the chip-first technology has a number of challenges:

- The chip, once it is embedded, is subjected to a number of processing steps and can be affected due to the fabrication.
- Serial chip-to-build-up processes accumulate yield losses associated with each process.
- Defective chips cannot be easily reworked in current embedded package structure. Thus, this technology needs 100% known good die (KGDs).
- The interconnections in the chip-first approach, which are direct metallurgical contacts, can encounter fatigue failures due to thermal stress.
- Thermal management issues are also evident since the chip is totally embedded within polymer materials during the substrate or build-up layer processes.

Ultra-thin flexible microelectronics were evaluated for use in applications such as conformal and wearable electronics by embedding less than 50- μm silicon die [38]. As shown in Figure 5-4, three techniques have been developed to fabricate ultra-thin, flexible electronics: 1) thinned die flip-chip bonded on polyimide or liquid crystal polymer (LCP) flex, 2) thinned die laminated into LCP films, and 3) thinned silicon die

embedded in polyimide. The manufacturing methods and materials for each of these approaches is described in the following sections.

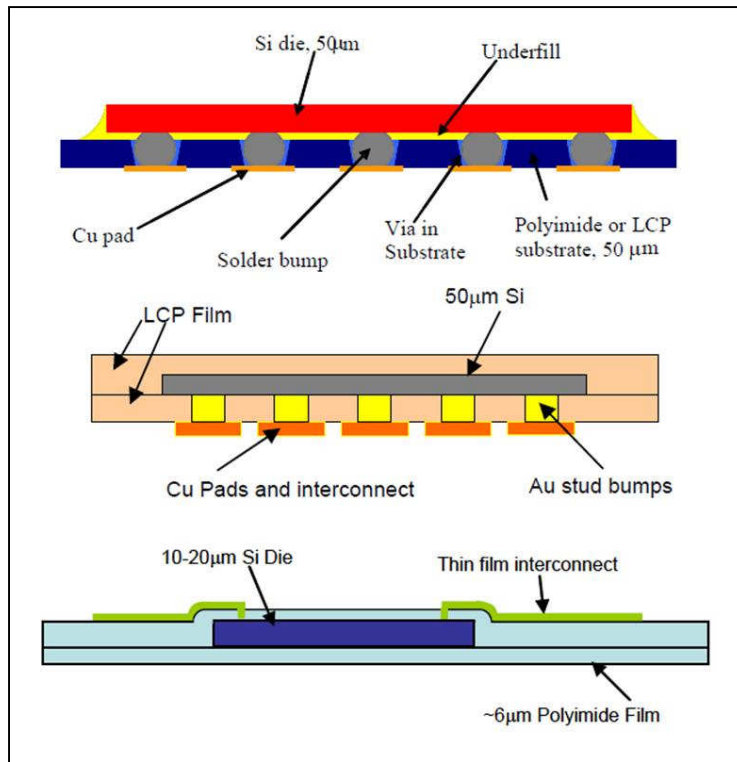


Figure 5-4. Three techniques of thinning die: polyimide and LCP substrate with solder assembly (top); LCP substrate with thermal compression bond Au stud bump assembly (middle); thinned Si die embedded in polyimide with thin film interconnect (bottom) [38].

A new embedded package configuration, wide strip fan-out package (WFOP), was presented in a recent conference [39]. The package is a face-down mounting (See Figure 5-5), which uses a metal plate (stainless steel or copper) as the base plate of the redistributed interconnection layer. The dies are mounted on the metal plate, and the resin between the dies acts as a stress buffer and insulator for the interconnections. The advantages are a lower package warpage, precise fabrication process control, lower thermal resistance, and shielding of noises. The author showed reliability test results and multiple die stacking configuration for use in memory devices.

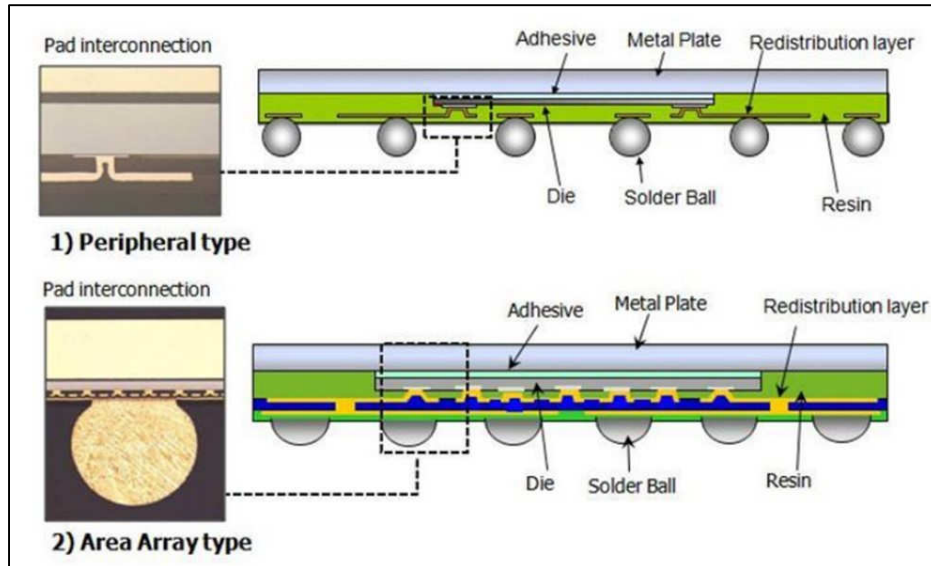


Figure 5-5. A new embedded package, wide strip fan-out package (WFOP) , which uses a metal plate like. [39].

PCB based embedding technologies combine the advantages of standard printed circuit manufacturing with additional highly precise component assembly. Generally, two different approaches of component assembly are used: Face up, where the assembly of the semiconductor die is down with its contact pads up, comparable to a die for wire bonding, or face down where the die is assembled with its contact pads down, like a flip chip. The face-up technology enables electrical and thermal contact using both conductive and non-conductive adhesives, solder, and low temperature sinter materials for the die-attachment. Because of its heat dissipation, this approach is widely used for various embedded active die including power metal oxide field effect transistors (power-MOSFETs), insulated gate bipolar (IGBTs), and diodes. Since the face-down technology is comparable to the conventional wire bonding, it is already in high volume application. The process starts with embedding the die with placement of resin-coated copper (RCC) or prepreg with conductive adhesive and vacuum lamination followed with a microvia build for electrical connection to the embedded chip. Such substrates with embedded dies can be further processed like standard PCB inner layers. Figure 5-6 shows an example of a face down embedded component technology, a DC-DC converter. This package has one embedded die with three SMD components assembled on top of the PCB [40, 41].

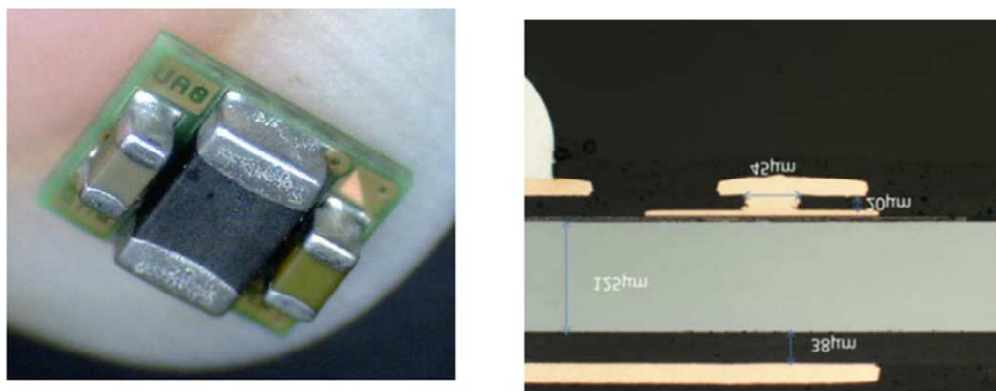



Figure 5-6. Configuration of wafer level chip scale module package (WLCSMP) [40, 41].

In a recent keynote luncheon talk, the speaker provided the status of embedded devices and application as shown in Figure 5-7 [42].



Embedded Devices: Today's Drivers and Applications

- **Embedded placed actives:**
 - Driver—package thinness
 - Secondary advantages are improved robustness and security
 - First applications—ultra-thin PoP for mobile products
 - Technology—thin-film, laminated or build-up
 - Companies with embedded die PoP activities Amkor, ASE, AT&S, DNP, FlipChip International/Fujikura, J-Devices, NANIUM, Shinko Electric, SPIL, STATS ChipPAC
- **Embedded placed passives:**
 - Driver—decoupling capacitance close to the processor to enable higher operating frequencies
 - Application processors with embedded capacitors in HVM for mobile phones
 - Future applications—high-end networking and communications
 - Technology—primarily capacitors in build-up or laminated substrates

Figure 5-7. Status of embedded component technology. [42].

6.0 PACKAGING INTERCONNECTIONS AND HIERARCHY

6.1 Surface Mount Technology Hierarchy

For surface mount technology (SMT), packaging hierarchy defines different manufacturing and system levels. Definition of electronics elements and system level (e.g., defining interconnects between system levels) allows value chain participants to capture value and enable innovation. Furthermore, the acceptance of definitions allows value chain members to develop materials and technologies optimized for use within specific system levels. For example, the JISSO international council (JIC), a mix of membership from Asian, European, and North American members, was formed with the aim of promoting a strategic partnership among organizations interested in the total solution for electronics interconnecting, assembling, packaging, mounting, and integrating system design. Figure 6-1 shows a recent proposal by JISSO with an added expansion on definition of packaging hierarchy [43, 44].

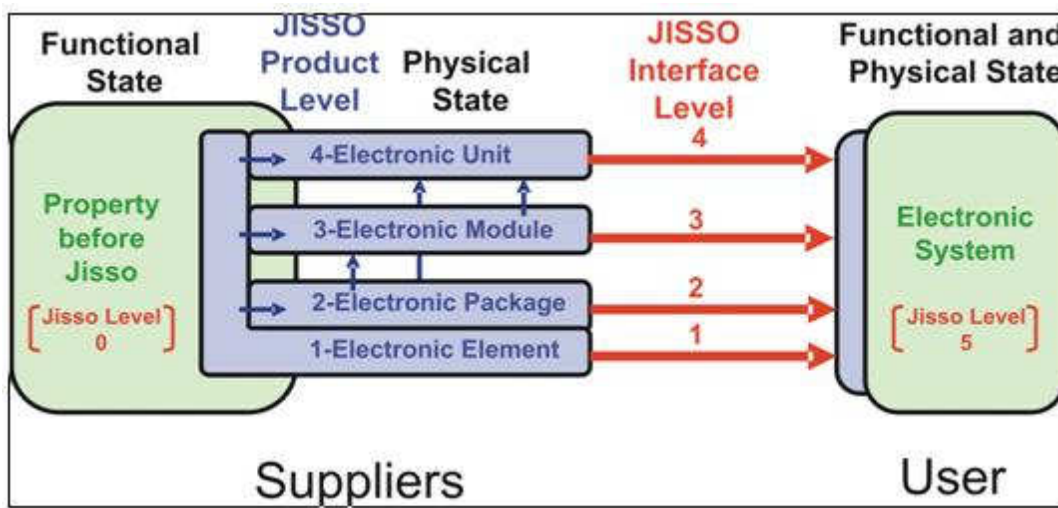


Figure 6-1. SMT packaging hierarchy presented by JISSO [43].

The definition of interconnection hierarchy includes the following levels [1,2, 43,44].

Level 0 – Electronic Element: The intellectual property of an item pertains to the idea or intelligence imported or described in a formal document (protocol, standards and/or specifications), design entity, or patent disclosure. The information may be in hard or soft copy and can include computer code or data format as a part of the descriptive analysis. The characteristics are described as to their physical, chemical, electrical, mechanical, electromechanical, environmental, and/or hazardous properties.

Level 1 –Electronic Element: Uncased bare die or discrete components (e.g., resistor, capacitor, diode, transistor, inductor, or fuse), with metallization or termination ready for mounting. This can be an IC or a discrete electrical, optical, or MEMS element. Individual elements cannot be further reduced without destroying their stated function.

Level 2 – Electronic Package: A container for an individual electronic element or elements that protects the contents and provides terminals for making connections to the rest of the circuit. The package outline is generally standardized or meets guideline standards. The package may function as electronic, optoelectronic, MEMS, or system in package (SiP), and may in the future include bio-electronic sensors.

Level 3 – Electronic Module: An electronic sub-assembly with functional blocks, which is comprised of individual electronic elements and/or component packages. An individual module having an application-specific purpose including electronic (including SiP), optoelectronic, or mechanical (MEMS). The module generally provides protection of its elements and packages, depending on the application to assure the

required level of reliability. The module may be a company standard (catalog item) or custom (OEM-specific). Note: there will likely be some subdivisions of Level 2 and Level 3 descriptions to increase the granularity and clarity relative to what is included within each of these levels.

Level 4 – Electronic Unit: Any group of functional blocks that have been designed to provide a single or complex function needed by a system in order for the system to serve a specific purpose. The electronic unit may be comprised of electronic elements, component packages and/or application -specific modules. The function of the electronic unit may be electronic, optoelectronic, electromechanical, or mechanical or any combination thereof. The function may in the future include bio-electronic applications.

Level 5 – Electronic System: A completed, market-ready unit dedicated to combining and interconnecting functional blocks. The functional blocks are generally comprised of electronic units, but may also include electronic modules, electronic packages, or electronic elements. The electronic system product can include the cabinetry, a backplane or motherboard (into which the assemblies, modules, packages, or elements are inserted), and the cabling (electrical, optical, or mechanical) needed to interconnect the total functional block(s) into a configured system. The electronic system can vary in complexity from very simple to highly complex.

The interconnect hierarchy has evolved since the introduction of the transistor in 1960 [44]. Figure 6-2 compares the traditional view of the hierarchy (lower left) to the emerging microelectronic technologies with growing ambiguity in interconnection level definition. In the early days, the divisions of levels for the various tasks involved in the creation of an electronic system were well defined. The semiconductor manufacturer created the integrated circuits (ICs); the IC chips were packaged for protection; a printed circuit facility built a substrate according to a design. Next, the package was assembled onto a board (using a soldering process) and used as “daughter card” for the next assembly of motherboard. The completed assembly would then be packaged in a suitable format, whether a computer, telephone switch, internet router, or any other product.

Now, there are new interconnections, such as a wafer-level packages and 3D stacks; some lack a clear category or definition. The blue area in the Figure shows added new interconnections with lack of clear category; therefore, there is a need to find a way to embrace the emerging technologies that are already being deployed to create next generation products.

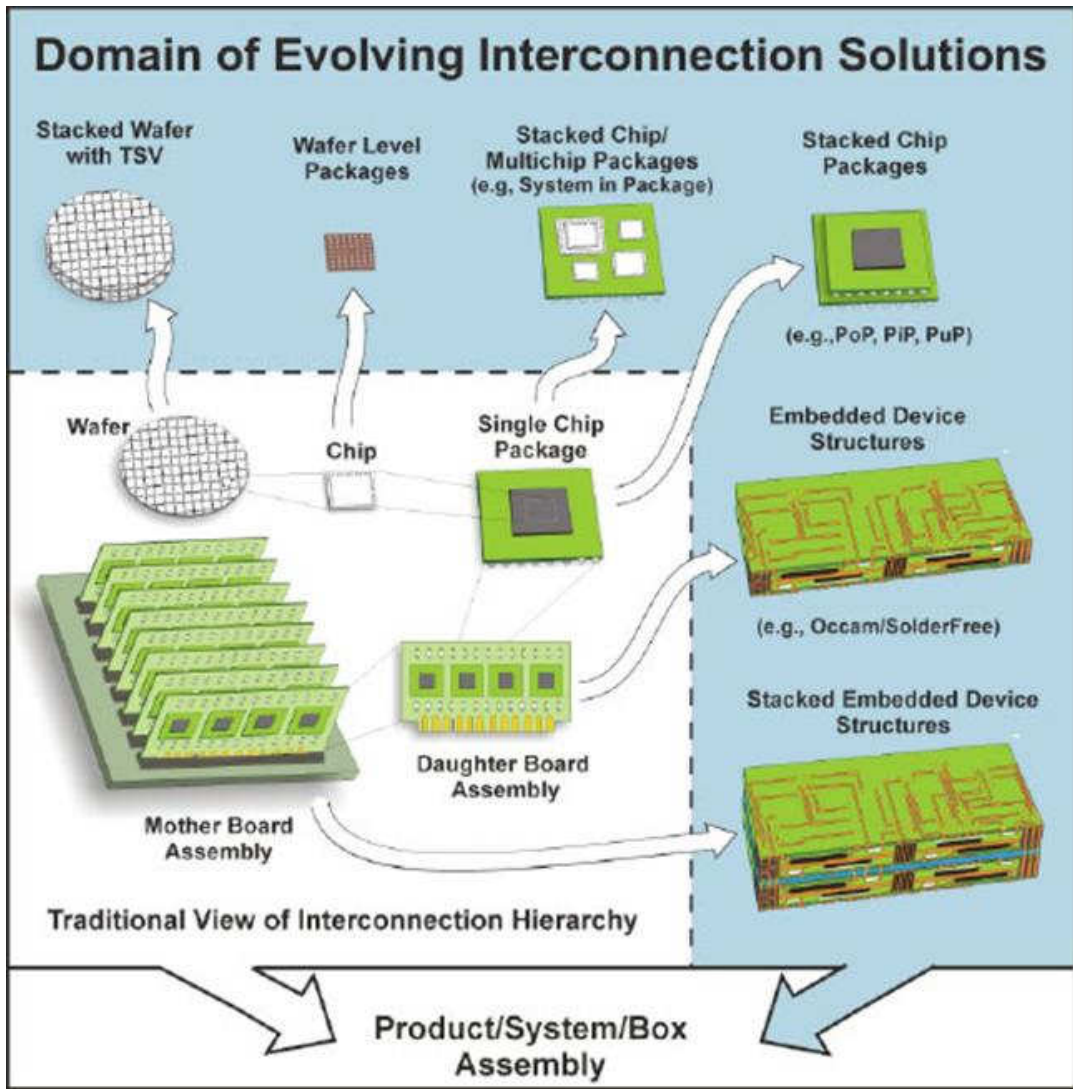


Figure 6-2. Expansion of SMT packaging hierarchy with inclusion of new developments in packaging, including wafer levels and 3D stacks [44].

7.0 SUMMARY

The success and proliferation of the integrated circuit since its discovery in the late 1950s has been due to the ability of manufacturers to continue offering more for the money. This ability to reduce the cost of ICs per performance has been driven by the continuous and rapid development of new and improved process technologies. The next shrinkage is packaging technology. Packaging shrinkage is enabled by using flip-chip ball grid array (FCBGA), through silicon via (TSV) interconnections, and 3D TSV stacking technologies.

For five decades, the semiconductor industries have distinguished itself from other industries by continuously shrinking ICs enabling functional improvement—Moore’s Law—and developed miniaturized electronics products with much lower cost. Now, IC shrinkage is hitting a brick wall, a new paradigm shift is emerging: IC packaging shrinkage, stacking, and system integration. A few key points on packaging trends discussed in this report are summarized below.

- Reviewed key packaging trends by surveying roadmaps generated from the key microelectronics industry standards groups, including ITRS, iNEMI, IPC, and OE-A, to define the pulse of development and potential areas for further evaluation for high reliability applications.
- The ITRS roadmap projects that by 2020–2025, CMOS physical dimensions will approach the 5–7nm range, beyond which it will become difficult to operate. System integration or “more than Moore” become the new option for miniaturization by utilizing the vertical dimension, a 3D approach.
- The INEMI projection on package growths predicts a moderate growth for QFP/LCC and COB whereas significant growth both for QFN and WLP. iNEMI projects a decline in conventional DIP leaded package as well wire bonded die BGA with conventional pitch, whereas a moderate increase for wire bonded die of finer pitch BGAs. Significant increases are projected for flip chip FPGA as well as stack packaging technology.
- Surveyed the status of QFN packaging technologies. The QFN are new category of packages—leadless; which have no ball or columns for interconnection, using only solder. These packages are also known as bottom-termination components (BTCs) and numerous other nomenclatures. The terms include quad flat no-lead (QFN) and dual-row/multi-row QFN (DRQFN/MRQFN), dual flat no-lead (DFN), and land grid array (LGA) packages.
- New packaging technologies identified by iNEMI are: (1) wafer level packaging (WLP) and bonding, (2) system in package (SiP), (3) printed electronics, (4) direct bonding interconnect, (5) New conductive and dielectric materials, and (6) 3D integration.
- Presented the hierarchy of device/package/systems to enable users to better define key implementation and reliability challenges associated with packaging technologies at various levels for high reliability applications.
- Commercial industry has now widely implemented the single chip packages (including BGAs and CSPs) for many electronics system applications including portable and telecommunication products. More than 1,000 I/O ceramic CGAs are now offered by package suppliers for high reliability applications. A new class of package – class Y- was added to the specification, MIL-PRF-38535, Revision K in order to cover high I/O CGA use.
- Summarized the key trends in electronic packages for high reliability applications. These include: (1) ceramic quad flat pack (CQFP) to area array packages, (2) CBGA to CCGA/CGA (>500 I/Os) and land grid array (LGA), (3) Wire-bond to flip-chip die within a package, (4) Hermetic to non-hermetic packages (>1000 I/Os), (5) high-lead solder columns to columns with Cu wrap, (6) Pb-Sn to Pb-free, including potential use of a Cu column, and (7) land grid with conductive interconnects rather than Pb-free solder
- Commercial industry also started using the finer pitch wafer level package (WLP) because of additional size and cost reduction as well as their wider applications including use for MEMs.

- For high density packaging, the migration to 3D using conventional interconnection method has become mainstream. Currently, 3D packaging consists of stacking of packaged devices, called package-on-package (PoP), stacking of die within a package called package-in-package (PiP), or stacked wire bonded die (primarily memory). The PoP packaging technologies were categorized in three styles: (1) PoP with center mold and flip chip, (2) PoP with partial cavity structure, and (3) through-mold via (TMV™).
- Reviewed the 3D packaging technology with through silicon via. The TSV technology implementation challenges introduced the 2.5D technology, an interim solution. The 2.5D packaging—active on passive-with TSV interposer—implemented by an FPGA manufacturer transitioning finer pitch die with 28 nm technology to coarser 65 nm technology.
- The 2.5D interposer materials were categorized in three main group. It is projected that the silicon interposer will dominate in the high end whereas, in the mid-end, silicon will be prominent and organic/glass may play a role. In the low end, organic, or low cost glass or even low cost silicon if they exist will play a role. Glass has been proposed to be a superior alternative to silicon because of its excellent electrical property and the scalability to large panel sizes leading to lower cost.
- The 3D chip stacking technology using through-silicon vias (TSVs) is the ultimate miniaturization since it offers the possibility of solving serious interconnection problems while offering integrated functions for higher performance.
- Integrated resistors and capacitors within PCB as thin film layer is a matured technology, but the trend is now towards implementation of insertion of passive and active components.
- Embedded components are defined as a passive/active discrete/devices that are placed or formed on inner layers of substrate/board. Embedded passives with board is near maturing whereas new classes of integrated passive devices within package are continue to emerge.
- Much work are needed for wider implementation of active devices. A rapid growth is projected for automobile/medical, consumer and mobile/wireless industry sectors. Generally, two different approaches of component assembly are used: face up and face down. Face up is where the assembly of the semiconductor die is down with its contact pads up, comparable to a die for wire bonding, or face down where the die is assembled with its contact pads down, like a flip chip. The face-up technology because of its heat dissipation characteristic is widely used for various embedded active including power-MOSFET, IGBT, and diodes.
- Printed electronic technology (PET) is complementary to silicon chip technology, which industry continues to find special applications for, with significant cost per area and throughput benefits. PET's key applications are briefly presented. It is forecasted that the PET market will outpace silicon chip electronics because of its ubiquity.

Understanding key roadmaps in microelectronics and technology development and the characteristics of packaging and printed electronics technologies—advantages and disadvantages—are important in judiciously selecting and narrowing the follow-up applicable technology, and quality assurance and reliability test methods in preparation for low-risk insertion into electronic or non-electronics systems for NASA use.

8.0 ACRONYMS AND ABBREVIATIONS

2D	two dimensional
3D	three dimensional
APU	Accelerated Processing Unit
aQFN	advanced quad flat no-lead
ASIC	application-specific integrated circuit
BGA	ball grid array
BOK	body of knowledge
BTC	bottom termination component
CBGA	ceramic ball-grid array
CCGA	ceramic column grid array
CGA	column grid array
CMOS	complementary metal oxide semiconductor
COB	chip-on-board
COTS	commercial-off-the shelf
CPU	central processing unit
CQFP	ceramic quad flat pack
CSP	chip scale package
CTE	coefficient of thermal expansion
DCA	direct chip attachment
DFN	dual flat no-lead (package)
DOE	design of experiment
DRIE	deep reactive ion etching
DRQFN	dual-row quad flat no-lead
EDA	electronic design automation
EMS	electronics manufacturing services
ESL	equivalent series inductance
eWLB	embedded wafer level ball grid array
FCBGA	flip-chip ball grid array
FCOB	flip chip on board
FC	flip-chip
FCBGA	flip-chip ball grid array
FCIP	flip-chip in package
FCOB	flip chip on board
FLI	first level interconnect

FPBGA	fine pitch ball grid array
GPU	graphics processing unit
HBM	high bandwidth memory
HDTV	high definition television
I/O	input/output
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IGBT	insulated gate bipolar transistor [?]
iNEMI	international electronics manufacturing initiative
IPC	(association connecting electronics industries)
IPD	integrated passive devices
ITRS	International Technology Research Society
JIC	JISSO international council
JISSO	Japanese acronym for a total solution for interconnecting, assembling, packaging, mounting, and integrating system design
JPL	Jet Propulsion Laboratory
KGD	known good die
LCC	leadless chip carrier
LCP	liquid crystal polymer
LED	light emitting diode
LGA	land grid array
LOC	lead on chip
MBD	micro-bumped die
MCP	multi chip package
MEMS	micro-electro-mechanical systems
MLF	micro lead frame
MOSFET	metal oxide field effect transistor
MPP	multi package on PCB
MRQFN	multi-row quad flat no-lead
MtM	more than Moore
NASA	National Aeronautics And Space Administration
NEPP	NASA Electronic Parts Program
ODM	original design manufacturer
OE-A	organic electronics association
OEM	original equipment manufacturer

OLED	organic light emitting diode
OPV	organic photovoltaic
OTFT	organic thin film transistor
PBGA	plastic ball grid array
PCB	printed circuit board
PE/OE	printed electronics/organic electronics
PET	printed electronics technology
PGA	pin grid array
PIDTP	package integrity demonstration test plan
PiP	package-in-package
PoP	package-on-package
PuP	package under package
PWB	printed wiring board
QFN	quad flat no-lead
QFP	quad flat pack
QML	qualified manufacturer list
R2R	roll to roll
RCC	resin-coated copper
RDL	redistribution layer
RF	radio frequency
RFID	radio frequency identification
RoHS	(European Union) restriction of hazardous substances
SEM	scanning electron microscope
SERDES	serializer/deserializer
SIA	Semiconductor Industry Association
SiP	system in package
SMT	surface mount technology
SOC	small outline chip
SSI	stacked silicon interconnect
TFT	thin film transistor
TMV	through mold via
TPV	through-package via
TQFN	thin quad flat no-lead
TSH	through-silicon hole
TSOP	thin small outline package

TSV	through silicon via
TWG	technology working groups
TV	test vehicle
USON	ultra-thin-small-outline
VDMA	Verband Deutscher Maschinen und Anlagenbau (German engineering federation)
VQFN	very thin quad flat no-lead
WCSP	wafer level chip scale package
WFOP	wide strip fan-out package
WLCSMP	wafer-level chip scale module package
WLCSP	wafer-level chip-scale packaging
WLP	wafer level package

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14. ABSTRACT
47The objective of this document is to update the NASA roadmap on packaging technologies (initially released in 2007) and to present the current trends toward further reducing size and increasing functionality. Due to the breadth of work being performed in the area of microelectronics packaging, this report presents only a number of key packaging technologies detailed in three industry roadmaps for conventional microelectronics and a more recently introduced roadmap for organic and printed electronics applications. The topics for each category were down-selected by reviewing the 2012 reports of the International Technology Roadmap for Semiconductor (ITRS), the 2013 roadmap reports of the International Electronics Manufacturing Initiative (iNEMI), the 2013 roadmap of association connecting electronics industry (IPC), the Organic Printed Electronics Association (OE-A). The report also summarizes the results of numerous articles and websites specifically discussing the trends in microelectronics packaging technologies.

15. SUBJECT TERMS
packaging technologies, roadmap, ITRS, iNEMI, IPC, FBGA, BGA, CGA, CSP, 3D, printed electronics, large area electronics, andpackaging hierarchy

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