BROADBAND PHASE SHIFTER DESIGN FOR PHASED ARRAY RADAR SYSTEMS

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Dedicated to My Beloved Parents and Wife

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Contents

Abstract

Phase shifters are one of the key control components in phased array radar systems to electrically shape and steer the antenna beam. In modern radar applications where multi-function capability and communication security are required, broadband phase shifters are essential.

This work mainly aims to improve the conventional phase shifters and explore novel topologies for broadband and high performance designs. One set of general formulas, which includes the formulas of conventional method as a special case, is found for the high-pass/low-pass phase shifter design, and closed-form equations for bandwidth enhanced and dual-band loaded-line phase shifter are provided. Several novel topologies using a phase slope alignment concept are also proposed, where trade-offs between phase error, return loss and bandwidth are possible. Based on this method, an octave band phase shifter with an RMS phase error of 3.6º and a return loss larger than 15 dB ($|S_{11}|$<-15dB) was designed. Further study of the all-pass phase shifter is also presented to establish multi-octave band performance. As a conclusion, a phase shifter guide table is built for designers' reference. Other novel microwave components associated with the insertion phase, e.g. broadband quadrature and dual-band power dividers are also covered.

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List of Abbreviations

AI	Amplitude Imbalance
APN	All-Pass Network
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
BPF	Band-Pass Filter
BW	Bandwidth
CAD	Computer Aided Design
CMOS	Complementary Metal-Oxide Semiconductor
HP	High-Pass
LNA	Low-Noise Amplifier
LP	Low-Pass
MEMS	Micro-Electro-Mechanical System
MMIC	Monolithic Microwave Integrated Circuit
PE	Phase Error
RMS	Root-Mean-Square
RTPS	Reflection Type Phase Shifter
SNR	Signal-to-Noise Ratio
SPDT	Single Pole Double Throw
TL	Transmission line
UWB	Ultra-Wide Band
VSWR	Voltage Standing Wave Ratio

Chapter 1

Introduction

Phased array antennas are used in various modern radars and wireless communication systems. In these antennas, multiple antenna elements are placed apart in one, two or three dimensions to form the antenna beams so that the signal strength to/from designated directions is increased and the emissions to/from unwanted receivers/ sources is eliminated [1]. Unlike conventional mechanically rotated antennas, the direction and the shape of the antenna beam can be controlled electronically. By constructive or destructive combining of the energy of each antenna element with different weight vectors, the antenna beams are steered and shaped. The speed of beam steering and beam shaping is determined by the switching speed of the circuits, i.e. the semiconductor devices in most cases [2].

Previously, phased array antennas were mainly used in military and government applications such as aircraft and weather surveillance, target searching, positioning, tracking, identification and velocity monitoring, etc. [3]. The antennas can be passive or active. In passive phased arrays, antenna elements have a central transmitter/ receiver (T/R) and a power distribution network. In active phased arrays, each of the antenna elements or sub-arrays has its own T/R module. Active phased arrays provide

higher flexibility for the beam forming, but at a higher cost. The technology of integrated circuits has matured and it is now possible to integrate the whole RF T/R module into a single monolithic microwave integrated circuit (MMIC), which reduces the cost of the active phased arrays [4], [5]. Additionally, the use of technologies such as CMOS and BiCMOS help to reduce cost further.

Another benefit of phased array antennas is the capability to simultaneously process multiple functions at different frequencies [6]. To increase the functionality and capability further, broadband performance is also highly desirable. In phased array front-ends, fundamental control elements include attenuators and phase shifters. Attenuators can achieve very broad bandwidth because broadband resistive networks are used. However, broadband phase shifters are more difficult to design.

In the past half century, a lot of research has been done to enlarge the bandwidth of phase shifters. The objective of this work is to further increase the bandwidth of conventional topologies and explore new methods and topologies which may also lead to new design tradeoffs of phase shifters.

1.1 Fundamental Timed/Phased Array Front-End

The principle of a one dimensional phased array receiver antenna with N antenna elements is illustrated in Fig. 1.1. The principle can also be applied to transmitters. Each antenna path consists of a bandpass filter (BPF), a low-noise amplifier (LNA), a phase shifter and an attenuator. The signals pass summed in the power combiner. The

signals before the combiner are required to be coherent for proper signal summation. Because the noise received by each antenna element is considered to be incoherent, the signal-to-noise ratio (SNR) of the phased array antenna with N path is improved by a factor between N and N^2, depending on the noise contribution and the system architecture, compared to a single antenna system [4], [7].

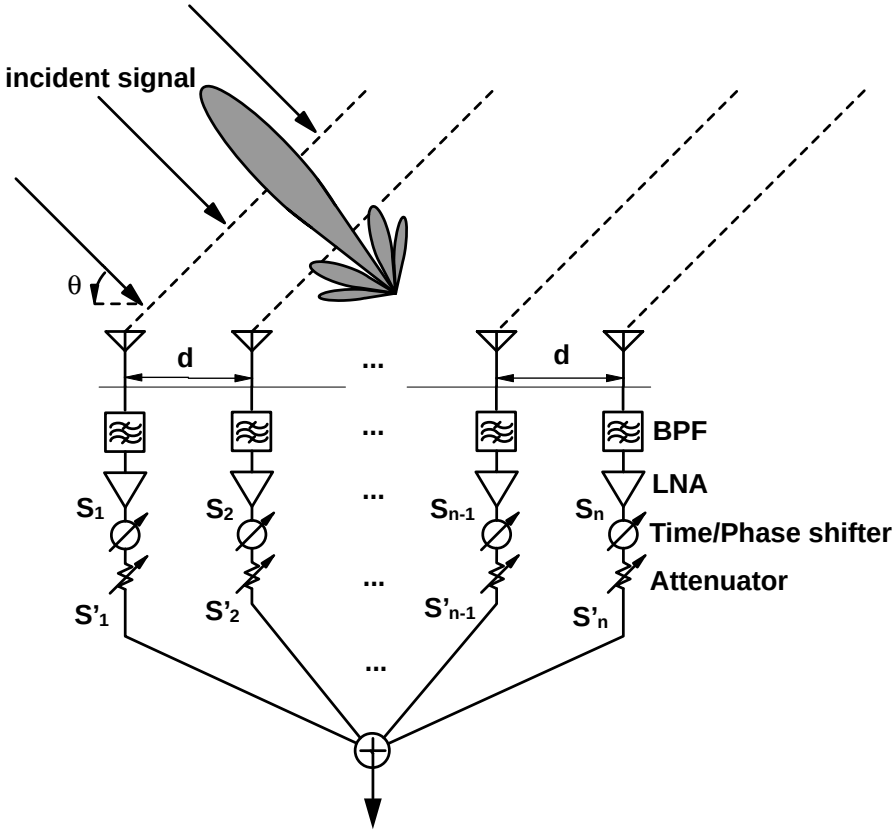


Fig. 1.1. Timed array and phased array receiver with N paths.

The antenna elements are placed apart from each other at a distance d. When an incident signal reaches an antenna element under an angle θ, the time delay at the adjacent element is $\tau = \frac{d\cos\theta}{c}$. After filtering and amplification, extra time and amplitude variations are found in the signal. Therefore, circuits for time and

amplitude compensations are required before the combiner.

The most straightforward way for the time compensation is to use time delay networks [8]. The problem, however, is the difficulty in realizing large time delays in integrated circuits, and to minimize the amplitude variation for different states. The transmission loss can be significant due to the low Q of the inductors and capacitors in MMICs. Therefore, integrated amplifiers, which limit the linearity of the circuits, need to be added into the time delay networks to compensate for the loss caused by the time delays [9], [10].

When the signal is narrow band, the time delay can be translated into a phase delay. The relation between the phase difference of the *i*th path ($1<i\leq N$) and the first path is given by:

$$\Delta\phi_i = \frac{(i-1)\,d\cos\theta}{c}\omega - 2k\pi, \quad \Delta\phi_i \in [0, 2\pi] \tag{1-1}$$

From (1-1), the time compensation of timed array becomes phase compensation between zero and 2π. This characteristic makes the implementation much easier, especially for integrated circuit design [11].

1.2 Architectures: RF, LO and IF Phase Shifting

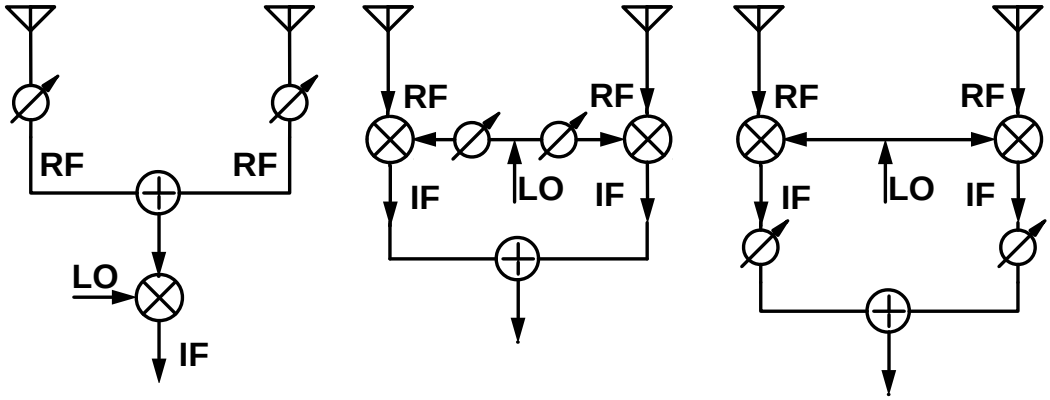
The phase shift can be implemented in the RF, LO or IF channel, which leads to three

different architectures as shown in Fig. 1.2 [12]. Note that only two adjacent paths are shown in the illustration.

The signals at the output of the mixers can be written as

$$v_{IF} = \frac{K}{2} v_{RF} v_{LO} \cos\left[\omega_{IF} t + \left(\phi_{RF} - \phi_{LO}\right)\right] \tag{1-2}$$

where K represents the conversion gain/loss of the mixer. From (1-2), the required phase shift does not change value for the three architectures.



(a) (b) (c)

Fig. 1.2. Three phased array architectures: (a) RF-channel phase shifting, (b) LO-channel phase shifting and (c) IF-channel phase shifting.

It is obvious from Fig. 1.2 that the RF-channel phase shift architecture only has one mixer while the other two architectures have N mixers for N signal paths, which may lead to a larger circuit area and a higher power consumption. However, in cases where the RF frequency is too high to obtain good passive components [13] and compact

switches [14], moving the phase shifter from the RF channel to the LO or the IF channel is an option.

1.3 Influence of Phase Error of Phase Shifters in Beam Forming

For a phased array with fixed antenna lattice, the radiation pattern is determined by the phase setting of the phase shifters and amplitude setting of the attenuators [15]. Therefore, the phase error and the amplitude imbalance between the signal paths will lead to distortion of the radiation pattern. For commonly used uniform arrays, where the power of each antenna is the same, the phase error is more critical.

As an example, a linear uniform eight-element array is considered to examine how the phase error influences the beam forming. All the eight elements have an isotropic radiation pattern. When antenna elements with other different radiation patterns are used in the array, the pattern multiplication rule can be applied [1]. In this example, a four-bit phase shifter that can provide 16 phase states with a phase step of 22.5º is used to control the direction of the beam, and the block diagram for one signal path is shown in Fig. 1.3.

Two types of phase error are considered. In the first type, the phase error *PE* of each phase state is assumed to be the same. In the second type, the *PE* is assumed to be the same in percentage of the phase shift but with an overall RMS phase error of PE_{RMS}.

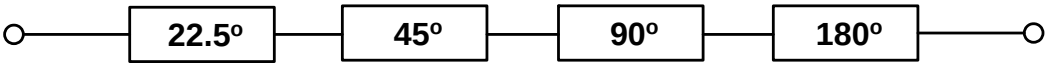


Fig. 1.3. Block diagram of the four-bit phase shifter.

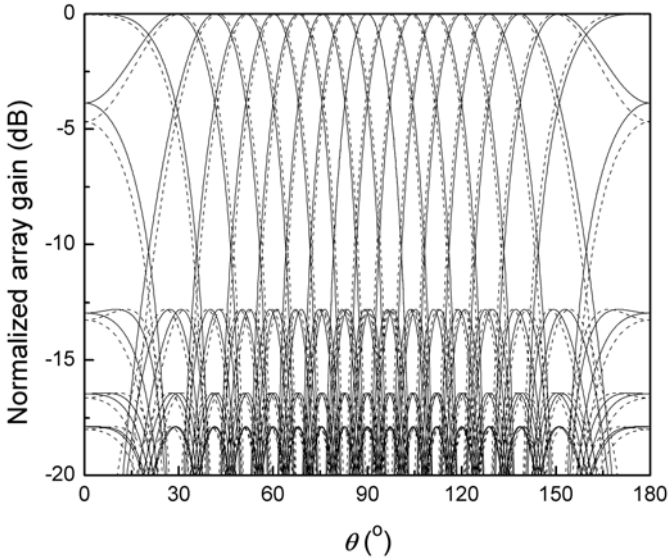


Fig. 1.4. Array gains of 16 beams of an eight-element array for fixed phase errors of 2º.

Fig. 1.4 and Fig. 1.5 show the 180º scanning range of the eight-element sub-array with fixed phase errors of 2º, and 5º, respectively. The response without phase error is also shown as a reference using solid lines. Fig. 1.6 and Fig. 1.7 show the 180º scanning range of the array with percentage phase errors and an overall RMS phase error of 2º, and 5º, respectively.

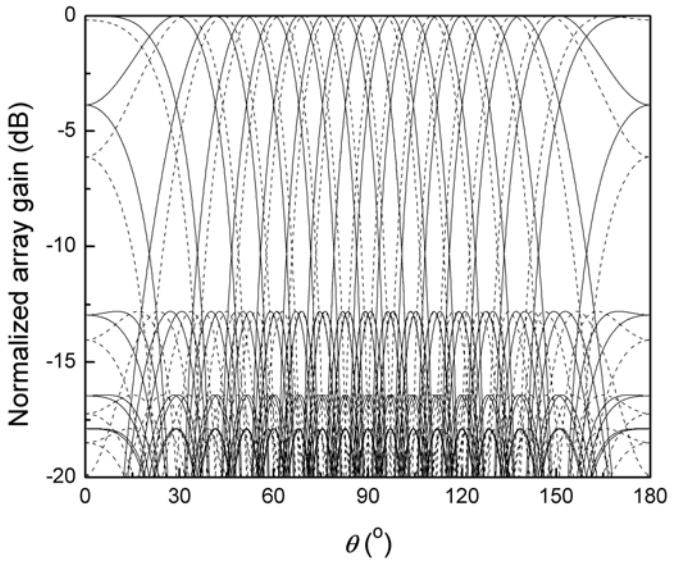


Fig. 1.5. Array gains of 16 beams of an eight-element array for fixed phase errors of 5º.

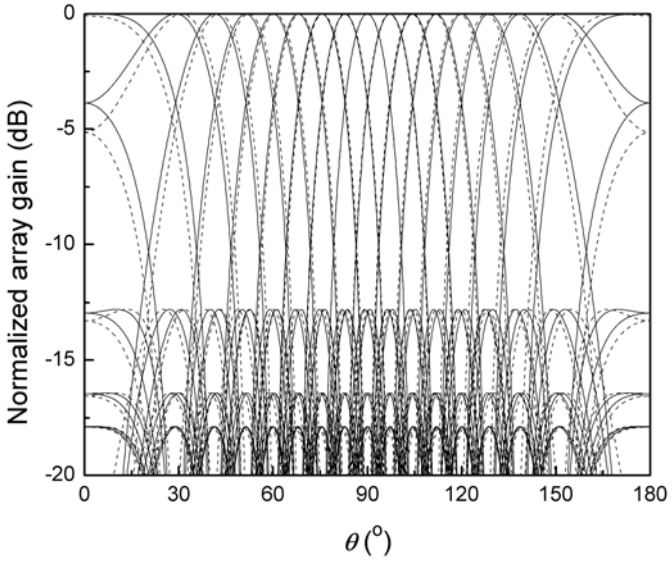


Fig. 1.6. Array gains of 16 beams of an eight-element array for a percentage phase error with RMS value of 2º.

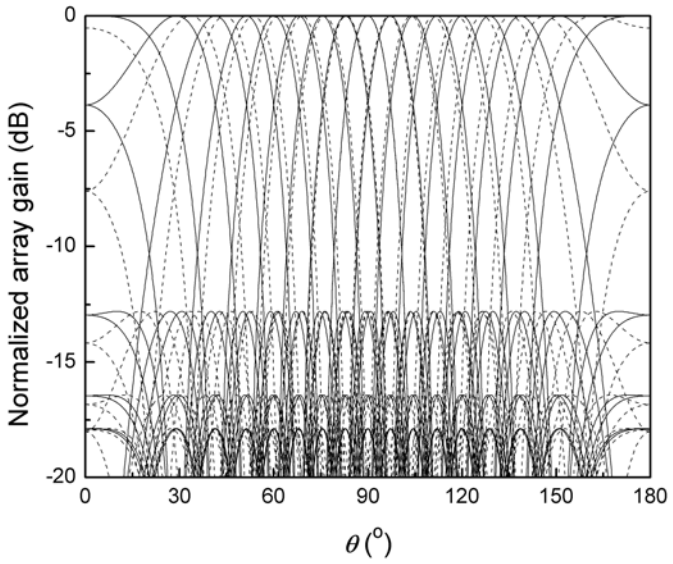


Fig. 1.7. Array gains of 16 beams of an eight-element array for a percentage phase error with RMS value of 5º.

It is obvious that a small phase error directly improves the scanning accuracy. It is also found that the percentage phase error with an RMS value less than 5º gives less beam direction error and does not influence the resolution accuracy when θ is within the range of [60º, 120º]. The same simulations are performed for a phase error of 10º, and acceptable resolution accuracy is found when θ is within the range of [75º, 115º].

For a given bandwidth, the phase error is due to the inherent phase characteristics of the topology and the parasitics of the components. It is also caused by the mismatch between the adjacent loads. The loads can be for example the SPDT switches, the adjacent phase bits or other cascaded networks. To show the effect of the mismatch, Fig. 1.8 shows a phase shifter with networks cascaded at its two ends. The reflection

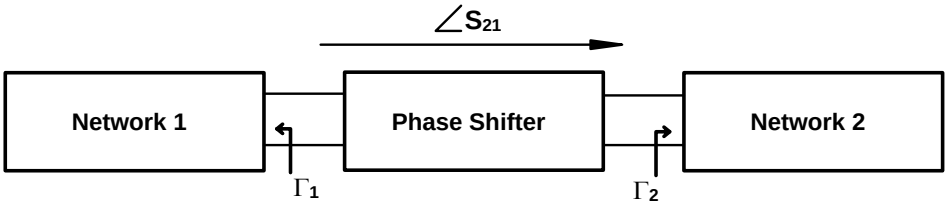


Fig. 1.8. A phase shifter and its loads at the two ends.

coefficient from network 1 is Γ_1 and the reflection coefficient from network 2 is Γ_2.

The effect of the mismatch is discussed in appendix A and is demonstrated for a particular case here. When all ports are matched, the phase shifter has a transmission coefficient of S_{21} and the insertion phase can be obtained from S_{21}. As in appendix A, the insertion phase is a function of the input and output reflection coefficients. The relations depend on the particular topologies. However, the larger the return loss, the less the phase shift will be affected. In [16], the third order high-pass/low-pass phase shifters are studied and it is found that a return loss of 10 dB results in a phase change of 5º, which causes considerable influence in beam forming as shown in Fig. 1.4. A return loss of 15 dB results in a phase change of less than 2º.

1.4 Motivation and Organization of the Thesis

The purpose of this work is to improve conventional phase shifter topologies and to develop new topologies with a small phase error and a high return loss for broadband and dual-band applications. Design tradeoffs and design procedures are considered specifically for Computer Aided Design (CAD) purposes.

The thesis consists of seven chapters. In Chapter 2, conventional phase shifter topologies are briefly reviewed. Then improvements and complementary designs for the conventional topologies are covered in Chapter 3. Chapter 4 describes a general broadband phase shifter design method using the phase slope alignment technique. Both distributed and discrete realizations and the necessary design procedures are provided. Chapter 5 uses the networks studied in Chapter 3 and Chapter 4 to design ultra-wideband quadrature and dual-band power dividers. Chapter 6 discusses another broadband approach using all-pass networks. The conclusions and recommendations are provided in Chapter 7 together with phase shifter design guidelines based on the contributions of this work.

1.5 Publications

Journal papers:

1. X. Tang and K. Mouthaan, "180° and 90° phase shifting networks with an octave bandwidth and small phase errors," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 8, pp. 506-508, Aug. 2009.
2. X. Tang and K. Mouthaan, "Phase shifter design using phase slope alignment with grounded shunt $\lambda/4$ stubs," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 6, pp. 1573-1583, Jun. 2010.
3. X. Tang and K. Mouthaan, "Compact dual-band power divider with single all-pass

coupled lines sections," *IET Electronics Lett.*, vol. 46, no. 10, pp. 688-689, May 2010.

4. X. Tang and K. Mouthaan, "Design considerations for octave-band phase shifters using discrete components," accepted in *IEEE Trans. Microw. Theory Tech.*.

5. X. Tang and K. Mouthaan, "Filter integrated Wilkinson power dividers," accepted in *Microw. Optical Tech. Lett.*.

6. X. Tang and K. Mouthaan, "Ultra-wideband quadrature power splitter," accepted in *Microw. Optical Tech. Lett.*.

Conference papers:

1. X. Tang and K. Mouthaan, "Design of dual-band Class III loaded-line phase shifters," accepted in *IEEE APMC* 2010, Yokohama, Japan.

2. X. Tang and K. Mouthaan, "Loaded-line phase shifter with enlarged phase shift range and bandwidth," accepted in *EuMC* 2010, Paris, France.

3. X. Tang and K. Mouthaan, "A broadband 180° phase shifter with a small error using lumped elements," *IEEE APMC* 2009, pp. 1315-1318, Singapore.

4. X. Tang and K. Mouthaan, "Analysis and design of compact two-way Wilkinson power dividers using coupled lines," *IEEE APMC* 2009, pp. 1319-1322, Singapore.

5. X. Tang and K. Mouthaan, "Design of a UWB phase shifter using shunt λ/4

stubs," *IEEE MTT-S (IMS) 2009*, pp. 1021-1024, Boston, USA.

6. X. Tang and K. Mouthaan, "A novel broadband 90° phase shifter," *IEEE APMC* 2008, pp. 1-4, Hong Kong.

7. X. Tang and K. Mouthaan, "A 180° phase shifter with small phase error for broadband applications," *IEEE EDSSC* 2007, pp. 997-1000, Taiwan.

Chapter 2

Review of Conventional Phase Shifters

Phase shifters have been developed for phased array antennas for more than half a century [17]. Generally, there are three types of phase shifters: mechanical phase shifters, ferrite phase shifters and semiconductor device phase shifters. In this thesis, only electrical planar phase shifters switched by semiconductor devices are covered.

2.1 Topologies to Achieve Phase Shifts

An ideal phase shifter is a two-port device whose insertion phase can be changed while its insertion loss remains the same. Assume the reference state has an insertion phase of ϕ_1, and the phase shifting state has an insertion phase of ϕ_2, the phase shift $\Delta\phi$ is the phase difference between the two states, which is given by

$$\Delta\phi = \phi_2 - \phi_1 \tag{2-1}$$

Normally, for phase shifters with multiple phase states the phase shifts all refer to one reference phase state. In the following, four commonly used types of phase shifter

topologies are reviewed: loaded-line phase shifters, switched network phase shifters, reflection type phase shifters and vector summation phase shifters.

2.1.1 Loaded-line Phase Shifter

The concept of the loaded-line phase shifters is to use the loads to change the electrical length of a fixed transmission line. And therefore, it is a transmission type phase shifter. The prototype is shown in Fig. 2.1.

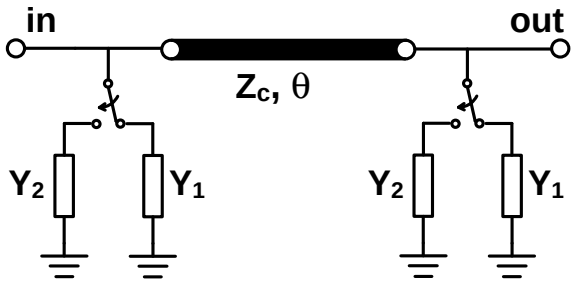


Fig. 2.1. Loaded-line phase shifter prototype.

The loads inserted at the two ends of the transmission line can be controlled digitally to change the electrical length of the center line with impedance of Z_c and original electrical length of θ. In an analog phase shifter, the loads are controlled continuously, however, the perfect matching may not be always met. Here we are discussing a binary phase shifter with two possible load states: Y_1 and Y_2. When the loss of the loads is neglected, the insertion phase ϕ_i (i=1, 2) can be obtained from [18]:

$$\phi_i = arc\cos\left(\cos\theta - \frac{Y_i}{Z_c}\sin\theta\right) \tag{2-2}$$

Therefore, when Y_1 changes to Y_2, the phase shift can be obtained from (2-1). Based on this prototype, the analysis for different loads and switching components are provided in detail in [19]-[23]. Three different classes with nonzero and unequal loads (Class I), load-unload loads (Class II) and complex-conjugate loads (Class III) are concluded in [23]. It is found that the loaded line phase shifter has the largest bandwidth and perfect matching at the center frequency for Class III when the original electrical length of θ is around 90º. The design parameters can be obtained from

$$Z_c = \cos\left(\frac{\Delta\phi}{2}\right)Z_0 \tag{2-3}$$

$$Y_i = \pm\tan\left(\frac{\Delta\phi}{2}\right)Y_0, \quad i = 1,2 \tag{2-4}$$

It is noted that this topology cannot be used for 180º phase shifters due to the extreme values from (2-4). When the design parameters are obtained, the return loss and phase error can be written as a function of the normalized frequency. Therefore, the return loss bandwidth (BW_{RL}) and phase error bandwidth (BW_{PE}) are related to the phase shift values. The relations for Class III loaded-line phase shifters with discrete loads are plotted in Fig. 2.2 for phase shift ranges from 5º to 120º.

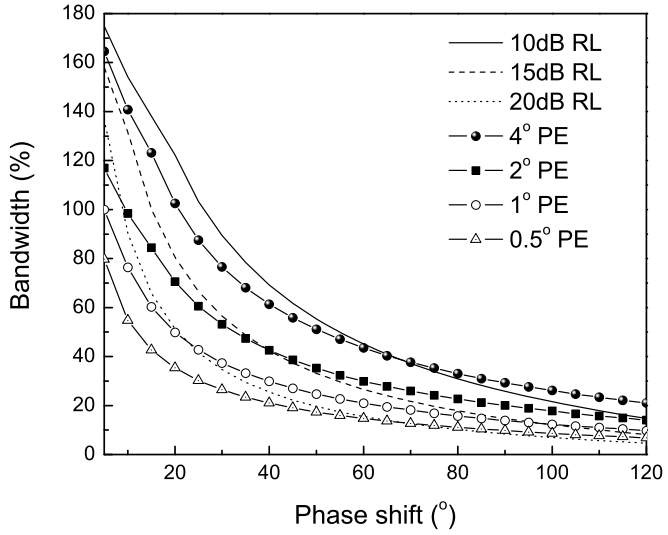


Fig. 2.2. Bandwidth versus the phase shifts for different phase errors and return losses of the lumped element loaded Class III phase shifters.

From Fig. 2.2, the overall bandwidth of the loaded-line phase shifter is mainly limited by the return loss when the required phase shift increases. For example, when the phase shift is 90º, the 4º (±2º) phase error bandwidth BW_{PE} is 35% while the 15 dB BW_{RL} is 14%, and the overall bandwidth is limited to 14% when the required return loss is 15 dB.

Besides high power applications, this prototype is also preferred for high frequency designs due to its simple structure. Recently, several millimeter wave designs using MEMS switches were presented [24]-[26].

2.1.2 Switched Network Phase Shifter

The switched network phase shifter is another type of transmission phase shifter. The development in this type of phase shifter is very active because the number of network combination is numerous.

Common switched network phase shifters switch between different passbands of different networks to obtain the phase difference as shown in Fig. 2.3.

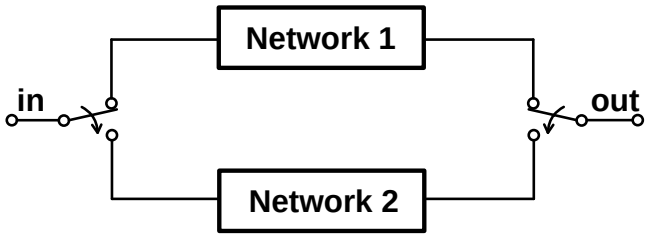


Fig. 2.3. Schematic of the switched network phase shifters.

Here, two popular used topologies are reviewed: the high-pass/low-pass phase shifter and the all-pass network phase shifter, which includes the Schiffman phase shifter.

High-pass/low-pass (HP/LP) phase shifter

The HP/LP phase shifter switches between high-pass filters and low-pass filters. A typical third order HP/LP phase shift bit is shown in Fig. 2.4. The T-network is chosen for the HP filter and the π-network is chosen for the LP filter to minimize the number of inductors used.

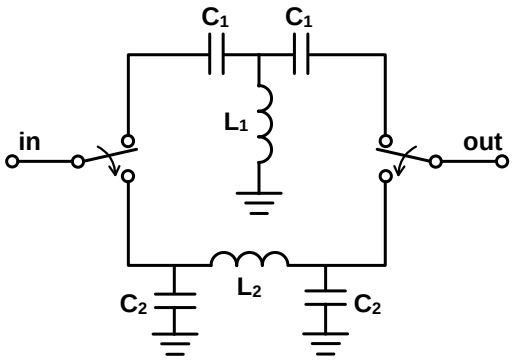


Fig. 2.4. Third order high-pass/low-pass phase shifter.

Design parameters can be obtained from [27], [28] for the T-network and π-network for a given center frequency ω_0 and desired phase shift $\Delta\phi$ at ω_0. For smaller phase shifters, larger inductors are needed for the high-pass filter using this topology. The insertion loss is affected by the parasitcis, the matching from the adjacent phase bits [16] and the two SPDT switches used in one phase bit [28]-[30]. For millimeter wave designs, semiconductor based SPDT switches suffer from a high insertion loss and poor isolation. The traveling wave concept can be adopted in the design of SPDT switches but the circuit size can be significant [31]-[33].

To minimize the circuit area and to extend the bandwidth, the parasitics of the switching components are absorbed rather than avoided in the FET-integrated designs. The ON state of the FET can be modeled by a small resistor and the OFF state of the FET can be modeled by a small capacitor as shown in Fig. 2.5.

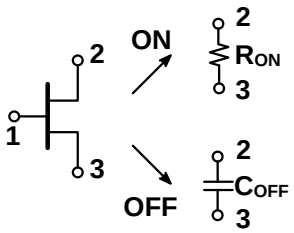


Fig. 2.5. Modeled ON and OFF state of the FET.

In [34]-[39], this methodology is used for phase shifter implementation and a bandwidth of nearly an octave is achieved in [39]. When more stages of HP/LP networks are used, larger bandwidth can be realized.

This topology is also popular in microwave systems where large phase shifts are required. Examples using the HP/LP circuits to provide the required phase difference include the TX-RX switches with leakage cancelation [40] and the broadband multi-port direct receiver [41].

All-pass network phase shifter

Another popular phase shifter switches between all-pass networks. In [42] a single stage four-element all-pass network to achieve a bandwidth ratio of 1.6:1 is presented.The two topologies of the all-pass networks shown in Fig. 2.6 share the same performance when the values satisfy:

$$LC = \frac{1}{\omega_0^2}, \quad \frac{L}{C} = Z_0^2 \tag{2-5}$$

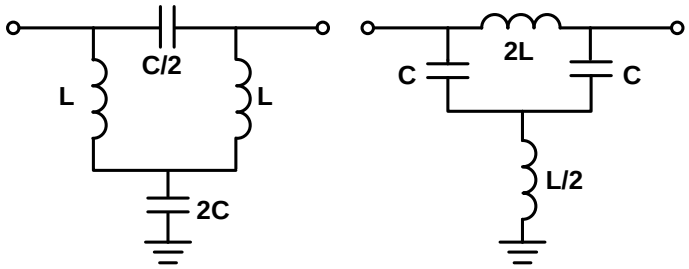


Fig. 2.6. Two four-element all-pass networks. (after [42])

where ω_0 is the transition frequency where the insertion phase is -180º and Z_0 is the characteristic impedance of the system. The phase shift can be obtained by changing ω_0 of two all-pass networks and a phase shift peak will be obtained for each setting. The advantage of the all-pass network is that the insertion phase can be treated separately due to the very high return loss. Therefore, when two stages are cascaded, two peaks in the phase response can be obtained to get a phase shift ripple and the bandwidth can be significantly improved. For the two-section phase shifter, the bandwidth ratio increases to 4:1 for the same performance of the single-section phase shifter [42].

Besides the large bandwidth applications, the all-pass network is also used in compact integrated circuit designs. Like the HP/LP topologies, FETs can be integrated into the circuits to minimize the circuit area. The transition frequency can be shifted much higher than the designed frequency and therefore the parameter values are smaller [43].

Furthermore, the capacitors in both the HP/LP phase shifters and the lumped all-pass

network phase shifters can be changed to varactors to realize continuous phase tuning [44], [45].

The Schiffman phase shifter

The all-pass network based phase shifter can also be realized in distributed form. Schiffman presented a topology based on a carefully designed coupled line and a transmission line [46]. The design theory is synthesized in [47] and a phase error of ±2º is achieved for a 90º phase shift over a bandwidth of 60%. However, it is assumed that the even- and odd-mode velocities of the RF signal are the same in the original design. Therefore, the topology was implemented in striplines. For microstrip lines, the Schiffman phase shifter needs to be modified to maintain the bandwidth [48], [49].

2.1.3 Reflection Type Phase Shifter

The reflection type phase shifters consist of two parts: a 3-dB directional coupler and two tunable terminations. As shown in Fig. 2.7, the input signal is first split into two parts, and then reflected by the two loads. When the loads are the same, the voltage at the output port can be written as [50]:

$$V_{out} = j\Gamma V_{in} \tag{2-6}$$

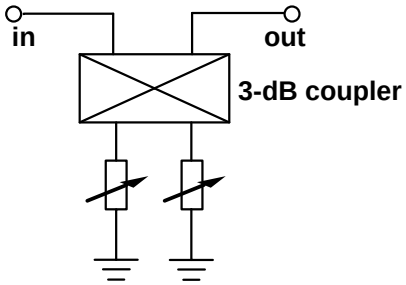


Fig. 2.7. Reflection type phase shifter prototype.

Compared with the transmission phase used in the transmission type phase shifters, reflection type phase shifters transform the reflection coefficient phase to the transmission phase first, and the phase shift is calculated from (2-1). When the power is fully reflected from the loads, the insertion loss is minimized.

The bandwidth of the reflection type phase shifter is determined by both the coupler and the terminations. For example in [51], broadband terminations are used, but the slot fin-line coupler limits the bandwidth to 15% only. The reported bandwidth using a branch line coupler is from 20% to 25% [52], [53]. In [54], it is claimed that the isolation and the return loss of the coupler influence the phase shifter performance, and ±3% to ±4% phase errors are achieved for a bandwidth ratio larger than 5 by using Lange couplers. Lange couplers can provide a large bandwidth and the bandwidth of the phase shifter is then limited by the terminations [55].

Because couplers are used, the circuit size increases especially for the digital designs [51]-[55]. Therefore, to reduce the number of cascaded phase bits, continuous tuning is proposed to cover small phase shifts to reduce the insertion loss and circuit size. In

[56], parallel series resonators are used as the reflective terminations and in [57] and [58], cascaded reflection type phase shifters with a phase shift peak summation methodology are used to achieve an analog phase shift over 100% bandwidth.

The problem for broadband analog reflective phase shifters is achieving a large phase shift range. To achieve 360º phase coverage, more stages are required which immediately degrades the performance. Research has been done to increase the phase coverage for a single section reflective phase shifter. However, the bandwidth is reduced. In [59], an impedance-transforming branch line coupler is used together with transformer integrated terminations and a full 360º phase shift is achieved. In [60] and [61], the circuit size is further reduced by implementing the coupler using lumped elements. As a tradeoff, the bandwidth reduces to 10% to 15%.

2.1.4 Vector Based Phase Shifter

The vector based phase shifter first generates base vectors, and then combines the vectors with different amplitude weights to achieve different phase shifts. The concept is shown in Fig. 2.8.

The commonly used phase difference between the vectors can be around 90º where four vectors are needed [62]-[67], or around 120º where three vectors are needed [68], [69]. The 90º phase difference is mainly realized using combiners, directional couplers, polyphase filters [70], and all-pass networks [71], and the 120º phase differ-

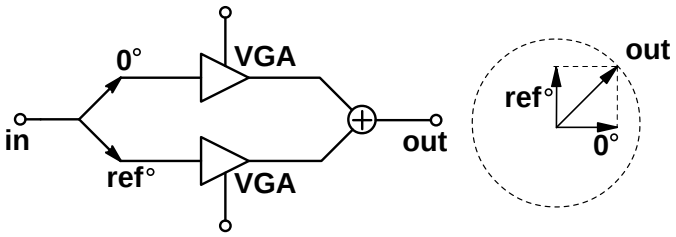


Fig. 2.8. Basic concept of the vector based phase shifters.

ence is mainly realized using HP/LP filters and all-pass networks. The main advantage of the vector based phase shifter is the potential for a small circuit size. For most vectors generated by polyphase filters, the amplitude variation is a concern. Usually the phase bandwidth is much larger than the return loss bandwidth. The phase shift response is quite smooth over a multi-octave band while the return loss is around an octave or less [66], [67]. For vectors generated by passive networks, the performance of the phase shifter still relies on the transmission phase response of the networks discussed in Section 2.1.2.

Another concern is the power consumption, power handling capability, and linearity of this type of phase shifters. Compared to the conventional phase shifter designs, the vector based phase shifter uses VGAs and DACs to control the weight of the vectors, which consume extra power of the circuits.

2.2 Conclusions

In the past, various phase shifter topologies were developed with different emphasis: to minimize the circuit area, to maximize the operation bandwidth, to minimize the

insertion loss and its variation, etc. This chapter reviews four most important phase shifters including the loaded-line phase shifter, the switched network phase shifter, the reflection type phase shifter and the vector based phase shifter.

The loaded-line phase shifter has the narrowest bandwidth and the other three types can have comparable bandwidth. However, the loaded-line topology has promising performance for millimeter wave implementations because of its simple structure.

The design flexibility of the switched network phase shifters is quite high as various types of high-pass, low-pass, band-pass and all-pass networks can be used in the design. For low frequency designs, the lumped elements can be used and for high frequency designs, the distributed networks can be used.

The reflection type phase shifter can achieve a large bandwidth. However, it is not a good option for low frequency designs or extremely high frequency designs. For low frequency designs, the broadband coupler consumes a large area. For high frequency design up to 80 GHz, the Lange coupler is difficult to implement due to the extremely narrow lines required and the associated high loss. Branch line couplers can be used for high frequency designs. However, the broadband characteristics of the reflection type phase shifter are eliminated.

The vector based phase shifter can be used for low frequency and high frequency designs and may lead to very compact circuits. The power consumption and the linearity should also be considered. Up to the date of this thesis, the largest bandwidth

reported for a vector based phase shifter is more than an octave considering both phase and return loss [66]. The highest frequency is a 40-45 GHz design presented in [72].

Compared to other microwave devices like filters, phase shifter designs are not flexible enough to easily adjust to different specifications. Only the Schiffman phase shifter and the broadband reflection type phase shifter are able to change the design parameters for different bandwidth requirements to achieve the optimum performance. Further study on the phase shifters are required for customized designs.

Chapter 3

Improvement of Conventional Phase Shifters

In this chapter, several approaches to improve the conventional HP/LP phase shifter topology and the loaded-line phase shifter topology, reviewed in Chapter 2, are discussed. The improvements provide more design flexibility and larger bandwidths compared to the original method. The improvements of the loaded-line phase shifter also facilitate dual-band designs.

3.1 Optimized Design for the Third Order HP/ LP Phase Shifter

The HP/LP topology is shown in Fig. 3.1 (a). The T-topology is chosen for the HP network and the π-topology is chosen for the LP network to minimize the number of inductors. The corresponding insertion loss and insertion phase of the two networks are shown in Fig. 3.1 (b). General design formulas are introduced first for the component values and the insertion phases as a function of frequency for the two networks. Then, the conventional design method and a new design method, which includes the conventional method as a special case, are analyzed. Considerations on the bandwidth, the return loss and the phase error will also be covered.

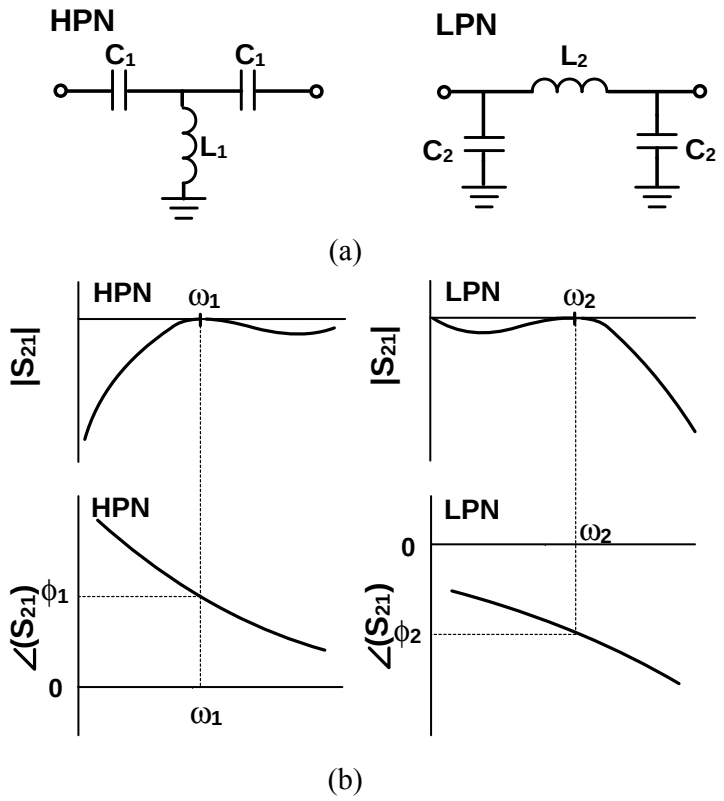


Fig. 3.1. (a) Topology of HP and LP network; (b) corresponding insertion loss and insertion phase response.

Throughout this section, the following symbols are used:

ω_1 Resonant frequency of the HP network

ω_2 Resonant frequency of the LP network

ω_0 Center frequency

ϕ_1 Insertion phase of the HP network at ω_1

ϕ_2 Insertion phase of the LP network at ω_2

$\Delta\phi$	Phase difference between the HP and the LP network
$\Delta\phi_r$	Required phase shift at ω_0
PE	Phase error, which is defined as $\Delta\phi-\Delta\phi_r$
AI	Amplitude imbalance between the two networks

For the two networks, when ω_1, ω_2, ϕ_1 and ϕ_2 are provided, the element values can be calculated from the general equations:

$$L_1 = \frac{Z_0}{\omega_1 \sin(\phi_1)} \tag{3-1}$$

$$L_2 = \frac{Z_0 \sin(-\phi_2)}{\omega_2} \tag{3-2}$$

$$C_1 = \frac{1}{\omega_1 Z_0 \tan(\phi_1/2)} \tag{3-3}$$

$$C_2 = \frac{\tan(-\phi_2/2)}{\omega_2 Z_0} \tag{3-4}$$

And the corresponding insertion phase of the two networks, as a function of frequency, is derived as:

$$\phi_{HP}(\bar{\omega}) = \tan^{-1}\left[\frac{\bar{\omega}_1 \tan\left(\frac{\phi_1}{2}\right)}{2\bar{\omega}} \cdot \frac{3\frac{\bar{\omega}^2}{\bar{\omega}_1^2} - 1 + \left(\frac{\bar{\omega}^2}{\bar{\omega}_1^2} + 1\right)\cos(\phi_1)}{\frac{\bar{\omega}^2}{\bar{\omega}_1^2} - 1 + \cos(\phi_1)}\right] \tag{3-5}$$

$$\phi_{LP}(\bar{\omega}) = \tan^{-1}\left[\frac{\bar{\omega}\tan\left(-\frac{\phi_2}{2}\right)}{2\bar{\omega}_2}\cdot\frac{\frac{\bar{\omega}^2}{\bar{\omega}_2^2}-3-\left(\frac{\bar{\omega}^2}{\bar{\omega}_2^2}+1\right)\cos(\phi_2)}{1-\frac{\bar{\omega}^2}{\bar{\omega}_2^2}+\frac{\bar{\omega}^2}{\bar{\omega}_2^2}\cos(\phi_2)}\right] \tag{3-6}$$

where $\bar{\omega} = \omega/\omega_0$. It is noted that the high-pass network has a positive insertion phase and the low-pass network has a negative insertion phase.

In the conventional design method [27], [28], it is assumed that the high-pass network and the low-pass network are resonant at the same frequency, i.e.:

$$\bar{\omega}_1 = \bar{\omega}_2 = \bar{\omega}_0 = 1 \tag{3-7}$$

To achieve the desired phase shift $\Delta\phi_r$, the insertion phase of the high-pass network and the low-pass network are given by:

$$\phi_1 = -\phi_2 = \Delta\phi_r/2 \tag{3-8}$$

The values of the components can be obtained by substituting (3-7) and (3-8) into (3-1) to (3-4). It is clear that there are only two design parameters in the conventional method: the center frequency ω_0 and the required phase shift $\Delta\phi_r$ at ω_0. Once these two parameters are set, no tradeoffs, for example between phase error and bandwidth, are possible. Therefore, the design flexibility is limited in this method. With (3-7) and (3-8), it is observed from (3-5) and (3-6) that:

$$\phi_{HP}(\bar{\omega}) = -\phi_{LP}\left(\bar{\omega}^{-1}\right) \tag{3-9}$$

And the phase shift is given by:

$$\Delta\phi(\bar{\omega}) = \phi_{HP}(\bar{\omega}) - \phi_{LP}(\bar{\omega}) \tag{3-10}$$

By substituting (3-9) into (3-10), it follows that

$$\Delta\phi(\bar{\omega}) = \Delta\phi\left(\bar{\omega}^{-1}\right) \tag{3-11}$$

Equation (3-11) shows the logarithmic symmetry around ω_0 of the phase shift in the conventional high-pass/low-pass method. Therefore, for a given frequency band from ω_L to ω_H, the center frequency that is used to obtain the component values from (3-1)-(3-4) should be

$$\omega_0 = \sqrt{\omega_L \cdot \omega_H} \tag{3-12}$$

With this choice, the phase error within the frequency band from ω_L to ω_H is the minimum achievable phase error. And the bandwidth is then defined by

$$BW = (\bar{\omega}_H - \bar{\omega}_L) \times 100\% \tag{3-13}$$

For an octave bandwidth where $\omega_H=2\omega_L$, by using (3-12) and (3-13), $\bar{\omega}_L = \sqrt{2}^{-1}$, $\bar{\omega}_H = \sqrt{2}$, and the bandwidth is 70.7%

To increase the design flexibility, the resonant frequency ω_1 of the high pass network and ω_2 of the low-pass network are shifted. This provides more design parameters, instead of the two in the conventional method.

The logarithmic symmetry of equation (3-11) still holds when the following conditions are satisfied:

$$\bar{\omega}_1 \cdot \bar{\omega}_2 = \bar{\omega}_0^2 = 1 \tag{3-14}$$

$$\phi_1 = -\phi_2 \tag{3-15}$$

Therefore, different combinations of $\bar{\omega}_1$, $\bar{\omega}_2$, ϕ_1, and ϕ_2 can be used to realize a phase shift of $\Delta\phi_t$ at ω_0.

As an example, in Fig. 3.2 the phase response for the case $\bar{\omega}_1 = 1/\bar{\omega}_2 = 0.2$ is shown, and the conventional case $\bar{\omega}_1 = \bar{\omega}_2 = 1$ is also shown. After the resonant frequencies are shifted, the insertion phase ϕ_1 at $\bar{\omega}_1$ must be determined to maintain the required phase shift $\Delta\phi_t$ at ω_0. Fig. 3.3 shows the insertion phase ϕ_1 as a function of $\bar{\omega}_1$ for binary phase shifts of 22.5º, 45º, 90º and 180º. Once ϕ_1 is obtained from Fig. 3.3 for a given $\bar{\omega}_1$, $\bar{\omega}_2$ and ϕ_2 can be calculated from (3-14) and (3-15). Then the component values are obtained from (3-1) to (3-4) again. Fig. 3.4 provides three examples to achieve the same phase shift of 90º at ω_0. From Fig. 3.4 it is observed that decreasing $\bar{\omega}_1$ leads to a smaller phase error. Although $\bar{\omega}_1 = 0.2$ provides the smallest phase error, it has the worst return loss, as will be discussed later.

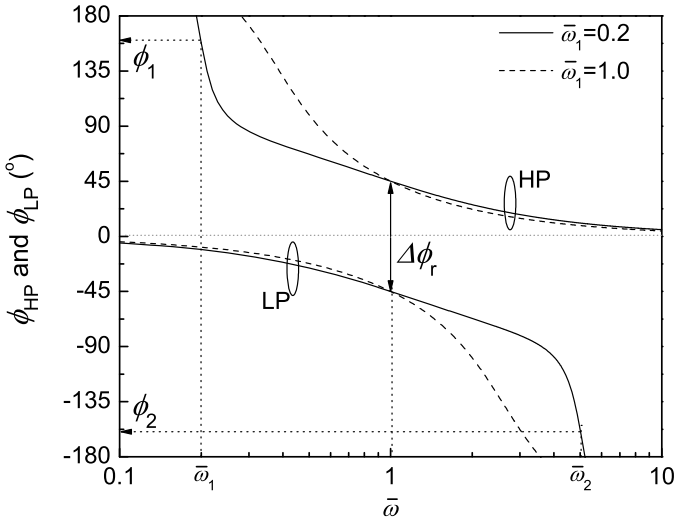


Fig. 3.2. Example of obtaining the same phase shift at ω_0 with different ω_1.

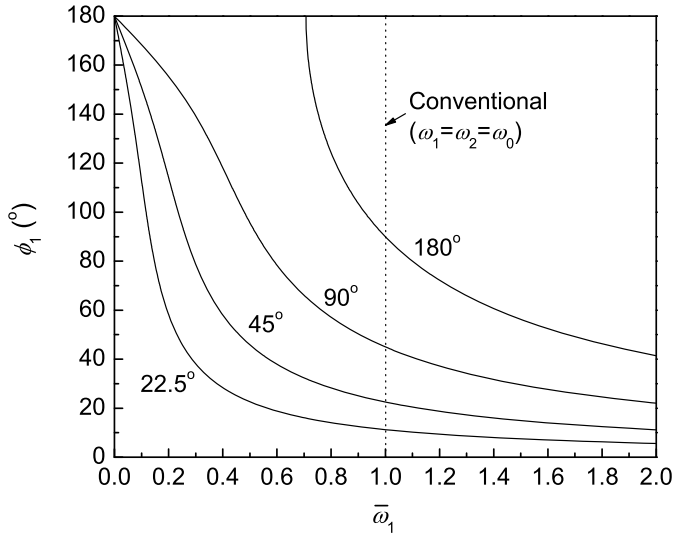


Fig. 3.3. Insertion phase of the high-pass filter versus resonant frequency ω_1 for desired phase shift of 22.5º, 45º, 90º and 180º at ω_0.

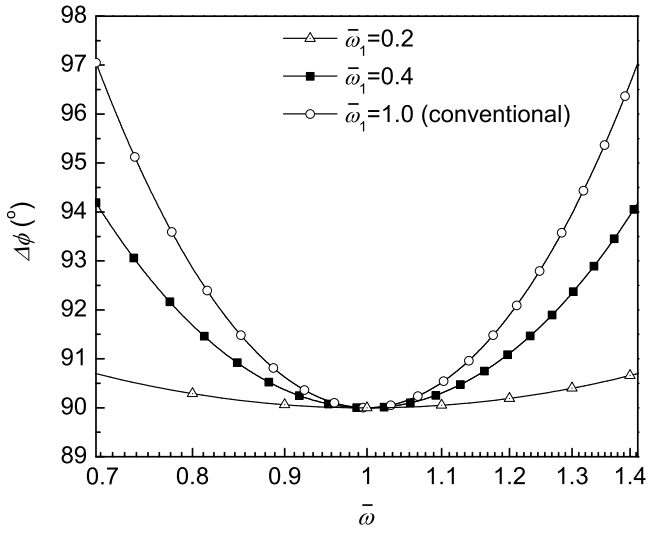


Fig. 3.4. Examples for different resonant frequency ω_1. They all have a phase shift of 90º at ω_0.

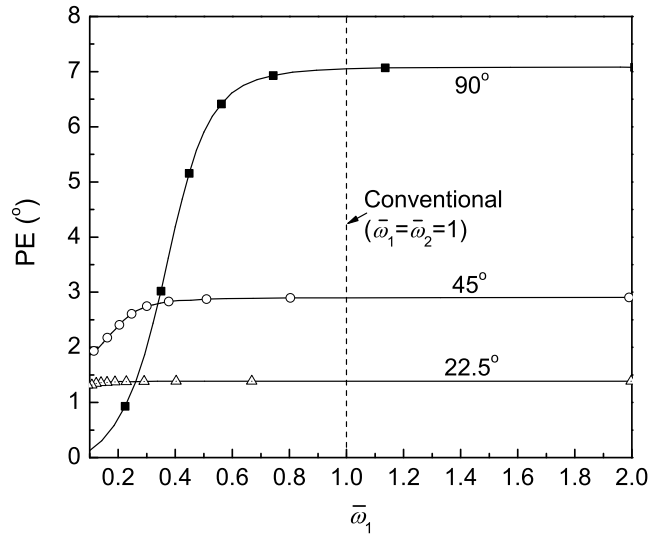


Fig. 3.5. Phase error as a function of ω_1 for a phase shift of 22.5º, 45º and 90º with an octave bandwidth.

The phase error of different phase bits of an octave bandwidth is then shown in Fig. 3.5 versus $\bar{\omega}_1$. The result of the conventional method where $\bar{\omega}_1 = \bar{\omega}_2 = 1$ is also included in the figure.

For phase shifter design, another critical specification is the return loss. Not only because it affects the overall return loss of a multi-bit phase shifter, but also because it affects the phase errors [28]. As shown in Fig. 3.6, when $\bar{\omega}_1$ is decreased, the maximum bandwidth for a given return loss is achieved when the return loss at the boundary frequencies $\bar{\omega}_L$ and $\bar{\omega}_H$ is equal to the lowest return loss between the two boundaries. Therefore, for a given bandwidth, the return loss can be optimized by shifting $\bar{\omega}_1$. Both the optimized return loss and the bandwidth are plotted as a function of $\bar{\omega}_1$ in Fig. 3.7 for the different phase bits. Note that the relation between the bandwidth and $\bar{\omega}_1$ is independent of the phase shifts. For an octave bandwidth, we derive $\bar{\omega}_1 = 0.8618$ from Fig. 3.7, and the resulting return loss is 63 dB, 45 dB and 27 dB for the 22.5º, 45º and 90º phase bits, respectively. For the 180º phase bit, the return loss is only 4.5 dB, which cannot be used in multi-bit phase shifter design.

When $\bar{\omega}_1$ decreases, both phase error and return loss are improved within a given bandwidth compared to the original design. If the required return loss is large, however, $\bar{\omega}_1$ cannot be small and the improvement on phase error is not significant.

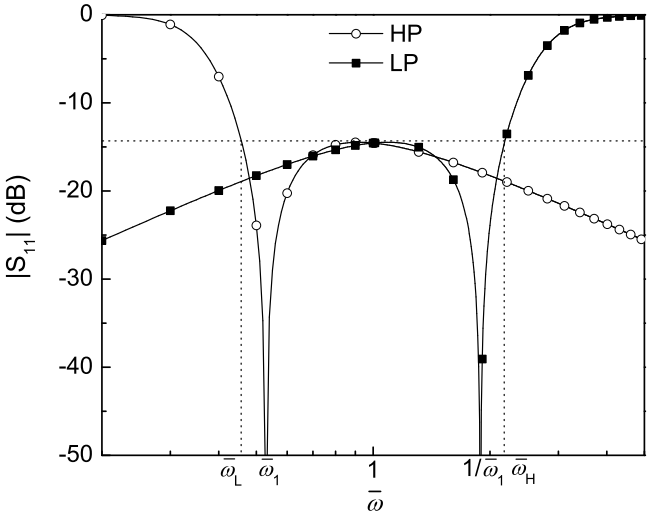


Fig. 3.6. Return loss bandwidth of the resonant frequency shifted HP/LP phase shifter topology.

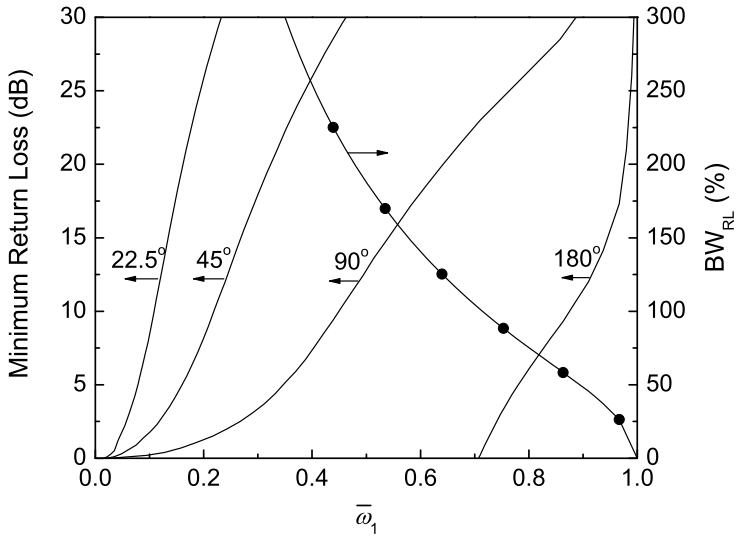


Fig. 3.7. Achievable optimum return loss within a specific BW_{RL} for phase shift of 22.5º, 45º, 90º and 180º.

To conclude, the phase error and the return loss of the third order high-pass/low-pass filter phase shifter can be improved simultaneously by shifting the resonant frequency of the two filters. However, this improvement mainly works for phase bits less than 90º when the return loss is considered.

An experiment is done to verify the improvement. The details will be discussed in Section 4.2 together with a lumped 180º phase bit.

3.2 Third Order High-pass/ Transmission Line (HP/TL) Phase Shifter

As shown in Fig. 3.1, to achieve the phase shift, the LP filter provides phase delay while the HP filer provides the phase advance. The difference in the phase flatness increases the phase error when the bandwidth gets larger. To reduce the phase error, the LP filter can be changed to a transmission line (TL) to obtain a flatter insertion phase. The topology is shown in Fig. 3.8.

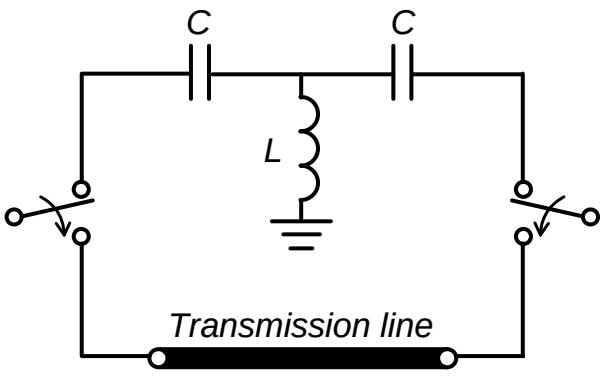


Fig. 3.8. Topology of high-pass and transmission line network.

When the TL is short, a third order LP filter can mimic the insertion phase of TL well, and the improvement on the phase error is not significant. Therefore, only the 180º phase bit is discussed in this section. The length of the TL is quarter-wavelength at the center frequency.

The insertion phase of the TL is given by

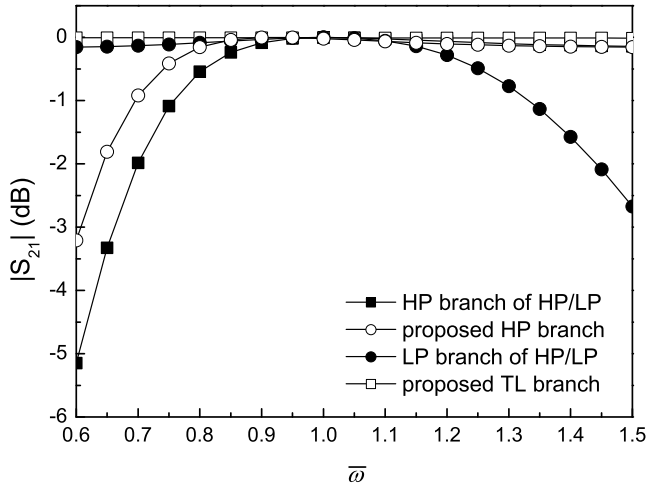
$$\phi_{TL} = \left(-\frac{\pi}{2}\right)\bar{\omega} \tag{3-16}$$

When $\bar{\omega} = 1$, *i.e.* $\omega=\omega_0$, we have $\phi_{HP} - \phi_{LP} = \phi_{HP} - \phi_{TL} = \Delta\phi_r$.

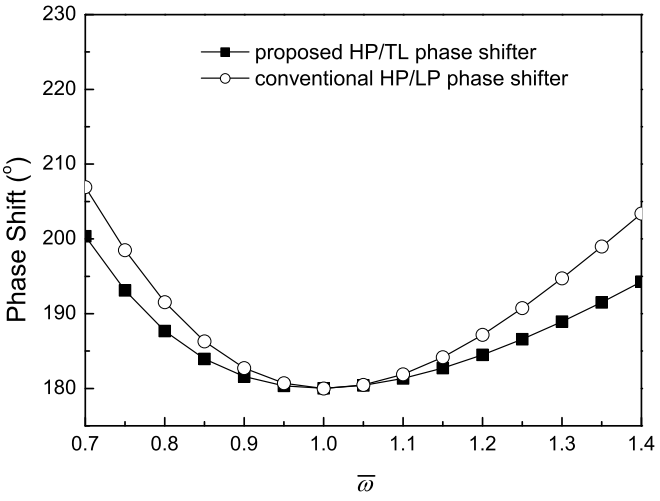
When $\bar{\omega}$ is between 1 and 2.38, we have

$$\phi_{HP} - \phi_{LP} \geq \phi_{HP} - \phi_{TL} \tag{3-17}$$

In this case, the HP/TL shifter has a phase error smaller than the HP/LP topology. Fig. 3.9 illustrates the simulated response of a HP/TL 180º phase shifter compared to the HP/LP phase shifter. The slopes of the two branches of the HP/LP phase shifter are tangential at frequency $\bar{\omega}$=1, which means the phase error is the minimum at this frequency. However, for the HP/TL phase shifter, this tangential frequency is $\bar{\omega}$=1.086. Thus, to optimize the phase error, the normalized frequency for the proposed phase shifter is slightly shifted down to 0.92 (1/1.086). This also leads to the phase error improvement when $\bar{\omega}$ is less than 1.



(a)



(b)

Fig. 3.9. Comparison between HP/LP and HP/TL phase shifters: (a) insertion loss and (b) differential phase.

From Fig. 3.9, it can be observed that both the amplitude imbalance and the phase error of the proposed phase shifter have been improved compared to the conventional HP/LP phase shifter over a broader bandwidth. As mentioned previously, the center frequency of the HP branch is slightly shifted down in the proposed phase shifter, which causes the difference in insertion loss of the two HP branches shown in Fig. 3.9 (a). The simulated phase errors of the proposed HP/TL phase shifter are 4º, 7º and 9º when the bandwidth is 33.7%, 45% and 50%, respectively.

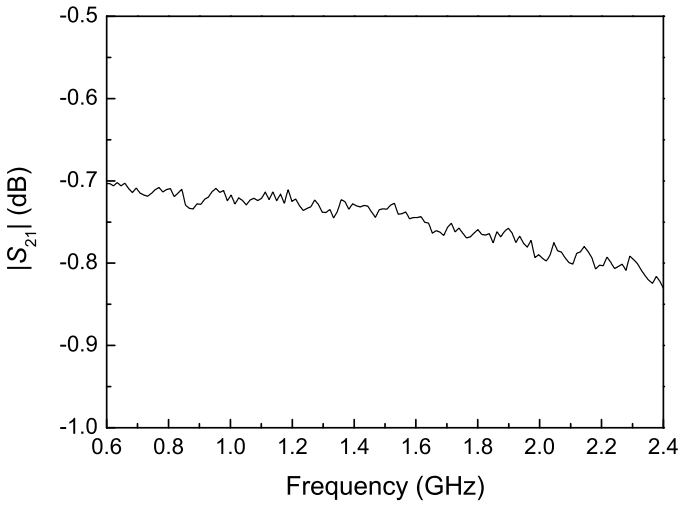


Fig. 3.10. Measured insertion loss of a single SPST switch.

To verify the topology, a 180º phase shifter was designed from 800 MHz to 1400 MHz using the proposed topology. MuRata capacitors and inductors were soldered on the Rogers 5880 (ε_r=2.2, tanδ=0.0012). To switch between the two branches, four broadband SPST switches (Hittite HMC550) covering the whole frequency band are utilized. As shown in Fig. 3.10, the switches have a measured insertion loss of around

0.75 dB over the designed frequency band. In Fig. 3.11, a photograph of the designed phase shifter is shown.

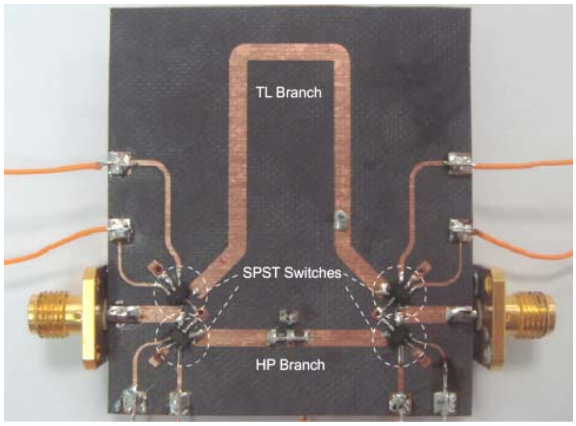


Fig. 3.11. Photograph of realized 180º phase shifter.

The measured phase shift, insertion loss and return loss of this phase shifter are shown in Fig. 3.12 to Fig. 3.15. The measured result is compared to simulations in Fig. 3.12. It shows a phase shift of 179.7º ± 2º over a frequency band from 888 to 1224 MHz (31.8%), 181.2º ± 3.5º from 843 to 1310 MHz (43.4%) and 182.2º ± 4.5º from 815 to 1349 MHz (49.3%). Fig. 3.13 presents the insertion loss of the two states of the phase shifter inclusive of the insertion loss of the two switches. The worst amplitude imbalance is 0.4 dB at the 843 MHz due to the characteristics of the high-pass filter. When frequency increases, the observed amplitude imbalance is only 0.1 dB. Fig. 3.14 and Fig. 3.15 show the input and output return loss of the two states of this phase shifter; all measured return losses are larger than 17 dB from 843 MHz to 1310 MHz.

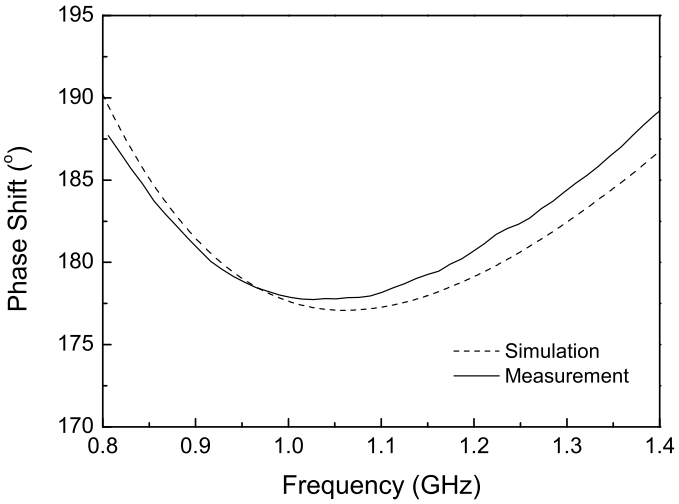


Fig. 3.12. Measured and simulated differential phase performance.

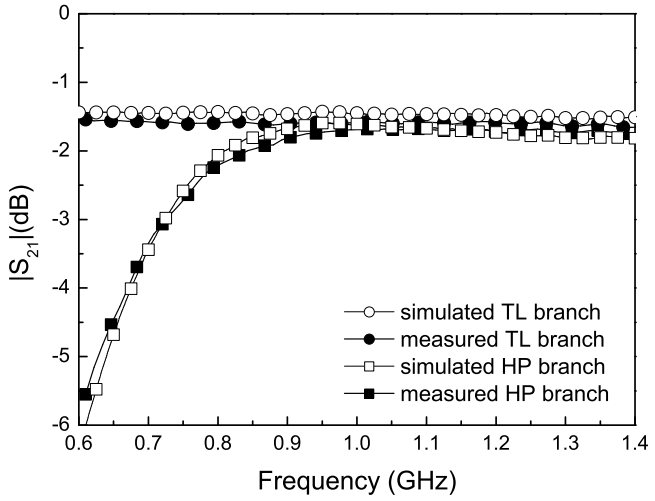


Fig. 3.13. Measured and simulated insertion loss of two states.

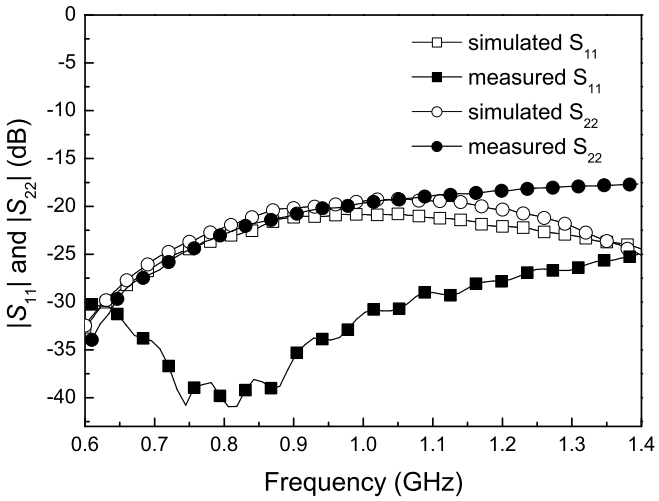


Fig. 3.14. Measured and simulated input/output return loss of TL branch.

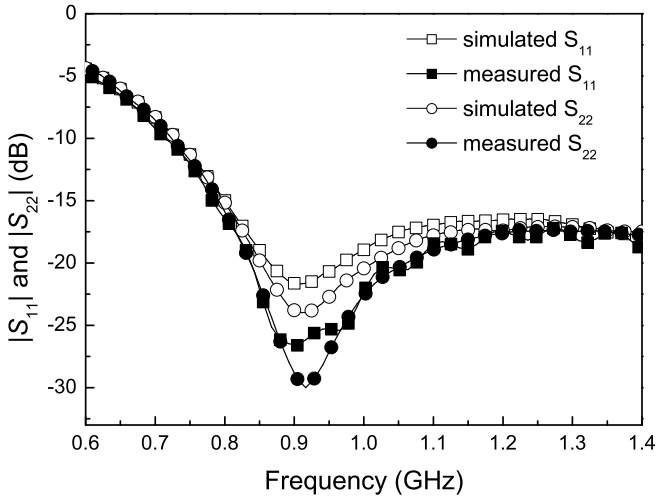


Fig. 3.15. Measured and simulated input/output return loss of HP branch.

3.3. Bandwidth Enhancement of Loaded-Line Phase Shifter

Another commonly used topology is the loaded-line phase shifters. They are used especially when the required power handling capability is high. However, this topology is chosen only when the required phase shift is less than 45º and the overall bandwidth is less than 25% with a ±2º phase error and a VSWR<1.5 [21]-[23], [73], [74]. Its simple structure gives it a high potential for millimeter wave design together with MEMS switching components [74]-[76]. As introduced in Chapter 1, the conventional loaded-line phase shifter uses two identical pairs of switchable loads at two ends of a transmission line to generate the phase difference. The phase response can be flat over a broad bandwidth. However, the return loss bandwidth is much smaller and therefore limits the overall bandwidth of the loaded line phase shifter. When the transmission line is around $\lambda/4$, the maximum bandwidth is achieved [21]. To achieve larger phase shifts, the return loss bandwidth reduces fast. Fig. 3.16 shows the return loss response of two conventional loaded-line topologies for a phase shift of 90º. It is found that the 20-dB return loss is not achievable for [27] and less than 10% for [23]. There is another method for narrow band matching which can be used to realize perfect match at the center frequency for both phase states [27]. However, the ±2º phase error bandwidth reduces to 2%. In [77], multiple phase bits with smaller a phase shift were cascaded to achieve 90º and 180º phase shifts with a bandwidth of 10%. However, the circuit size is multiplied by a factor of 2 to 4 because one $\lambda/4$ transmission line is required for each of the cascaded sections.

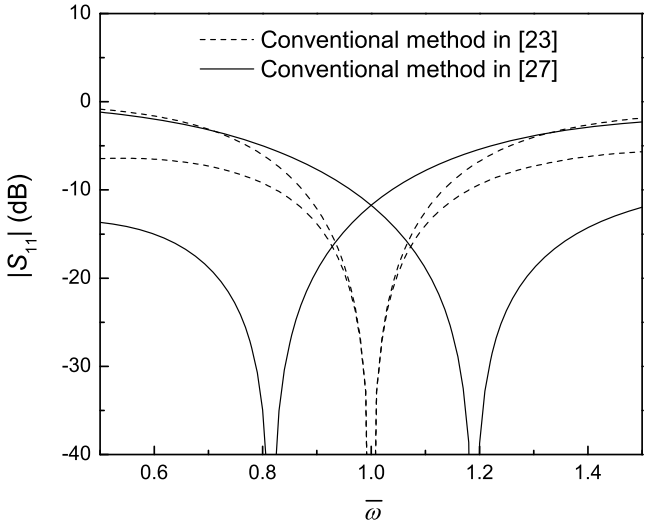


Fig. 3.16. Return loss response of two conventional loaded-line phase shifters using capacitive and inductive loads [23], [27].

A proposed topology of the loaded-line phase shifter still using a quarter-wavelength transmission line for larger phase shifts and broader bandwidth is shown in Fig. 3.17. Three single pole double throw (SPDT) switches are used to change the loads for the two phase states. In state 1, three shunt open circuited stubs together with two series $\lambda/8$ transmission lines achieve an insertion phase of $\phi_1(\omega)$ at frequency ω [78], [79]. The two $\lambda/8$ transmission lines have an impedance of $\overline{Z}_1$ and the stubs have an impedance of $\overline{Z}_2$ and $0.5\,\overline{Z}_2$.

As shown in Fig. 3.18, state 1 can be divided into two halves, each with an insertion phase of $0.5\phi_1(\omega_0)$ at the centre frequency ω_0. To match each half to 50 Ω, the normalized impedances $\overline{Z}_1$ and $\overline{Z}_2$ are found as:

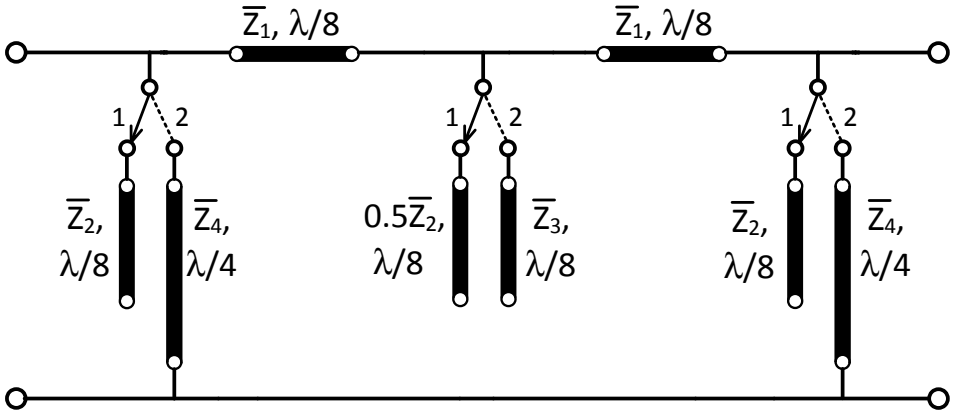


Fig. 3.17. Proposed loaded-line phase shifter.

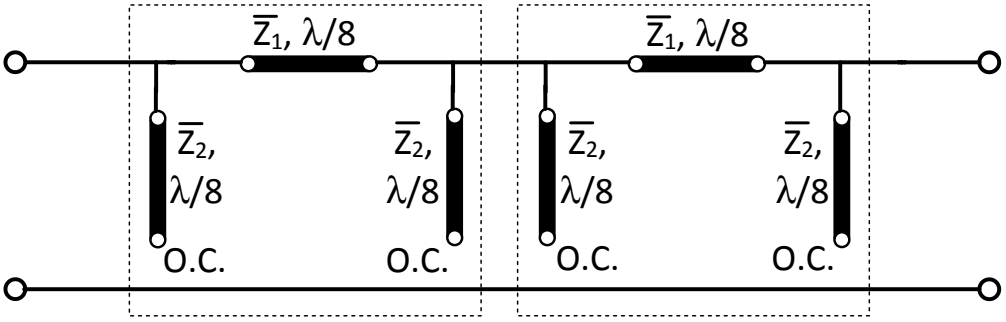


Fig. 3.18. State 1 is divided into two identical halves. The total insertion phase is ϕ_1 at the center frequency.

$$\overline{Z}_1 = \sqrt{2}\sin\left[0.5\phi_1(\omega_0)\right] \tag{3-18}$$

$$\overline{Z}_2 = \frac{\sqrt{2}\sin\left[0.5\phi_1(\omega_0)\right]}{1-\sqrt{2}\cos\left[0.5\phi_1(\omega_0)\right]} \tag{3-19}$$

In state 2, the two $\lambda/8$ transmission lines and the centre stub are considered first as shown in Fig. 3.19. Then the additional effect of the two outer grounded shunt $\lambda/4$ stubs shown in Fig. 3.17 is considered. According to (3-18), the impedance $\overline{Z}_1$ of the two $\lambda/8$ transmission lines is larger than one when $\phi_1(\omega_0)$ is between 90º and 270º. To

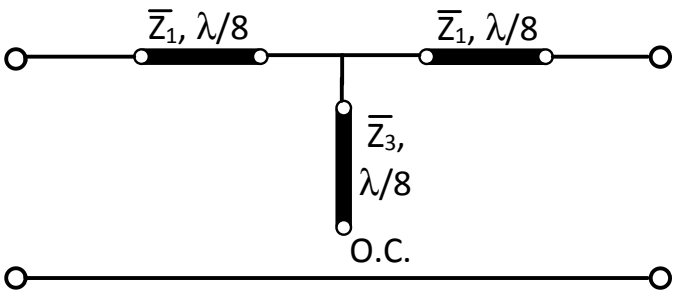


Fig. 3.19. The center open stub of state 2 is first analyzed.

achieve matching at the centre frequency, an open stub is added at the centre. The normalized impedance $\overline{Z}_3$ is found as:

$$\overline{Z}_3 = \frac{\overline{Z}_1\left(\overline{Z}_1^2+1\right)}{2\left(\overline{Z}_1^2-1\right)} \tag{3-20}$$

The insertion phase at the centre frequency of state 2 is given by

$$\phi_2(\omega_0) = \cos^{-1}\left(-\frac{\overline{Z}_1}{2\overline{Z}_3}\right) = \cos^{-1}\left(-\frac{\overline{Z}_1^2-1}{\overline{Z}_1^2+1}\right) \tag{3-21}$$

When switching between state 1 and state 2, the phase shift at the center frequency $\Delta\phi(\omega_0)$ is given by

$$\Delta\phi(\omega_0) = \phi_1(\omega_0) - \phi_2(\omega_0) \tag{3-22}$$

From (3-18) to (3-21), it is found that the insertion phase of both states is determined by $\overline{Z}_1$. Therefore, the relation between $\overline{Z}_1$ and the phase shift can be simplified to

$$\Delta\phi(\omega_0) = \sin^{-1}\left[\bar{Z}_1 \frac{\bar{Z}_1^2 - 1}{\bar{Z}_1^2 + 1}\left(2 \pm \sqrt{2 - \bar{Z}_1^2}\right)\right] \tag{3-23}$$

In (3-23), the "+" sign should be used when $\Delta\phi(\omega_0)$ is smaller than $\sin^{-1}(2\sqrt{2}/3) \cong 70.5°$, and the "-" sign should be used when $\Delta\phi(\omega_0)$ is between 70.5º and 90º.

By using $\bar{Z}_1$, $\bar{Z}_2$ and $\bar{Z}_3$ obtained from (3-18), (3-19), (3-20) and (3-23), the required phase shift is achieved at the center frequency. To align the phase slopes of the two states at the center frequency, two grounded shunt stubs with a characteristic impedance of $\bar{Z}_4$ are added [80]. At the center frequency, the phase slope for state 1 is given by

$$\left.\frac{\partial\phi_1(\omega)}{\partial\omega}\right|_{\omega=\omega_0} = \begin{cases} \dfrac{-4 + 3\sqrt{2 - \bar{Z}_1^2}}{\bar{Z}_1}\dfrac{\pi}{2}, & \Delta\phi(\omega_0) \le 70.5° \\ \dfrac{-4 - 3\sqrt{2 - \bar{Z}_1^2}}{\bar{Z}_1}\dfrac{\pi}{2}, & 70.5° \le \Delta\phi(\omega_0) \le 90° \end{cases} \tag{3-24}$$

The phase slope for state 2 at the same frequency, inclusive of the two additional $\lambda/4$ stubs, is given by

$$\left.\frac{\partial\phi_2(\omega)}{\partial\omega}\right|_{\omega=\omega_0} = -\frac{1 + \bar{Z}_1\bar{Z}_4}{\bar{Z}_4}\frac{\pi}{2} \tag{3-25}$$

By equating (3-24) to (3-25), the impedance $\bar{Z}_4$ of the grounded shunt stubs is found as

$$\bar{Z}_4 = \begin{cases} \dfrac{\bar{Z}_1}{4-\bar{Z}_1^2-3\sqrt{2-\bar{Z}_1^2}}, & \Delta\phi(\omega_0) \le 70.5° \\ \dfrac{\bar{Z}_1}{4-\bar{Z}_1^2+3\sqrt{2-\bar{Z}_1^2}}, & 70.5° \le \Delta\phi(\omega_0) \le 90° \end{cases} \tag{3-26}$$

The impedances $\bar{Z}_1$, $\bar{Z}_2$, $\bar{Z}_3$, and $\bar{Z}_4$ are shown in Fig. 3.20 as a function of the desired phase shift $\Delta\phi(\omega_0)$. It is noted that the topology proposed in Fig. 3.17 is limited when phase shifts less than 20º are required due to the required high impedance of $\bar{Z}_2$, $\bar{Z}_3$ and $\bar{Z}_4$. However, conventional topologies can be applied for small phase shifts.

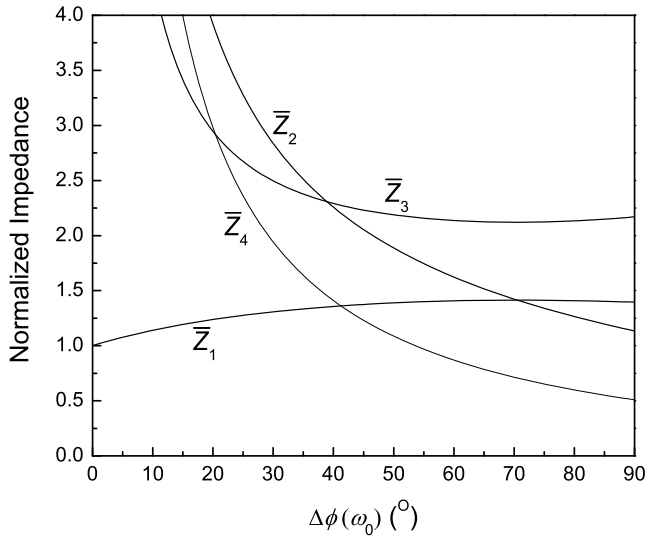


Fig. 3.20. Relation between $\bar{Z}_1$, $\bar{Z}_2$, $\bar{Z}_3$, $\bar{Z}_4$ and the phase shift.

In conclusion, the procedure to find the respective impedance for a given phase shift is as follows: first, (3-23) is solved for $\overline{Z}_1$ and then $\overline{Z}_2$, $\overline{Z}_3$, and $\overline{Z}_4$ are obtained from (3-19), (3-20) and (3-26), respectively. As examples, 45º and 90º phase shifters are designed using the method presented. For a phase error of ±2º, the required phase shift at the centre frequency should be 43º and 88º, respectively. The parameters of the two designs are listed in Table 3.1.

TABLE 3. 1
DESIGN PARAMETERS FOR 45º AND 90º PHASE SHIFTERS

$\Delta\phi(\omega_0)$ (º)	$\overline{Z}_1$	$\overline{Z}_2$	$\overline{Z}_3$	$\overline{Z}_4$
45-2=43	1.3681	2.1313	2.2534	1.2984
90-2=88	1.3989	1.1584	2.1614	0.5248

Simulation results using ideal components are shown in Fig. 3.21 and Fig. 3.22 as function of the normalized frequency $\overline{\omega} = \omega / \omega_0$. Fig. 3.21 shows the simulated phase shifts and Fig. 3.22 shows the simulated magnitude of S_{11}. The ±2º phase error bandwidths are 40% and 21.6% for the 45º and the 90º phase shifts respectively. Within the frequency band of each phase shifter, the worst return loss is 16.3 dB for the 45º phase shifter and 16.8 dB for the 90º phase shifter. At the centre frequency, all states are perfectly matched.

To validate the topology, 45º and 90º phase shifters at 1 GHz are designed using the parameters of Table 3.1. Three HMC545E SPDTs from Hittite are used. Because the SPDT switches have an insertion phase of approximately 17.5º at the centre frequency,

the lengths of the stubs are reduced to compensate for this additional insertion phase. The measured data of the SPDT switches is incorporated in the design and co-simulated with the loads.

The substrate used is Rogers 5870 with ε_r of 2.33 and a height of 31 mils. The fabricated 45º and 90º phase shifters are shown in Fig. 3.23. When incorporating the effect of the switches in the design, the maximum return loss frequencies had to be shifted in order to achieve the best phase response. Nevertheless, the return loss of the phase shifters remained better than 15 dB at the centre frequency.

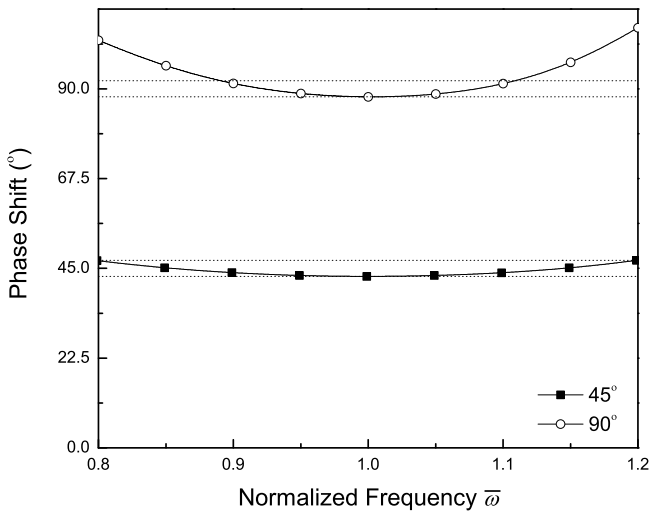
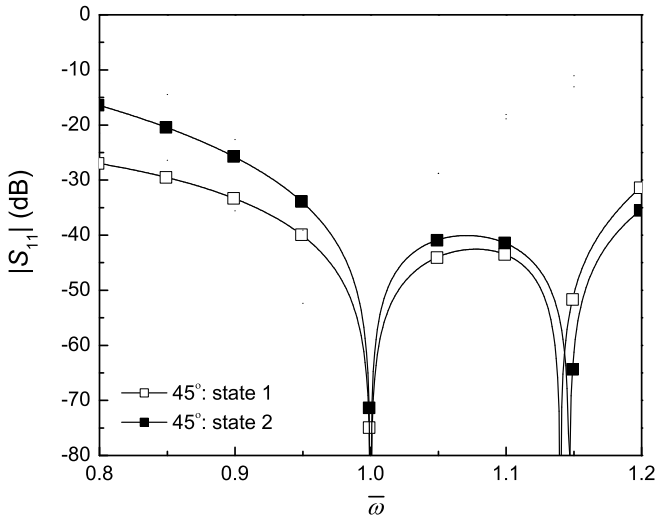
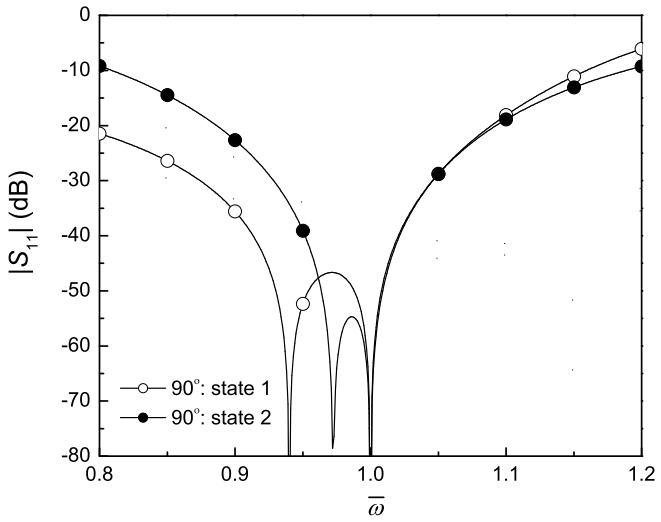


Fig. 3.21. Simulated phase shifts for 45º and 90º phase shifters.



(a)



(b)

Fig. 3.22. Simulated $|S_{11}|$ for (a) 45º and (b) 90º phase shifters.

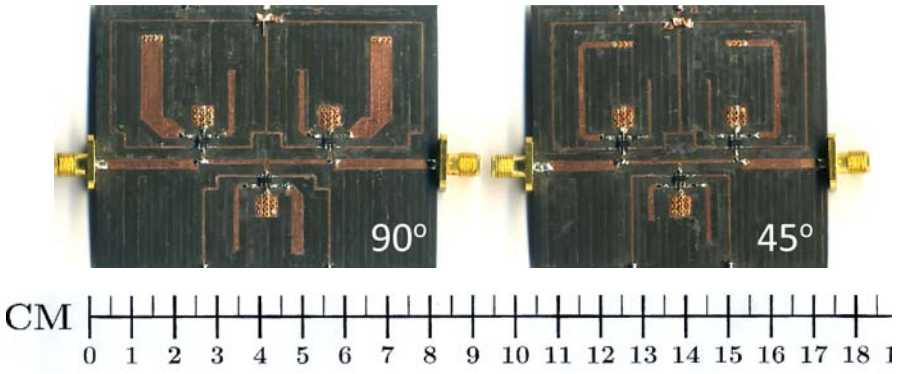


Fig. 3.23. Photo of the fabricated phase shifters.

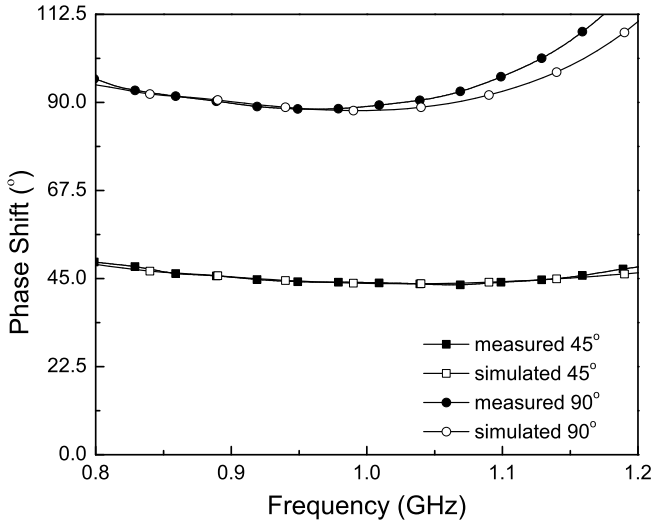


Fig. 3.24. Co-simulated and measured phase shifts.

The simulated and measured results are shown in Fig. 3.24 to Fig. 3.27. In Fig. 3.24 a 45.4º±2º phase shift is measured from 841 MHz to 1187 MHz (34%) and a 90.3º±2º phase shift is measured from 861 MHz to 1063 MHz (21%). In Fig. 3.25 and 3.26, the 45º phase shifter has a measured return loss better than 14 dB from 841 MHz to 1187 MHz and the 90º phase shifter has a measured return loss better than 10 dB from 861 MHz to 1063 MHz. The insertion losses are shown in Fig. 3.27.

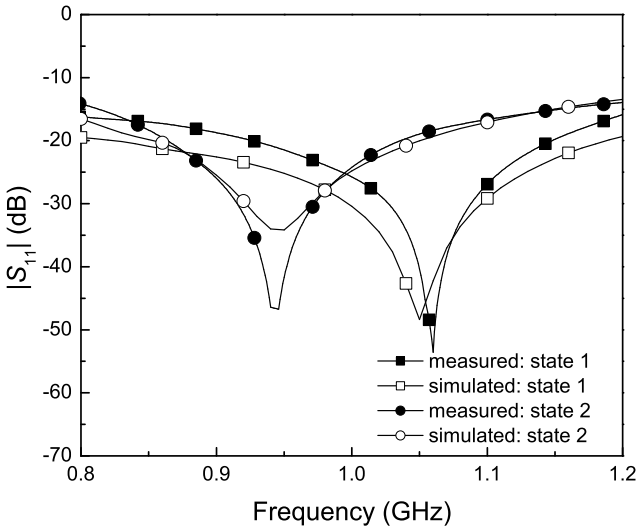


Fig. 3.25. Co-simulated and measured $|S_{11}|$ for 45º phase shifter.

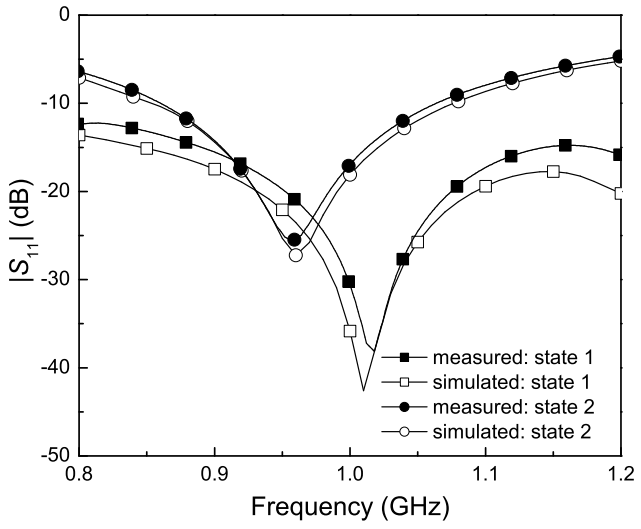


Fig. 3.26. Co-simulated and measured $|S_{11}|$ for 90º phase shifter.

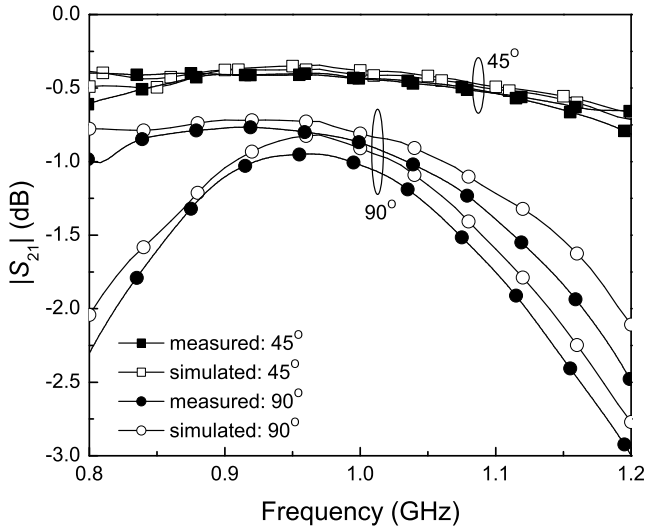


Fig. 3.27. Co-simulated and measured $|S_{21}|$ for both phase shifters.

TABLE 3. 2
MEASURED PERFORMANCE OF THE LOADED-LINE PHSAE SHIFTERS

45º			90º		
BW	PE (º)	RL (dB)	BW	PE (º)	RL (dB)
34%	±2	14	21%	±2	10

The measured amplitude imbalance is within 0.11 dB for the 45º phase shifter from 841 MHz to 1187 MHz and 0.67 dB for the 90º phase shifter from 861 MHz to 1063 MHz. The measured performance of this loaded-line phase shifters is in Table 3.2.

In conclusion, by using the proposed topology, the phase shift range and the corresponding overall bandwidth of the loaded-line phase shifter is increased to almost twice compare to the conventional performance without increasing the circuit size.

3.4. Dual-band loaded-line phase shifter

The conventional loaded-line phase shifter can also be extended to dual-band designs for dual-band phased array applications such as automotive short range radars. Recently, several dual-/multi-band phase shifters were reported [81]-[85]. In [81], multiple sections of varactor tuned LC networks are cascaded to achieve phase shifts and matching at multiple frequencies. In [82], two single-band phase shifters were used in parallel to realize the dual-band phase shifter. Both works use embedded amplifiers for loss compensation and therefore the linearity of the phase shifter is limited [83]. In [84], dual-band hybrid couplers are used and reflection type phase shifters are realized. In [85], a dual-band phase shifter was obtained by switching the path instead of the loads, and the circuit size is doubled compared to the conventional loaded-line phase shifters.

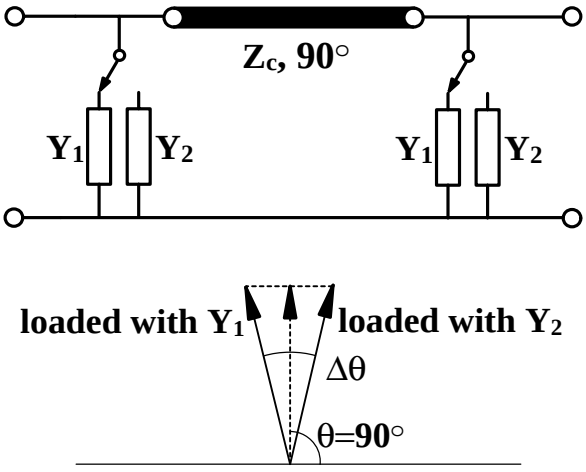


Fig. 3.28. Topology and vector diagram for Class III loaded-line phase shifter.

As introduced in Chapter 2, the Class III loaded-line phase shifter has the largest bandwidth in the loaded-line designs, and it is used for dual-band designs here. Fig. 3.28 shows the conventional topology and the vector diagram for the Class III loaded-line phase shifter where θ=90º is the insertion phase of the unloaded center line at the design frequency. By switching between the two loads, θ is either reduced or increased to create a phase shift of $\Delta\theta$.

For perfect matching, the following three conditions are derived [23]:

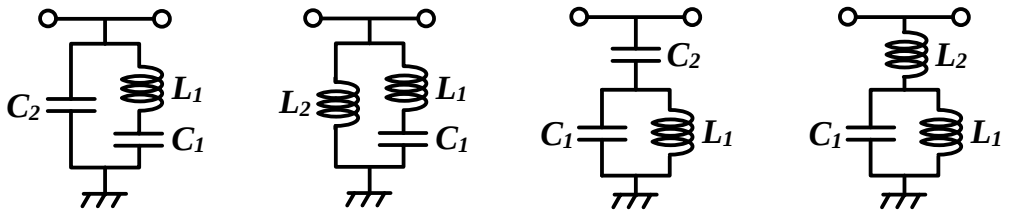
$$\overline{Z}_c = \cos\left(\Delta\theta/2\right) \tag{3-27}$$

$$\overline{Y}_1 = \tan\left(\Delta\theta/2\right) \tag{3-28}$$

$$\overline{Y}_2 = -\tan\left(\Delta\theta/2\right) \tag{3-29}$$

Note that for dual-band design, these conditions should be satisfied at the two dual-band frequencies. The ratio between the higher frequency f_2 and lower frequency f_1 is denoted by R. In the following, the dual-band loads $\overline{Y}_1$ and $\overline{Y}_2$ satisfying (3-28) and (3-29) will be found.

Figs. 3.29(a)-(d) show the four possible combinations. In all combinations for the loads, $\overline{B}_i = \omega C_i Z_0$, $\overline{X}_i = \omega L_i / Z_0$, i=1, 2.



(a) (b) (c) (d)

Fig. 3.29. Proposed loads for the dual-band loaded-line phase shifter.

In Fig. 3.29(a), $\bar{B}_1$ and $\bar{X}_1$ are found as a function of $\bar{B}_2$:

$$\bar{B}_1 = \frac{(1+R)\left[R\bar{B}_2 - \tan(\Delta\theta/2)\right]}{(1+R)\bar{B}_2 - \tan(\Delta\theta/2)} \times \frac{\tan(\Delta\theta/2) - \bar{B}_2}{R} \tag{3-30}$$

$$\bar{X}_1 = \bar{B}_1^{-1} + \left[\bar{B}_2 - \tan(\Delta\theta/2)\right]^{-1} \tag{3-31}$$

In Fig. 3.29(b), $\bar{B}_1$ and $\bar{X}_1$ are found as a function of $\bar{X}_2$:

$$\bar{X}_1 = -\frac{R\bar{X}_2 \tan(\Delta\theta/2) + R + 1}{\left[R\bar{X}_2 \tan(\Delta\theta/2) + 1\right](R+1)} \times \frac{\bar{X}_2}{\bar{X}_2 \tan(\Delta\theta/2) + 1} \tag{3-32}$$

$$\bar{B}_1 = \left[\bar{X}_1 + \frac{\bar{X}_2}{1 + \bar{X}_2 \tan(\Delta\theta/2)}\right]^{-1} \tag{3-33}$$

In Fig. 3.29(c), $\bar{B}_1$ and $\bar{X}_1$ are found as a function of $\bar{B}_2$:

$$\bar{B}_1 = \frac{\bar{B}_2}{R+1} \times \frac{R + 1 - R\bar{B}_2 \cot(\Delta\theta/2)}{\left[1 - \bar{B}_2 \cot(\Delta\theta/2)\right] \times \left[R\bar{B}_2 \cot(\Delta\theta/2) - 1\right]} \tag{3-34}$$

$$\bar{X}_1 = \left[\bar{B}_1 + \frac{\bar{B}_2}{1 - \bar{B}_2 \cot(\Delta\theta/2)}\right]^{-1} \tag{3-35}$$

In Fig. 3.29(d), $\bar{B}_1$ and $\bar{X}_1$ are found as a function of $\bar{X}_2$:

$$\overline{X}_1 = -\frac{(R+1)\left[R\overline{X}_2 + \cot(\Delta\theta/2)\right]}{(R+1)\overline{X}_2 + \cot(\Delta\theta/2)} \times \frac{\overline{X}_2 + \cot(\Delta\theta/2)}{R} \tag{3-36}$$

$$\overline{B}_1 = \overline{X}_1^{-1} + \left[\overline{X}_2 + \cot(\Delta\theta/2)\right]^{-1} \tag{3-37}$$

Once the dual-band frequency ratio *R* and the phase shift $\Delta\theta$ are chosen, the design procedure is to sweep $\overline{B}_2$ for Fig. 3.29(a) and Fig. 3.29(c) to obtain $\overline{B}_1$ and $\overline{X}_1$, and sweep $\overline{X}_2$ for Fig. 3.29(b) and Fig. 3.29(d) to obtain $\overline{B}_1$ and $\overline{X}_1$. Then the realizable combinations for the loads are determined and the most suitable loads can be selected.

As an example, consider a dual-band phase shifter at 900 MHz and 1800 MHz (*R*=2) with a phase shift of 45º. First, the center line is replaced by a transmission line and two shunt series resonators at both ends as shown in Fig. 3.30 to realize an insertion phase of 90º at 900 MHz and 90º+360º at 1800 MHz. The loads $\overline{Y}_i$ are designed using equations (3-30)-(3-37). $\overline{Y}_1$ can be realized by either Fig. 3.29(a) or Fig. 3.29(c). The parameters are $\overline{B}_1$=0.066, $\overline{B}_2$=0.3, $\overline{X}_1$=6.5 for Fig. 3.29(a) and $\overline{B}_1$=1.25, $\overline{B}_2$=0.3, $\overline{X}_1$=0.43 for Fig. 2(c). $\overline{Y}_2$ can be realized by either Fig. 2(b) and Fig. 2(d). The parameters are $\overline{B}_1$=0.07, $\overline{X}_1$=7.25, $\overline{X}_2$=1.8 for Fig. 3.29(b) and $\overline{B}_1$=1.5, $\overline{X}_1$=0.39, $\overline{X}_2$=1.5 for Fig. 3.29(d). To obtain the smallest inductance possible, Fig. 3.29(c) is chosen for the realization of $\overline{Y}_1$ and Fig. 3.29(d) is chosen for the realization of $\overline{Y}_2$.

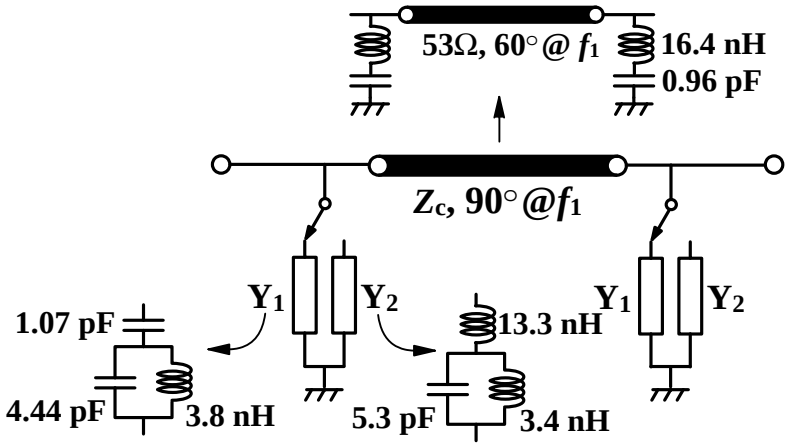


Fig. 3.30. Schematic of the dual-band loaded-line phase shifter at 900 and 1800 MHz.

The complete schematic is shown in Fig. 3.30 and Figs. 3.31(a)-(b) show the simulated phase shifts and $|S_{11}|$ at the two dual-band frequencies using ideal components. When the practical insertion phase of the SPDT switches is considered, the selection of the loads may be very different and new design equations are required.

SPDT switches are used to switch between the two loads in Class III loaded-line phase shifters. In transmission type digital phase shifters where switched networks are used, the SPDT switches can be simply modeled as a resistor in the ON state because the insertion phase introduced by the switches cancels out for the two phase states [23]. However, in loaded-line phase shifters, the SPDT switch should be modeled as a transmission line which provides an impedance transformation of the loads. This effect is significant and may change the choice of the loads shown in Fig. 3.29. In the following analysis, the SPDT switches are considered lossless [86] and are modeled as a transmission line with an impedance of $\overline{Z}_s$ and an insertion phase of θ_s at the

lower frequency in the ON state. The four loads of Fig. 3.29 then change to Fig. 3.32 and the closed-form formulas for the elements are also updated.

In Fig. 3.32(a), $\overline{B}_1$ and $\overline{X}_1$ are found as a function of $\overline{B}_2$:

$$\overline{B}_1 = \left[\frac{\tan(\Delta\theta/2)\tan(R\theta_s) + \overline{Y}_s}{N_a} - R \times M_a \right] \frac{R}{R^2 - 1} \tag{3-38}$$

$$\overline{X}_1 = \overline{B}_1^{-1} + M_a \tag{3-39}$$

where $M_a = \dfrac{\tan(\Delta\theta/2)\tan\theta_s + \overline{Y}_s}{\overline{Y}_s^2 \tan\theta_s + \overline{Y}_s \overline{B}_2 + (\overline{B}_2 \tan\theta_s - \overline{Y}_s)\tan(\Delta\theta/2)}$

and

$$N_a = \overline{Y}_s^2 \tan(R\theta_s) + R\overline{Y}_s\overline{B}_2 + \left[R\overline{B}_2 \tan(R\theta_s) - \overline{Y}_s \right] \tan(\Delta\theta/2)$$

In Fig. 3.32(b), $\overline{B}_1$ and $\overline{X}_1$ are found as a function of $\overline{X}_2$:

$$\overline{X}_1 = \left[\frac{\tan(\Delta\theta/2)\tan(R\theta_s) + \overline{Y}_s}{N_b} - \frac{M_b}{R} \right] \frac{R}{R^2 - 1} \tag{3-40}$$

$$\overline{B}_1 = \left(\overline{X}_1 - M_b \right)^{-1} \tag{3-41}$$

where $M_b = \dfrac{\tan(\Delta\theta/2)\tan\theta_s + \overline{Y}_s}{\overline{Y}_s^2 \tan\theta_s - \overline{Y}_s/\overline{X}_2 - (\tan\theta_s/\overline{X}_2 + \overline{Y}_s)\tan(\Delta\theta/2)}$

and $N_b = \overline{Y}_s^2 \tan(R\theta_s) - \dfrac{\overline{Y}_s}{R\overline{X}_2} - \left[\dfrac{\tan(R\theta_s)}{R\overline{X}_2} + \overline{Y}_s \right] \tan(\Delta\theta/2)$

In Fig. 3.32(c), $\bar{B}_1$ and $\bar{X}_1$ are found as a function of $\bar{B}_2$:

$$\bar{B}_1 = \left[\frac{\cot(\Delta\theta/2) \times \tan(R\theta_s) - \bar{Z}_s}{N_c} + \frac{M_c}{R} \right] \left(\frac{1}{R} - R \right) \tag{3-42}$$

$$\bar{X}_1 = \left[\bar{B}_1 - M_c \right]^{-1} \tag{3-43}$$

where $M_c = \dfrac{\bar{Z}_s - \cot(\Delta\theta/2)\tan\theta_s}{\bar{Z}_s^2 \tan\theta_s - \bar{Z}_s/\bar{B}_2 + (\tan\theta_s/\bar{B}_2 + \bar{Z}_s)\cot(\Delta\theta/2)}$

and

$$N_c = \bar{Z}_s^2 \tan(R\theta_s) - \frac{\bar{Z}_s}{R\bar{B}_2} + \left[\frac{\tan(R\theta_s)}{R\bar{B}_2} + \bar{Z}_s \right] \cot(\Delta\theta/2)$$

In Fig. 3.32(d), $\bar{B}_1$ and $\bar{X}_1$ are found as a function of $\bar{X}_2$:

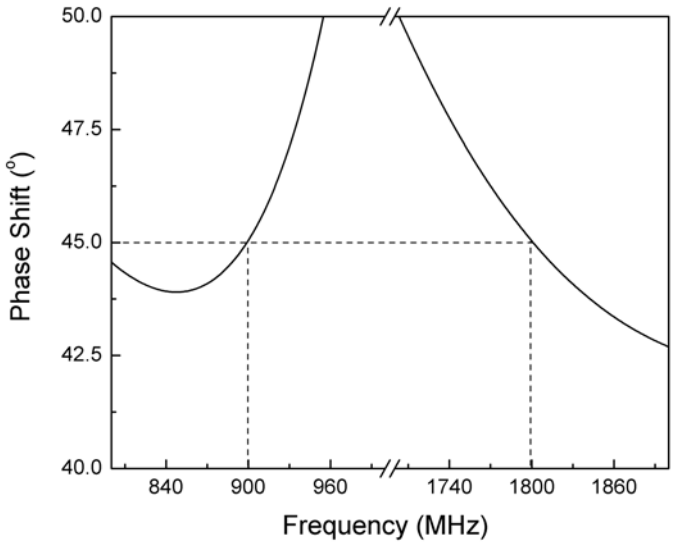
$$\bar{X}_1 = \left[\frac{\bar{Z}_s - \cot(\Delta\theta/2)\tan(R\theta_s)}{N_d} - RM_d \right]^{-1} \left(R - \frac{1}{R} \right) \tag{3-44}$$

$$\bar{B}_1 = \bar{X}_1^{-1} + M_d \tag{3-45}$$

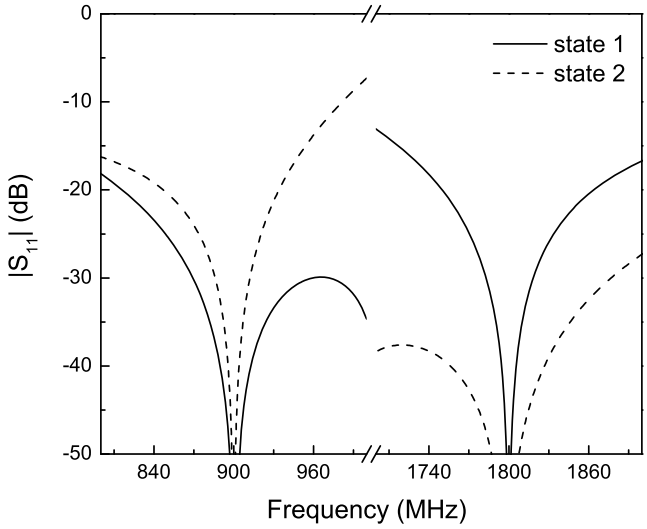
where $M_d = \dfrac{\bar{Z}_s - \cot(\Delta\theta/2)\tan\theta_s}{\bar{Z}_s^2 \tan\theta_s + \bar{Z}_s\bar{X}_2 - (\bar{X}_2 \tan\theta_s - \bar{Z}_s)\cot(\Delta\theta/2)}$

and

$$N_d = \bar{Z}_s^2 \tan(R\theta_s) + R\bar{Z}_s\bar{X}_2 - \left[R\bar{X}_2 \tan(R\theta_s) - \bar{Z}_s \right] \cot(\Delta\theta/2)$$

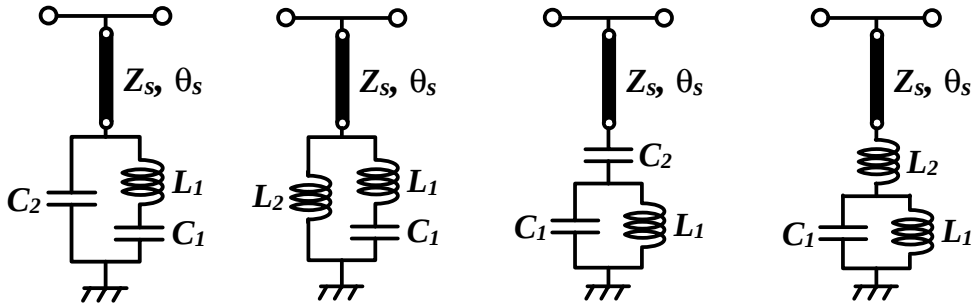


(a)



(b)

Fig. 3.31. Simulated dual-band response using ideal components: (a) phase shift, and (b) $|S_{11}|$.



(a) (b) (c) (d)

Fig. 3.32. Updated loads when the SPDT switches in the ON-state is modeled as a transmission line.

To validate the design method, a 45º dual-band phase shifter at 900 MHz and 1800 MHz is designed. Rogers 5870 (ε_r=2.33, height=31 mils), discrete MuRata *L*, *C* components and the HMC545E SPDT switch from Hittite are used. Using the measured data of the switch, the ON state is modeled as a transmission line with $\overline{Z}_s = 0.9$ and θ_s=24.5º at 900 MHz. To find the other parameters, equations (3-38)-(3-45) are used. It is found that instead of Fig. 3.29(c) for realization of $\overline{Y}_1$ and Fig. 3.29(d) for realization of $\overline{Y}_2$, Fig. 3.32(b) and Fig. 3.32(d) should be used for the realization of $\overline{Y}_1$ and $\overline{Y}_2$. The other two loads are not able to meet the requirement due to the effect of the switches. The parameters found are $\overline{B}_1$=0.24, $\overline{X}_1$=2.2, $\overline{X}_2$=1.5 for Fig. 3.32(b) and $\overline{B}_1$=1.92, $\overline{X}_1$=0.2, $\overline{X}_2$=0.5 for Fig. 3.32(d). The photo of the fabricated circuit is shown in Fig. 3.33.

The simulated responses are compared with the measured responses in Fig. 3.34 to Fig. 3.36. Fig. 3.34 shows the phase shifts at the two frequency bands. The measured phase shift is 46.1º±2º from 841 MHz to 930 MHz and 44.9º±2º from 1743 MHz to

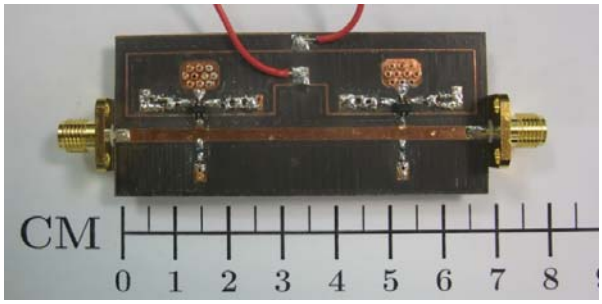


Fig. 3.33. Photo of the fabricated circuit.

1924 MHz. Fig. 3.35 shows that the return loss of the two phase states is larger than 15 dB. Fig. 9 shows the insertion loss of the two phase states. From 841 MHz to 930 MHz, the measured insertion loss of the two phase states is smaller than 1.2 dB and from 1743 MHz to 1924 MHz, the measured insertion loss of the two phase states is smaller than 1.1 dB. The amplitude imbalance at the two frequency bands is less than 0.33 dB and 0.4 dB, respectively.

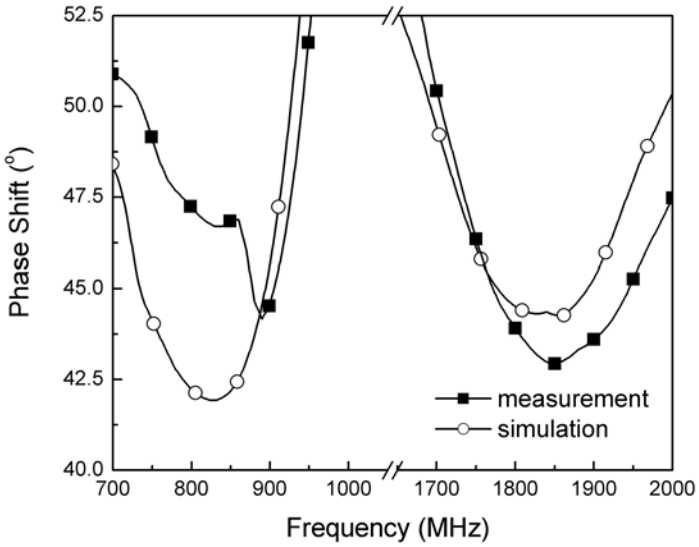


Fig. 3.34. Simulated and measured phase shift.

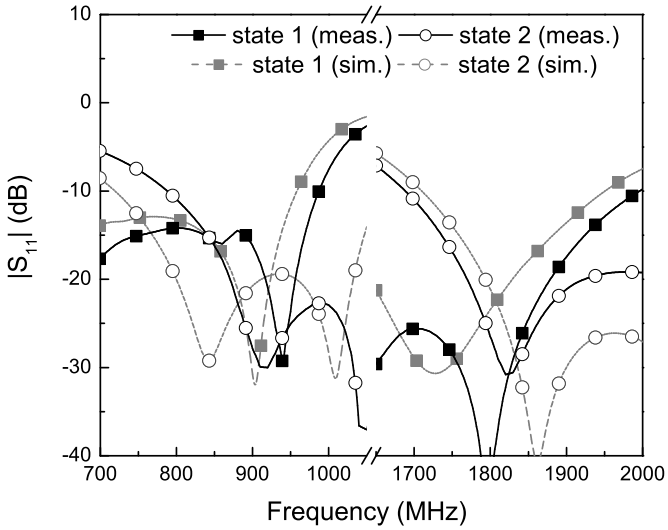


Fig. 3.35. Simulated and measured $|S_{11}|$.

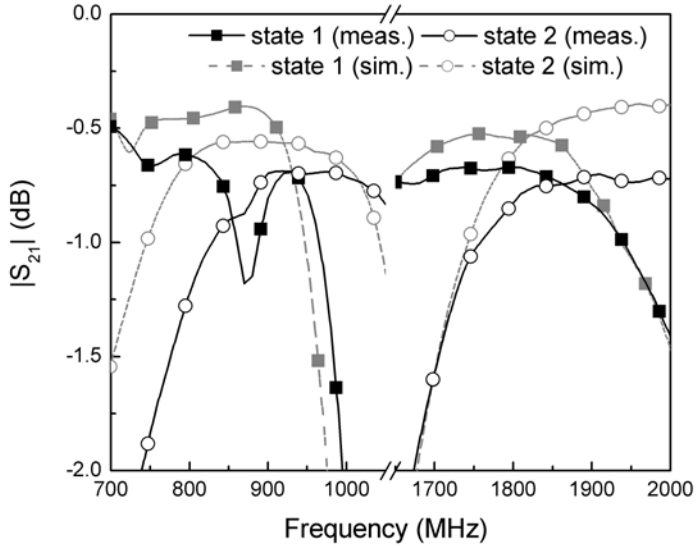


Fig. 3.36. Simulated and measured $|S_{21}|$.

3.5. Conclusions

In this chapter, several modifications of conventional HP/LP and loaded-line phase shifter topologies are proposed to improve their performance and increase the design flexibility.

A more general design method for the high-pass/low-pass topology, which includes the conventional design as a special case, is presented. The return loss and the phase error are both improved for phase shifts equal or less than 90º for a given bandwidth. Tradeoffs between the performance and the bandwidth are also possible. Then for the 180º phase shift, a transmission line instead of a LP filter is used to improve the phase linearity and thus increase the phase error bandwidth of this phase bit. The same approach can be applied to smaller phase bits, but the improvement is not significant because the shorter transmission lines can already be mimicked well by the LP filter.

For the loaded-line phase shifters, one more SPDT switch is added to the main line to improve the overall bandwidth of this topology. Closed-form design formulas are provided for an arbitrary phase shift. After the modification, the overall bandwidth is extended by a factor of around 2 without increasing the circuit area. Furthermore, the conventional single band design is extended to a dual-band design. The modeling of the switching components and the associated design formulas are also provided. To the best of our knowledge, this is the first dual-band loaded-line phase shifter.

Chapter 4

Broadband Phase Shifter Design and Tradeoffs Using Phase Slope Alignment Technique

In most conventional phase shifter design methods, when the center frequency and the required phase shift at the center frequency are fixed, the performance is then fixed. There is no room for tradeoffs to obtain an optimum performance for a given bandwidth. In the previous chapter, improvements are possible in terms of return loss and phase error. However, more substantial tradeoffs between the performance and the bandwidth are needed, so that designers may synthesize phase shifters according to the requirement, similar to the expert filter design methods.

This chapter introduces more tradeoffs between the performance and the bandwidth of several novel phase shifter topologies, where the optimum phase error for a given bandwidth is realized.

4.1 Phase Slope Alignment Using Quarter Wavelength Stubs

In Fig. 4.1, the topology for a phase shift bit consisting of a transmission line branch, a bandpass filter branch and two SPDT switches to switch between the two branches

is shown. In the analysis that follows, the insertion phase of the transmission line branch at the center frequency ω_c is chosen as the sum of the desired phase shift and the insertion phase of the bandpass filter at ω_c:

$$\phi_{TL}(\omega_c) = \Delta\phi(\omega_c) + \phi_{BPF}(\omega_c) \tag{4-1}$$

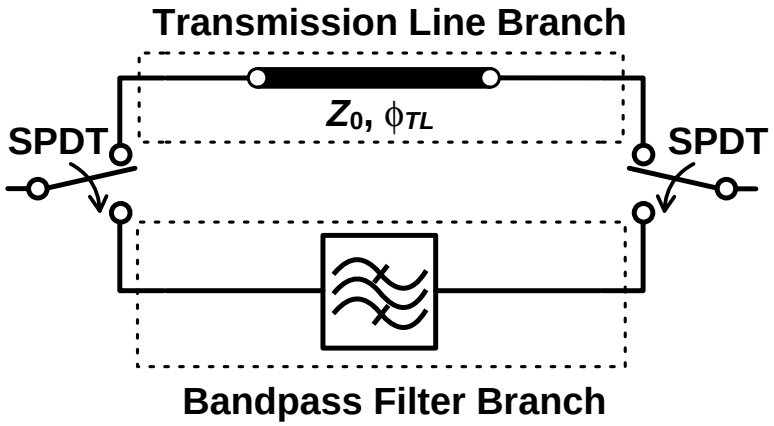


Fig. 4.1. Topology for broadband phase shifter bit.

In the following, bandpass filters with one, two and three transmission poles for the bandpass filter branch are analyzed. The bandwidth of the phase shifter increases with the number of poles. The return loss, phase error and the achievable phase shift for each case are discussed in detail.

4.1.1 Topology 1: BPF with one pole.

Fig. 4.2 shows the topology of the single pole bandpass filter which consists of a $\lambda/4$ short circuited shunt stub resonant at ω_c. At an arbitrary frequency, the insertion phase

of the bandpass filter is given by

$$\phi_{BPF}(\bar{\omega}) = \arctan\left[\frac{1}{2\bar{Z}_1}\tan\left(\frac{\pi}{2}-\frac{\pi}{2}\bar{\omega}\right)\right] \tag{4-2}$$

where $\bar{Z}_1 = Z_1/Z_0$ is the normalized impedance and $\bar{\omega} = \omega/\omega_c$ is the normalized frequency.

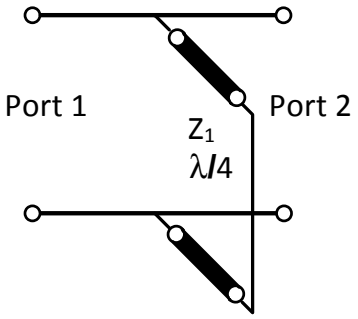


Fig. 4.2. Topology 1: Single pole bandpass filter.

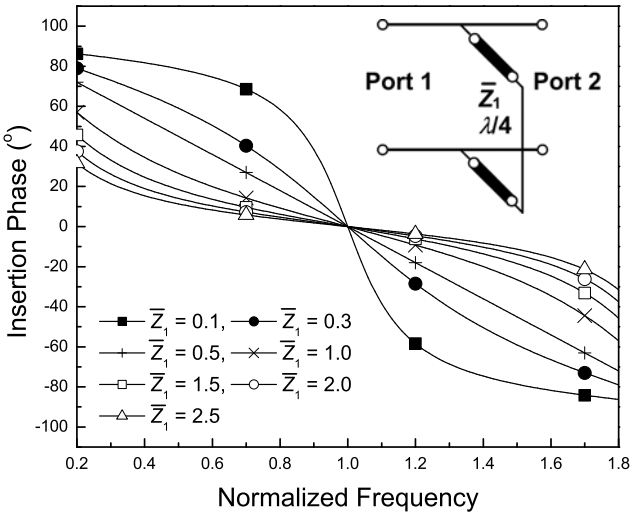


Fig. 4.3. Insertion phase versus normalized frequency of a grounded shunt stub.

In Fig. 4.3 the insertion phase is shown versus the normalized frequency for different $\overline{Z}_1$. It is observed that when $\overline{Z}_1$ is changed, the phase slope of the branch can be controlled without changing the insertion phase at the center frequency.

In Fig. 4.4(a) and (b) two possible phase shift responses $\Delta\phi(\overline{\omega})$ are shown. In these figures four characteristic frequencies are defined: $\overline{\omega}_L$ and $\overline{\omega}_H$ are the lower bound and upper bound of the desired bandwidth, and $\overline{\omega}_{r1}$ and $\overline{\omega}_{r2}$ are the frequencies where the phase slope of the TL branch and the BPF branch are equal.

The maximum phase error in the desired bandwidth is denoted by *PE* and the phase shift within the desired bandwidth satisfies

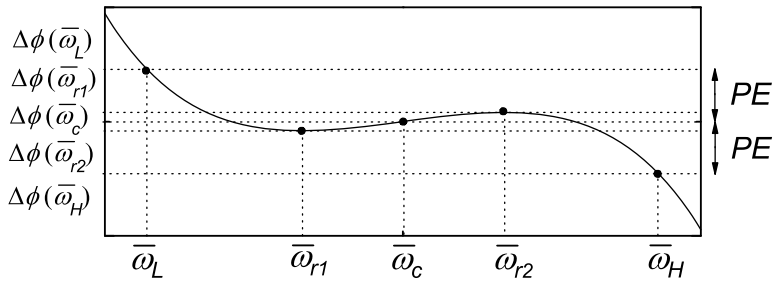
$$\Delta\phi(\overline{\omega}_C) - PE \le \Delta\phi(\overline{\omega}) \le \Delta\phi(\overline{\omega}_C) + PE \tag{4-3}$$

As shown in Fig. 4.4(c), the optimum maximum phase error PE_{opt} is achieved when:

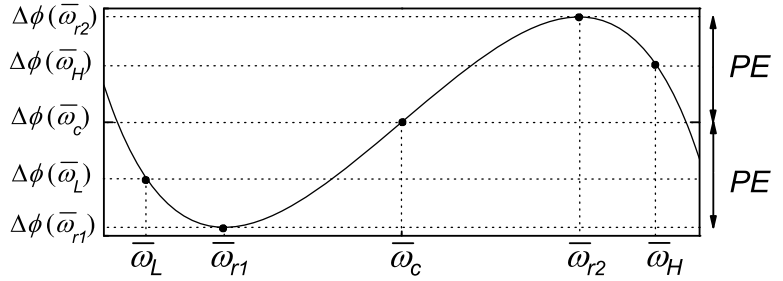
$$\Delta\phi(\overline{\omega}_L) = \Delta\phi(\overline{\omega}_{r2}) \quad \text{and} \quad \Delta\phi(\overline{\omega}_H) = \Delta\phi(\overline{\omega}_{r1}) \tag{4-4}$$

Note that if one of these conditions is satisfied, the other is automatically satisfied too. Because the phase shift is anti-symmetric around $\overline{\omega}_c$, only frequencies below $\overline{\omega}_c$ are considered in the following discussion. To find the optimum phase error PE_{opt}, $\overline{\omega}_{r1}$ must be determined first. The phase shift $\Delta\phi(\overline{\omega})$, given by

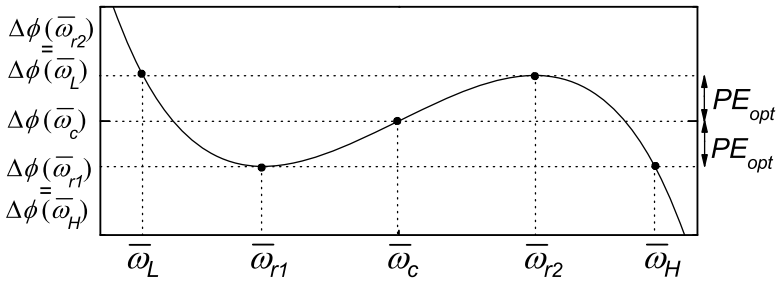
$$\Delta\phi(\overline{\omega}) = \phi_{BPF}(\overline{\omega}) - \phi_{TL}(\overline{\omega}) \tag{4-5}$$



(a)



(b)



(c)

Fig. 4. 4. (a), (b) Typical phase shift responses (c) optimum phase shift response.

is differentiated with respect to $\bar{\omega}$ and equated to zero:

$$\frac{d\Delta\phi(\bar{\omega})}{d\bar{\omega}} = \frac{d\phi_{BPF}(\bar{\omega})}{d\bar{\omega}} - \frac{d\phi_{TL}(\bar{\omega})}{d\bar{\omega}} = 0 \tag{4-6}$$

The phase slope of the bandpass filter is found using (4-2):

$$\frac{d\phi_{BPF}(\bar{\omega})}{d\bar{\omega}} = -\frac{\pi\left[1+\tan^2\left(\frac{\pi\bar{\omega}}{2}\right)\right]\bar{Z}_1}{1+\bar{Z}_1^2\tan^2\left(\frac{\pi\bar{\omega}}{2}\right)} \tag{4-7}$$

and the phase slope of the transmission line is constant

$$\frac{d\phi_{TL}(\bar{\omega})}{d\bar{\omega}} = -\Delta\phi(\bar{\omega}_c) \tag{4-8}$$

Substituting (4-7) and (4-8) in (4-6), we can solve for $\bar{\omega}_{r1}$:

$$\bar{\omega}_{r1} = \frac{2}{\pi}\arctan\sqrt{\frac{\pi\bar{Z}_1 - \Delta\phi(\bar{\omega}_c)}{\bar{Z}_1\left[4\bar{Z}_1\Delta\phi(\bar{\omega}_c) - \pi\right]}} \tag{4-9}$$

with the condition:

$$\frac{\pi\bar{Z}_1 - \Delta\phi(\bar{\omega}_c)}{\bar{Z}_1\left[4\bar{Z}_1\Delta\phi(\bar{\omega}_c) - \pi\right]} \geq 0 \tag{4-10}$$

By substituting (4-9) into (4-5), the phase shift at $\bar{\omega}_{r1}$ is

$$\Delta\phi(\bar{\omega}_{r1}) = \arctan\frac{\sqrt{\bar{Z}_1\left[4\bar{Z}_1\Delta\phi(\bar{\omega}_c)-\pi\right]}}{2\bar{Z}_1\sqrt{\pi\bar{Z}_1-\Delta\phi(\bar{\omega}_c)}} + \frac{2\Delta\phi(\bar{\omega}_c)}{\pi}\sqrt{\frac{\pi\bar{Z}_1-\Delta\phi(\bar{\omega}_c)}{\bar{Z}_1\left[4\bar{Z}_1\Delta\phi(\bar{\omega}_c)-\pi\right]}} \qquad (4\text{-}11)$$

The optimum phase error PE_{opt} is then obtained by numerically solving

$$\Delta\phi(\bar{\omega}_L) - \Delta\phi(\bar{\omega}_c) = \Delta\phi(\bar{\omega}_c) - \Delta\phi(\bar{\omega}_{r1}) \qquad (4\text{-}12)$$

In Fig. 4.5 PE_{opt} and $\bar{Z}_1$ are shown versus the phase shift for bandwidths of 30%, 50%, 67% (one octave) and 100% (3:1). When the bandwidth and phase shift are specified, the characteristic impedance $\bar{Z}_1$ is obtained from the left axis of Fig. 4.5, and the corresponding optimum phase error is found from the right axis.

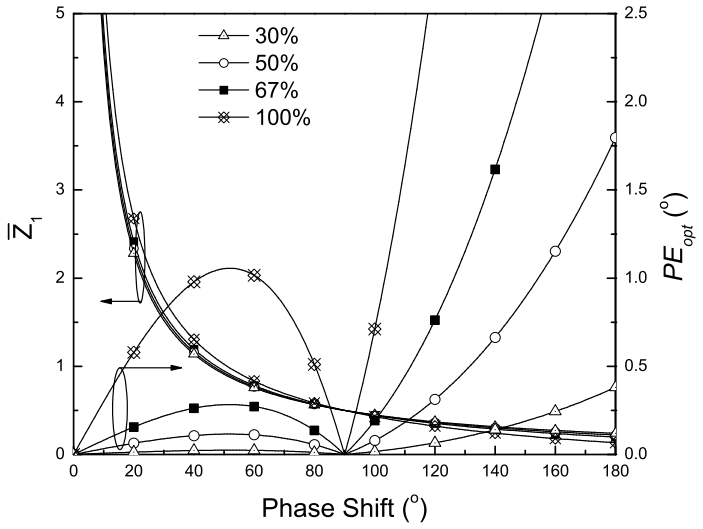


Fig. 4.5. PE_{opt} and $\bar{Z}_1$ of the grounded shunt stub versus the phase shift.

Note that so far only the bandwidth for the phase error is considered. However, for phase shifter design the bandwidth of a specified return loss should also be considered. Because the return loss bandwidth of the TL branch ideally is infinite, the bandwidth is limited by the return loss bandwidth of the BPF branch. In the case of the grounded shunt $\lambda/4$ stub, the return loss is determined by the impedance $\overline{Z}_1$. For an impedance $\overline{Z}_1$ and a desired return loss *RL*, the bandwidth is given by:

$$BW_{RL} = 2\left(1 - \frac{2}{\pi}\arctan\frac{\sqrt{10^{RL/10}-1}}{2\overline{Z}_1}\right)\times 100\% \qquad (4\text{-}13)$$

In Fig. 4.6 the return loss bandwidth BW_{RL} is shown versus the impedance $\overline{Z}_1$ for return losses of 10, 15, and 20 dB. Because the return loss and the phase shift are both determined by $\overline{Z}_1$, their relation is shown in Fig. 4.7.

As an example, consider a phase shifter with an octave bandwidth (67%) and a required return loss of 15 dB. From Fig. 4.7 it is found that only phase shifts up to 30º can be achieved. The associated phase error is found in Fig. 4.5.

In conclusion, when large bandwidths are required with return losses of 15 dB or larger, the achievable phase shift with the single grounded shunt λ/4 stub is limited to small phase shifts. Therefore, other topologies must be considered to improve the bandwidth of the return loss of the BPF branch. The single pole BPF is used for the 22.5° phase bit of the realized four-bit phase shifter discussed later.

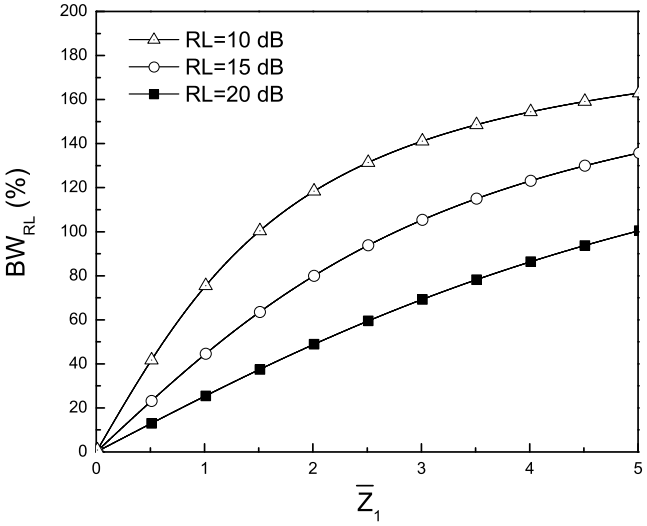


Fig. 4.6. Return loss bandwidth versus $\overline{Z}_1$.

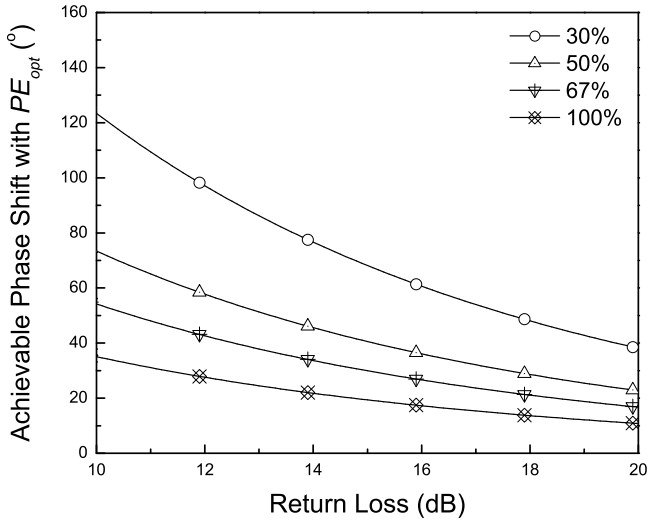


Fig. 4.7. Relation between the return loss and the achievable phase shift with optimum phase error for different bandwidths.

4.1.2 Topology 2: BPF with two poles

To improve the bandwidth of the return loss for the larger phase shifting bits, transmission poles are added to the single stub bandpass filter. To achieve two poles a series $\lambda/4$ transmission line is inserted between two short circuited shunt $\lambda/4$ stubs as shown in Fig. 4.8.

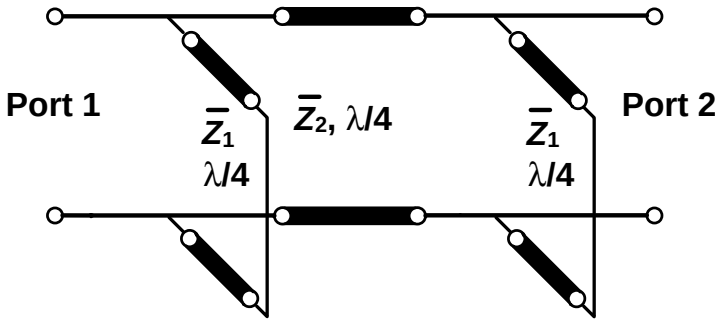


Fig. 4.8. Topology 2: Double pole bandpass filter.

The insertion phase of the double pole bandpass filter is

$$\phi_{BPF}\left(\bar{\omega}\right) = \arctan\left[\frac{2\bar{Z}_1\bar{Z}_2 + \Omega\bar{Z}_2^2 - \Omega^2\bar{Z}_2^2\left(\bar{Z}_2^2+1\right)}{2\Omega\bar{Z}_1\bar{Z}_2\left(\bar{Z}_1+\bar{Z}_2\right)}\right] \tag{4-14}$$

where $\Omega = \tan\left(0.5\pi\bar{\omega}\right)$.

When $\bar{Z}_2 < 1$, two transmission poles are found:

$$\bar{\omega}_{1,2} = 1 \pm \left[1 - \frac{2}{\pi}\arctan\sqrt{\frac{\bar{Z}_2}{\bar{Z}_1^2}\cdot\frac{2\bar{Z}_1+\bar{Z}_2}{1-\bar{Z}_2^2}}\right] \tag{4-15}$$

Note that when $\bar{Z}_2 = 1$, only one transmission pole is found at $\bar{\omega}_c$ and when $\bar{Z}_2 > 1$, no transmission poles are found.

The optimum phase error is found again by solving (4-12) and the solution is a set of combinations of $\bar{Z}_1$ and $\bar{Z}_2$. Therefore, the combination of $\bar{Z}_1$ and $\bar{Z}_2$ that satisfies the return loss requirement within the required bandwidth must be determined.

There are two extreme cases that meet the return loss requirement. This is illustrated in Fig. 4.9 for a return loss requirement of 15 dB. In case 1, the return loss requirement is met at the band edges $\bar{\omega}_L$ and $\bar{\omega}_H$ and the requirement is exceeded at $\bar{\omega}_c$. In case 2 the requirement is met at $\bar{\omega}_c$ and exceeded at $\bar{\omega}_L$ and $\bar{\omega}_H$. Each case has an optimum phase error and the case with the smaller optimum phase error should be selected.

As a further illustration, in Fig. 4.10 the optimum phase error is shown versus the required return loss for an octave bandwidth of 22.5°, 45° and 90° phase bits. For all three phase bits, case 1 and case 2 intersect at the point when the return loss at the band edges is equal to the return loss at $\bar{\omega}_c$. The inset of Fig. 4.10 shows that in case 1 there can be zero, one or two poles when $\bar{Z}_1$ is larger than, equal to, or smaller than 1 respectively.

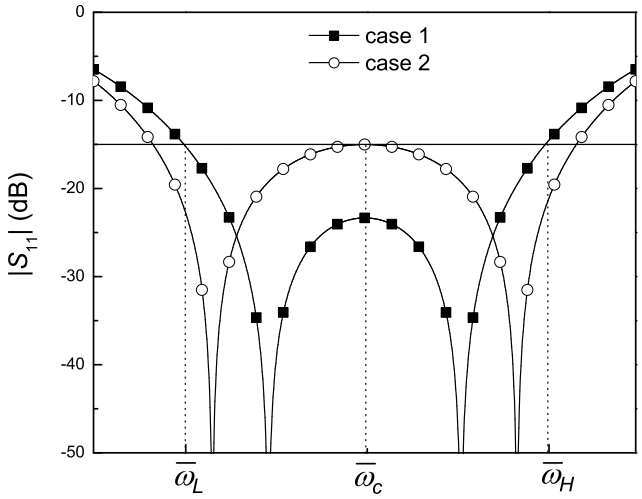


Fig. 4.9. Return loss of BPF with two poles. Case 1: return loss requirement is met at $\overline{\omega}_L$ and $\overline{\omega}_H$. Case 2: return loss requirement is met at $\overline{\omega}_c$.

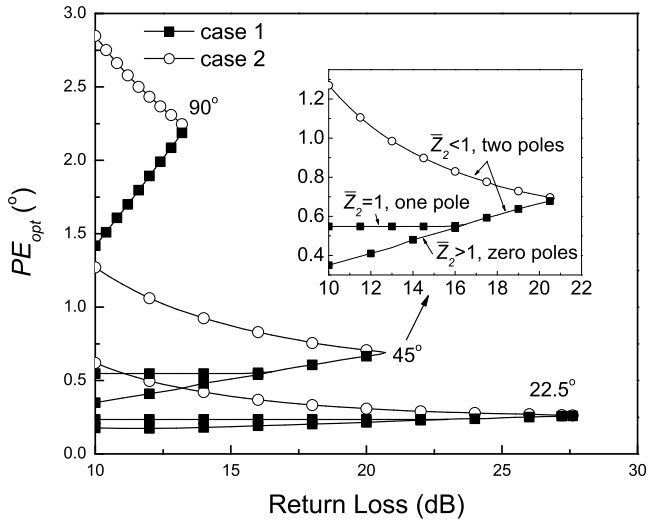


Fig. 4.10. Two cases of PE_{opt} versus return loss for 22.5º, 45º and 45º phase shifts in an octave bandwidth. In case 1 the return loss requirement is met at $\overline{\omega}_L$ and $\overline{\omega}_H$ and in case 2 the requirement is met at $\overline{\omega}_c$.

For the three phase shifts, it is observed that case 1 provides the smaller optimum phase error. For a return loss requirement of 15 dB the optimum phase error for the 22.5° and 45° phase bit is 0.24° and 0.55°, respectively. It is also observed that it is not possible to achieve a return loss of 15 dB for the 90° phase bit.

In conclusion, the procedure to determine $\bar{Z}_1$ and $\bar{Z}_2$ is as follows:

1. Set the requirements for the frequencies $\bar{\omega}_L$ and $\bar{\omega}_H$, return loss *RL* and phase shift $\Delta\phi(\bar{\omega}_c)$.
2. Use (4-8) and (4-14) in (4-6) to find the expression for PE_{opt} with $\bar{Z}_1$ and $\bar{Z}_2$ as variables.
3. Substitute $\bar{\omega}_L$ and $\bar{\omega}_c$ in the expression for $|S_{11}|$ of the BPF branch, provided in appendix A, to determine the return loss for case 1 and case 2 respectively.
4. Using the expressions found in step 2 and step 3, determine $\bar{Z}_1$ and $\bar{Z}_2$ for the two cases and select the case with the smallest PE_{opt}.

The above procedure is applied to determine the relation between bandwidth and achievable phase shift for the three return loss cases of 10, 15, and 20 dB. The results are shown in Fig. 4.11. It is observed that the achievable phase shift decreases when the required return loss increases.

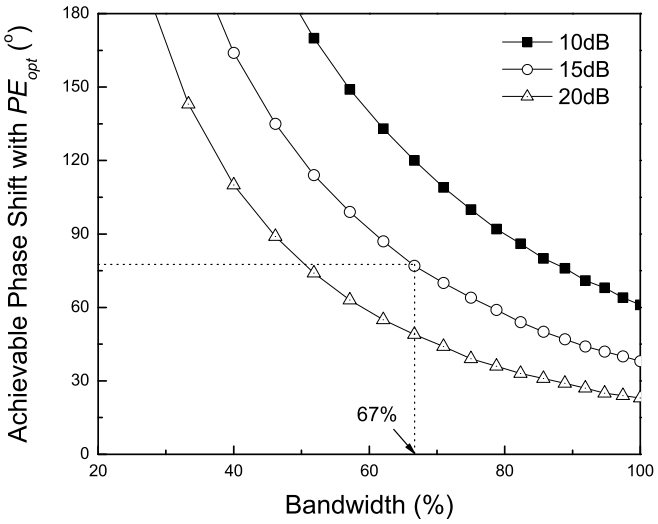


Fig. 4.11. Relation between the achievable phase shift with PE_{opt} and bandwidth for different return losses.

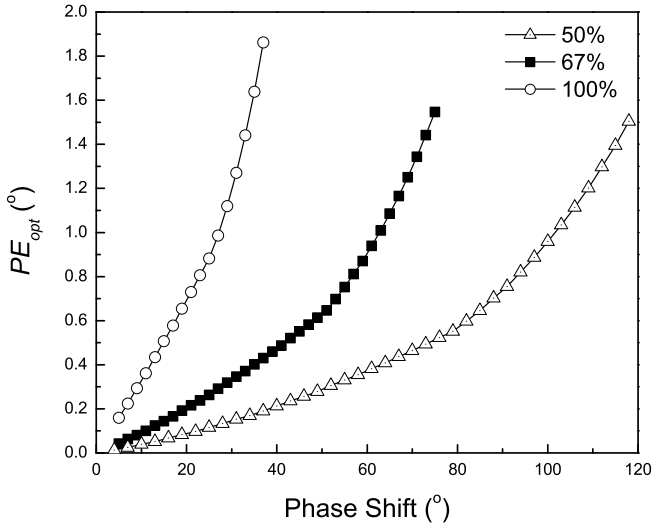


Fig. 4.12. PE_{opt} versus phase shift for a bandwidth of 50%, 67%, and 100% with a return loss of 15 dB.

The specific case of an octave bandwidth is also indicated in the figure. For a return loss of 15 dB the maximum achievable phase shift is 77°.

For a return loss requirement of 15 dB the relation between the optimum phase error and the required phase shift is shown in Fig. 4.12 for bandwidths of 50%, 67%, and 100%. Note that all three traces end at the point where the return loss requirement can no longer be met. For the design of an octave bandwidth four bit phase shifter, as discussed later, the topology with two poles is used for the 45° phase bit. As observed from Fig. 4.10, the topology with two poles still can not achieve a return loss of 15 dB for the 90° and 180° phase bits with an octave bandwidth.

4.1.3 Topology 3: BPF with three poles.

To achieve an improvement in the return loss for larger phase shifts a topology with three transmission poles is introduced. This topology with a single shunt $\lambda/4$ stub and two $\lambda/4$ transmission lines is shown in Fig. 4.13.

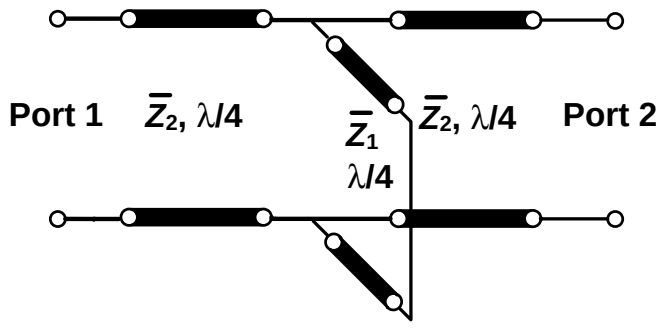


Fig. 4.13. Topology 3: Three pole bandpass filter.

The insertion phase of the triple pole bandpass filter is

$$\phi_{BPF}\left(\bar{\omega}\right)=\arctan\left[\frac{\bar{Z}_2-\Omega\bar{Z}_2^3-2\Omega^2\bar{Z}_1\left(\bar{Z}_2^2+1\right)}{2\Omega\bar{Z}_2\left(\bar{Z}_1+\bar{Z}_2-\Omega^2\bar{Z}_1\right)}\right] \tag{4-16}$$

There is one pole at $\bar{\omega}_c$ and two poles at

$$\bar{\omega}_{1,2}=1\pm\left[1-\frac{2}{\pi}\arctan\sqrt{\frac{\bar{Z}_2}{M}}\right] \tag{4-17}$$

where $M=2\bar{Z}_1-2\bar{Z}_1\bar{Z}_2^2-\bar{Z}_2^3$.

Note that the conditions $M>0$ and $\bar{Z}_2<1$ must be satisfied. When $\bar{Z}_2=1$, the topology reduces to the single stub topology of Fig. 4.2. When $\bar{Z}_2>1$, the return loss bandwidth is smaller than the single stub topology.

When three transmission poles exist, there are two frequencies between $\bar{\omega}_L$ and $\bar{\omega}_H$ where the return loss reaches a minimum. These frequencies are given by:

$$\bar{\omega}_{\min 1,2}=1\pm\left[1-\frac{2}{\pi}\arctan\sqrt{\frac{M+3\bar{Z}_2+\sqrt{\left(M+3\bar{Z}_2\right)^2+4M\bar{Z}_2}}{2M}}\right] \tag{4-18}$$

Similar to the topology with two poles, discussed in the previous section, there are two cases meeting the return loss requirement. This is illustrated in Fig. 4.14 for a return loss requirement of 15 dB. In case 1, the requirement is met at the band edges

$\bar{\omega}_L$ and $\bar{\omega}_H$ and exceeded in between them. In case 2 the requirement is exceeded at $\bar{\omega}_L$ and $\bar{\omega}_H$, and met at two frequencies in between them.

Similar to Fig. 4.10 the relation between optimum phase error and return loss is shown in Fig. 4.15 for the 45°, 90° and 180° phase bits with an octave bandwidth. It is observed that 45° and 90° phase bits can be achieved with respective phase errors of 0.2° and 1.1° over an octave bandwidth with a minimum return loss of 15 dB. The 180° phase bit can only achieve a return loss of 12.8 dB, with an associated phase error of 4.7°. Therefore, two cascaded 90° phase bits are used for the 180° to achieve a larger return loss and a smaller phase error. As a drawback, cascading two sections requires a larger area than a single section.

The procedure to obtain $\bar{Z}_1$ and $\bar{Z}_2$ is the same as the procedure given in Topology 2. However, (4-16) is used for the insertion phase of the BPF and the S_{11} for the three-pole BPF, also provided in Appendix B, is used. In Fig. 4.16 the achievable phase shift versus bandwidth is shown for return losses of 10 dB, 15 dB, and 20 dB. For a bandwidth of 67% and a return loss of 15 dB the maximum achievable phase shift is 157°.

Finally, in Fig. 4.17 the optimum phase error versus phase shift is shown for bandwidths of 50%, 67%, and 100% with a return loss of 15 dB. The bandwidth of 30% is not shown, because the topologies with one or two poles are better suited for it from a circuit size point of view.

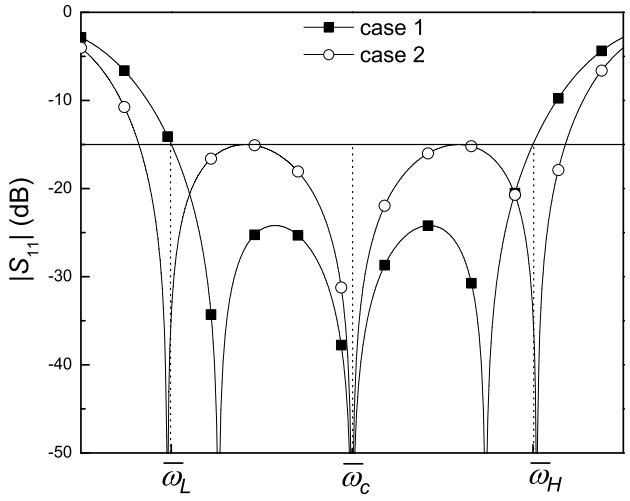


Fig. 4.14. Return loss of BPF with three poles. In case 1 the return loss requirement is met at $\bar{\omega}_L$ and $\bar{\omega}_H$. In case 2 the return loss requirement is met at two frequencies between $\bar{\omega}_L$ and $\bar{\omega}_H$.

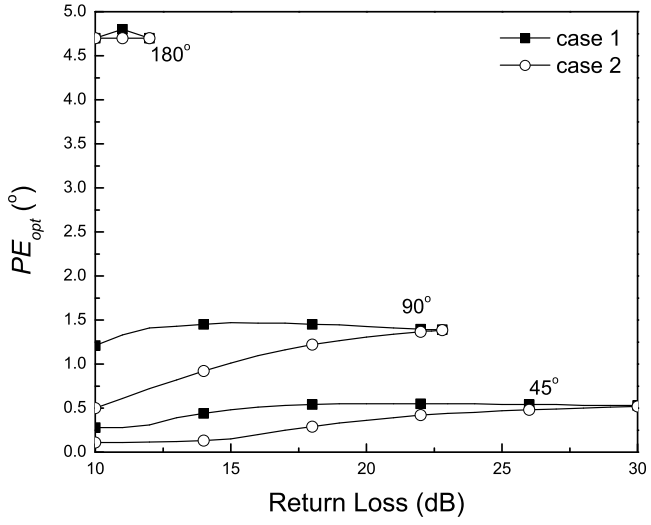


Fig. 4.15. Optimum phase error PE_{opt} versus return loss for 45°, 90°, and 180°phase bits with an octave bandwidth.

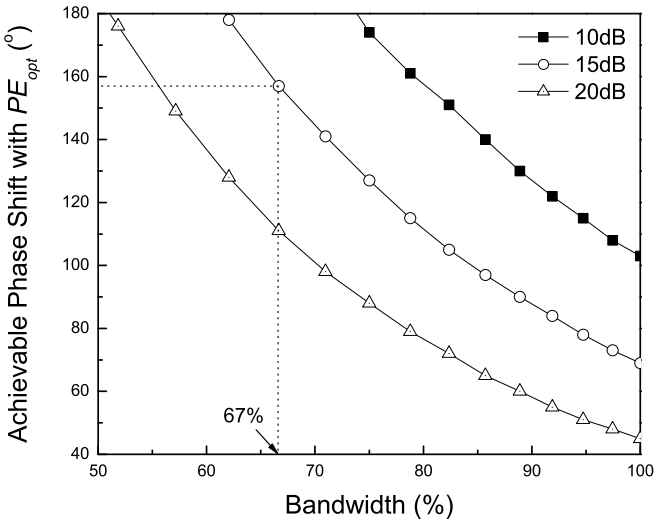


Fig. 4.16. Achievable phase shift with PE_{opt} versus bandwidth for a return loss of 10, 15, and 20 dB.

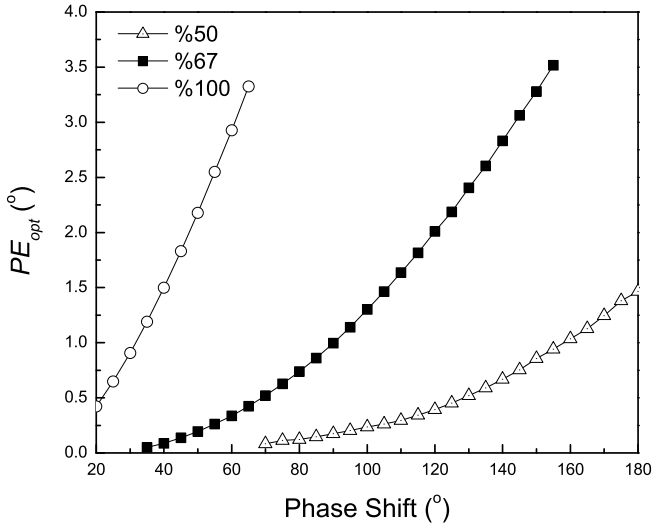


Fig. 4.17. Optimum phase error PE_{opt} versus phase shift for bandwidths of 50%, 67%, 100% with a return loss of 15 dB.

In case of large phase shifts the required shunt stub impedance is low necessitating very broad microstrip transmission lines. To raise the impedance level, the T-topology can be transformed to a π-topology. Both topologies have the same response.

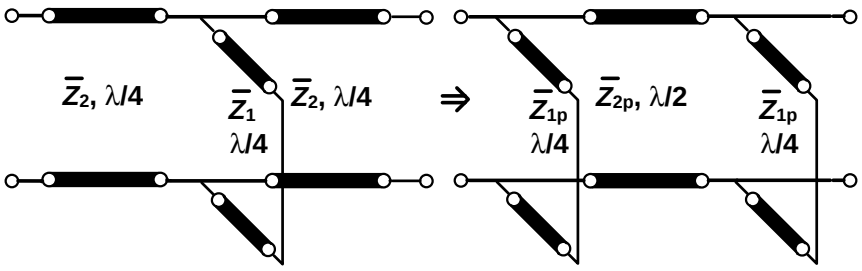


Fig. 4.18. Transformation of the T-topology to the π-topology to increase the required transmission line impedances.

This transformation is depicted in Fig. 4.18 and the associated transformation formulas are given by:

$$\bar{Z}_{1p} = 2\bar{Z}_1 + \bar{Z}_2$$
$$\bar{Z}_{2p} = \bar{Z}_2 + \frac{\bar{Z}_2^2}{2\bar{Z}_1} \qquad (4\text{-}19)$$

From (4-19) it is observed that the impedances of the Π-topology are larger than the impedances of the T-topology.

4.1.4 Influence of SPDT switches

Because transmission lines with relatively long electrical lengths are used, the

non-ideal performance of the SPDT switches can introduce resonances. This problem is solved by using SPDT switches with a small off-capacitance or by employing the resistive loading technique introduced in [87]. Because two SPDT switches are used per bit, the insertion loss of the switches should be as low as possible.

4.1.5 Design of binary phase bits

The three topologies and the method to find $\bar{Z}_1$ and $\bar{Z}_2$ are used to determine the design parameters of phase bits with bandwidths of 30%, 50%, 67% and 100% and binary phase shifts of 22.5º, 45º, 90º and 180º. The design parameters are listed in Table 4.1. The return loss and the phase error are provided for each case. Based on Table 4.1, individual phase bits covering the L-band (1-2 GHz) are designed. The phase errors of the first three bits are below ±1.1º. For the 90 º phase bit the transformation of Fig. 4.18 is used and for the 180º phase bit, two sections of 90º are cascaded to achieve the required return loss. All four phase bits are simulated using ADS Momentum and the effect of the T-junctions connecting the stubs and the transmission lines are included in the results. The four individual phase bits, without the switches, were fabricated on Rogers Duroid 5870 (ε_r=2.33, h=31 mils). The comparison between simulated and measured results of the four phase bits is shown in Fig. 4.19. The measured phase error of the 90º and 180º bits increases to ±2.1º and ±5.2º, respectively due to the effect of the T-junctions. The phase error of the 45º and 22.5º bits is less than ±2º.

TABLE 4. 1
DESIGN PARAMETERS FOR 4-BIT PHASE SHIFTERS

BW (%)	$\Delta\phi(\bar{\omega}_c)$ (º)	Topology	$\bar{Z}_1$	$\bar{Z}_2$	RL (dB)	PE (º)
30	22.5	1	2.0266		24.5	0.02
	45	1	1.0106		18.5	0.03
	90	2	1.0392	1	21.9	0.17
	180	2	0.5229	0.9734	15.0	0.60
50	22.5	1	2.0766		20.0	0.07
	45	2	2.1411	1	20.5	0.25
	90	2	1.0688	0.9633	15.0	0.73
	180	3†	0.0788	0.3939	15.0	1.50
67	22.5	1	2.1428		17.5	0.18
	45	2	2.2456	1	16.1	0.55
	90	3†	0.2552	0.5282	15.0	1.10
	180	3*	0.2886	0.6049	19.0	3.10
100	22.5	2	4.9773	1	16.2	0.80
	45	3	0.7828	0.6533	15.0	1.90
	90	3*	0.8797	0.7157	18.2	5.20
	180	3**	0.8797	0.7157	16.0	9.30

†: The low impedance can be converted to a higher impedance using (4-19).
*: Two sections are cascaded.
**: Four sections are cascaded.

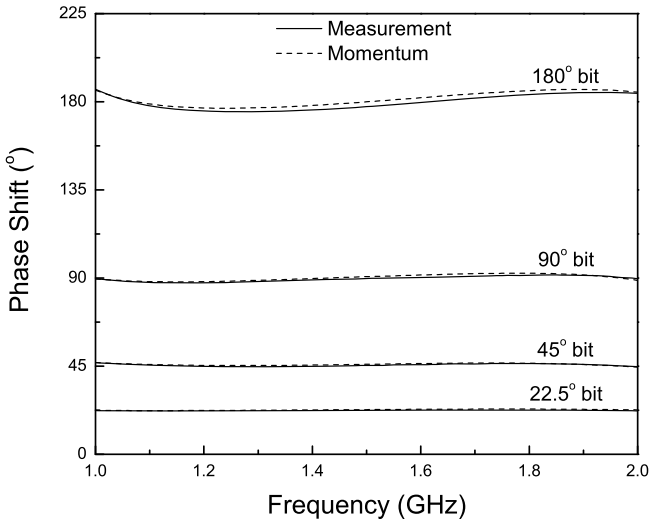


Fig. 4.19. Comparison of the phase response of the four phase bits.

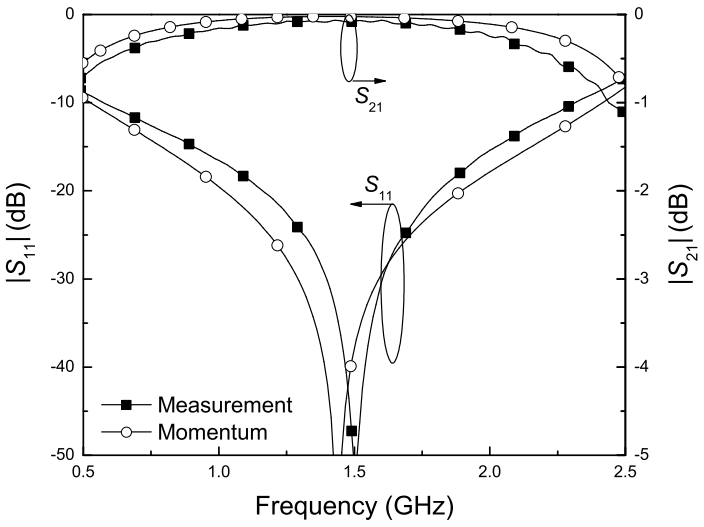


Fig. 4.20. 22.5º BPF comparison.

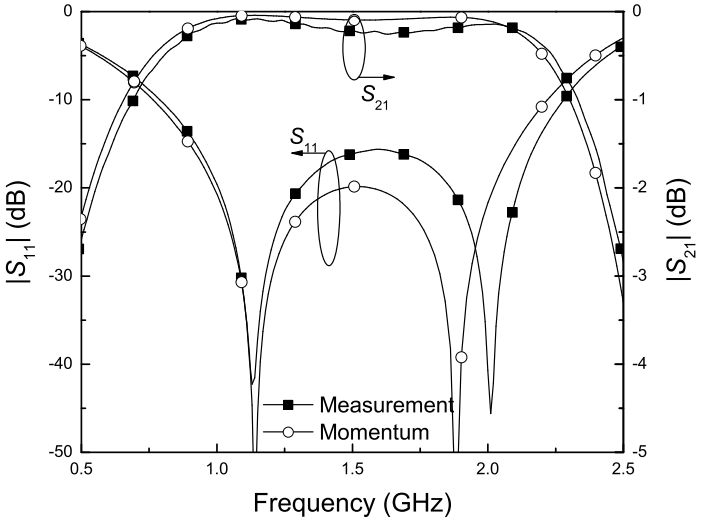


Fig. 4.21. 45º BPF comparison.

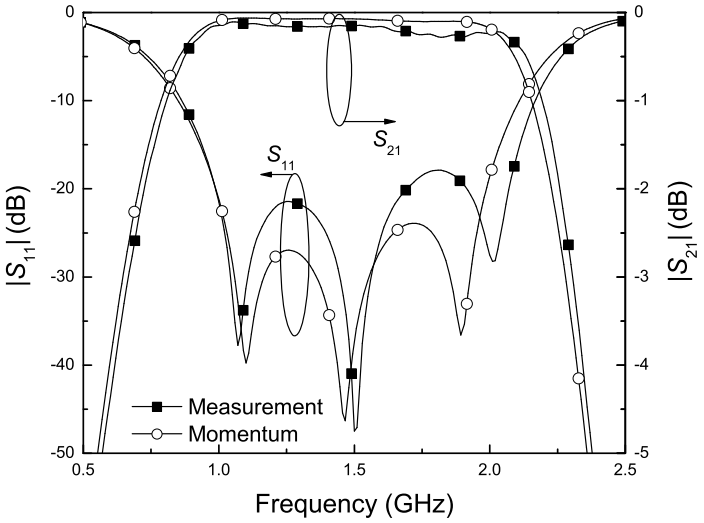


Fig. 4.22. 90º BPF comparison.

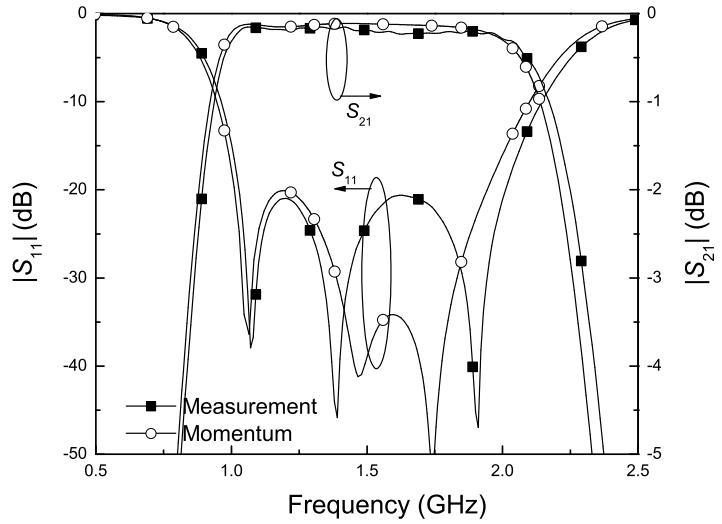


Fig. 4.23. 180º BPF comparison.

A comparison between the measured and simulated insertion loss and return loss of the BPF branches without the switches are provided from Fig. 4.20 to Fig. 4.23. The simulated and measured TL branches are not shown because their characteristic impedances are 50 Ω and their return losses are low. The measured insertion loss of the TL branches is between 0.1 and 0.2 dB. The return loss of the 22.5º and 45º bits is greater than 16 dB and the return loss of the 180º and 90º bits is greater than 18 dB over the whole L-band. These high return losses provide a good match between the individual phase bits when they are cascaded.

4.1.6 Four-bit L-band phase shifter

Based on the individual 22.5º, 45º, 90º, and 180º bits a complete four-bit phase shifter is designed. Hittite HMC545E SPDT switches with an insertion loss of 0.25 dB to 0.3 dB and an isolation better than 30 dB below 2 GHz are used. In total, eight SPDT switches are used for the complete phase shifter design. MuRata decoupling capacitors are used for the realization.

The 16 phase shifts are shown in Fig. 4.24 and the RMS phase error is shown in Fig. 4.25. Note that the Momentum simulation results of the branches are imported into ADS and the measured S-parameters of the switches are used to simulate the phase shifter. The measured RMS phase error is less than 3.6º over the entire L-band. The measured and simulated insertion loss from 0.2 GHz to 3 GHz for all 16 states is shown in Fig. 4.26. The band pass filter behavior is clearly visible. The inset of Fig. 4.26 shows the detailed response in the passband. The measured insertion loss of the phase shifter for all 16 states varies between 3 dB and 4 dB and the worst amplitude imbalance is 0.8 dB at 1.24 GHz. For other frequencies in the L-band, the amplitude imbalance is less than 0.5 dB. The measured and simulated return loss is shown in Fig. 4.27. The measured return loss of the phase shifter for all states is larger than 12 dB from 1.02 GHz to 2.1 GHz and larger than 15 dB from 1.06 GHz to 1.95 GHz. The measured group delay for the 16 states is shown in Fig. 4.28. The group delay varies between 2.8 ns and 3.5 ns from 1 GHz to 2 GHz. The measured RMS amplitude imbalance is less than 0.2 dB, which is shown in Fig. 4.29. Finally, the measured IIP_3

of the phase shifter is shown in Fig. 4.30. Note that the linearity of this phase shifter is determined by the SPDT switches.

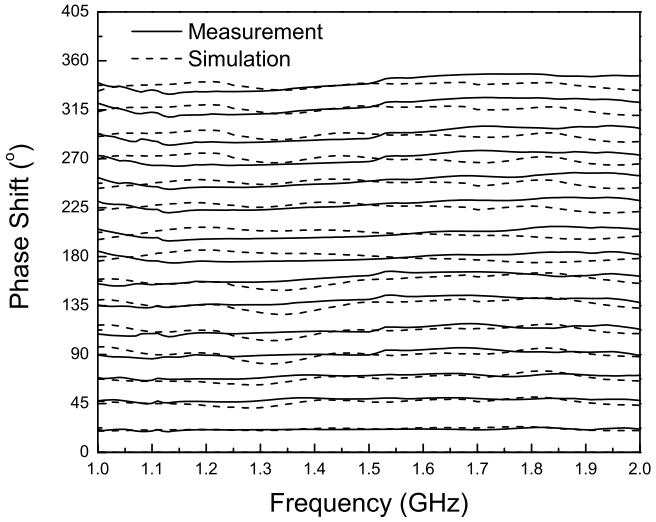


Fig. 4.24. Measured and simulated phase shifts for the 16 states.

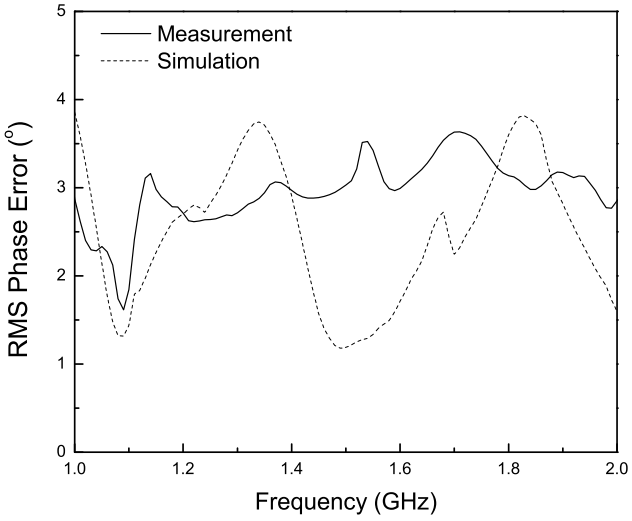


Fig. 4.25. Measured and simulated RMS phase error.

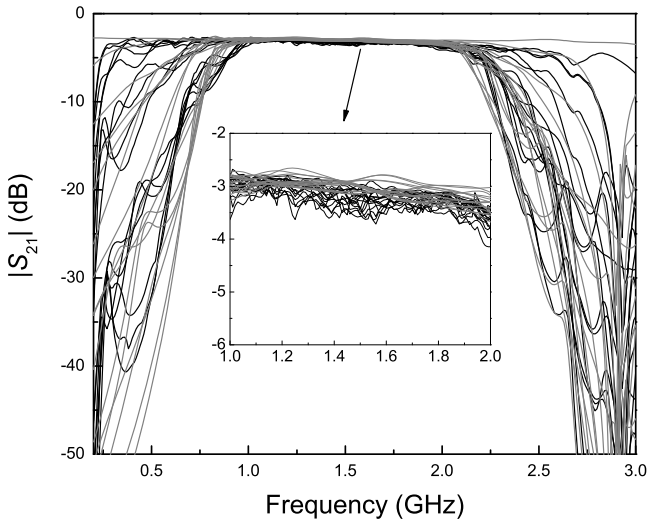


Fig. 4.26. Measured (black) and simulated (gray) insertion loss for the 16 states.

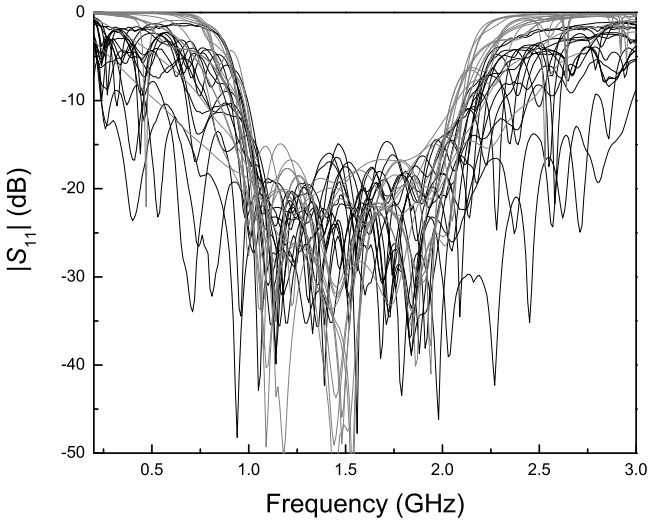


Fig. 4.27. Measured (black) and simulated (gray) return loss for the 16 states.

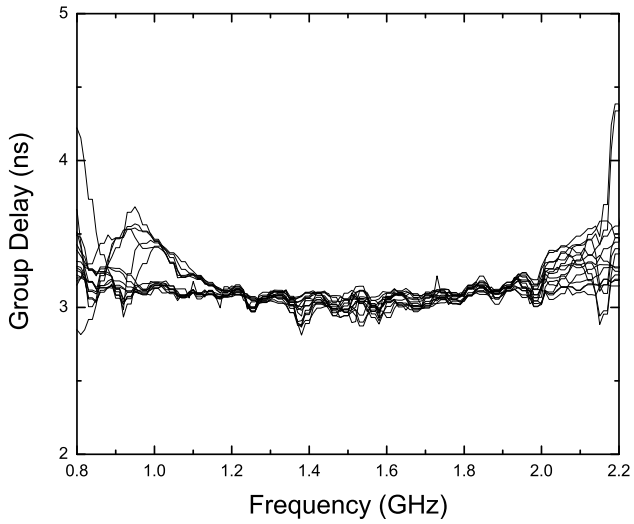


Fig. 4.28. Measured group delays for all 16 states.

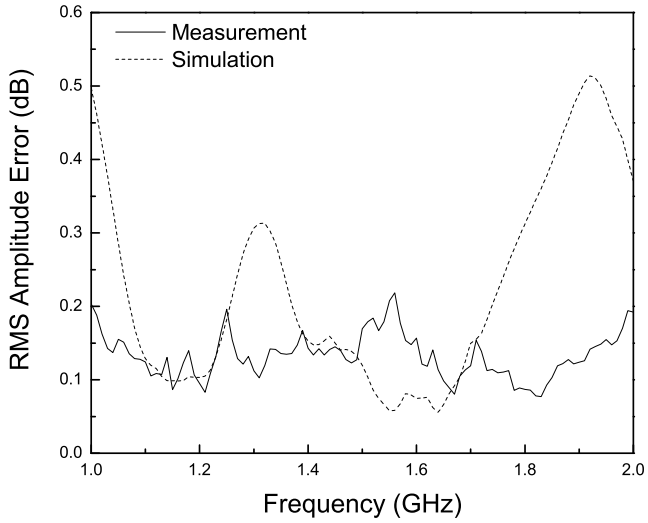


Fig. 4.29. Measured and simulated RMS amplitude imbalance.

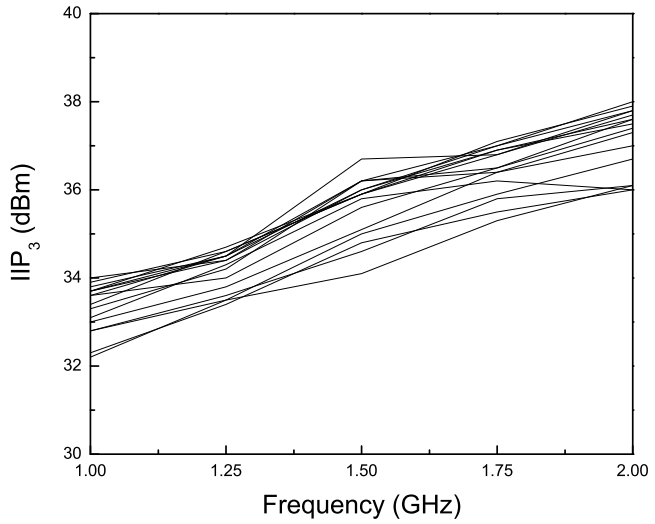


Fig. 4.30. Measured IIP_3 for all 16 states.

4.1.7 Discussions on size and insertion loss reduction

The size of the proposed phase shifter depends on the frequency of operation because λ/4 stubs are used. The size can be reduced by employing substrates with a higher permittivity. For example, by increasing ε_r from 2.33 to 10.2, the length of the lines is approximately halved. By using stripline instead of microstrip the effective dielectric constant can be raised further, and the size can be further reduced. The layout can also be made more compact with the aid of EM tools to accurately assess and mitigate undesired couplings, which can reduce the area by 40-50%. Various miniaturization techniques can also aid in reducing the size [78], [79]. Note that these techniques can not be easily applied to phase shifters using coupled lines. Finally, by using multilayer substrate techniques the total area can be further reduced. However, cavities will be

required for the discrete switches and the discrete capacitors.

The measured insertion loss of the BPF branches and the SPDT switches for the four bits are listed in Table 4.2. It is found that the insertion loss from the switches contributes approximately 70% of the total insertion loss. When low loss switches are used, such as MEMS switches, the insertion loss of the phase shifter can be reduced further.

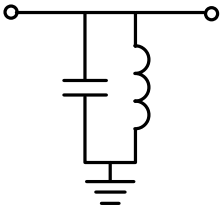
TABLE 4.2
MEASURED INSERTION LOSS

Phase	22.5º	45º	90º	180º
BPF branch (dB)	0.1-0.25	0.1-0.25	0.1-0.3	0.2-0.3
TL branch (dB)	0.08-0.13	0.09-0.15	0.1-0.19	0.15-0.25
2 x SPDT (dB)	0.6	0.6	0.6	0.6
Total (dB)	0.68-0.85	0.69-0.85	0.7-0.9	0.75-0.9
Four Bit (dB)	2.8-4.0			

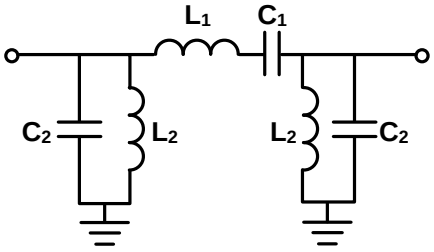
4.2 Phase Slope Alignment Using LC Resonators

Resonators employing inductors and capacitors can also be used to control the phase slope. Fig. 4.31 shows series and parallel LC resonators and their combination. The combination of one series and two shunt parallel LC resonators shown in Fig. 4.31(c) is actually a BPF. Both of the two types of resonators can be used to control the phase slope. Therefore, the insertion phase slope of the BPF can be controlled to achieve the best alignment with the insertion phase of the reference state over a large bandwidth.

(a)



(b)



(c)

Fig. 4.31. The (a) series (b) parallel LC resonators and their (c) combination.

How to control the phase slope using a single LC resonator is first described. For a series LC resonator resonating at ω_0, the *S*-parameters are found as

$$S_{11} = \frac{j\bar{X}\left(\bar{\omega} - \bar{\omega}^{-1}\right)}{2 + j\bar{X}\left(\bar{\omega} - \bar{\omega}^{-1}\right)}$$
$$S_{21} = \frac{2}{2 + j\bar{X}\left(\bar{\omega} - \bar{\omega}^{-1}\right)} \qquad (4\text{-}20)$$

where $\bar{X} = \omega_0 L / Z_0 = 1/\omega_0 C Z_0$ and $\bar{\omega} = \omega/\omega_0$.

For a shunt parallel LC resonator resonating at ω_0, the *S*-parameters are found as

$$S_{11} = \frac{-j\bar{B}\left(\bar{\omega} - \bar{\omega}^{-1}\right)}{2 + j\bar{B}\left(\bar{\omega} - \bar{\omega}^{-1}\right)}$$
$$S_{21} = \frac{2}{2 + j\bar{B}\left(\bar{\omega} - \bar{\omega}^{-1}\right)} \tag{4-21}$$

where $\bar{B} = \omega_0 C Z_0 = Z_0 / \omega_0 L$.

From (4-20) and (4-21), it is found that when $\bar{X} = \bar{B}$, the $|S_{11}|$ and the insertion phase of the two types of LC resonators are the same. For reason of brevity, only the response of the shunt LC resonator is plotted in Fig. 4.32. $\bar{B}$ is used as the design parameter and $r = \bar{X} / \bar{B}$. From Fig. 4.32, a steeper phase slope is obtained with a smaller return loss bandwidth for a single LC resonator when $\bar{B}$ increases.

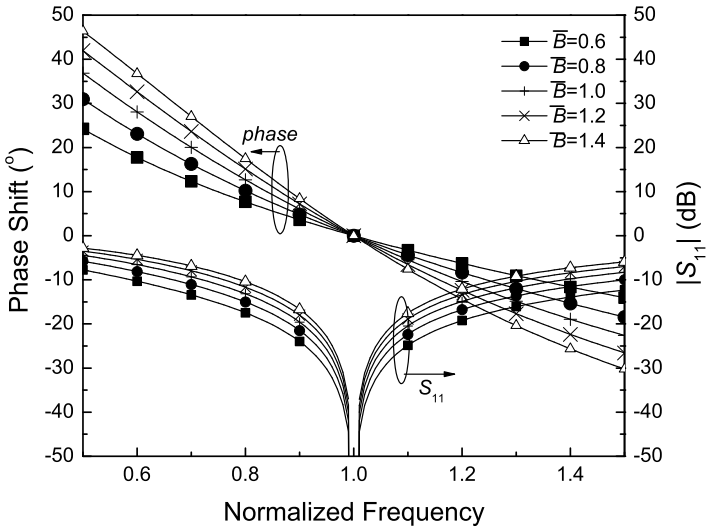


Fig. 4.32. Influence of $\bar{B}$ on the phase and $|S_{11}|$.

The return loss bandwidth can be increased by changing the single LC resonator to a BPF as shown in Fig. 4.31(c). The normalized returned power of the BPF can be written as

$$\left|S_{11}(\bar{\omega})\right|^2 = \frac{f(\bar{\omega})\left\{r\bar{B} - \left[2 - r\bar{B}^2 f(\bar{\omega})\right]^2\right\}^2}{2\left[1 - r\bar{B}^2 f(\bar{\omega})\right]^2 + f(\bar{\omega})\left\{r\bar{B} + \left[2 - r\bar{B}^2 f(\bar{\omega})\right]^2\right\}^2} \tag{4-22}$$

where $f(\bar{\omega}) = \left(\bar{\omega} - \frac{1}{\bar{\omega}}\right)^2$.

It is found that the following equation always holds:

$$\left|S_{11}(\bar{\omega})\right|^2 = \left|S_{11}\left(\frac{1}{\bar{\omega}}\right)\right|^2 \tag{4-23}$$

Therefore, the response is logarithmically symmetric around ω_0, which fits the definition of an equal-ripple filter prototype [88]. The transmission poles can be found when $|S_{11}(\bar{\omega})|=0$. It is obvious that one transmission pole always exists at the center frequency. The extra transmission poles can be found by solving

$$\left(\bar{\omega} - \frac{1}{\bar{\omega}}\right)^2 = \frac{1}{r\bar{B}^2}(2 - r) \tag{4-24}$$

The solutions are given by:

$$\bar{\omega}_{r1,2} = \left[\frac{1}{2} \left(\frac{1}{\bar{B}} \sqrt{\frac{1}{r}(2-r)} + \sqrt{\frac{1}{r\bar{B}^2}(2-r)+4} \right) \right]^{\pm 1} \tag{4-25}$$

Fig. 4.33 shows an example of the comparison between a single LC resonator and the BPF. The 15 dB return loss bandwidth increases from 9.4% for the single LC resonator to 82% for the BPF. In Fig. 4.33, a maximum reflection coefficient (MRC) is introduced, which is a result of the equal-ripple response. The MRC for the BPF in Fig. 4.33 is -18 dB. It is found that the MRC is determined by *r*. The relation between *r* and the MRC is shown in Fig. 4.34. When *r*<2, a Chebyshev response is found, and when *r*=2, a Butterworth response is found.

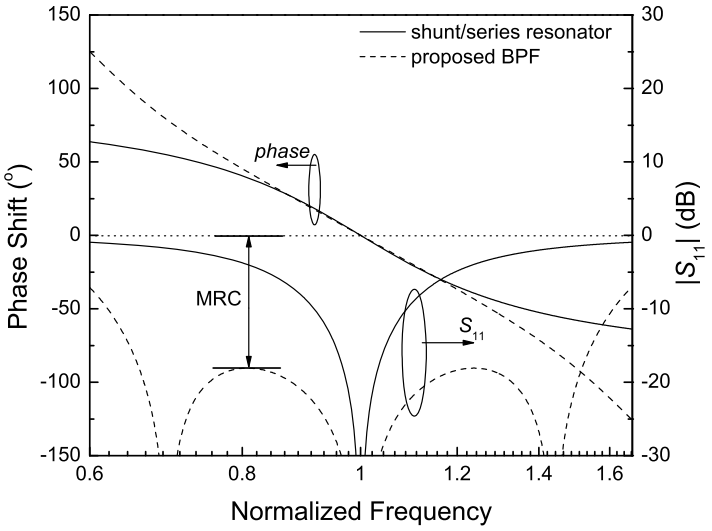


Fig. 4.33. Phase shift and return loss for a single LC resonator and a BPF.

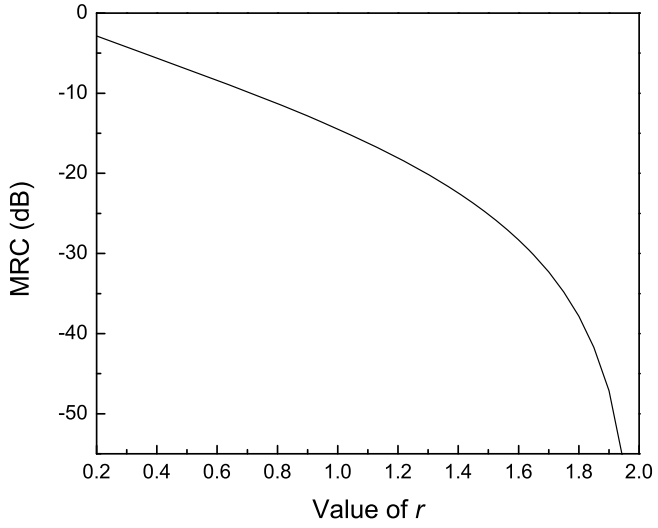


Fig. 4.34. Relation between parameter r and the maximum reflection coefficient (MRC).

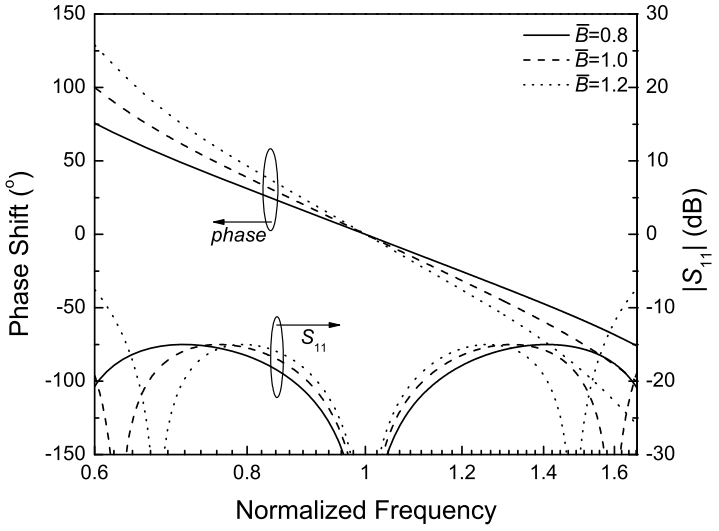


Fig. 4.35. Influence of $\overline{B}$ on the phase and return loss when r is fixed to obtain 15 dB return loss.

When r is fixed to achieve a certain MRC, the response of the BPF is determined by $\overline{B}$. Fig. 4.35 shows how $\overline{B}$ influences the phase and the return loss when the MRC is -15 dB.

A combination of BPF and APN can be used for 180º phase shifter design, as shown in Fig. 4.36. Because the insertion phase of the BPF at ω_0 is zero, the transition frequency of the APN should be located at ω_0 to achieve a phase shift of 180º. The insertion phase of the APN is then given by

$$\phi_{APN}\left(\overline{\omega}\right) = -180° - 2\tan^{-1}\left(\overline{\omega} - \overline{\omega}^{-1}\right) \tag{4-26}$$

At the resonant frequencies calculated in (4-25), the insertion phase of the BPF is only related to the parameter r:

$$\phi_{BPF} = \pm\tan^{-1}\frac{\sqrt{r\left(2-r\right)}}{1-r} \tag{4-27}$$

The ϕ_{APN} at the boundary frequency is calculated using (4-26). To achieve a 180º phase difference at the two resonant frequencies, ϕ_{BPF} must be equal to $\phi_{APN} + 180°$ at ω_0. Under this condition, $\overline{B}$ is found to be 1 from (4-25), (4-26) and (4-27). The performance is then only determined by the parameter r, which can be obtained from (4-25). Therefore, the phase response is affected by the resonant frequency $\overline{\omega}_{r1}$.

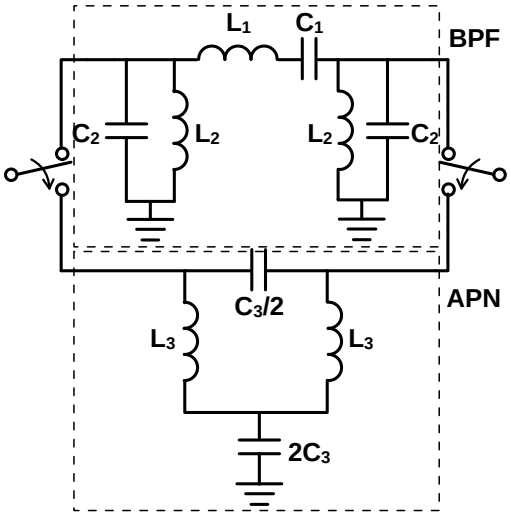


Fig. 4.36. 180º phase shifter switching between a BPF and an APN.

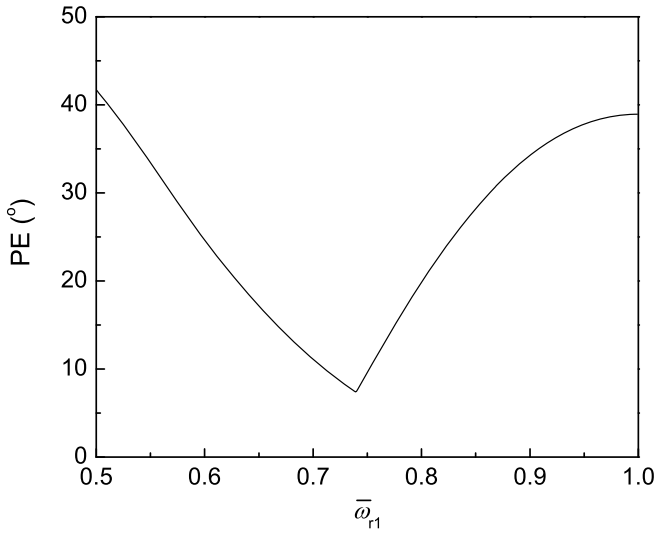


Fig. 4.37. The phase error versus $\bar{\omega}_{r1}$.

For an octave bandwidth, the resulting phase error versus $\bar{\omega}_{r1}$ is plotted in Fig. 4.37, and the optimum phase error is found to be 7.4º when $\bar{\omega}_{r1} = 0.74$. The other frequency with an exact 180º phase shift is at $\bar{\omega}_{r2} = 1/0.74 = 1.35$. The corresponding r=1.45 is calculated from (4-25) to (4-27), and the associated return loss is 23.8 dB from Fig.

4.34. The phase shift response is shown in Fig. 4.38 from ω_L to ω_H. Compared to the conventional HP/LP network topology shown in Fig. 3.7, the much larger return loss makes it possible to cascade the 180º phase bit with other phase bits to realize a one octave multi-bit binary phase shifter.

Further study of the optimum phase error using the proposed topology for different bandwidth is shown in Fig. 4.39. The optimized phase errors are obtained with the design method described in this section. The conventional third-order HP/LP topology is also shown for comparison. The phase error over an octave bandwidth is improved from 25º to 7.4º. When the 180º phase shifter is cascaded with the optimized high-pass/low-pass phase shifters designed from Chapter 3, the overall performance can be improved.

Fig. 4.40 to Fig. 4.42 show the comparison between two four-bit phase shifters, one uses the proposed method and the other one uses the conventional method. The return loss is shown in Fig. 4.40 and the conventional design has a return loss of 5 dB at the frequency boundaries while the proposed design achieves a return loss larger than 19 dB. Fig. 4.41 and Fig. 4.42 show the phase shift and the RMS phase error over the octave bandwidth. It is observed that the RMS phase error is improved from 13.5º to 4.3º.

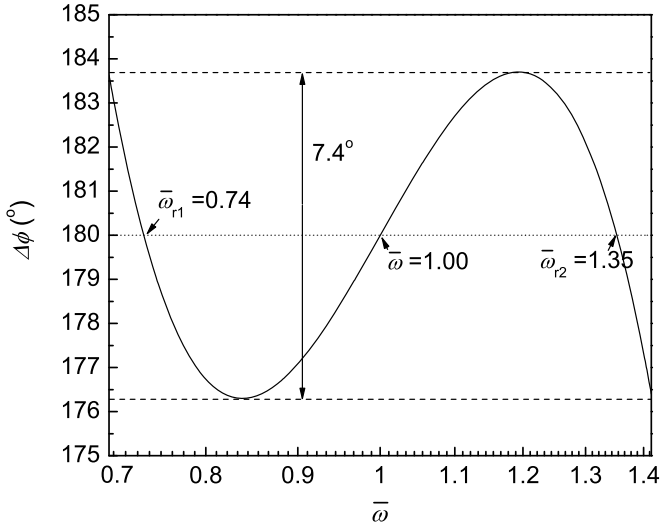


Fig. 4.38. The 180º phase bit with optimum phase shift response for the octave band.

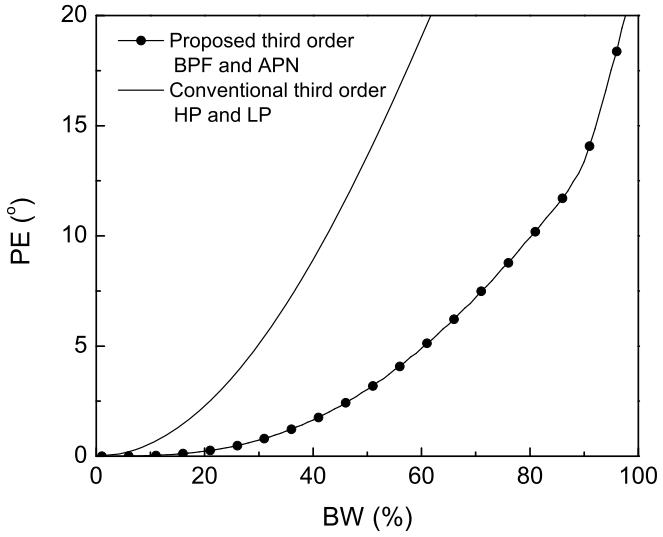


Fig. 4.39. Phase error comparison between the proposed 180º phase bit and the conventional high-/low-pass network phase bit.

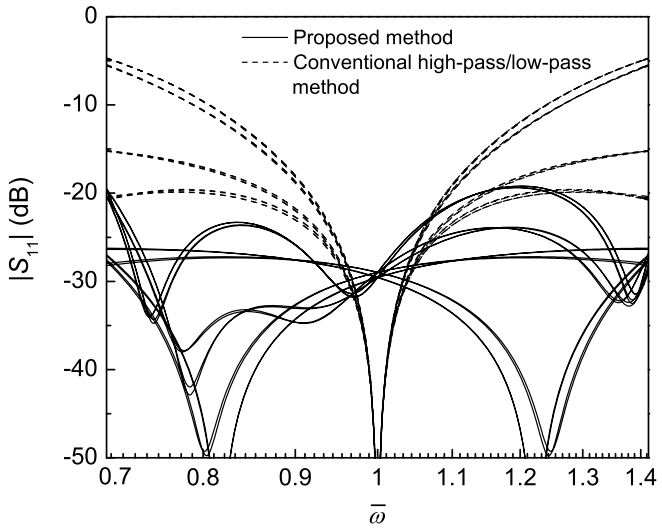


Fig. 4.40. Return loss comparison for all 16 phase bits.

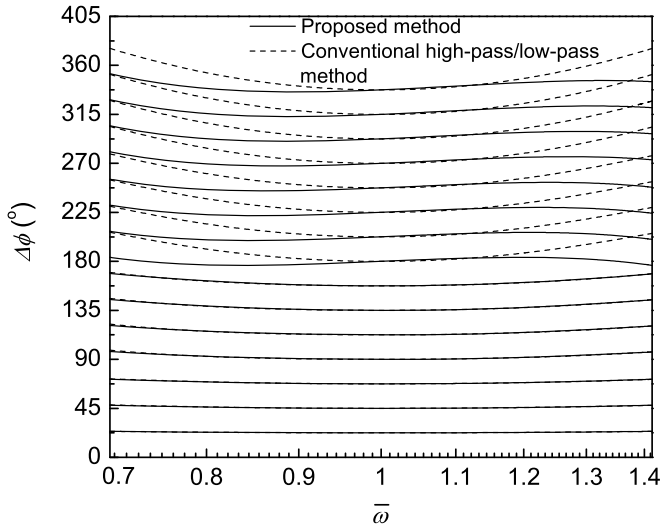


Fig. 4.41. 16 phase states of the proposed topology and the conventional topology.

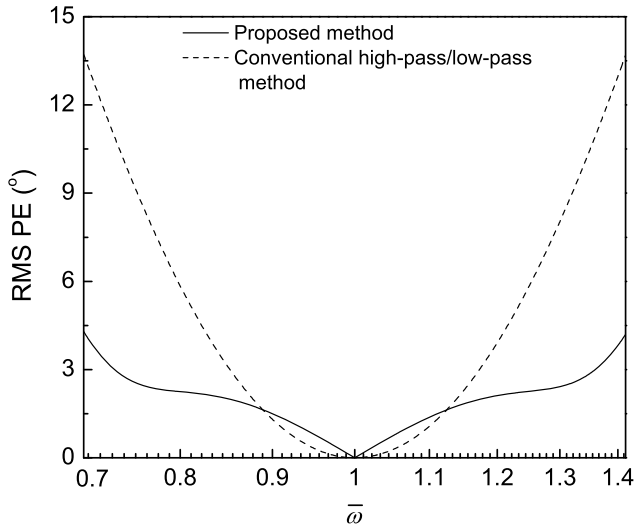
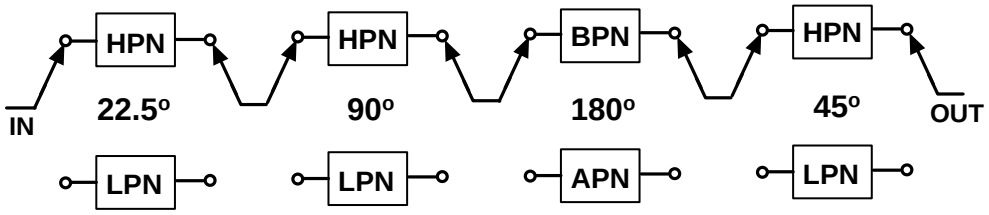
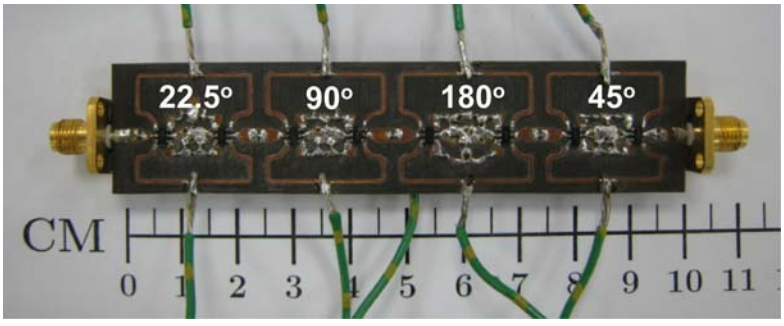


Fig. 4.42. RMS phase error comparison.



(a)



(b)

Fig. 4.43. (a) Block diagram of the four-bit phase shifter, and (b) fabricated four-bit phase shifter (500 MHz to 1 GHz).

To validate the proposed method, a four-bit phase shifter from 500 MHz and 1000 MHz is designed and measured. Discrete inductors and capacitors from Murata's LQW series and GJM series are used. The values of the ideal components and the practically available components are listed in Table 4.3. SPDT switches from Hittite (HMC545) are chosen in the design. The maximum insertion loss of a single SPDT switch is 0.23 dB from 500 MHz to 1000 MHz. Rogers Duroid 5880 with ε_r =2.33 and a height of 31 mils is used. A diagram and a photograph of the phase shifter are shown in Fig. 4.43 (a) and Fig. 4.43 (b).

TABLE 4.3.
COMPONENT VALUE FOR DESIGN

	22.5º	45º	90º	180º
L_1 (nH)	58 (75)†	29.4 (33)	16.7 (18)	16.4 (15)
L_2 (nH)	2.2 (2.2)	4.3 (4.1)	7.6 (7.5)	11.3 (11)
L_3 (nH)	--	--	--	11.3 (10)
C_1 (pF)	46 (47)	22.6 (18)	10.4 (10)	3.1 (3.0)
C_2 (pF)	0.4 (0.6)	0.9 (1.0)	2.0 (2.0)	4.5 (4.3)
$C_3/2$ (pF)	--	--	--	2.3 (2.4)
$2C_3$ (pF)	--	--	--	9.2 (9.1)

†format: ideal value (practical value)

The measured performance is shown from Fig. 4.44 to Fig. 4.47. The return loss is shown in Fig. 4.44 for all 16 phase states. The measured return loss is above 13 dB from 530 MHz to 1100 MHz. Fig. 4.45 shows that the insertion loss varies from 2.3 dB to 3 dB over the frequency band and the amplitude imbalance at any frequency is

less than 0.6 dB. The worst amplitude imbalance of 0.6 dB is found near 800 MHz. In total eight SPDT switches are used in the design, which introduces a total insertion loss of 1.6 dB to 1.8 dB. Fig. 4.46 shows the phase shifts of the 16 states and Fig. 4.47 shows the RMS phase error. A RMS phase error of less than 5.9º from 500 MHz to 1090 MHz is observed. Note that practical values of the capacitors and inductors differ from the ideal values, which influences the performance of the phase shifter.

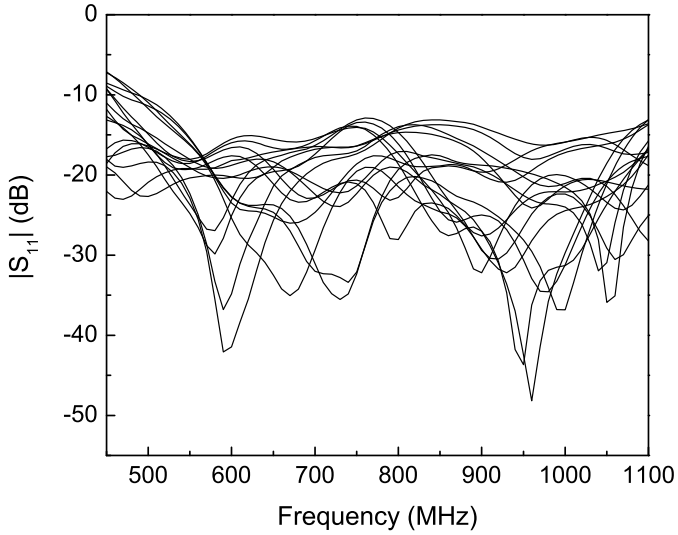


Fig. 4.44. Measured return loss for all 16 phase bits.

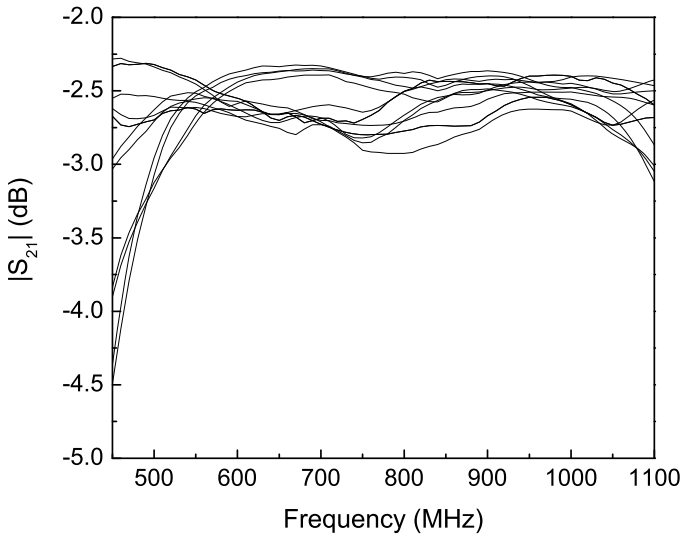


Fig. 4.45. Measured insertion loss for all 16 phase states.

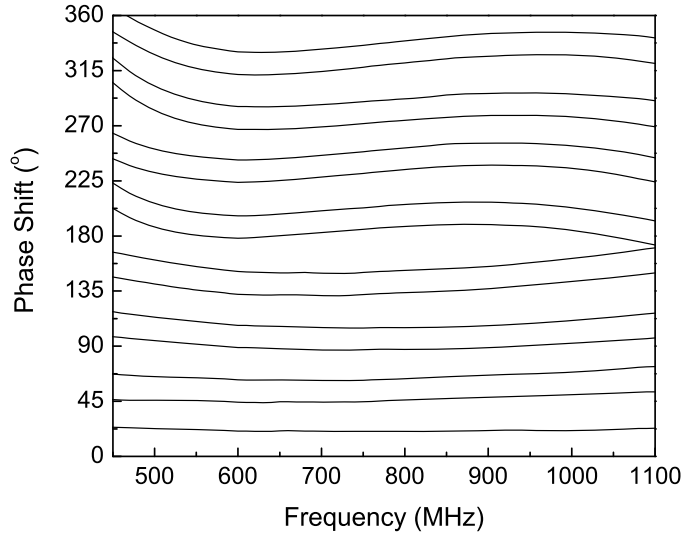


Fig. 4.46. Measured phase shifts for all 16 phase states.

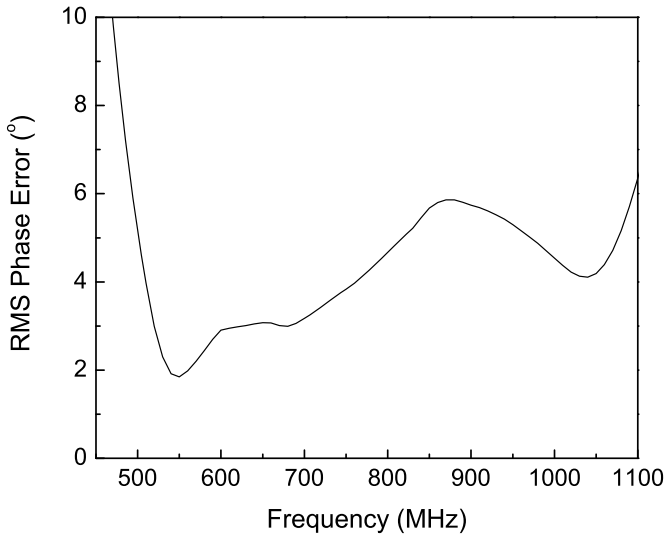


Fig. 4.47. RMS phase error of the measured phase shifts.

4.3 Phase Slope Alignment Using Both Quarter Wavelength Stubs and LC Resonators

The distributed components and the discrete components can also be combined as shown in Fig. 4.48. For the BPF branch, the magnitude of the returned power is given by

$$|S_{11}|^2 = \frac{\left[\bar{X}_R + \frac{1}{\bar{Z}_\theta \tan\theta}\left(2 + \frac{\bar{X}_R}{\bar{Z}_\theta \tan\theta}\right)\right]^2}{4 + \bar{X}_R^2\left(1 - \frac{1}{\bar{Z}_\theta^2 \tan^2\theta}\right) + \frac{1}{\bar{Z}_\theta^2 \tan^2\theta}\left(2 + \frac{\bar{X}_R}{\bar{Z}_\theta \tan\theta}\right)^2} \qquad (4\text{-}28)$$

where $\theta = \bar{\omega} \times \frac{\pi}{2}$, $\bar{Z}_\theta$ is the normalized impedance of the shunt TLs, $\bar{X}_R = \bar{X}_L - \bar{X}_C = \omega L / Z_0 - 1/\omega C Z_0$, and $\bar{X}_L$ and $\bar{X}_C$ represent the normalized reactance of the inductor and capacitor.

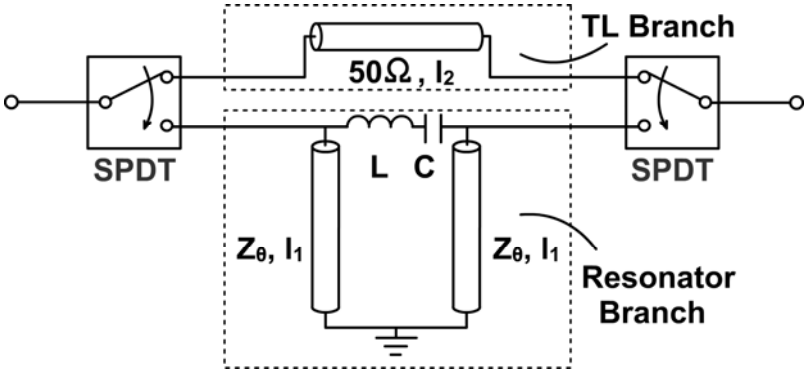


Fig. 4.48. Broadband 180˚ and 90˚ phase shifter topology.

Assume that at the center frequency ω_0, $\bar{X}_L = \bar{X}_C = X_O$, then

$$\bar{X}_R = X_O\left(\bar{\omega} - \frac{1}{\bar{\omega}}\right) \tag{4-29}$$

The return loss in equation (4-28) is then determined by $\bar{Z}_\theta$ and X_O when the frequency changes. Fig. 4.49 shows the relation between the 10 dB return loss BW, $\bar{Z}_\theta$ and X_O.

When the return loss BW is large, the overall BW of the phase shifter is limited by the phase error BW. The insertion phase of the BPF branch is given by

$$\phi_{BPF} = \tan^{-1}\left[\frac{\left(2-\bar{X}_R\right)\bar{Z}_\theta^2\tan^2\theta + \bar{X}_R}{2\bar{Z}_\theta\tan\theta\left(\bar{Z}_\theta\tan\theta + \bar{X}_R\right)}\right] \tag{4-30}$$

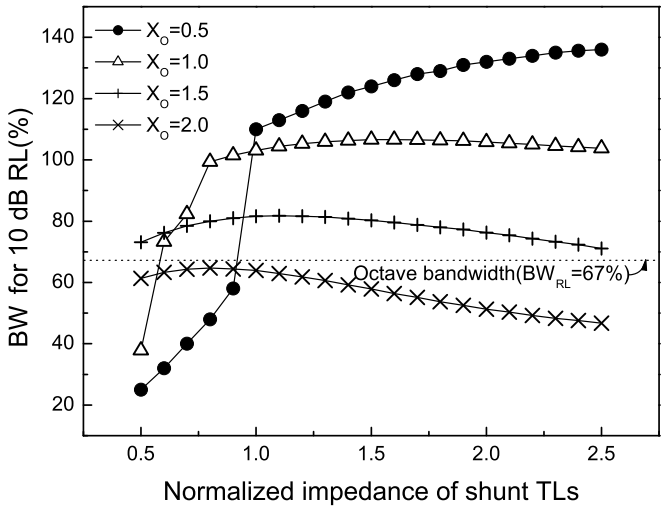


Fig. 4.49. 10 dB return loss bandwidth versus $\overline{Z}_\theta$ and X_O.

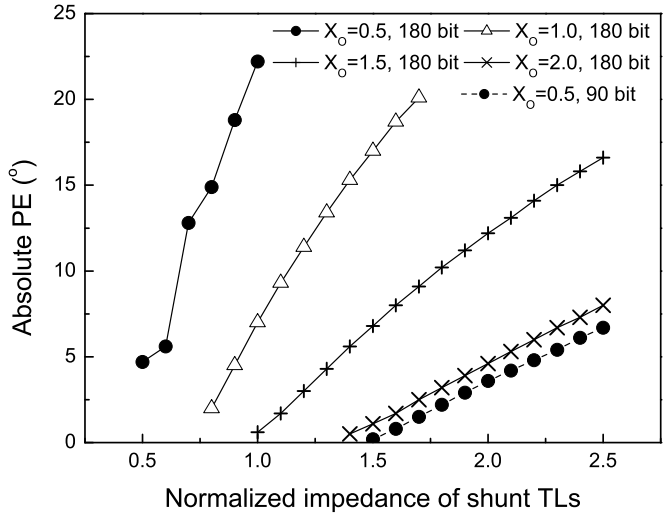


Fig. 4.50. Absolute phase error versus $\overline{Z}_\theta$ and X_O.

At the center frequency, the insertion phase of the BPF branch is 0º. To achieve phase shifts of 90º and 180º with an absolute phase error of 0º, the TL branch should be 90º and 180º at ω_0, respectively. For other absolute phase errors, the insertion phase of the TL branch is not required to be precisely 90º and 180º at ω_0. Instead, the values should be tuned slightly to maximize the bandwidth for the desired phase errors. The phase difference between the TL branch and the BPF branch contains a ripple that determines the absolute phase error. Fig. 4.50 shows how $\overline{Z}_\theta$ and X_0 influence the absolute phase error. For the 90º phase bit, when $\overline{Z}_\theta$ increases, more curves can be plotted. However, the resulting high impedance TLs are more difficult to fabricate. The overall bandwidth, accounting for a 10 dB return loss and the required phase error, is shown versus the absolute phase error in Fig. 4.51.

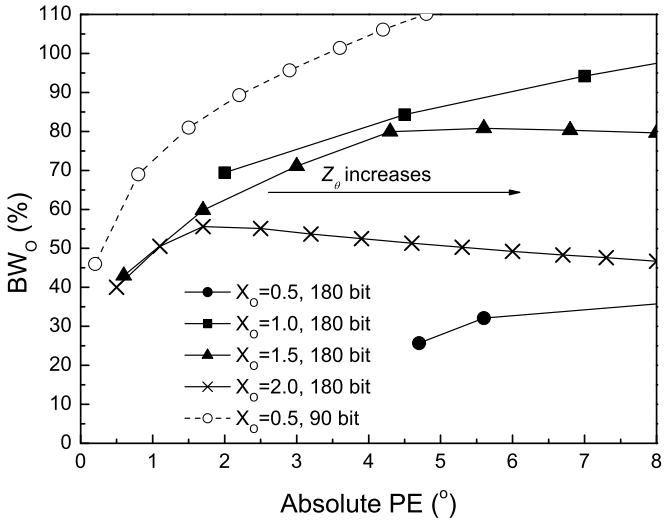


Fig. 4.51. Overall bandwidth versus absolute phase error.

When the tolerable phase error increases, the overall BW also increases. With the overall bandwidth and the maximum tolerable phase error as requirements, a designer should start from Fig. 4.51 to read the value of X_O. With that value of X_O and the tolerable phase error, the normalized impedance of the shunt TLs is then obtained from Fig. 4.50. Note from Fig. 4.50 that for increasing Z_θ the absolute phase error increases.

As an example, phase shifters with an absolute phase error of 2º are designed and the values shown in Table 4.4 are obtained. To realize the optimum phase alignment between the TL branch and the BPF branch with the available discrete capacitors and inductors, the values are tuned slightly. Note that the parameters listed in Table 4.4 can be scaled to different frequencies. Both bits have an overall BW larger than an octave.

TABLE 4. 4
OPTIMIZED PARAMETERS OF PHASE SHIFTER

Phase bits	Shunt TL	X_O	Ref. TL	BW_{PE}	BW_{RL}	BW_O
180º	45 Ω, 90º	1.17	50Ω, 178.6º	67%	94%	67%
90º	108 Ω, 90º	0.660	50Ω, 88.6º	86%	129%	86%

Using the data from Table 4.4, a 180º phase bit and a 90º phase bit were designed at a center frequency of 2 GHz. Duroid 5870 (ε_r=2.33, tanδ= 0.0012, h=31 mils) and MuRata discrete capacitors and inductors were used. The measurement results are compared with two simulations. In the first simulation ideal components were used and in the second simulation the measured S parameters of the Murata components were used. The phase shift response is shown in Fig. 4.52. For the 180º bit, the measured

phase error is ±3.5º from 1.29 GHz to 2.78 GHz (73%). For the 90º bit, the measured phase error is ±2.5º from 0.94 GHz to 2.89 GHz (102%). The measured return loss for the resonator branches of the two bits are shown to be better than 18 dB and 12 dB in Fig. 4.53 and Fig. 4.54, respectively.

The return losses for the TL branches are not shown here since 50 Ohm impedance lines are used which provide a very high return loss. It is shown that both measured results fit the trend plotted in Fig. 4.51, and they achieve a BW_O of an octave.

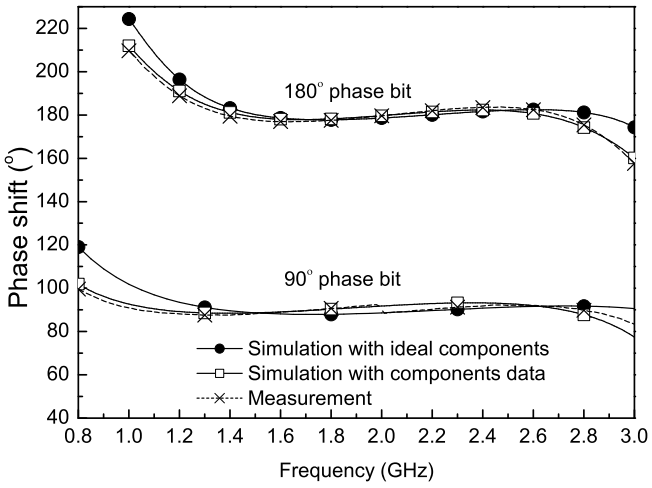


Fig. 4.52. Simulated and measured phase shift of the two bits.

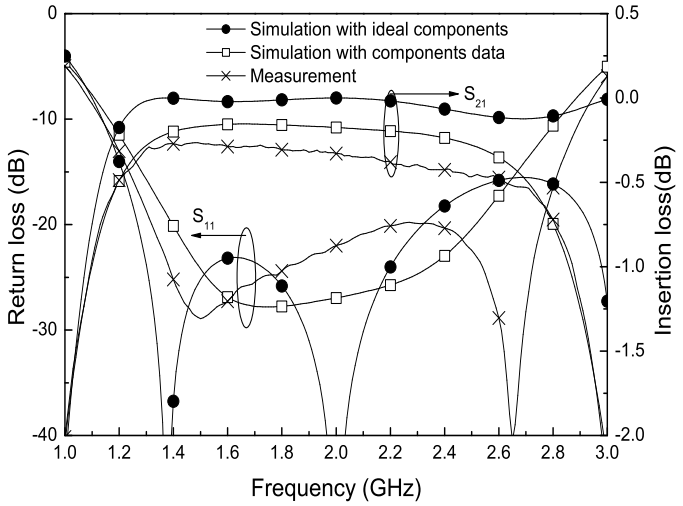


Fig. 4.53 . Insertion loss and return loss of the 180° bit.

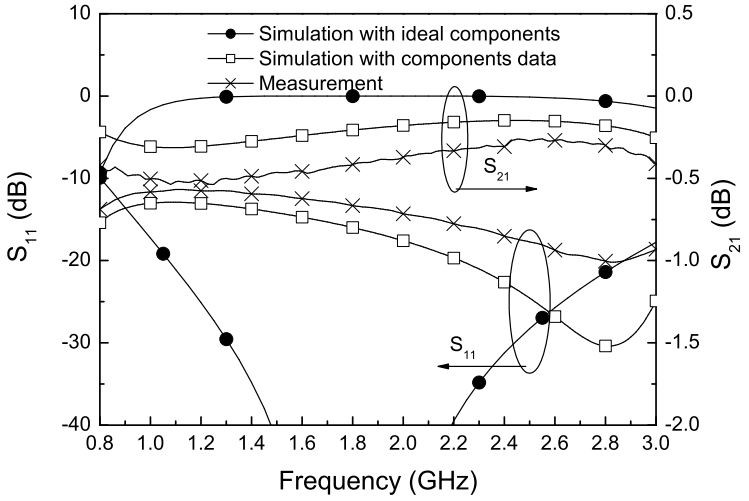


Fig. 4.54 . Insertion loss and return loss of the 90° bit.

4.4 Conclusions

This chapter focuses on the novel phase shifter topologies based on a technique to align the phase slope of two networks. Resonators are used to change the phase slope at the center frequency without changing the insertion phase at that frequency. They can also add additional transmission poles to the network so that the return loss bandwidth can be also improved.

In the development of the topologies, the phase error, return loss and the bandwidth are considered simultaneously. The tradeoffs between these parameters are found and can be used for customized designs. Scalable parameters for phase shifters with bandwidth larger than an octave are provided. Distributed and discrete octave band 4-bit phase shifters are designed and measured. For the distributed design, a measured RMS phase error of 3.6º and a return loss larger than 12 dB are achieved. For the discrete design, a measured RMS phase error of 5.9º and a return loss of 13 dB are achieved. When the distributed components and the discrete components are used together, smaller phase error is expected. Examples are provided for 180º and 90º phase shifts. The theoretical phase error of an octave band for the two phase shifts is less than 2º and the test result is less than 3.5º with return loss larger than 12 dB.

The potential of this technique can be further studied especially for millimeter wave designs. A microwave resonator can always be considered to improve the phase response of any phase shifters.

Chapter 5

Quadrature and Dual-band Power Divider Designs Based on Insertion Phase Study

The insertion phase has been intensively studied for phase shifters. Besides phase shifters, other devices in modern microwave systems also utilize the special insertion phase. This chapter applies different networks to fulfill the insertion phase requirement for several different devices, such as ultra-wideband (UWB) quadrature power dividers and dual-band power dividers.

5.1 Quadrature UWB Power Divider

The quadrature power divider, which ideally provides a phase difference of 90º between the two output ports with the same amplitude, can be used in balanced amplifiers, image-rejection mixers [89], and vector modulators [90]. The broadband quadrature power divider can be realzied by a tandem Lange coupler configuration [91] or by a broadband in-phase power divider and phase shifting networks. Using Lange couplers, bonding wires are required at the joints, which increases the circuit complexity and fabrication cost. With phase shifting networks, however, a single layer layout is feasible. A bandwidth up to 104% (1.1 GHz to 3.5 GHz) with a return loss

better than 10 dB and a phase error less than ±5º can be achieved by using composite right/left handed transmission lines and metamaterials [92], [93]. However, at higher frequencies, the bandwidth degrades to 67% (3.5 GHz to 7 GHz) and the phase variation increases to ±10º due to the parasitics of the discrete inductors and capacitors [94]. To further reduce the size, discrete elements can be used in an integrated circuit realization at the expense of a reduced bandwidth [95].

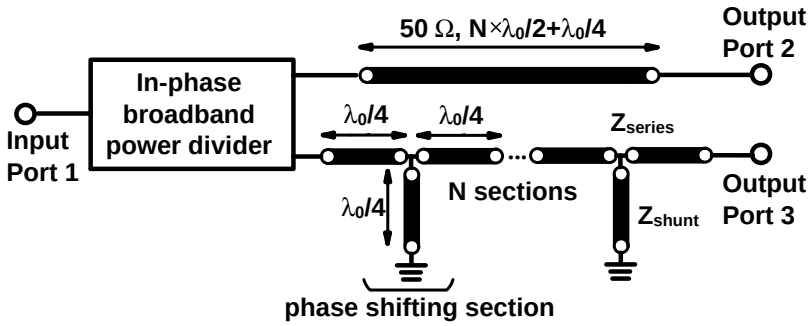


Fig. 5.1. Topology for UWB quadrature power divider.

Fig. 5.1 shows the topology proposed for a UWB quadrature power divider. The in-phase broadband power divider is designed by following the procedure outlined in [96]. Three stages of stepped impedance transformers and resistors are used in the power divider to ensure good matching over the whole frequency band. One output port of the power divider is connected to a 50 Ohm transmission line with an electrical length of $N\times\lambda_0/2+\lambda_0/4$ at the center frequency of 6.85 GHz providing an insertion phase of $N\times180^\circ+90^\circ$. The other output port is connected to N cascaded phase shifting sections. One phase shifting section consists of a grounded shunt $\lambda_0/4$ transmission line, with an impedance of Z_{shunt}, to control the phase response, and two

series $\lambda_0/4$ transmission lines, with impedance of Z_{series}, to improve the return loss. At the center frequency, the grounded shunt $\lambda_0/4$ stubs have an insertion phase of zero degrees and the two series $\lambda_0/4$ transmission lines have an insertion phase of 180º. Therefore, the N phase shifting sections provide an insertion phase of $N\times180º$. The phase difference at the center frequency between the two output ports is then ($N\times180º+90º-N\times180º$) = 90º. By carefully selecting the impedance Z_{shunt} of the shunt stubs, the phase of the two output ports can be aligned to achieve a broadband constant phase shift. When the number of sections N is increased, both the return loss and the phase error improve. However, when N is increased, the circuit area also increases.

The relation between phase error and return loss is plotted in Fig. 5.2 versus N. Each section is designed to have three transmission poles and an equal ripple response. Table 5.1 lists the respective characteristic impedances of the series and shunt transmission lines. It is observed that relatively high impedance shunt stubs are required when N increases.

TABLE 5.1.
DESIGN PARAMETERS FOR THE PHASE SHIFTING NETWORK

	N									
	1	2	3	4	5	6	7	8	9	10
Z_{series} (Ω)	24	35	39	42	43	44	45	46	46	47
Z_{shunt} (Ω)	17	45	75	106	137	168	199	230	261	292

Using Table 5.1 and Fig. 5.2, N=4 is chosen for the design. The quadrature power splitter is designed using Duroid 6002 (ε_r=2.94, h=30 mils). The layout is simulated in Momentum and then imported into ADS where the effects of the measured data of the lumped resistors are incorporated. For the measurement, a TRL calibration was performed from 3 GHz to 11 GHz. Fig. 5.3 shows the measured return loss at all three ports. Within the frequency band of interest, the measured minimum return loss for all three ports is 13.8 dB. Fig. 5.4 and Fig. 5.5 show the comparison between the measured and simulated insertion loss, amplitude imbalance and phase difference between the two output ports. In Fig. 5.4, the measured amplitude imbalance is less than 0.5 dB while the simulated imbalance is less than 0.15 dB. The minimum isolation is 14 dB at 10.6 GHz, which is due to the parasitic capacitance of the resistors and the inaccuracy in the fabrication.

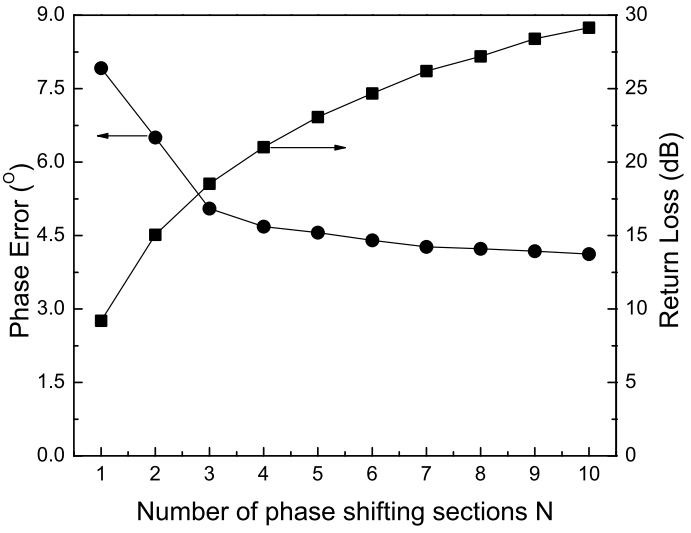


Fig. 5.2. Phase error and return loss versus N.

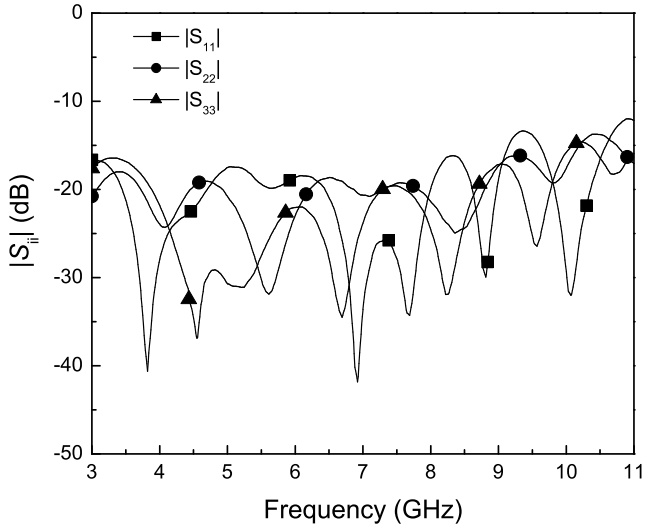


Fig. 5.3. Measured $|S_{11}|$, $|S_{22}|$, and $|S_{33}|$ of the UWB quadrature power divider.

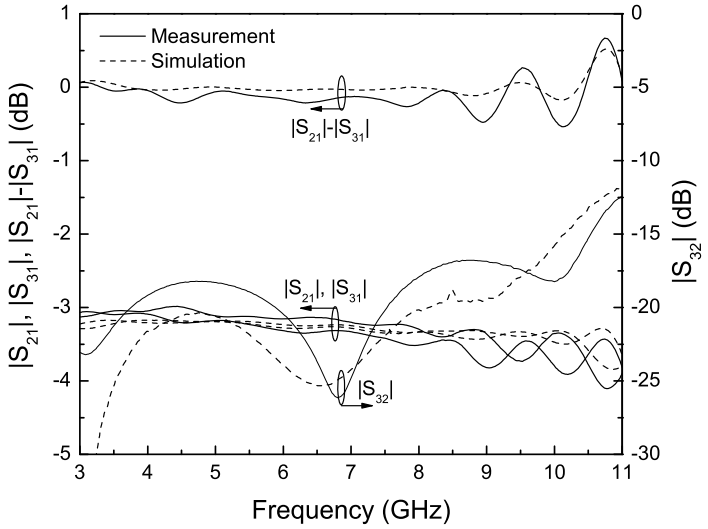


Fig. 5.4. $|S_{21}|$, $|S_{31}|$, $|S_{32}|$ and the amplitude imbalance of the UWB quadrature power divider.

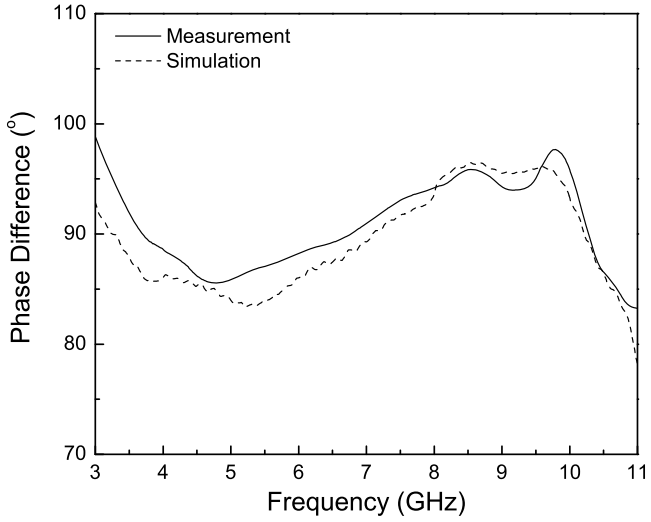


Fig. 5.5. Phase difference between port 2 and port 3.

In Fig. 5.5, a measured phase difference of 90.9º±6.0º is achieved between the two output ports while the simulated phase difference is 89.9º±6.0º. The ripple in the phase response between 8 and 10 GHz is caused by the parasitic capacitance of the discrete resistors.

5.2 Dual Band In-phase Power Divider Design I

Dual-band power dividers with their specific design tradeoffs can be obtained through various approaches [97]-[102]. However, almost all approaches use two cascaded sections of transmission lines to achieve an impedance transformation as originally introduced in 1968 [96]. A single resistor is used in [97] to relax the layout constraint at the cost of a poorer isolation. And a discrete inductor and a capacitor in parallel

with the resistor improve the isolation [98]. However, the parasitic effect of the inductor and capacitor affect the performance in high frequency designs. To eliminate the parasitics, a distributed design with closed-form expressions is given in [99]. However the circuit area is relatively large and the bandwidth is limited. Coupled line impedance transformers with a coupling factor as the design parameter are introduced in [100] and [101]. Only one of the two sections can be replaced by coupled lines and the circuit area remains relatively large. In [102], coupled lines together with two transmission lines are proposed. The maximum theoretical frequency ratio is 1.67.

Fig. 5.6(a) shows the topology of the dual band power divider which is based on the Wilkinson power divider.

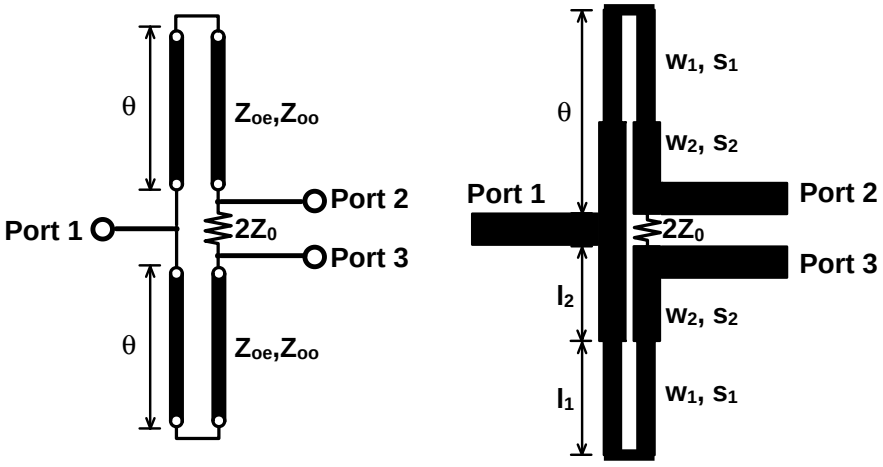


Fig. 5.6. (a) Proposed dual-band power divider topology, (b) implementation using microstrip lines.

It is assumed that the even-mode velocity and odd-mode velocity of the coupled lines are constant and equal. There are three design parameters for a given frequency ratio: Z_{0e}, Z_{0o} and the electrical length θ of the coupled lines. Each coupled lines section is designed to have an image impedance of $\sqrt{2}Z_0$. Therefore, we have

$$\sqrt{2}Z_0 = \sqrt{Z_{0e}Z_{0o}} \tag{5-1}$$

The insertion phase ϕ of the coupled line section is determined by

$$\phi = \cos^{-1}\left(\frac{\frac{Z_{0e}}{Z_{0o}} - \tan^2\theta}{\frac{Z_{0e}}{Z_{0o}} + \tan^2\theta}\right) \tag{5-2}$$

To achieve dual band impedance transformation, the insertion phase should be 90º at the lower frequency f_1 and 270º at the upper frequency f_2:

$$\phi_1 = 90°, \quad \phi_2 = 270° \tag{5-3}$$

Substituting (5-3) into (5-2), the following relations are obtained:

$$\frac{Z_{0e}}{Z_{0o}} = \tan^2\theta_1 \quad \text{and} \quad \frac{Z_{0e}}{Z_{0o}} = \tan^2\theta_2 \tag{5-4}$$

where θ_1 and θ_2 represent the electrical length of the coupled line section at f_1 and f_2, respectively. From (5-4), it follows that

$$\theta_2 = 180° - \theta_1 \tag{5-5}$$

The frequency ratio is then given by:

$$r = \frac{f_2}{f_1} = \frac{\theta_2}{\theta_1} \tag{5-6}$$

From (5-5) and (5-6), we have

$$\theta_1 = \frac{180°}{r+1} \tag{5-7}$$

Therefore, the procedure to design the dual band power divider is as follows:

(i) determine the required frequency ratio r;

(ii) calculate the electrical length θ_1 of the coupled lines at the lower frequency from (5-7);

(iii) calculate Z_{0e} and Z_{0o} using (5-1) and (5-4).

The three design parameters Z_{0e}, Z_{0o} and θ_1 are plotted in Fig. 5.7 versus the frequency ratio. It is observed that when the frequency ratio increases, the required coupling factor $(Z_{0e}-Z_{0o})/(Z_{0e}+Z_{0o})$ decreases.

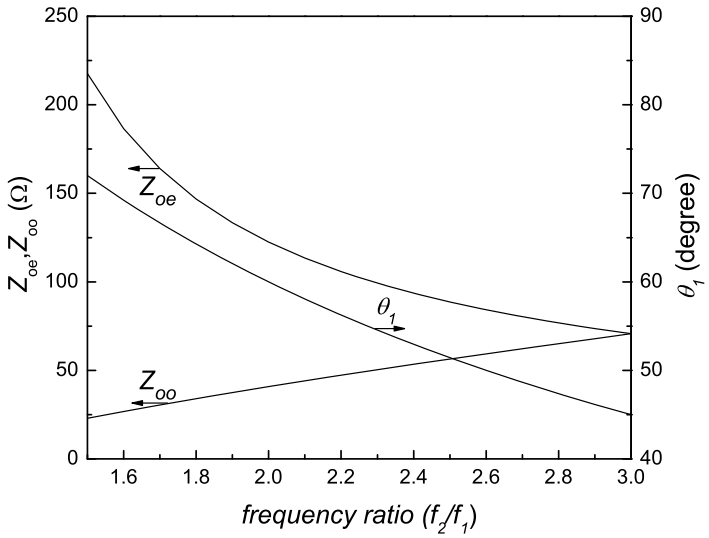


Fig. 5.7. Design parameters for different frequency ratio.

To verify the concept, a dual-band power divider is designed at 2.4 GHz and 5.8 GHz, i.e. r=2.42. The simulation results using ideal components are shown in Fig. 5.8. Perfect matching for all three ports and isolation between the two output ports is observed. However, these results are only valid when the even-mode and odd-mode velocities of the coupled lines are equal, a condition that is not satisfied in microstrip implementations. To compensate for the difference in phase velocities, stepped impedance coupled lines are used as shown in Fig. 5.6(b).

The single section of coupled lines with even-mode and odd-mode impedances of 92.8 Ohm and 53.9 Ohm is replaced by two sections of coupled lines with even-mode

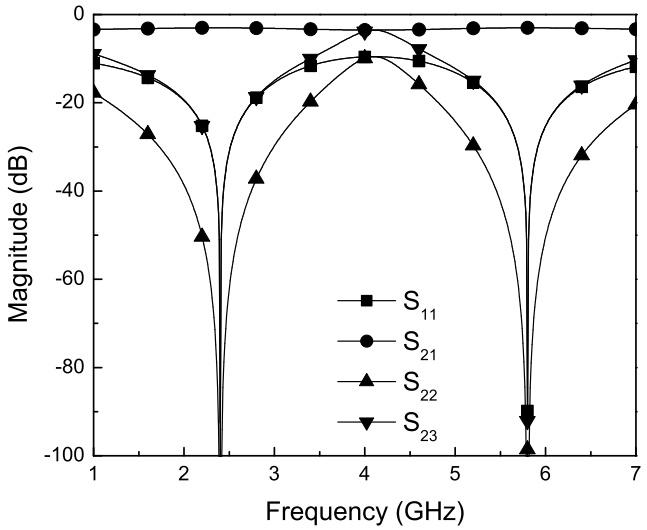


Fig. 5.8. Simulation results using ideal components for dual-band power divider at 2.4 GHz and 5.8 GHz.

and odd-mode impedances of 90.4 Ohm and 51.9 Ohm for the first section and 98.2 Ohm and 58.2 Ohm for the second section using [103]. Duroid 5870 (ε_r=2.33, h=31 mils) is used as the substrate, and the design dimensions are listed in Table 5.2.

TABLE 5.2. DESIGN DIMENSIONS

s_1	s_2	l_1	l_2	w_1	w_2
0.34 mm	0.27 mm	6.32 mm	6.3 mm	1.06 mm	1.24 mm

Fig. 5.9 to Fig. 5.12 show the comparison between the simulation results and the measurements. The measured amplitude imbalance is within 0.2 dB from 1 GHz to 7 GHz. The measured 20 dB input return loss bandwidth is 610 MHz and 410 MHz for the lower and higher band, respectively.

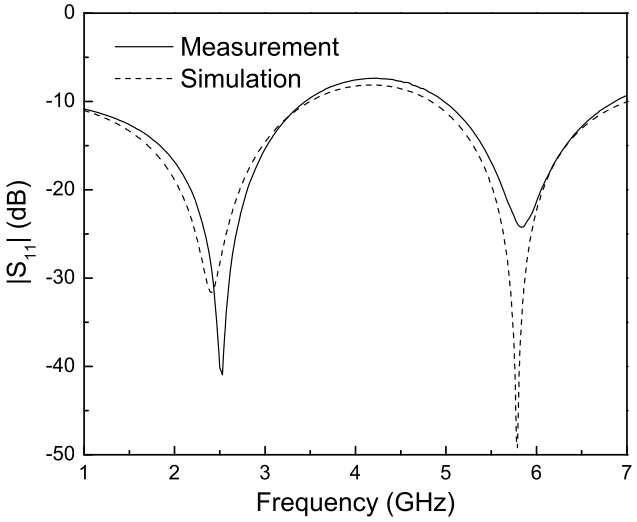


Fig. 5.9. $|S_{11}|$ of the dual band power divider.

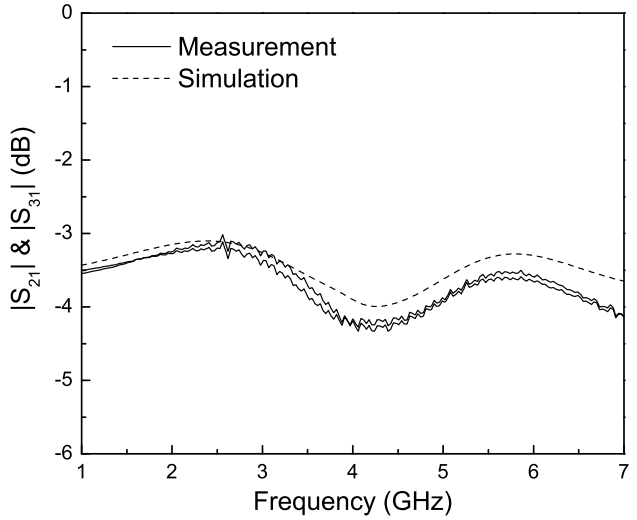


Fig. 5.10. $|S_{21}|$ of the dual band power divider.

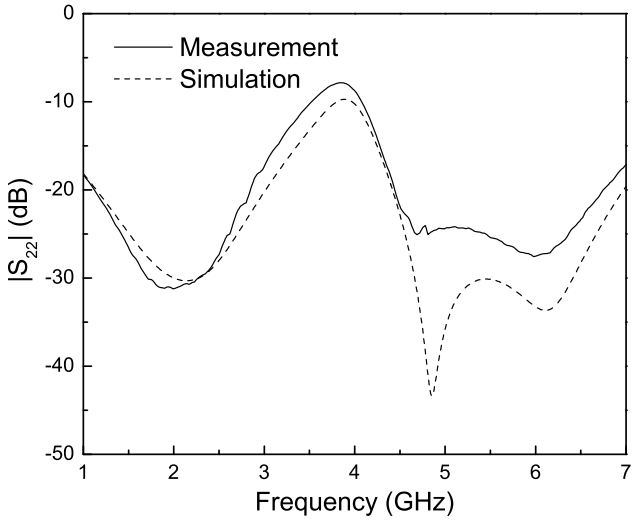


Fig. 5.11. $|S_{22}|$ of the dual band power divider.

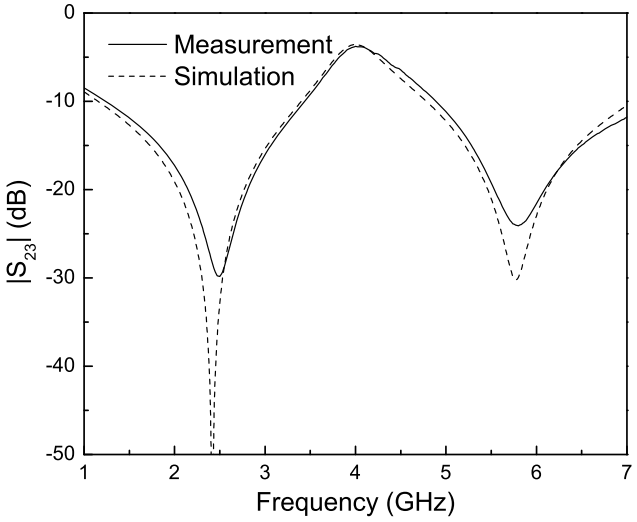


Fig. 5.12. $|S_{23}|$ of the dual band power divider.

5.3 Dual Band In-phase Power Divider Design II

In this session, another dual band in-phase power splitter design method is introduced. Two general types are analyzed, and the second type has comparable size with the first design in Section 5.2. However, the frequency ratio of the two dual-band is enlarged. The topology for the dual-band power divider is shown in Fig. 5.13. The dual-band response is determined by the π-network of each branch. Each branch should provide impedance transformation and an insertion phase of $(0.5+N)\pi$ (N=0, 1, 2,…) at the two dual-band frequencies. Note that a T network can also be used.

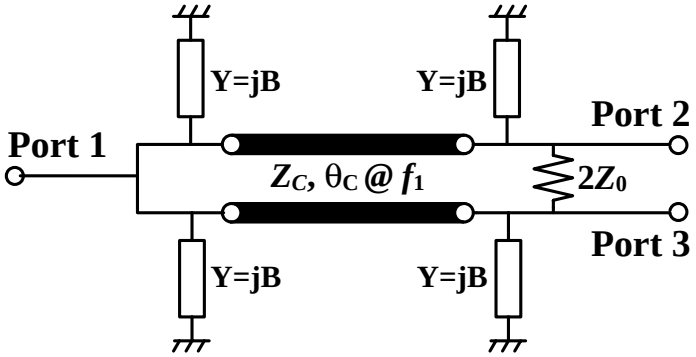


Fig. 5.13. Topology of the proposed dual-band power divider.

The π-network contains one center TL with an impedance of Z_c and an insertion phase of θ_c at the lower frequency f_1. To provide matching and correction of the insertion phase, two loads with admittance B are added at the two ends of the TL. Given a design frequency ratio of r (f_2/f_1), the following condition is obtained:

$$Z_c = \sqrt{2}Z_0 \frac{\sin 0.5\pi}{\sin \theta_c} = \sqrt{2}Z_0 \frac{\sin\left(0.5+N\right)\pi}{\sin\left(r\times\theta_c\right)} \tag{5-8}$$

It follows that

$$\sin\theta_c = \left(-1\right)^N \sin\left(r\times\theta_c\right) \tag{5-9}$$

For the Type I divider, N=1, 3, 5, … and θ_c is found as

$$\theta_c = \frac{\pi}{r-1} \quad or \quad \theta_c = \frac{2\pi}{r+1} \tag{5-10}$$

For the Type II divider, N=2, 4, 6, … and θ_c is found as

$$\theta_c = \frac{\pi}{r+1} \quad or \quad \theta_c = \frac{2\pi}{r-1} \tag{5-11}$$

To achieve a compact circuit, the first solution of (5-11) will be selected in Type II power dividers. The relation between the line impedance, line length and the frequency ratio for the two types is shown in Fig. 5.14.

To achieve impedance and phase matching, the loads must satisfy

$$B = \frac{\cos\theta_c}{\sqrt{2}Z_0 \sin\left(0.5\pi + N\times\pi\right)} \tag{5-12}$$

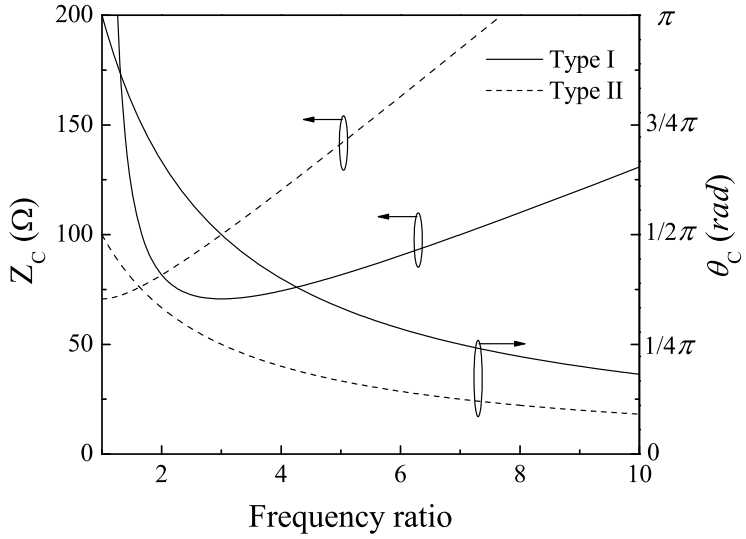


Fig. 5.14. Parameters of the central TL versus the frequency ratio for Type I and Type II power divider.

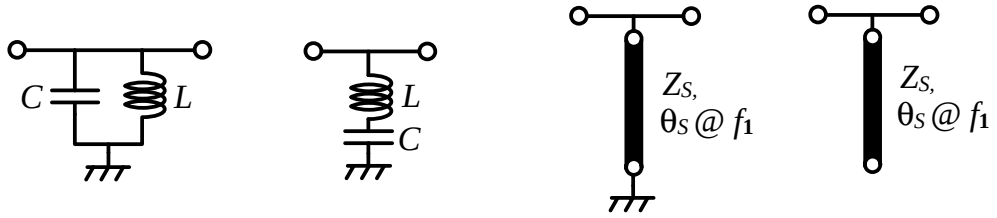


Fig. 5.15. Four possible loads for the dual-band power dividers. (a), (b): the lumped LC loads, (c), (d): the distributed short/open loads.

Assume the load is B_1 at f_1 and B_2 at f_2. When $\theta_c = \pi/(r-1)$, B_2=B_1 and when $\theta_c = 2\pi/(r+1)$ or $\theta_c = \pi/(r+1)$, $B_2 = -B_1$. To realize these reactances, two possible lumped LC loads are considered first, and then two distributed loads are considered as shown in Fig. 5.15. Solutions are only found when $B_2 = -B_1$. For Type I, when r<3, the parallel loads in Fig. 5.15(a) should be used and the capacitance is

found as:

$$C = \frac{\cos\theta_c}{2\pi f_1 \sqrt{2} Z_0 (1-r)} \tag{5-13}$$

When r>3, the series loads in Fig. 5.15(b) should be used and the capacitance is

$$C = \frac{\cos\theta_c}{2\pi f_1 \sqrt{2} Z_0}\left(1-\frac{1}{r}\right) \tag{5-14}$$

For both cases, the inductance is given by:

$$L = \frac{1}{r \times C \times (2\pi f_1)^2} \tag{5-15}$$

For Type II, Fig. 5.15(b) should be used for all r values, (5-14) and (5-15) are used to find the capacitance and inductance in that case.

For realization of the power dividers at higher frequencies, the distributed loads of Fig. 5.15(c) and 5.15(d) with impedance of Z_s and electrical length of θ_s at f_1 are considered. The admittance is $-jY_s(\tan\theta_s)^{-1}$ for the shorted stub and $jY_s\tan\theta_s$ for the open stub. At f_2, the admittance changes to $-jY_s(\tan r\theta_s)^{-1}$ and $jY_s\tan(r\theta_s)$, respectively. The solutions are also found when $B_2 = -B_1$, which leads to the fixed electrical length of the stub:

$$\theta_s = \frac{\pi}{r+1} \tag{5-16}$$

For Type I, and $\theta_c = 2\pi/(r+1)$, when r<3, Fig. 5.15(c) should be used, and the impedance is

$$Z_s = -\frac{\sqrt{2}Z_0}{\tan\theta_s \cos\theta_c} \tag{5-17}$$

When r>3, Fig. 5.15(d) should be used, and the impedance is given by:

$$Z_s = \frac{\sqrt{2}Z_0 \tan\theta_s}{\cos\theta_c} \tag{5-18}$$

For Type II, and $\theta_c = \pi/(r+1)$, Fig. 5.15(d) should be used for all r values, equations (5-16) and (5-17) determine the stub dimension.

Note that the conventional Wilkinson power divider is a special case of Type I when r=3 for both lumped load and distributed load designs.

To validate the design method, two dual-band power dividers centered at 0.5/2.0 GHz and 2.4/5.8 GHz are designed. Rogers Duroid 5870 (ε_r=2.33, h=31 mil) and discrete MuRata components are used. The photo of the fabricated designs is shown in Fig. 5.16.

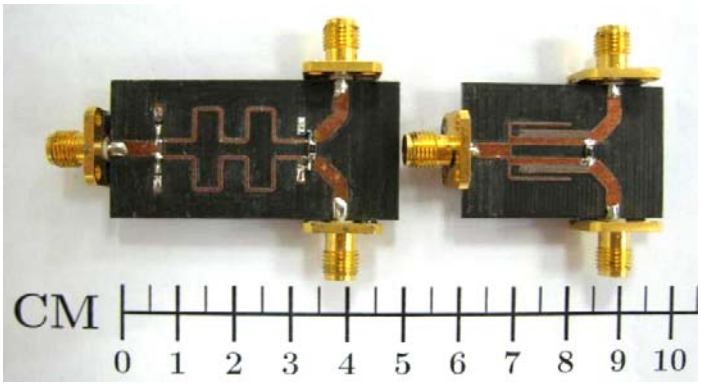


Fig. 5.16. Photo of the fabricated circuits. Left circuit is centered at 0.5/2.0 GHz and right circuit is centered at 2.4/5.8 GHz.

For the first design, lumped loads are used. From the design equations, Z_c=74.4 Ω, θ_c=0.4π, L=24.3 nH, C=1.0 pF are obtained for Type I and Z_c=120 Ω, θ_c=0.2π, L=9.3 nH, C =2.7 pF are obtained for Type II. As predicted, Type II is half the size of Type I and the required inductance is smaller in Type II designs. Therefore, Type II is selected for the design.

Figs. 5.17 and 5.18 compare the simulated and measured responses of the first power divider. The measured return loss at all three ports is larger than 17 dB, and the measured isolation between the two output ports is larger than 20 dB. The amplitude imbalance is less than 0.03 dB.

For the second design, distributed loads are used. The values Z_c=73.3 Ω, Z_s=205.1 Ω, θ_c= 0.58π, θ_s=0.29π are obtained for Type I and the values Z_c=89.0 Ω, Z_s=152.6 Ω, θ_c=θ_s=0.29π are obtained for Type II.

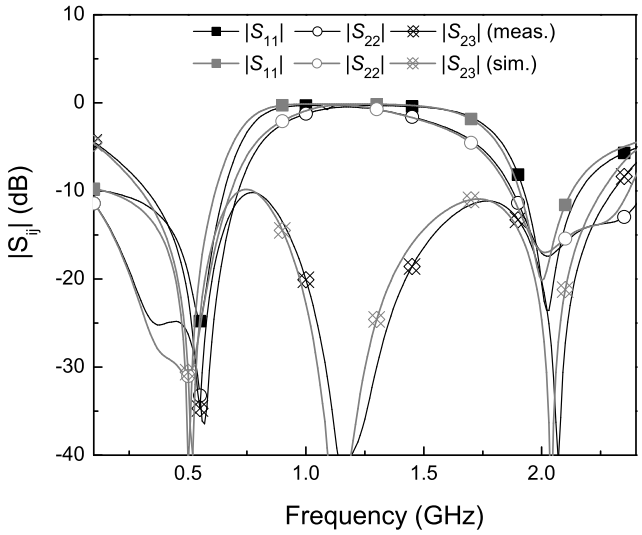


Fig. 5.17. Simulated and measured $|S_{11}|$, $|S_{22}|$ and $|S_{23}|$ (0.5/2.0 GHz).

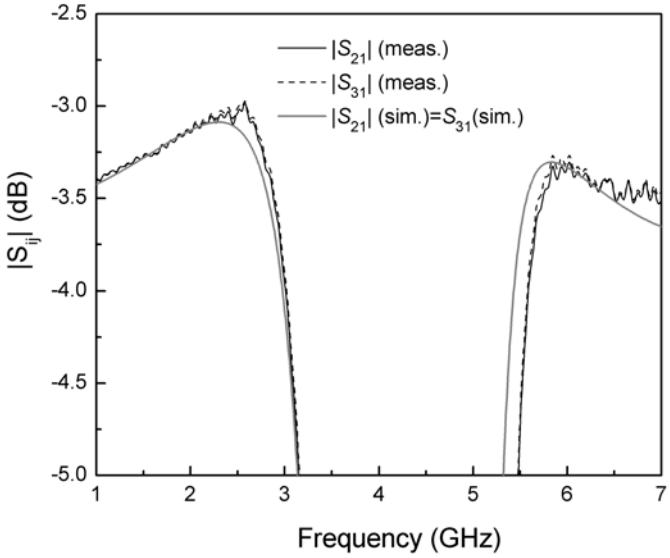


Fig. 5.18. Simulated and measured $|S_{21}|$ and $|S_{31}|$ (0.5/2.0 GHz).

Type II is selected again due to the compact size and the realizable impedance using the Rogers substrate. Note that for some frequency ratios, Type I may be used due to fabrication limits of the Type II dividers.

Figs. 5.19 and 5.20 compare the simulated and measured responses of the second power divider. The measured return loss of all three ports is larger than 18.8 dB, and the measured isolation between the two output ports is larger than 17 dB. The amplitude imbalance is less than 0.05 dB. The circuit size of the proposed Type II topology is almost half compared to other reported designs due to the fact that a quarter wavelength TL, instead of half a wavelength TL at the center frequency is used as the center transmission line. The discrepancy found near 3.75 GHz in Fig. 5.19 is due to the resonance caused by the coupled lines and the parasitics of the discrete resistor.

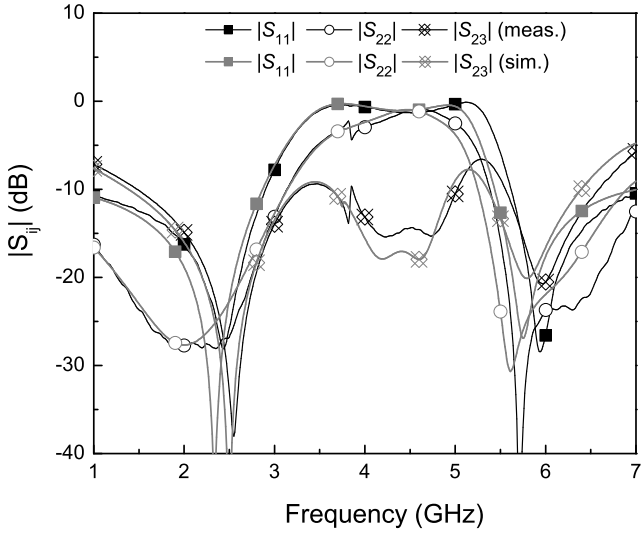


Fig. 5.19. Simulated and measured $|S_{11}|$, $|S_{22}|$ and $|S_{23}|$ (2.4/5.8 GHz).

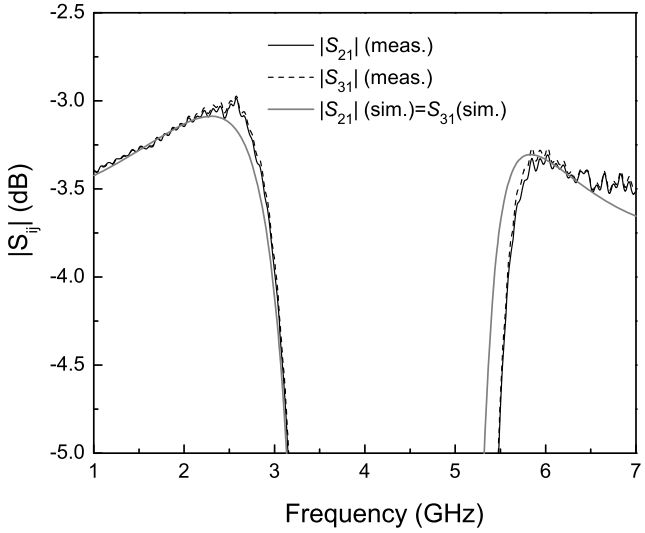


Fig. 5.20. Simulated and measured $|S_{21}|$ and $|S_{31}|$ (2.4/5.8 GHz).

5.4 Conclusions

In this chapter, an ultra-wideband quadrature power divider and two dual-band power dividers are proposed. The design of the these circuits are based on the insertion phase study in Chapter 3 and Chapter 4.

The UWB power divider consists of a broad band in-phase power divider and a four-section phase shifting network. A phase difference of 90º over a bandwidth of 110% was achieved at the two output ports. Over the whole bandwidth, the return losses of the three ports are higher than 13.8 dB and the isolation between the two output ports are larger than 14 dB.

For the dual-band power dividers, sections with an insertion phase that is multiple of 90º are designed at the dual frequencies. Two topologies are proposed to realize the function and different frequency ratio range are achieved due to the fabrication limits. The topology uses coupled lines can be used for frequency ratio between 2 and 3, and the topology uses loaded lines can be used for frequency up to 10. Note that the size of the dual-band power dividers proposed is almost half of other reported dual-band power dividers.

Chapter 6

Broadband Phase Shifter Design Using All-pass Networks

From the discussions in Chapter 3 and Chapter 4, it is noted that both the phase response and the return loss should be considered simultaneously for phase shifter design. The phase response of cascaded phase bits relies on the matching condition between the bits. The phase of the cascaded bits only is the sum of the individual bits when the return loss of each bit is high. If all-pass networks with a high return loss are used for the phase bits, the design problem may be simplified to a phase summation problem.

In this chapter, a further study of phase shifters based on all-pass networks is provided. It is found that the two-section all-pass network reported by Adler and Popovich [42] is a sub-optimum solution.

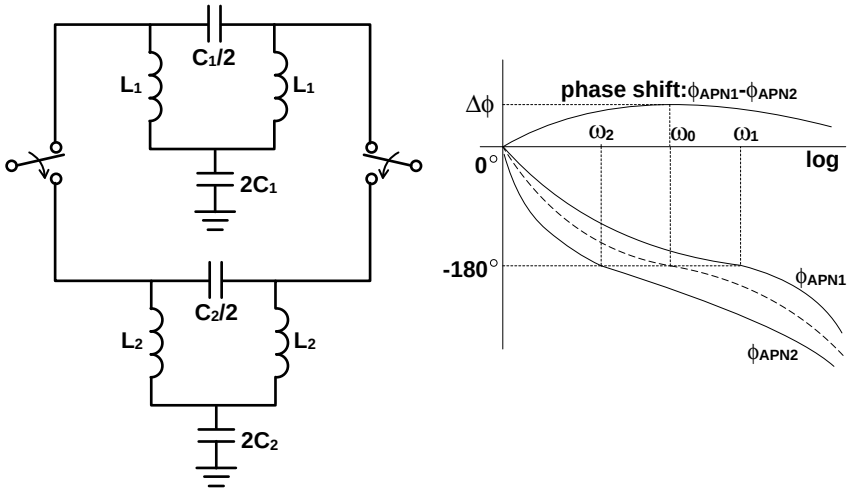
6.1 Single Section All-pass Network

The single section all-pass phase shifter and its phase illustration are shown in Fig. 6.1. The insertion phase is given by (4-26). To achieve a phase difference, the first network shifts the transition frequency from ω_0 to ω_1, and the second network from

ω_0 to ω_2 with the relation

$$\frac{\omega_1}{\omega_0} = \frac{\omega_0}{\omega_2} \tag{6-1}$$

where ω_0 is the center frequency.



(a) (b)

Fig. 6.1. Single-section all-pass phase shifter.

The phase shift is the difference between the insertion phase ϕ_{APN1} and ϕ_{APN2} of the two networks. In the following, a positive phase shift is obtained by subtracting ϕ_{APN2} from ϕ_{APN1}. The phase shift as a function of frequency is also shown in Fig. 6.1(b). A peak value can be found at ω_0. Note that for the APNs, only the phase response is considered. The phase shift at ω_0 is determined by the transition frequencies ω_1 and ω_2. Once the transition frequencies are set, the component values can be calculated from the work by Adler and Popovich [42].

The relation between the phase shift $\Delta\phi$ and ω_2 is shown in Fig. 6.2. ω_2 is chosen because its normalized value varies in [0, 1] while ω_1 varies from 1 to infinity. Two APNs that satisfy (6-1) and that have a phase shift as shown in Fig. 6.2 is considered to be an APN pair. A single section APN phase shifter has performance comparable to a third order HP/LP phase shifter. To enlarge the bandwidth, multiple APNs can be cascaded.

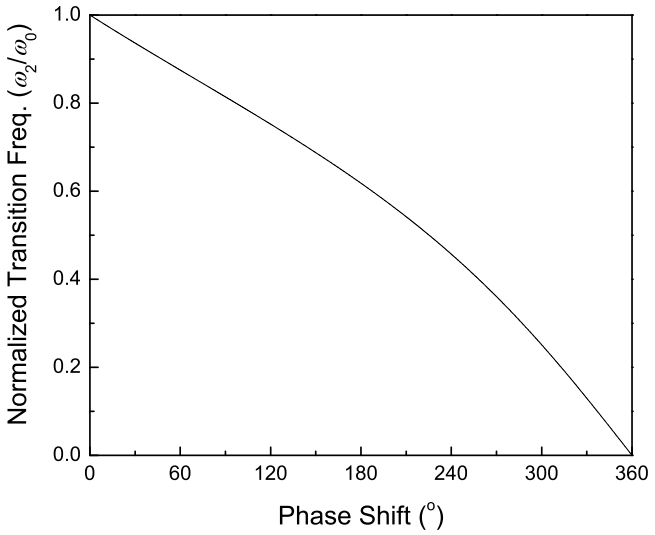


Fig. 6.2. The phase shift at ω_0 and its corresponding normalized transition frequency.

6.2 Cascaded Multi-section All-pass Networks

When multiple sections of APNs are cascaded, the overall phase shift is the summation of individual APN pairs. When the APN pairs are arranged properly,

multiple phase shift peaks can be obtained. For a given required phase shift $\Delta\phi_r$ and phase error *PE*, the BW_{PE} is extended when more phase shift peaks are generated. Fig. 6.3 shows the phase response for all-pass phase shifters with *N* sections. When the phase shift at the center frequency of an APN pair is selected, the transition frequencies of the two APN are determined from Fig. 6.2 and (6-1), and the components values can be calculated.

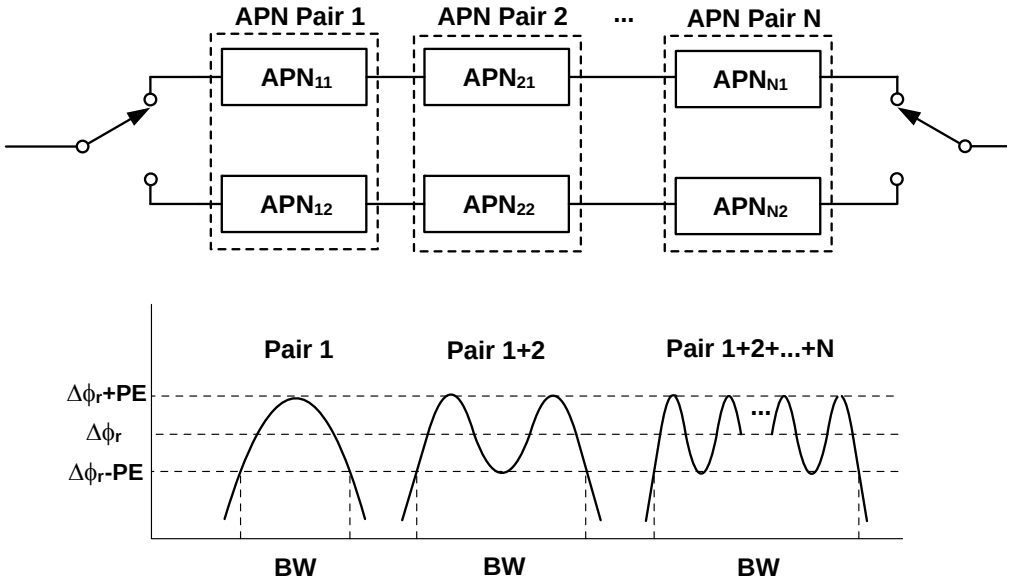


Fig. 6.3. Design concept for the cascaded APN phase shifter.

Therefore, the main objective for multi-section APN phase shifter design is to find the best phase shift combination of each APN pair at ω_0. The phase shift of the *i*th APN pair is a function of frequency, and is represented by $\Delta\phi_i(\bar{\omega})$, where $\bar{\omega} = \omega/\omega_0$. Here, a numerical approach is used because analytical solutions are not available at the moment. The procedure to find the BW and the corresponding component values for a given required phase shift and phase error is:

1. Get the required phase shift $\Delta\phi_r$, and the tolerable phase error PE according to the design specification.

2. For an all-pass network phase shifter with an odd number of pairs, $\sum(-1)^{i+1}\Delta\phi_i(1) = \Delta\phi_r + PE$, and for an even number, $\sum(-1)^{i+1}\Delta\phi_i(1) = \Delta\phi_r - PE$. The factor $(-1)^{i+1}$ represent that the added APN pair has an opposite sign of phase shift compared to the previous APN pair. Sweep all possible $\Delta\phi_1(1)$ to fulfill the condition. Note that for each $\Delta\phi_1(1)$, there is a set of corresponding components values according to Fig. 6.2 and [42].

3. For each set of $\Delta\phi_1(1)$, a pair of transition frequencies can be found. Then the phase shift can be written as a function of frequency: $\Delta\phi_1(\bar{\omega})$. Calculate the frequencies where the phase shift slope is zero, which means an extreme value can be found at those frequencies: $\frac{d}{d\bar{\omega}}\left[\sum(-1)^{i+1}\Delta\phi_i(\bar{\omega})\right] = 0$. For an N-section all-pass phase shifter, N frequencies will be found from [0, 1] for the optimum design, where $\bar{\omega} = 1$ is always a solution. Examine the phase shift at the N frequencies: from smallest frequency $\bar{\omega}_{slope1}$ to the largest frequency $\bar{\omega}_{slopeN} = 1$. If the phase shift at the odd number of frequencies $\bar{\omega}_{slopeodd}$ are $\sum(-1)^{i+1}\Delta\phi_i(\bar{\omega}_{slopeodd}) = \Delta\phi_r + PE$, and the phase shift at the even number of frequencies $\bar{\omega}_{slopeeven}$ are $\sum(-1)^{i+1}\Delta\phi(\bar{\omega}_{slopeeven}) = \Delta\phi_r - PE$, the calculation can be terminated and the final solution is achieved. Otherwise, repeat step 2.

4. Find the solution of $\sum(-1)^{i+1}\Delta\phi_i(\bar{\omega}) = \Delta\phi_r - PE$ between 0 and $\bar{\omega}_{slope1}$, the

frequency found is the lower band of the BW_{PE}, and the inverse frequency is the higher band of the BW_{PE}.

As examples, two and three cascaded all-pass phase shifters are designed. Fig. 6.4 shows the optimum phase response of the phase shifter with two stages in bold dash line and three stages in bold solid line.

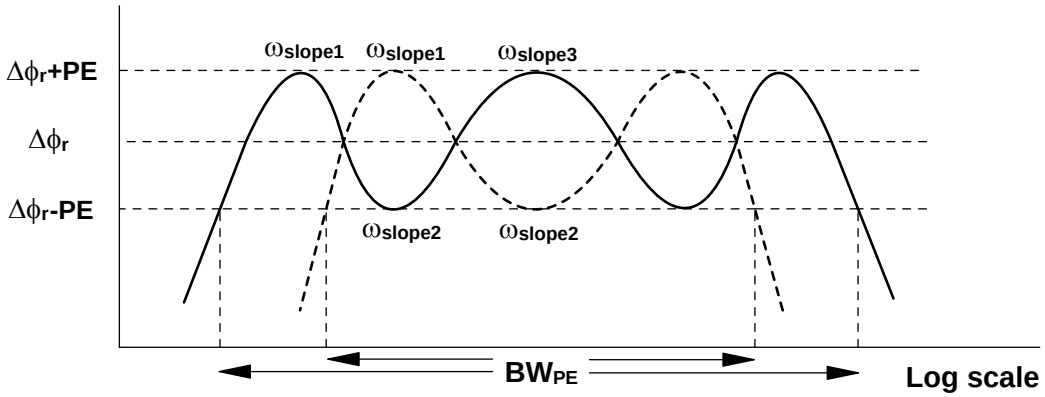


Fig. 6.4. Optimum phase response of the two and three cascaded APN phase shifter.

Fig. 6.5 and Fig. 6.6 show the relation between the phase error and the BW for two and three cascaded APNs, respectively. It is found that when more stages are added, the improvement on the phase error within a given frequency band is significant. The frequency band is represented by *r*, which is the ratio of the highest frequency over the lowest frequency of the frequency band. E.g. *r* is 2, 4, 8 and 10 for one, two, three octaves and one decade, respectively.

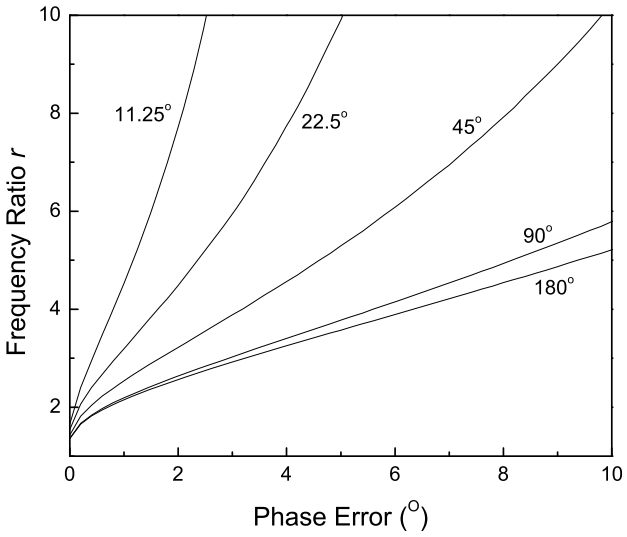


Fig. 6.5. Frequency ratio *r* versus the phase error of the phase shifter with two APNs.

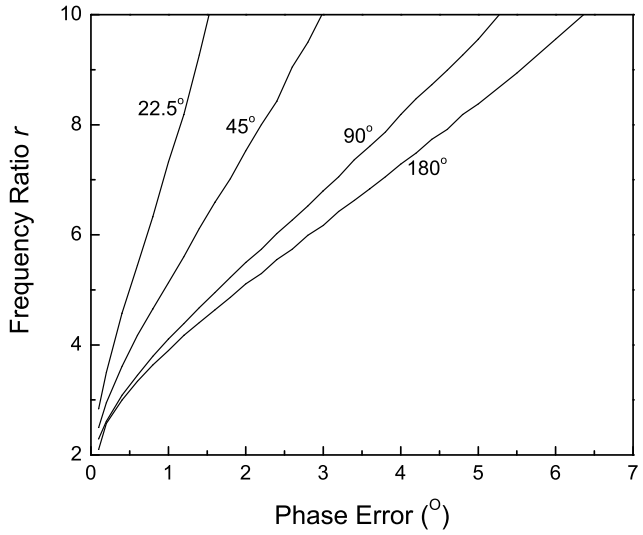


Fig. 6.6. Frequency ratio *r* versus the phase error of the phase shifter with three APNs.

The numerical solutions are time consuming. It is experimentally found that when the bandwidth is fixed, the frequencies $\bar{\omega}_{slopeN}$ are fixed for different phase shifts. The relation between the $\bar{\omega}_{slopeN}$ and the bandwidth for two and three APNs is plotted in Fig. 6.7.

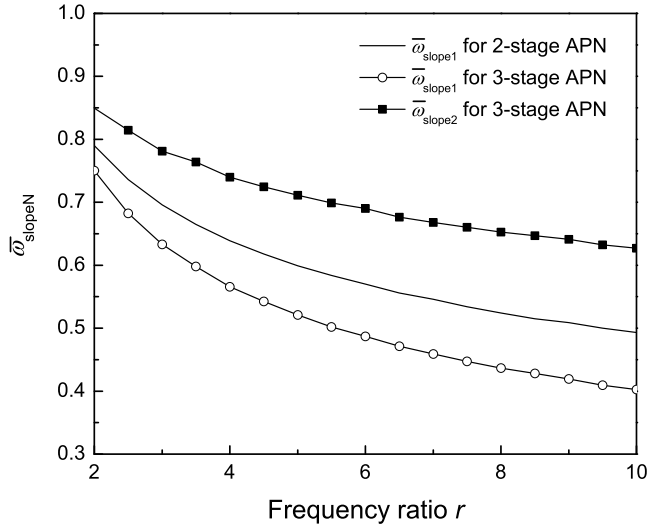


Fig. 6.7. The value of $\bar{\omega}_{slope1}$ and $\bar{\omega}_{slope2}$ for different bandwidth.

With this finding, the numerical solution can be simplified to

1. Get the required phase shift $\Delta\phi_r$, and the frequency ratio r according to the design specification.
2. Read $\bar{\omega}_{slopeN}$ from Fig. 6.7.
3. Numerically solve $\sum(-1)^{i+1}\Delta\phi_i\left(\bar{\omega}_{slopeodd}\right)+\sum(-1)^{i+1}\Delta\phi_i\left(\bar{\omega}_{slopeeven}\right)=2\Delta\phi_r$.
4. Return the solution and calculate PE from $PE=\sum(-1)^{i+1}\Delta\phi_i\left(\bar{\omega}_{slopeodd}\right)-\Delta\phi_r$.

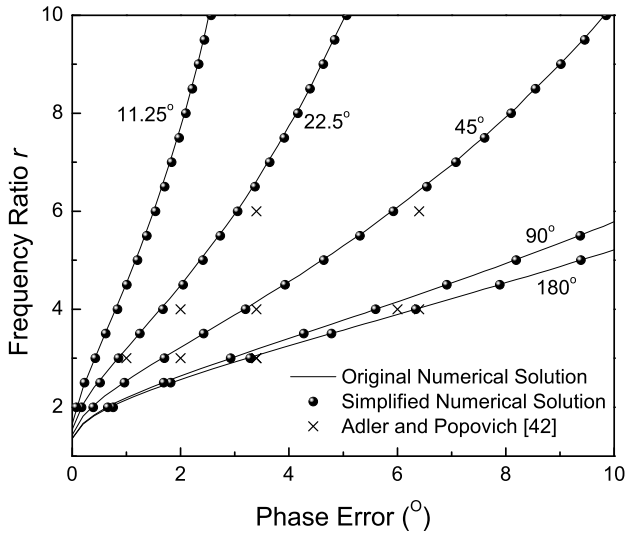


Fig. 6.8. Performance of the phase shifters with two APN sections.

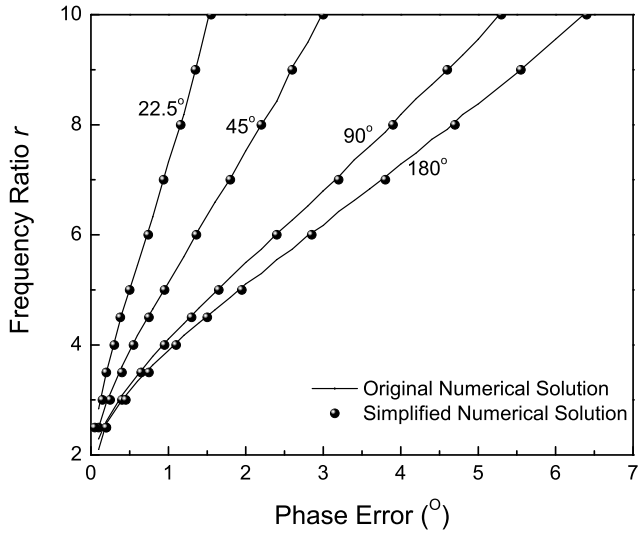


Fig. 6.9. Performance of the phase shifters with three APN sections.

The simplified numerical solution helps to reduce the calculation time significantly. The phase shifter performances are shown in Fig. 6.8 and Fig. 6.9. As a comparison, the reported two-section APN phase shifter by Adler and Popovich is also included. It should be noted that this method can be applied to broadband designs but that large inductor values may be required.

6.3 Experimental Results

A phase shifter is realized to verify this method. Fig. 6.10 shows the single phase bit of the three-section APN phase shifter and Table 6.1 lists the component values of the ideal components and the practical MuRata components for phase bits of 45º, 90º, and 180º. Parallel capacitors are used to realize some of the capacitor values. The ideal APN phase shifter reaches a bandwidth of 10:1, and when the practical components are used, the bandwidth reduces to 8:1. Fig. 6.11 shows the photo of the three-bit phase shifter.

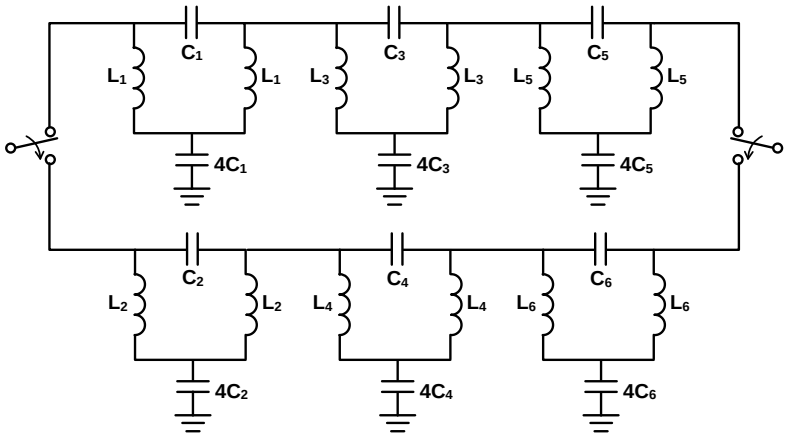


Fig. 6.10. Single phase bit of the 3-section APN phase shifter.

TABLE 6.1. COMPONENT VALUES FOR 3-SECTION APN PHASE SHIFTERS

	45º		90º		180º	
	Ideal	MuRata	Ideal	MuRata	Ideal	MuRata
C_1 (pF)	12.3	12+1.5	11.4	12	9.8	10
$4C_1$ (pF)	49.2	8.2+47	45.6	47	39.2	39
C_2 (pF)	2.1	2.4	2.2	2.4	2.6	2.7
$4C_2$ (pF)	8.4	8.2	8.8	9.0	10.4	10
C_3 (pF)	1.75	2.0	1.6	1.8	1.25	1.6
$4C_3$ (pF)	7.0	7.0	6.4	6.3	5.0	5.0
C_4 (pF)	14.5	15	16	18	20.2	20
$4C_4$ (pF)	58	47+10	64	68	80.8	82
C_5 (pF)	4.7	4.7	4.4	4.3	3.9	4.0
$4C_5$ (pF)	18.8	18+0.9	17.6	10+6.0	15.6	12+3.6
C_6 (pF)	5.4	5.1	5.7	5.6	6.5	6.8
$4C_6$ (pF)	21.6	15+5.0	22.8	10+10	27	22+4.7
L_1 (nH)	61	56	57	56	49	47
L_2 (nH)	10.3	10	11	10	12.9	13
L_3 (nH)	8.7	8.7	7.9	8.2	6.3	6.8
L_4 (nH)	72	75	80	82	101	100
L_5 (nH)	23.6	23	22	23	19.6	20
L_6 (nH)	26.8	27	28.6	30	32.3	33

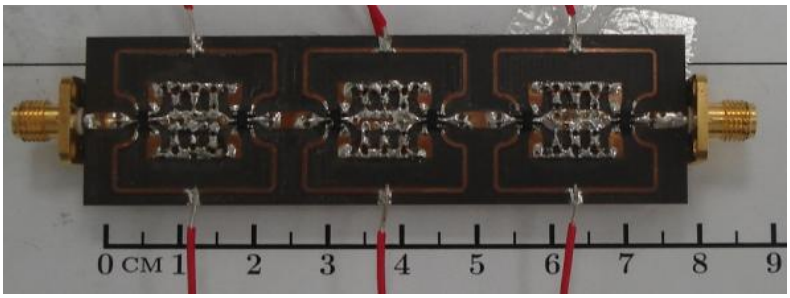


Fig. 6.11. Photo of the three-bit APN phase shifter.

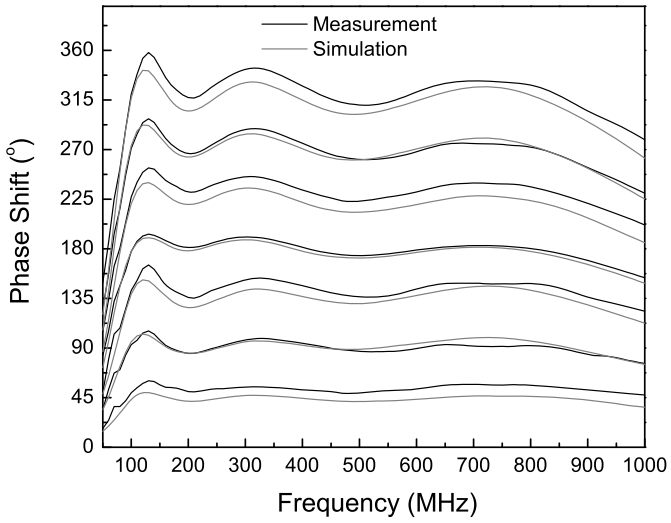


Fig. 6.12. Measured phase shifts of the three-bit phase shifter.

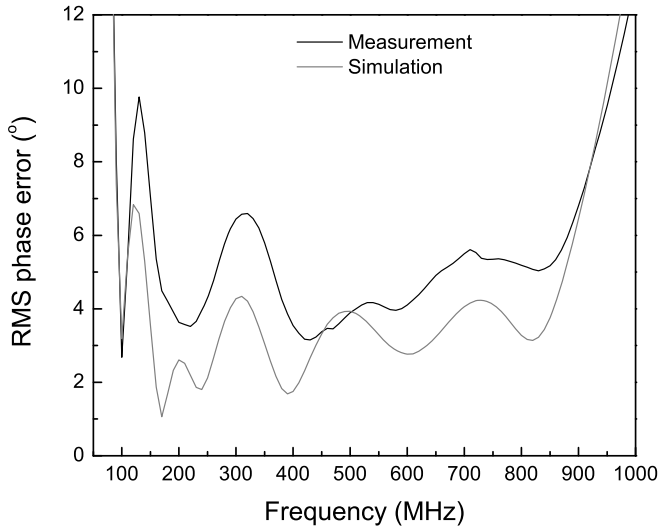


Fig. 6.13. Measured RMS phase error.

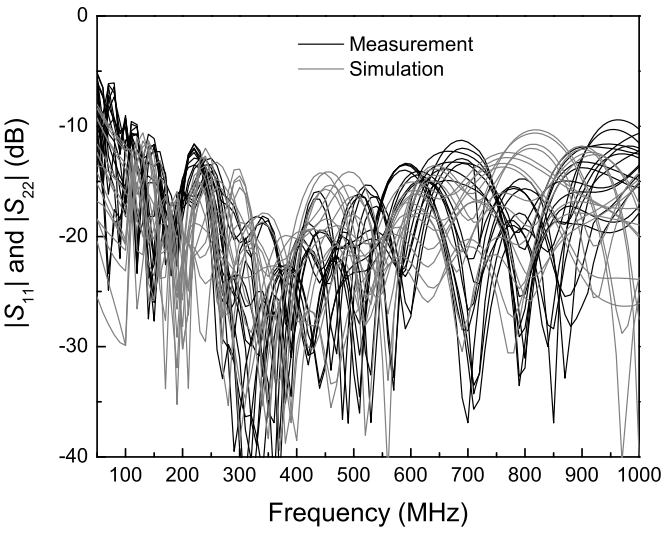


Fig. 6.14. Simulated and measured $|S_{11}|$ and $|S_{22}|$ of the three-bit phase shifter.

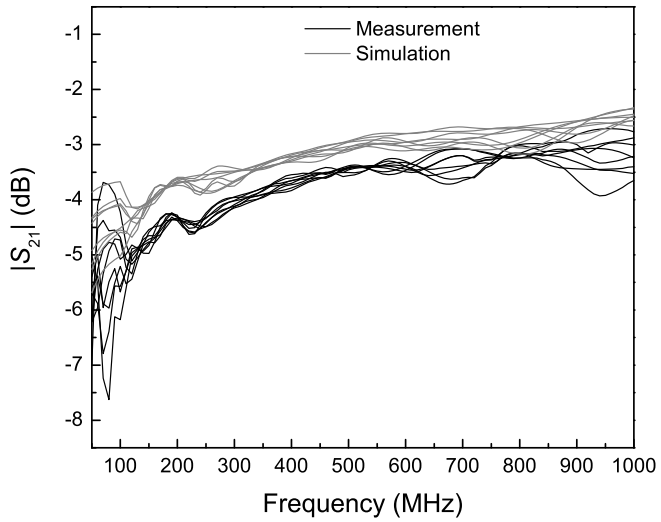


Fig. 6.15. Simulated and measured $|S_{21}|$ of the three-bit phase shifter.

Fig. 6.12 to Fig. 6.15 show the measured performance of the three-bit phase shifter. From 100 MHz to 940 MHz, the measured RMS phase error is less than 10º, the return loss is less than 10 dB and the amplitude imbalance is less than 1.5 dB. The higher insertion loss found at lower frequencies is due to the large inductors in the low-pass path.

6.4 Conclusions

APNs simplify the phase shifter design because no matching. When N sections of APNs are used, a phase response with N peaks is obtained. By proper selection of the circuit components, the phase shift can reach an optimum performance within a given bandwidth.

Because no analytical solution is available now, numerical procedures are used. It is found that the optimum performance of the phase shifter is only determined by the bandwidth. Therefore, a simplified numerical solution is found to solve the design equations efficiently. A bandwidth of one decade can be achieved by a three-section APN phase shifter with a theoretical phase error less than 6.7%. To verify the method, a 3-bit phase shifter is designed with a RMS phase error of 10º from 100 MHz to 940 MHz.

The drawback of the cascaded APN phase shifter, however, is the large value required for the inductors. The more stages are cascaded, the larger the inductors used, which influences the insertion loss at the low frequency.

Chapter 7

Conclusions and Recommendations

Phase shifters are extensively used in active phased array radar systems. It allows the beam of the antenna to change in shape and direction electrically.

The aim of this work is to:

1. Improve conventional phase shifter circuit and design methods.
2. Develop novel topologies for flexible and high performance designs.

Complementary analysis of the HP/LP filter phase shifter, the loaded-line phase shifter and the APN phase shifter are provided to extend the bandwidth. The design methodology for the improved HP/LP phase shifter and APN phase shifter is to include the bandwidth into the design considerations. The phase error and the return loss of the third-order HP/LP phase shifter are both improved by shifting the resonance frequency of the HP and LP filters. This work includes the conventional design as a special case. For the APN phase shifter, optimum performance is achieved for two and three cascaded networks. Three-octave bandwidth (8:1) can be achieved by using three-stage APN phase shifters with a measured RMS phase error of less than 10º and a return loss larger than 10 dB. And this work also allows tradeoffs

between the bandwidth and the phase errors. For the loaded-line phase shifter, the overall bandwidth of the 45º and the 90º phase bits is doubled compared to the conventional designs. Furthermore, the first dual-band loaded-line phase shifter with ideal and non-ideal switches is developed using closed form equations. The equations can be used for different frequency ratios.

Several novel topologies based on the phase slope alignment concept were synthesized in this work. Octave band performance was achieved and, most importantly, the tradeoff between the phase error, return loss and bandwidth is possible, which can be used in phase shifter computer aided design programs. Before this work, only the Schiffman phase shifter and the reflection type phase shifter can optimize the performance according to the bandwidth. However, Schiffman phase shifters require the same even-mode and odd-mode phase velocities and tightly coupled structures. The reflection type phase shifter is limited by the couplers. This work, instead, employs structures without any coupled lines and has better performance compared to the previous topologies. Octave band 4-bit phase shifters using a distributed design and using a discrete design are developed. For the distributed design, a measured RMS phase error of 3.6º and a return loss larger than 12 dB are achieved. For the discrete design, a measured RMS phase error of 5.9º and a return loss of 13 dB are achieved. When the distributed components and the discrete components are used together, a smaller phase error is expected. Examples are provided for 180º and 90º phase shifts. The theoretical phase error within an octave

band for the two phase shifts are less than 2º and the measured phase error less than 3.5º while the return loss is larger than 12 dB.

A phase shifter topology selection table based on the updated and newly developed work in this thesis is provided in Table 7.1. This table can be used as a topology selection reference for phase shifter designers. Design considerations such as circuit size, amplitude imbalance, operation frequency, bandwidth, tradeoff design feasibility and dual-band design feasibility are listed in the table. The tradeoff design feasibility shows whether the topology can be optimized for a specific bandwidth. The insertion loss is not taken into account because it is highly dependent on the switches and the Q factors of the components. Active phase shifters are not covered and therefore the power handling capability is not discussed. In the passive phase shifters, the power characteristics are mainly determined by the switches. The footnotes of the table show the focus of this thesis and some future possibilities to extend this work.

Generally, the topologies with distributed components have a large circuit size but also potential for higher operating frequencies. The amplitude imbalance is mainly determined by the practical considerations of the components. For example, for the RTPS, varactors are commonly used where perfect matching cannot be achieved for the whole tuning range. Thus, the amplitude imbalance is considerably larger compared to other topologies. The operating frequency shown in Table 7.1 has three categories: High (above 30 GHz), Medium (3 GHz-30 GHz), Low (below 3 GHz). The Lange coupler RTPS is limited by the required tight coupling and narrow strip

width for high frequencies, which may lead to a high insertion loss. For phase shifters with discrete components, the inductors mainly limit the high end of their operating frequency range. However, these designs are quite suitable for low frequency designs where many commercial applications are found. Typical bandwidths for different topologies are also listed. The bandwidth of the lumped designs relies on the components for different center frequencies while the bandwidths of the distributed designs are relatively stable. The feasibility of design tradeoffs and potential for dual-band design are also listed. Broadband designs, especially for the APN topology (lumped and the Schiffman phase shifter), are inherently suitable for multi-band designs because phase shifts at different frequency bands can be summed.

TABLE 7. 1. PHASE SHIFTER DESIGN TABLE

Phase shifter	Circuit Size	Amplitude Imbalance	Operating Frequency	Bandwidth	Tradeoff Possible	Dual-band Possible
Loaded-line	Large	Low/Medium	High	10%-15%	No	Yes*
HP/LP	Small	Low	Medium	30%-40%	Yes*	No
BP/APN	Large/Small	Low	High	50%-80%	Yes*	No
APN	Small	Medium	Low	20%-150%	Yes**	Yes***
Schiffman	Large	Low	Medium	50%-70%	Yes	Yes***
Branch coupler reflection type	Large/Small	Medium/High	High	10%	No	Yes***
Lange coupler reflection type	Large	Small/Medium	Medium	60%-100%	To some extent	To some extent***

*: Developed in this thesis **: Extended in this thesis ***: Theoretically possible but have not been reported

Using phase shifter design methods, microwave devices employing networks with ±90º insertion phase and certain characteristic impedance for transformation were also studied. In the last part of this work, an ultra-wideband (UWB) quadrature power splitter and two dual-band splitters were demonstrated.

For future research, the following aspects should be considered:

- Loaded-line phase shifters: The improvement in the bandwidth is achieved for distributed loads with fixed length TLs. Design procedures which provide e.g. bandwidth-performance tradeoffs should be further developed. For the dual-band designs, varactor based analog phase shifters should be considered.

- HP/LP phase shifters: only third order HP/LP filters were considered in this work. It is shown that the shifting of the resonant frequencies can improve both the phase and return loss performance. For further study, higher order HP/LP networks can be considered as the number of resonant frequency increases. The analysis will be more complicated but the design freedom will be increased.

- Phase slope alignment technique: various resonators can be used for this technique, and it can be combined with existing phase shifter topologies such as the HP/LP topology and the APN topology to get the balance of phase response and return loss within a given bandwidth. This technique can be especially used for millimeter wave designs to get an accurate phase shift over a certain

bandwidth by employing millimeter wave resonators.

- APN phase shifters: like the HP/LP phase shifters, higher order APN phase shifters should be investigated. It should be noted that when the bandwidth increases, the value of the components also increases, which poses a problem in practical designs. The distributed realization of this topology is also of interest.

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Appendix A: Influence of Load Mismatch on Network Insertion Phase

For analysis convenience, the signal flow graph of Fig. 1.8 is plotted

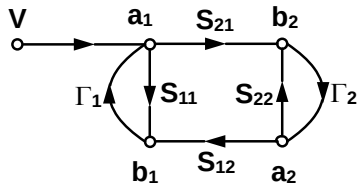

Fig. A.1. Signal flow graph of Fig. 1.8.

The cascaded networks are represented by two loads with reflection coefficients of Γ_1 and Γ_2. Based on Fig. A.1, the following equations can be obtained:

$$b_2 = a_1 S_{21} + a_2 S_{22} \tag{A-1}$$

$$a_2 = b_2 \Gamma_2 \tag{A-2}$$

$$b_1 = a_1 S_{11} + a_2 S_{12} \tag{A-3}$$

$$a_1 = b_1 \Gamma_1 + V \tag{A-4}$$

Note that V is obtained by loading Z_0 in an environment of Z_1, which leads to

$$V = V_S \frac{Z_0}{Z_0 + Z_1} = \frac{V_S}{2}\left(1 - \frac{Z_1 - Z_0}{Z_1 + Z_0}\right) = \frac{V_S}{2}\left(1 - \Gamma_1\right) \tag{A-5}$$

By solving (A-1) to (A-5), the transmission coefficient is found as

$$S'_{21} = \frac{1-\Gamma_1}{\left(1-S_{22}\Gamma_2\right)\left(1-S_{11}\Gamma_1\right)-S_{21}S_{12}\Gamma_1\Gamma_2} S_{21} \tag{A-6}$$

Appendix B: *S*-parameters of BPF with Two Poles and Three Poles

The S-parameters of the BPF with two poles are:

$$S_{11} = S_{22} = \frac{j\left(\Omega\bar{Z}_2 + \frac{2}{\Omega\bar{Z}_1} + \frac{\bar{Z}_2}{\Omega\bar{Z}_1^2} - \frac{\Omega}{\bar{Z}_2}\right)}{2\left(1 + \frac{\bar{Z}_2}{\bar{Z}_1}\right) + j\left(\Omega\bar{Z}_2 + \frac{\Omega}{\bar{Z}_2} - \frac{2}{\Omega\bar{Z}_1} - \frac{\bar{Z}_2}{\Omega\bar{Z}_1^2}\right)} \tag{B-1}$$

$$S_{21} = S_{12} = \frac{2\sqrt{1+\Omega^2}}{2\left(1 + \frac{\bar{Z}_2}{\bar{Z}_1}\right) + j\left(\Omega\bar{Z}_2 + \frac{\Omega}{\bar{Z}_2} - \frac{2}{\Omega\bar{Z}_1} - \frac{\bar{Z}_2}{\Omega\bar{Z}_1^2}\right)} \tag{B-2}$$

The S-parameters of the BPF with three poles are:

$$S_{11} = S_{22} = \frac{j\left(2\Omega\bar{Z}_2 + \frac{\Omega\bar{Z}_2^2}{\bar{Z}_1} + \frac{1}{\Omega\bar{Z}_1} - \frac{2\Omega}{\bar{Z}_2}\right)}{2\left(1 + \frac{\bar{Z}_2}{\bar{Z}_1} - \Omega^2\right) + j\left(2\Omega\bar{Z}_2 + \frac{\Omega\bar{Z}_2^2}{\bar{Z}_1} + \frac{2\Omega}{\bar{Z}_2} - \frac{1}{\Omega\bar{Z}_1}\right)} \tag{B-3}$$

$$S_{21} = S_{12} = \frac{j\sqrt{1+\Omega^2}}{2\left(1 + \frac{\bar{Z}_2}{\bar{Z}_1} - \Omega^2\right) + j\left(2\Omega\bar{Z}_2 + \frac{\Omega\bar{Z}_2^2}{\bar{Z}_1} + \frac{2\Omega}{\bar{Z}_2} - \frac{1}{\Omega\bar{Z}_1}\right)} \tag{B-4}$$

where $\Omega = \tan\left(0.5\pi\bar{\omega}\right)$.