Big Memories

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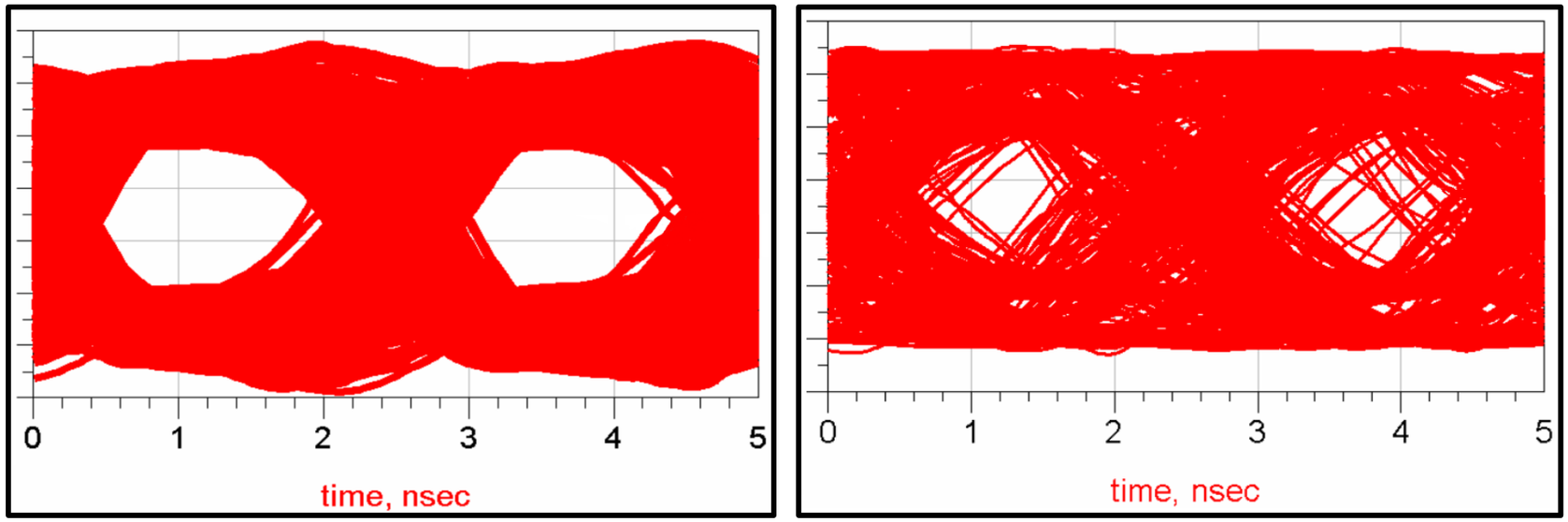
OUTLINE

- The Capacity Problem
- Solution I: BOB Memory Systems
- Solution II: Hybrid Memory Cube
- Solution III: Non-volatile Main Memories

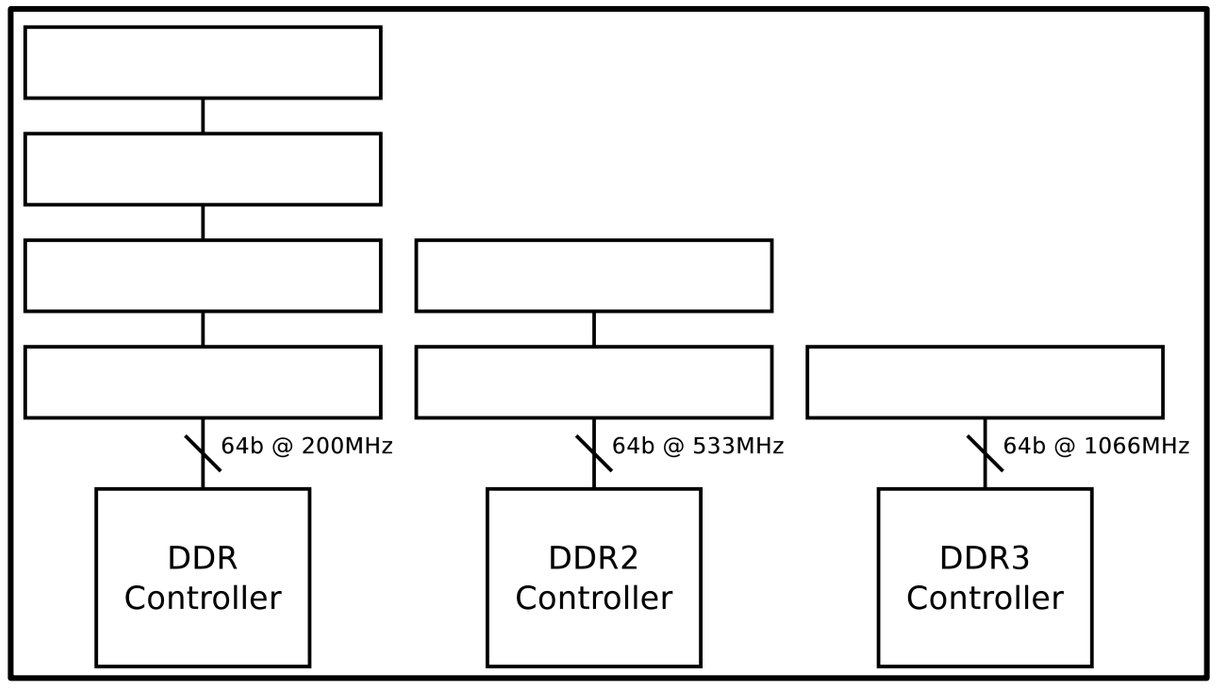
The Capacity Problem



Two DDR2-400 DIMMs **Four** DDR2-400 DIMMs

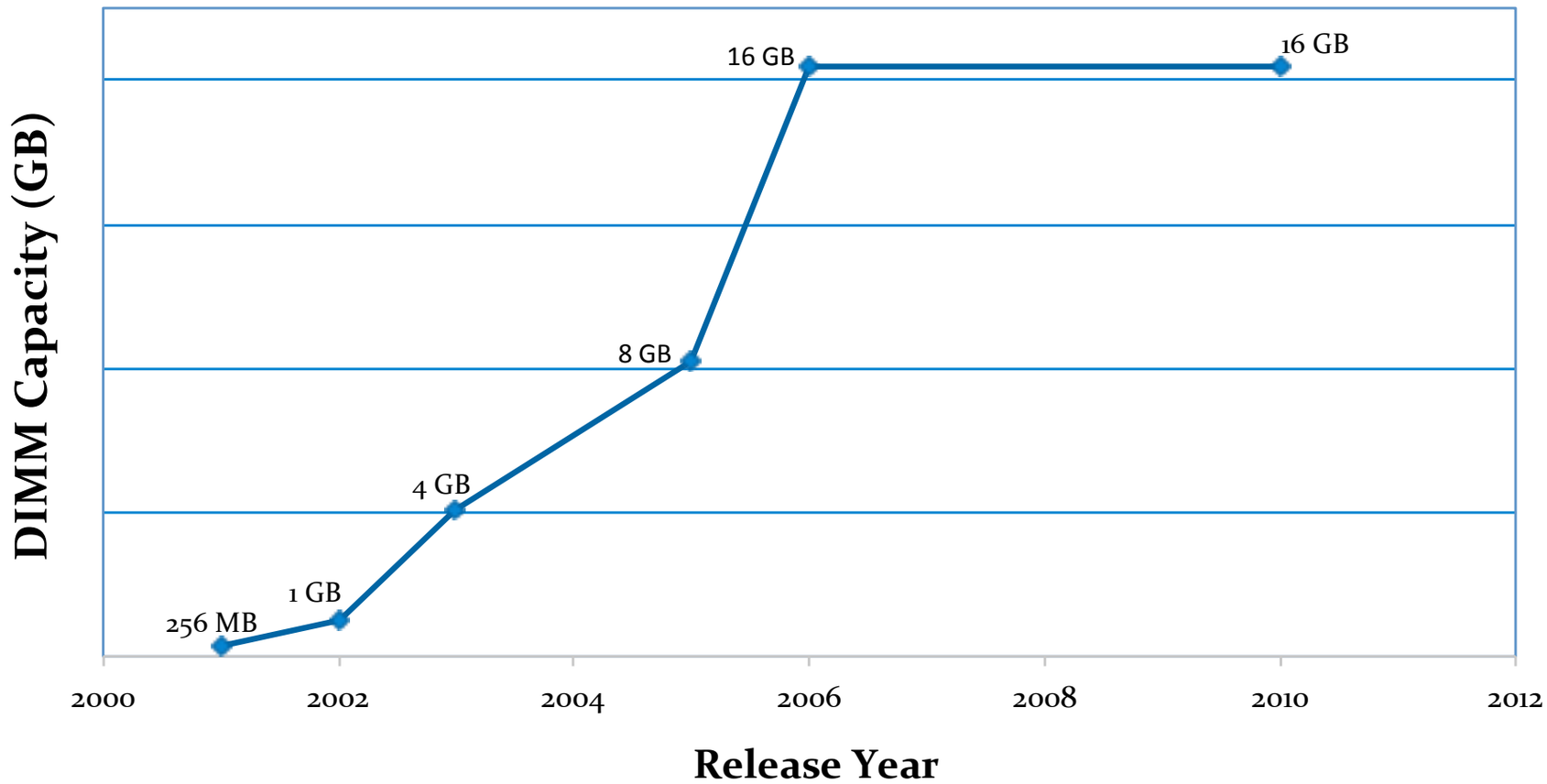
Source: Steve Woo. DRAM and Memory System Trends. October 2004.

=>



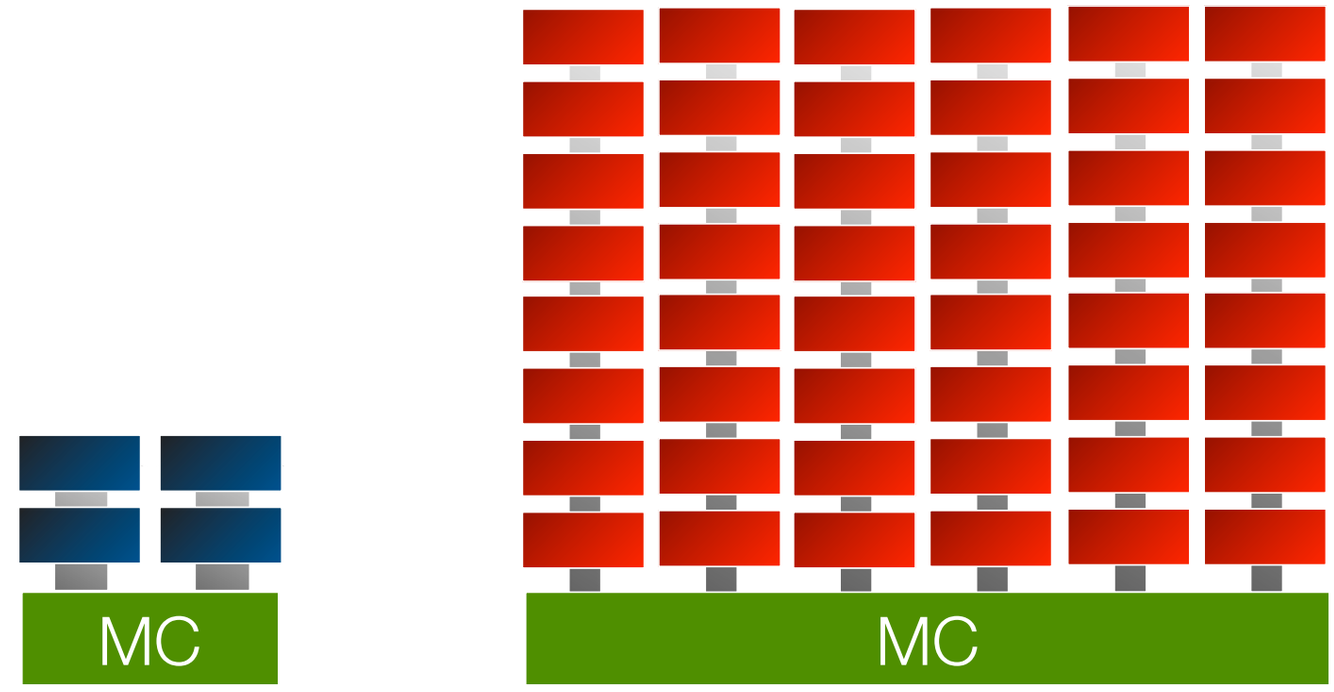
The Capacity Problem

… but wait, there's more:



Attempts at a Solution

- Highly Engineered DIMMs
  (can cost $1000+ per DIMM)
- Fully-Buffered DIMM
  (pushes the power envelope)



JEDEC DDRx
~10W/DIMM, ~20W total

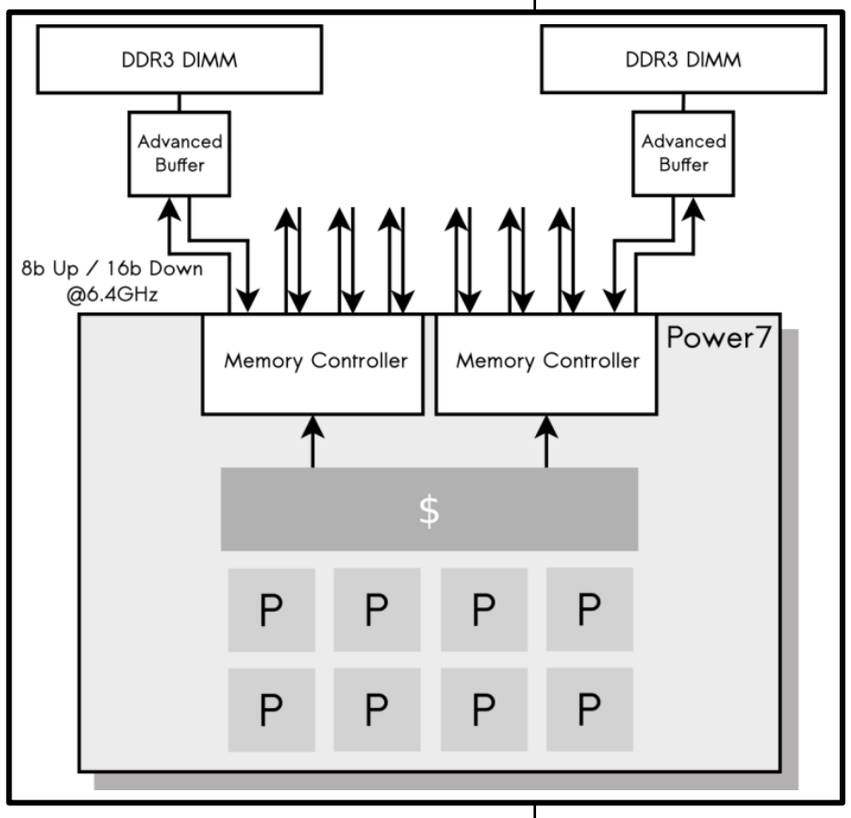
FB-DIMM
~10W/DIMM, ~300W total

Observations

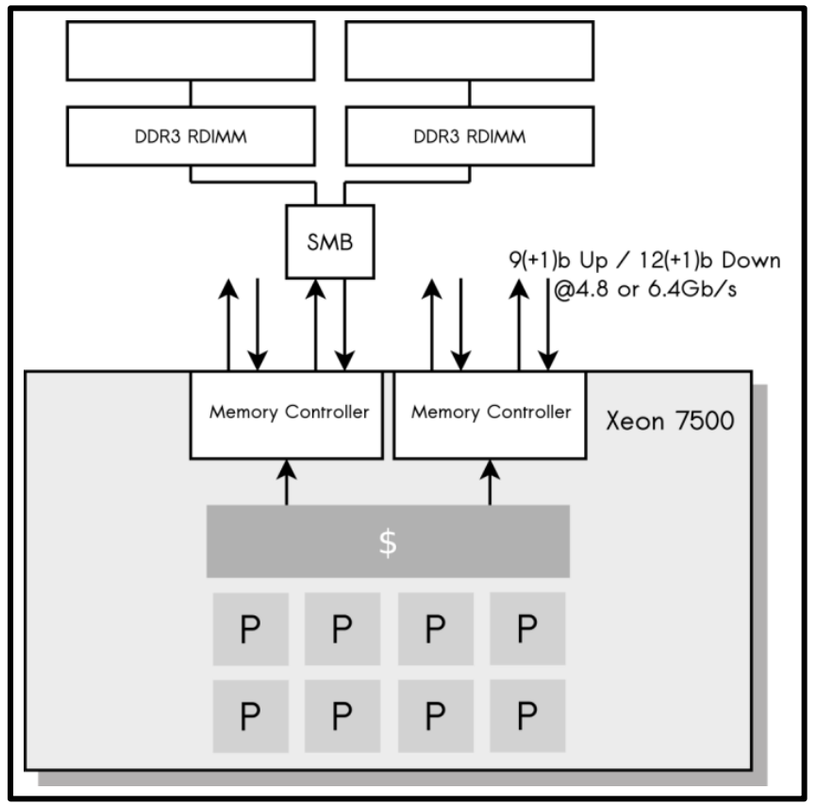
- **Cannot increase power** significantly (e.g. to CPU scale)
- **Cannot sacrifice bandwidth**
- Need to approach **commodity pricing**
- **Future-proof** design would be highly desirable

Solution I: BOB

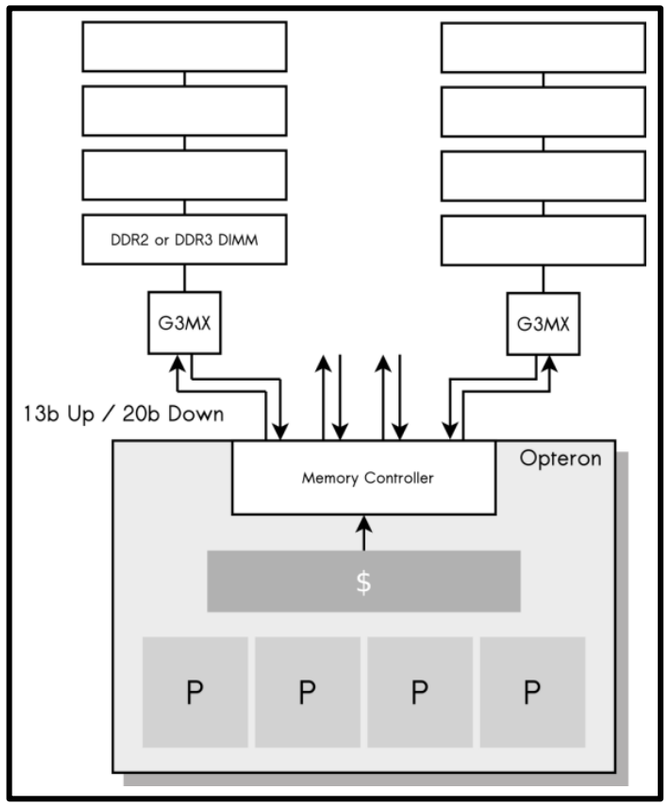
Buffer On (mother-)Board



IBM Power 795



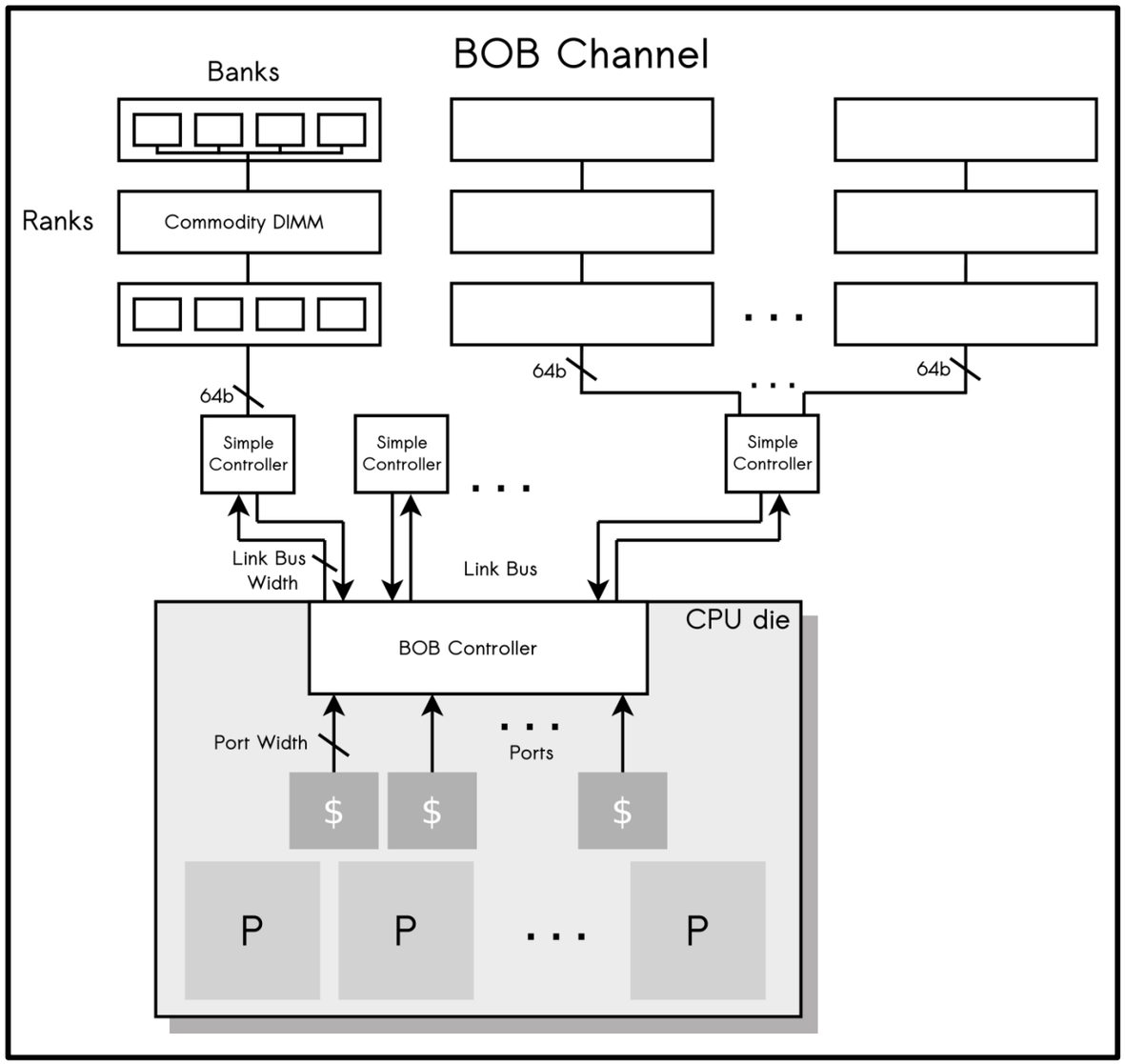
Intel SMI/SMB



AMD G3MX

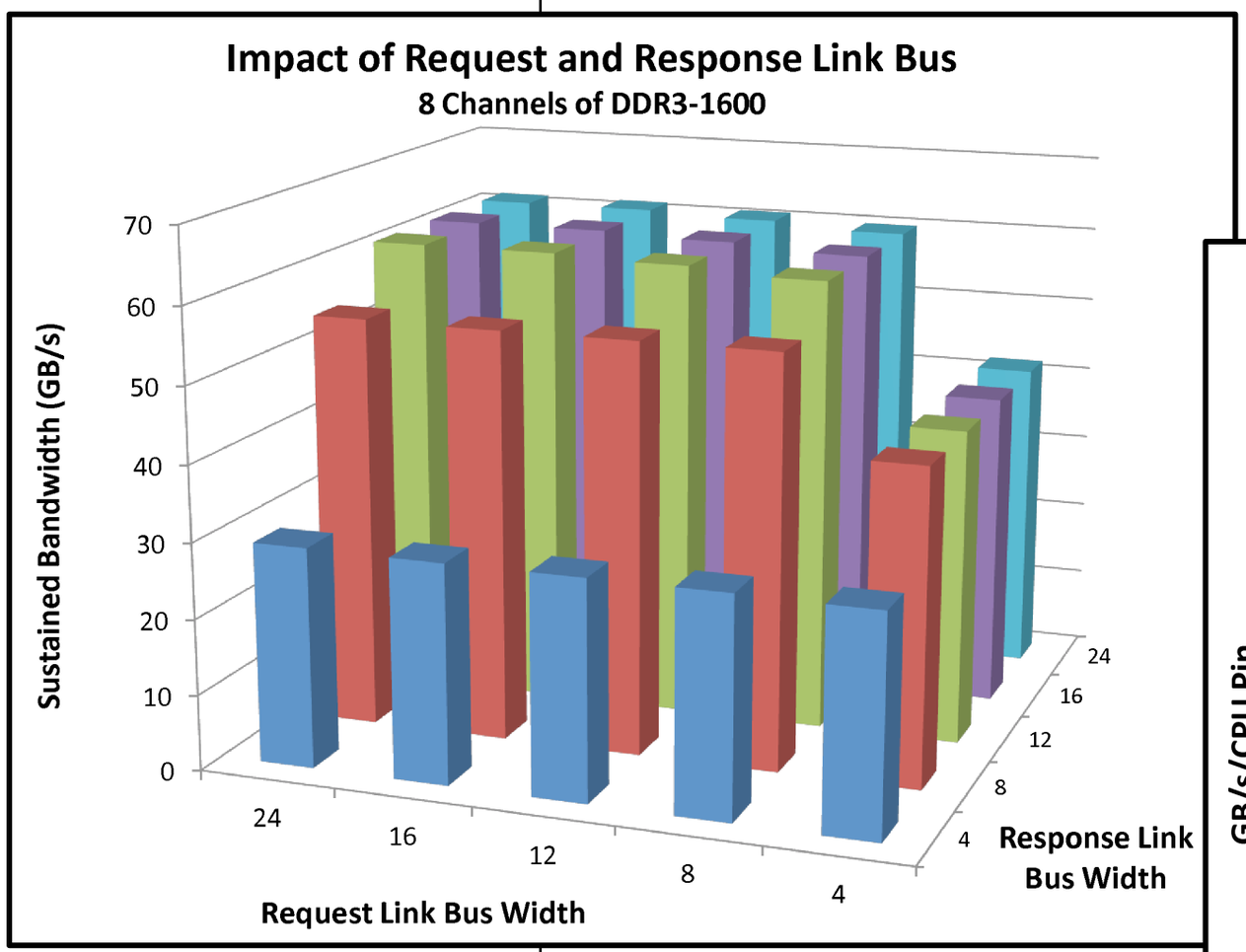
Solution I: BOB

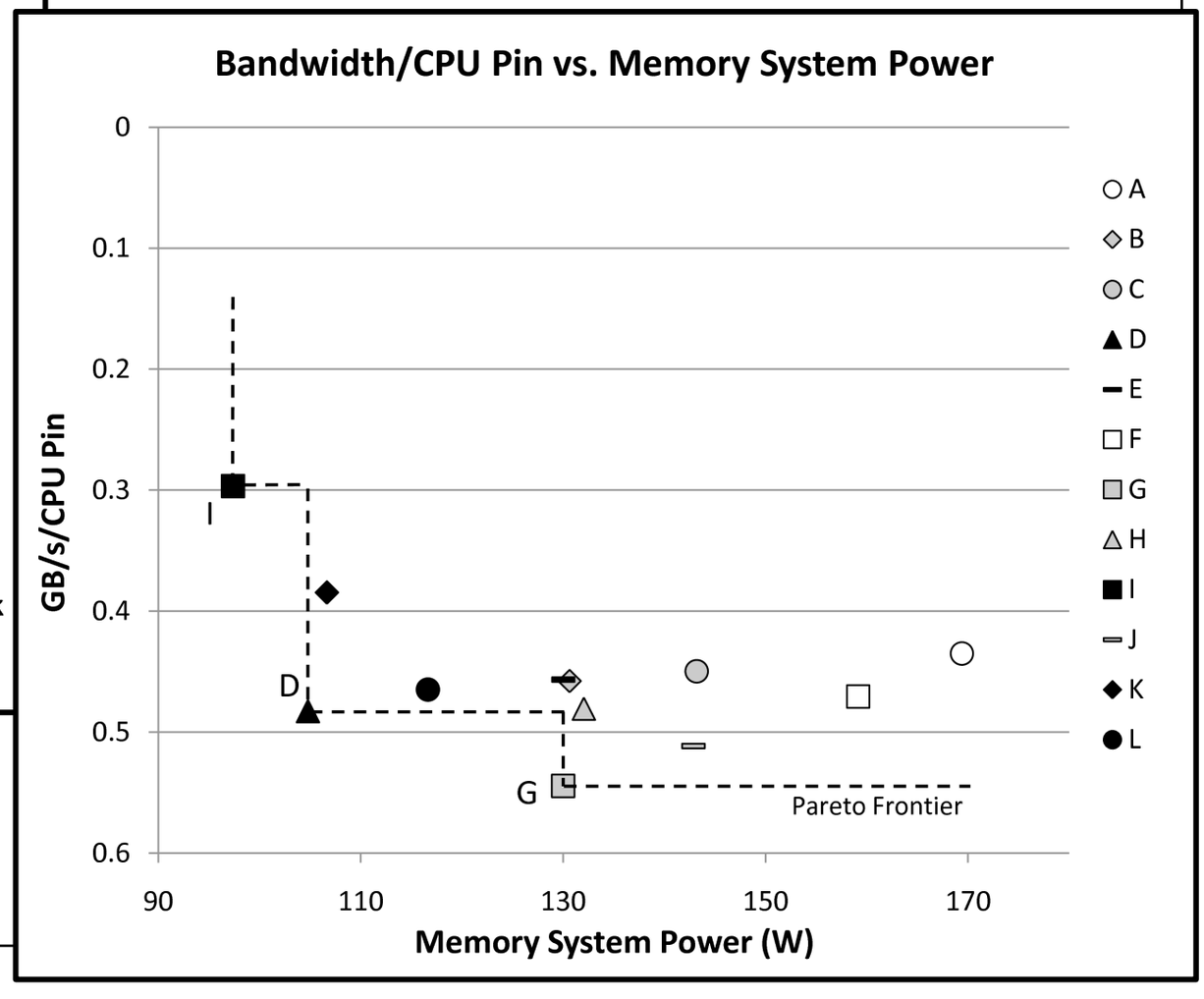
Buffer On (mother-)Board



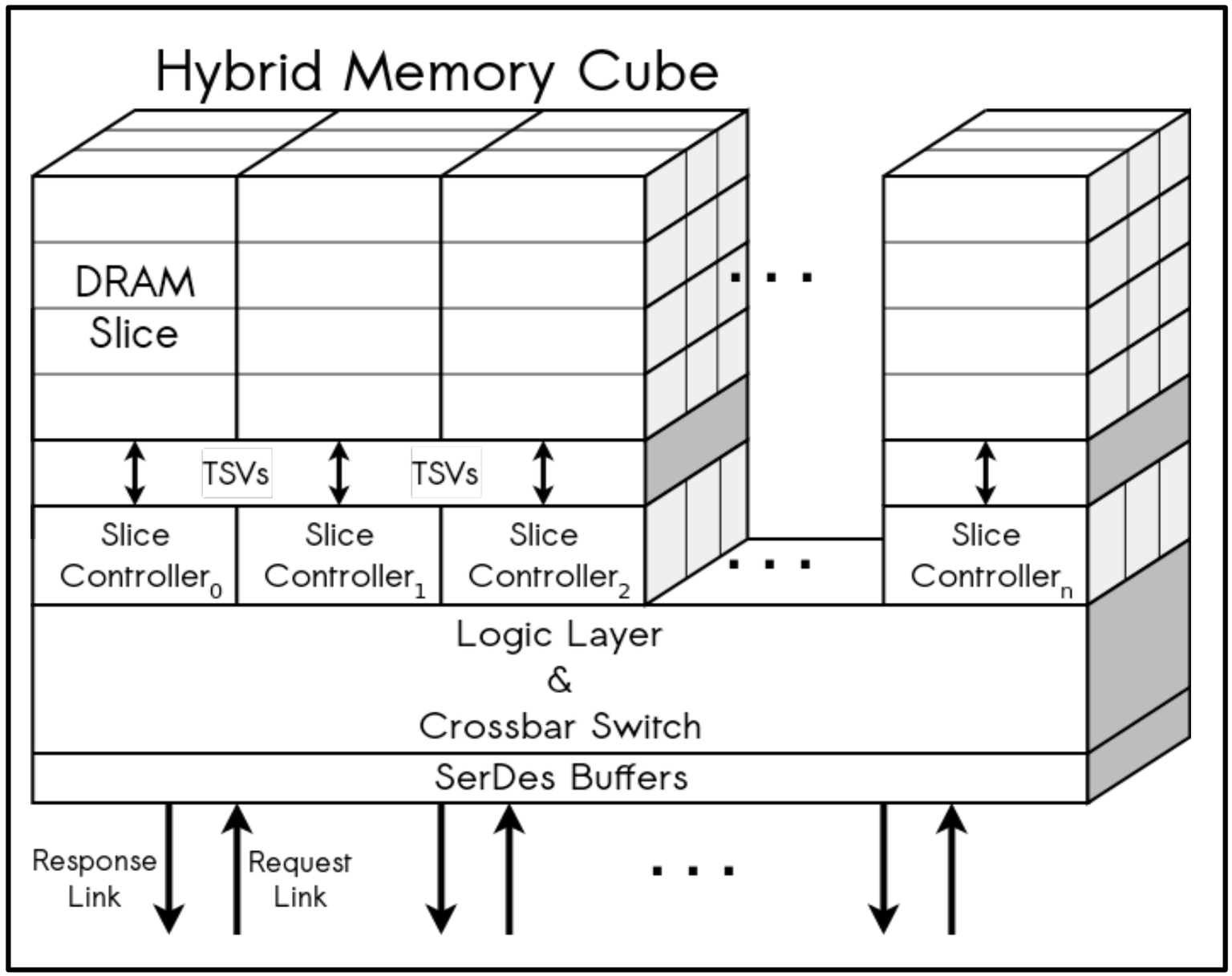
Solution I: BOB

Buffer On (mother-)Board





Solution II: Micron HMC



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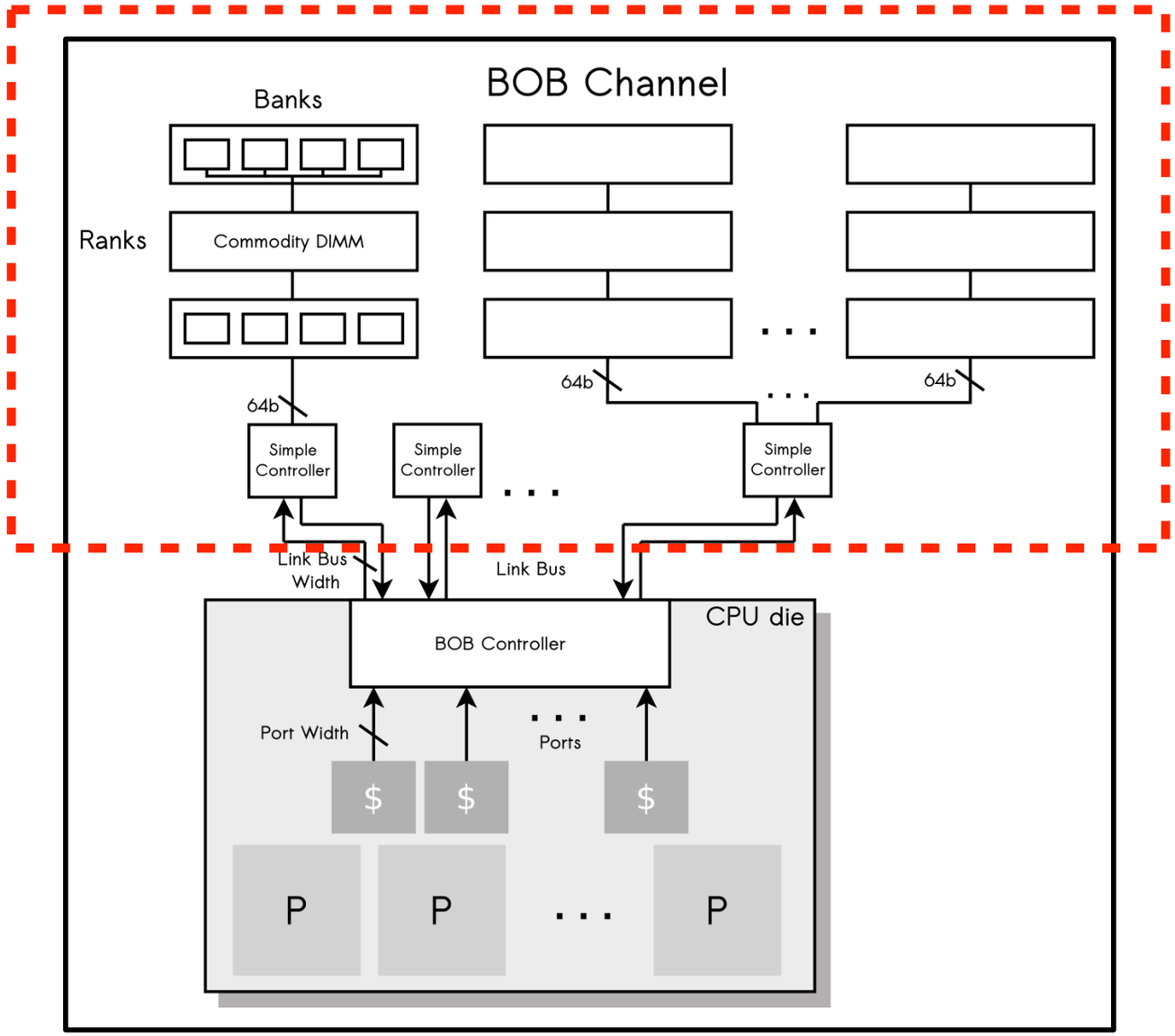
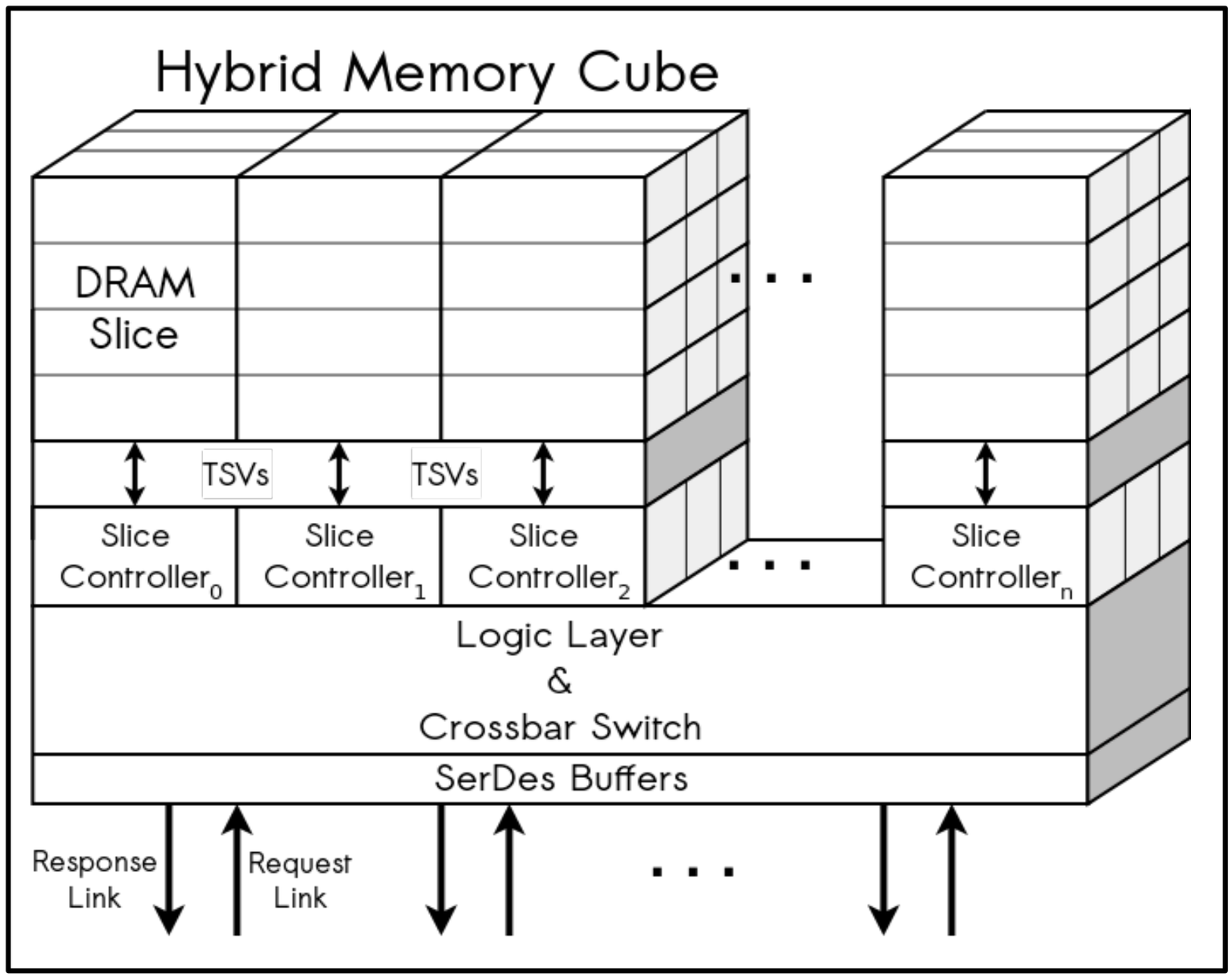
Solution II: Micron HMC

A single-chip BOB system



Solution II: Micron HMC



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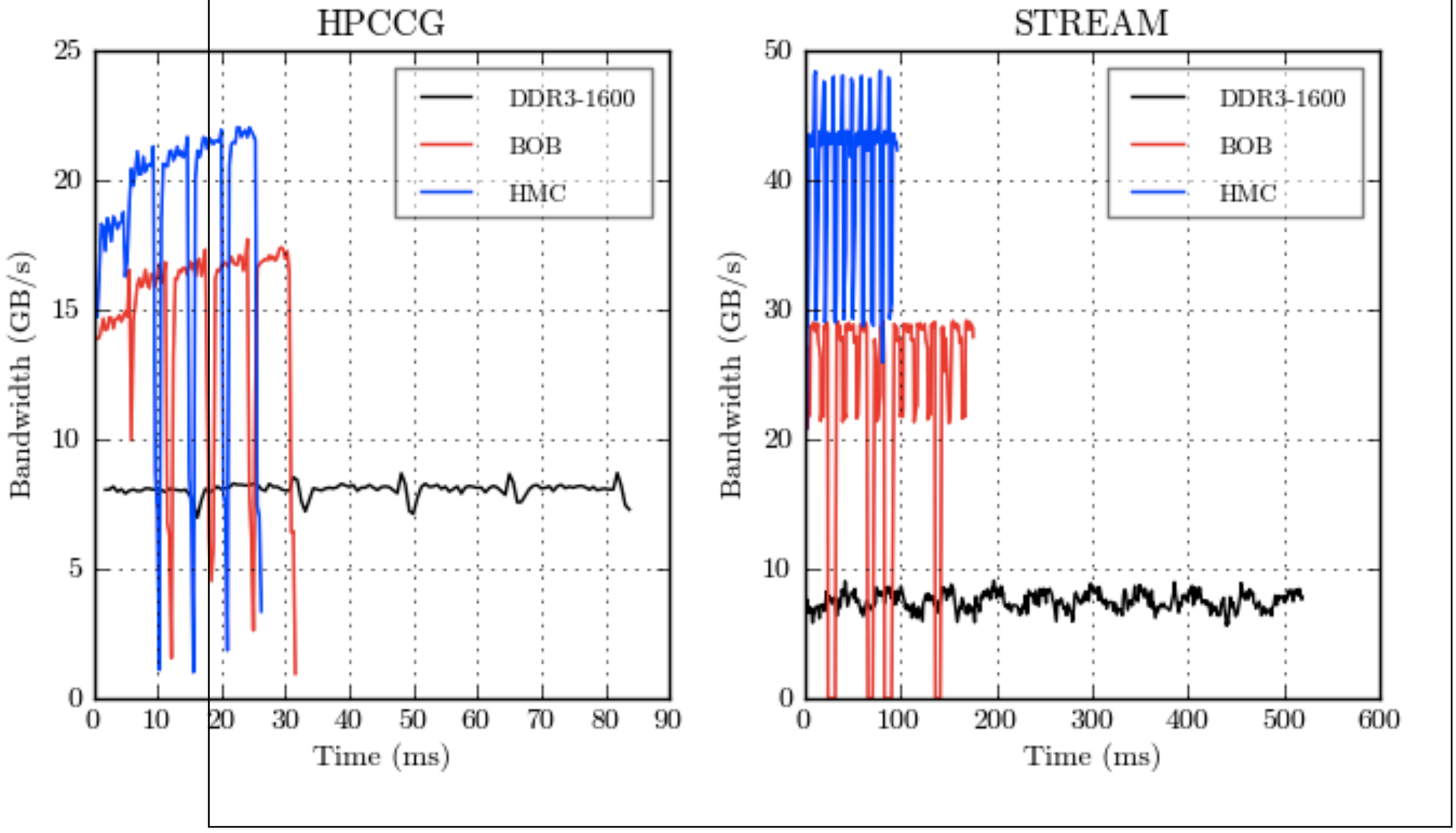

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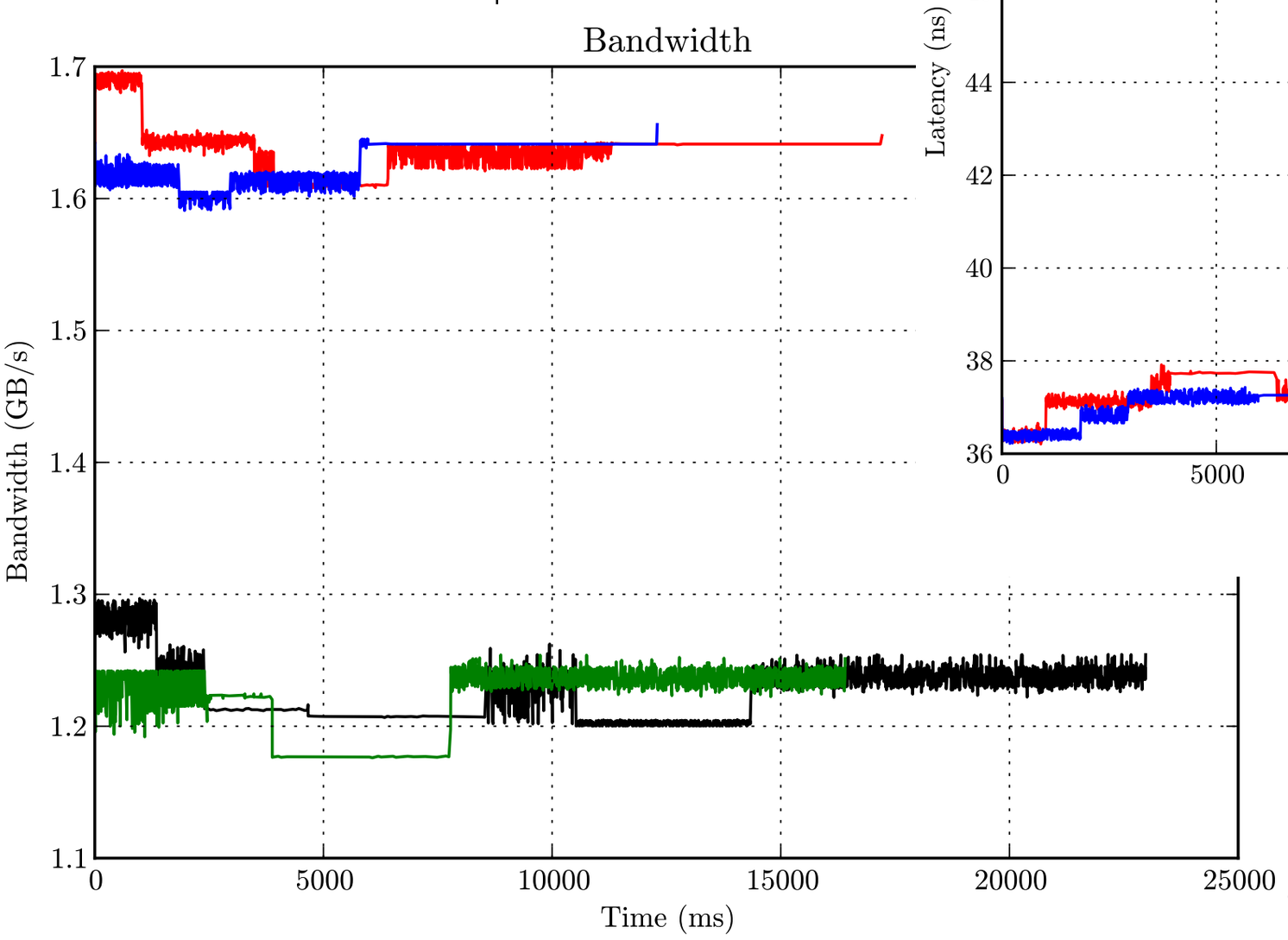
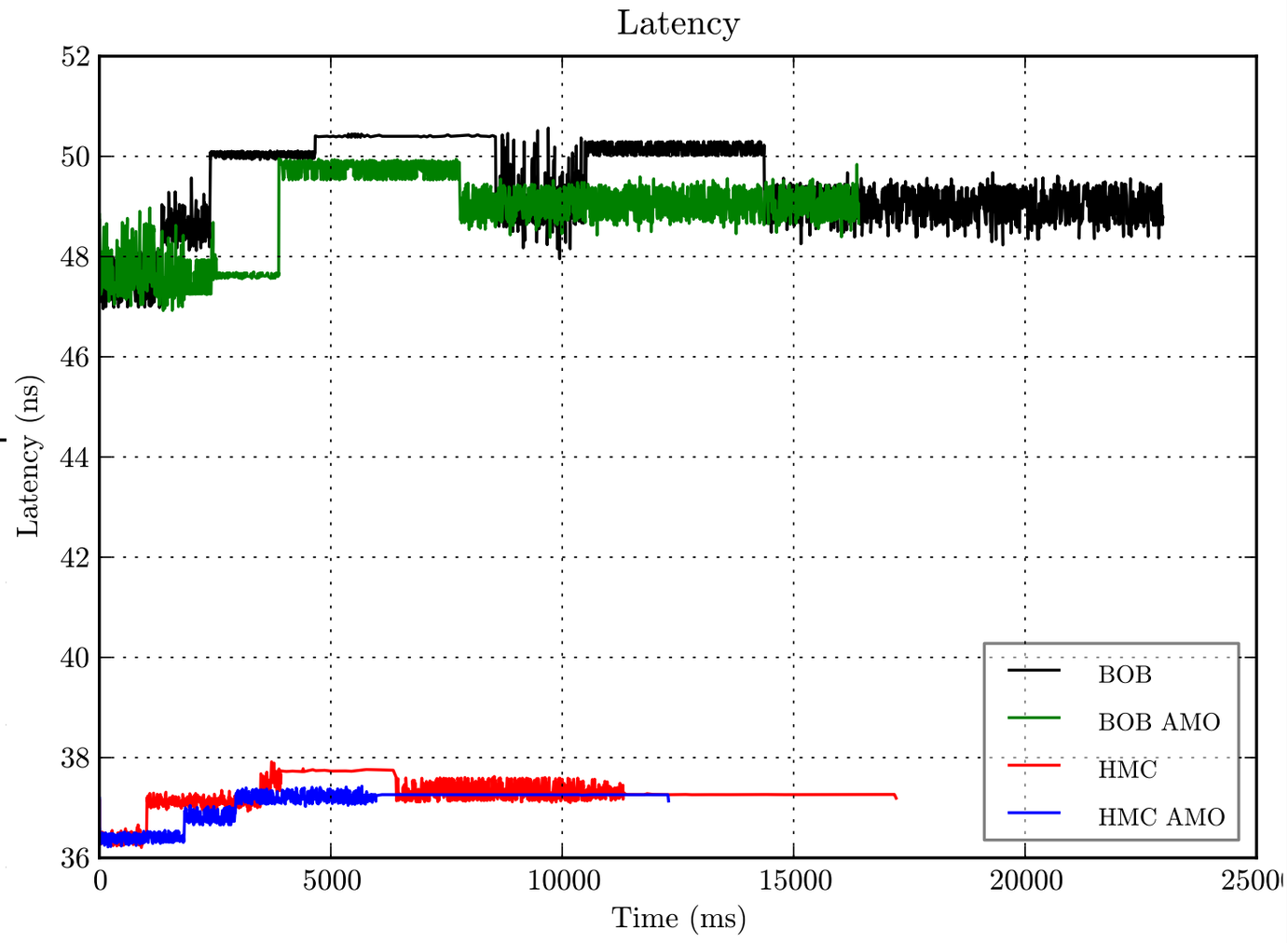
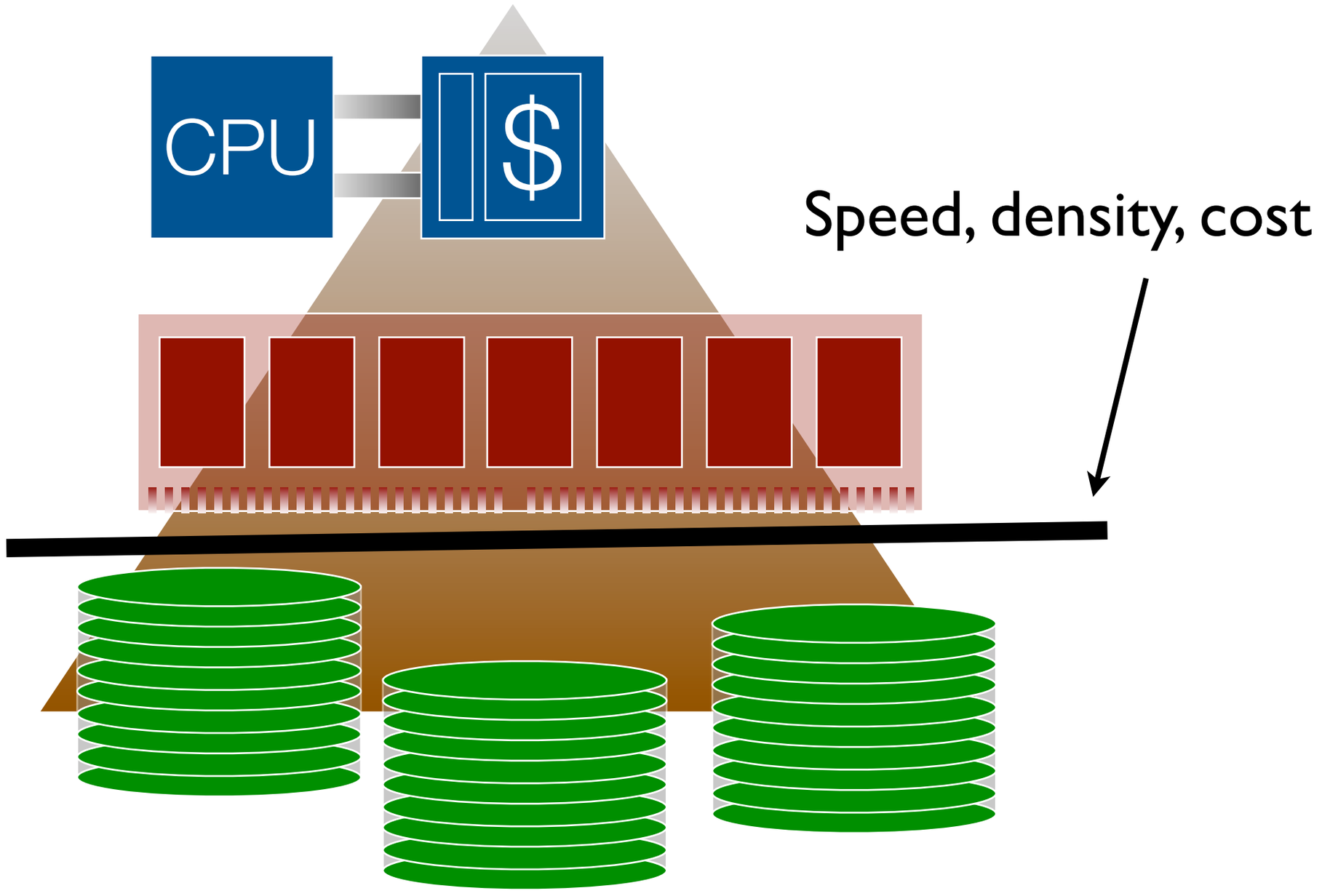


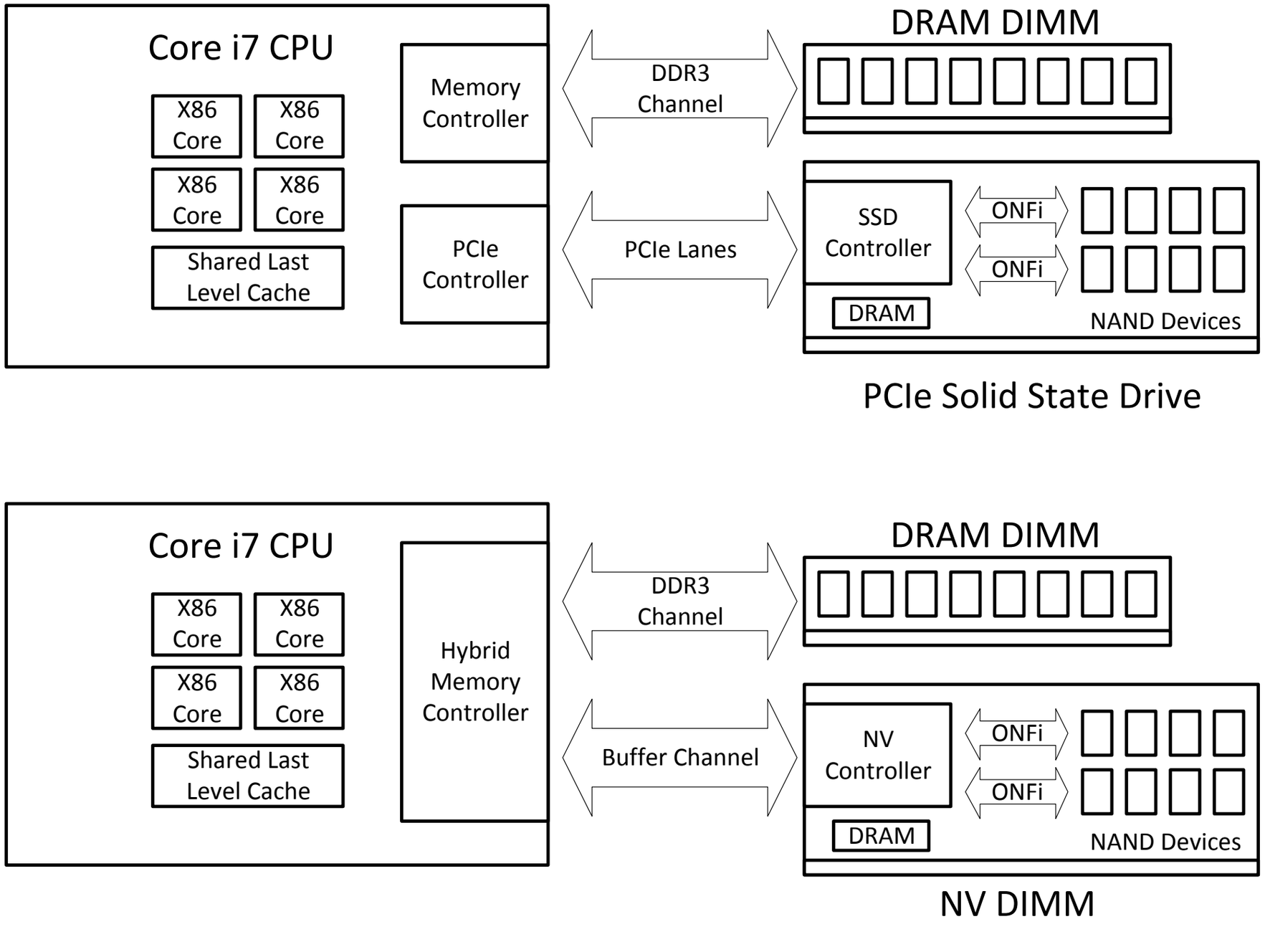


Solution III: Non-Volatiles



Can have TB-scale DIMMs today

Solution III: Non-Volatiles



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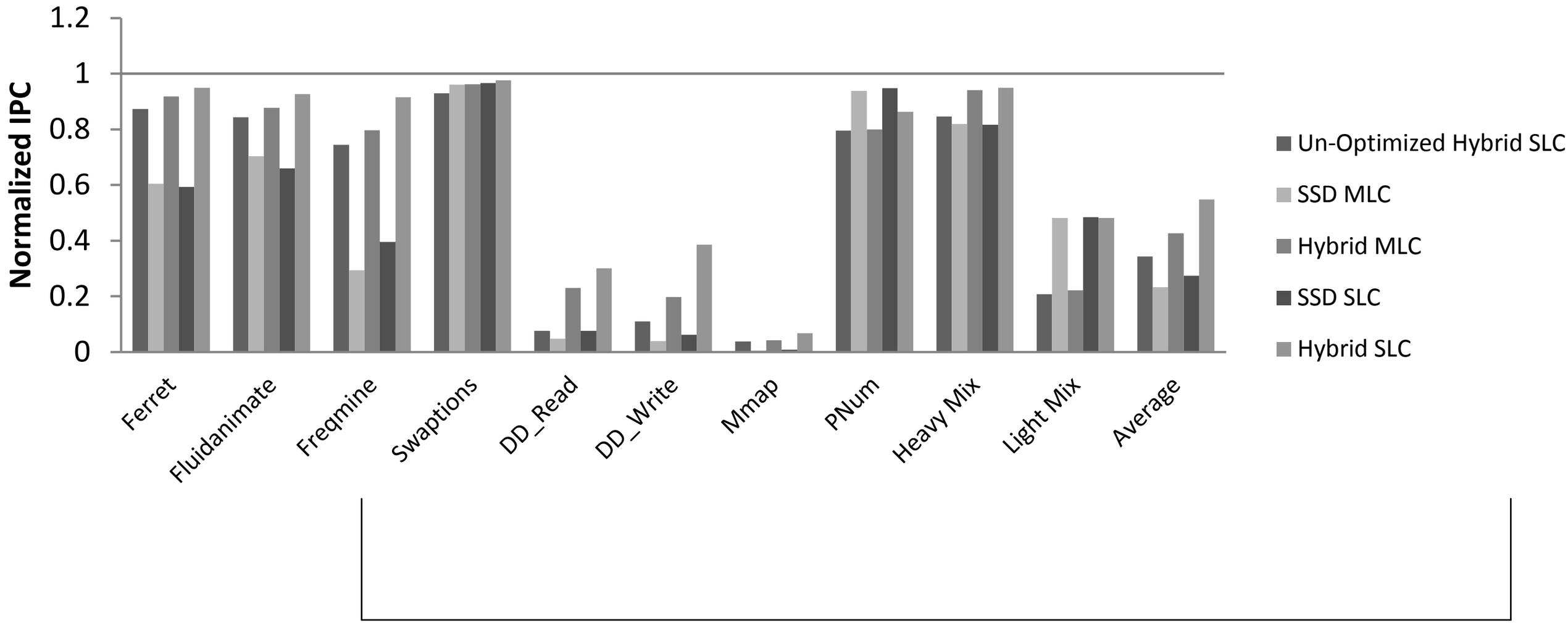
Solution III: Non-Volatiles

Performance normalized to that of TB-sized DRAM system



Bottom Line

- All three solutions are composable (this is GOOD)
- Power problem: solvable
- Bandwidth problem: solvable
- Cost problem: solvable
- HMC-style generic interface is future-proof by definition

Thank You!

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