CADENCE DESIGN TUTORIAL

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Table of Contents

Legend

BOLD TEXT	Designates Cadence windows and screens that should emerge when the user selects a specific action
ITALIC TEXT	Designates specific buttons, checkboxes, or radio buttons the user should select to perform specific actions
`COURIER TEXT`	Designates any codes the user should write either within the Cadence Environment or the Unix Environment

Abstract

As technology trends continue to grow in complexity, the need for Engineering Students to understand complex Electronic Design Automation (EDA) tools becomes ever-present. As it stands, many students entering the workforce lack experience with these design tools, despite the availability of University licenses. With this gap in experience in mind, this tutorial was written to expose students to the Cadence Design Tools available from the UCCS Electrical and Computer Engineering Department.

Introduction

The purpose of this tutorial is to introduce students to using Cadence Design Tools for the use in the design, simulation, and layout of a typical CMOS inverter. At the end of this tutorial the user should be familiar with Cadence Design Tools including the design environment, library and cell creation, and layout design. Through the completion of this tutorial, the student should be able to apply the skills learned to more complex designs whether for University projects or in the workforce.

Introduction to Cadence

To begin, the user should be logged into the Unix Environment, whether from a school laboratory computer or a VPN connection. The following sections detail how to setup the Cadence Environment from the Unix Environment as well as set up the correct directories.

Directory Setup

The user should begin by logging into a campus computer either directly from the lab, or from the LATS System (for more information on connecting with LATS, please see the UCCS IT Help Desk Page). When connected (from either VPN access or a school computer), the user should see the following screen:

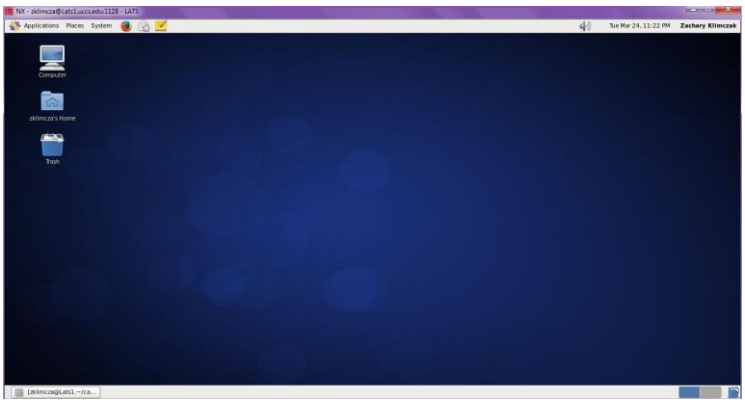


Figure 1: Default Unix Environment Desktop

Cadence will be run directly from the terminal window, so the user should open a terminal window as shown below:

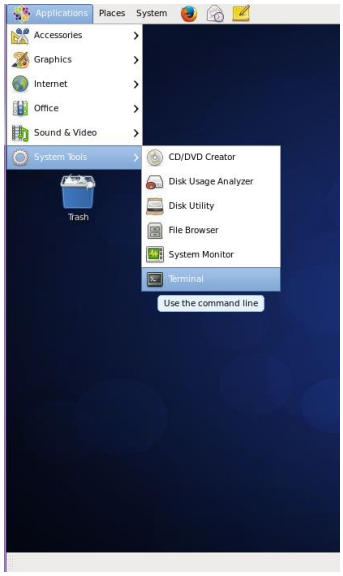
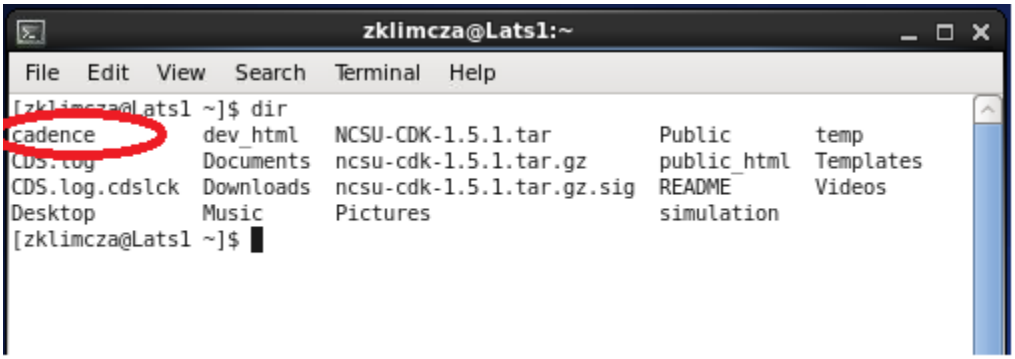


Figure 2: Opening a Unix Terminal Window

To check whether a cadence directory has already been created, the user should type `dir` and look for the directory titled "cadence", similar to the figure below:



THIS IS THE DIRECTORY WHERE ALL USER DEVELOPED CADENCE CELL VIEWS, LAYOUT DESIGNS, AND SIMULATION FILES WILL BE STORED

If this directory does not exist, the user needs to create the directory by typing `mkdir cadence`. The user can then navigate to this directory by typing `cd cadence`. The user now needs to create an instance of Cadence by typing `setcadence` or `setcadencedemo`. Please note: by typing "setcadencedemo" the user will have access to additional design files created by Dr. Kyle Webb; this may assist the user in using Cadence effectively, but is not necessary to the completion of this tutorial. The user can now run Cadence Virtuoso by typing `virtuoso` in the terminal window.

If working properly, the user should have two separate program windows open (the **Cadence Log Window** and the **Cadence Overview Window**), similar to the figure below:

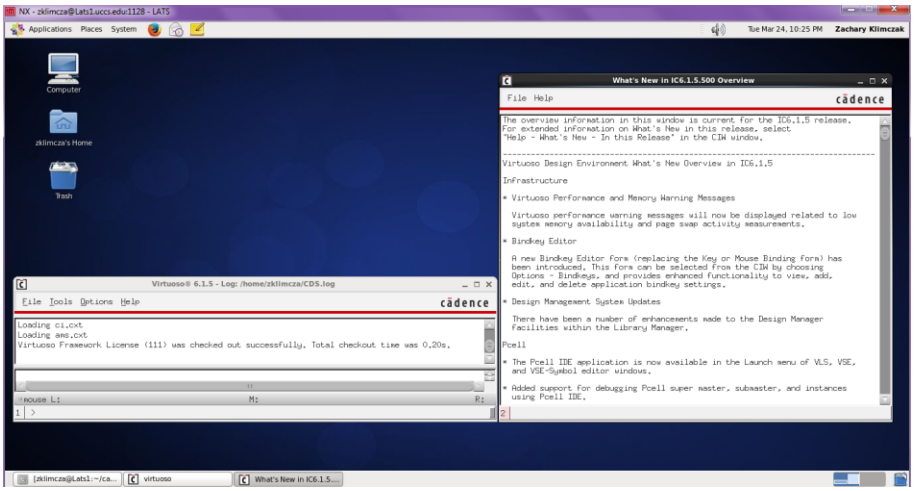


Figure 3: Cadence Log and Cadence Overview

Library Setup

As per figure 3 above, the left window is the **Cadence Log** (CDS.log), while the right is the **Cadence Overview**. The **Cadence Overview** window can be closed by clicking on the *x* in the upper right hand corner. THE USER SHOULD NOT CLOSE THE CDS.LOG FILE WINDOW FOR THE DURATION OF THE USE OF CADENCE. IF THE USER CLOSES THIS WINDOW, CADENCE WILL BE SHUT DOWN.

To assist the user in the collection and creation of schematic cell views (explained later), the user is recommended to create their own library. To do this, the user needs to click on *Tools*, then *Library Manager* from the CDS.log screen where an additional **Library Manager** window will come up similar to the figure below.

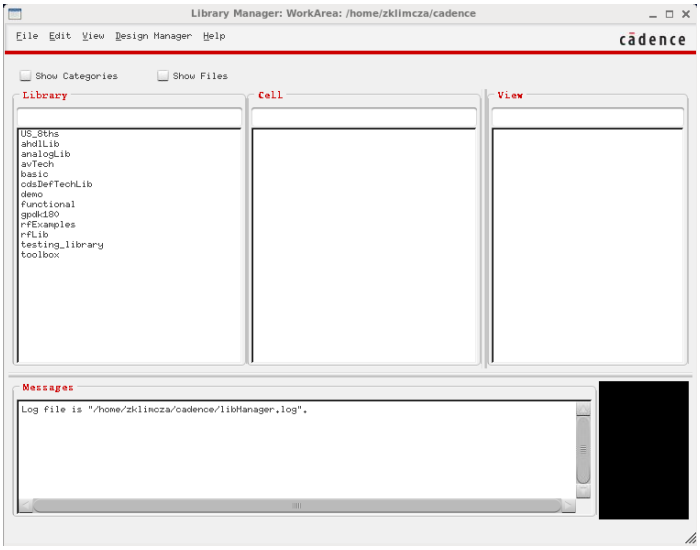


Figure 4: Cadence Library Manager

The user should then select *File*, then *New*, then *Library* from the options available, similar to the figure below. This will assist the user in creating a new library.

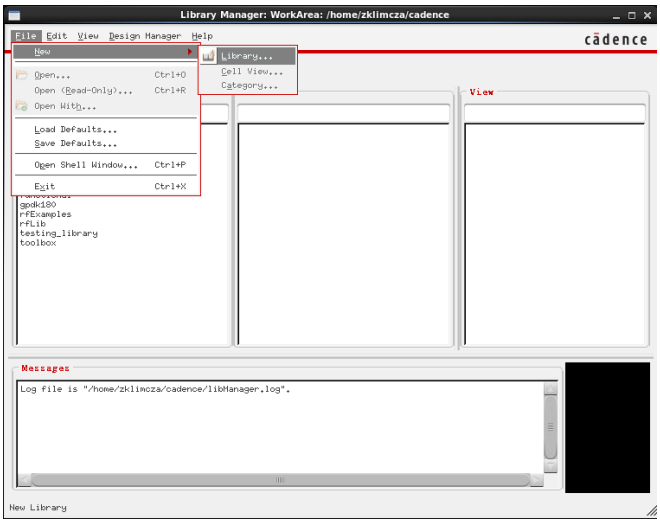


Figure 5: New Cadence Library Creation

A **New Library** window will be created. The user should type in a name of their choosing for their library. Traditionally, something such as `UserInitials_Cadence_Library` will be sufficient; however the user is free to select their own folder name. The user should then select *OK* when finished. The user should now see their recently created library in the **Library Manager** window on the left hand side, under the Libraries heading. The user should highlight their newly created library, right click, and select *Properties*. At this point, the user should be prompted to select a technology file for their library. For this, the user is recommended to select the option marked *Reference Existing Technology Libraries*.

The user should then be given a list of available libraries to reference to, shown in the left-hand column of the **Reference Existing Technology Libraries** window. The user should select the gpdk180 library and then select the → button to reference this library to their own library. The user can now hit *OK* to add these reference files.

At this point, the user has gone through the directory and library setup and created their own library to contain all of their Cadence Schematic, Simulation, and Layout files. The rest of this tutorial will rely on this library for design.

CMOS Inverter

Schematic Design

Now that the user has set up the necessary workspace, the user can now begin developing individual schematics for circuit design. To show this process, the user will begin by designing and simulating a simple inverter – a device used in countless Integrated Circuits.

Cell views are designated views for circuits within the Cadence Environment. It is possible to create cell views within cell views (subcircuits), similar to creating subcircuits within programs such as LTSpice.

To create a new cell view, the user should select *File,* then *New*, then *Cell view…* similar to the figure below. This can be done from either the **Cadence Log** window, or from the **Library Manager** window.

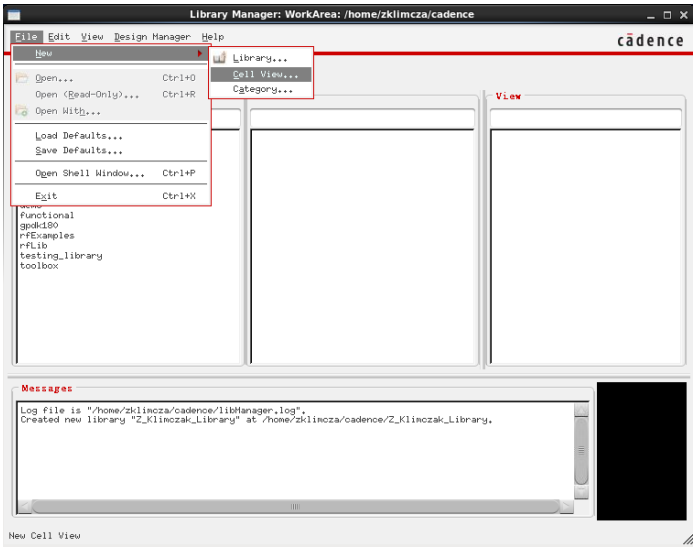


Figure 6: New Cell View Creation

From this, Cadence will bring up the **New File** window:

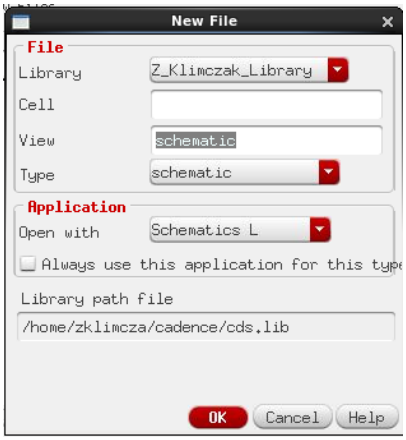


Figure 7: New File Window

Cadence allows the user to designate the view type for a given circuit (hence the name 'cell view'). For this example, the user will only be designing an Inverter; therefore the user should give this design the name of `UserInitials_Inverter` for ease of finding, selecting *schematic* as the type ('schematic' should be automatically selected as the default View), and then select *OK*. The following **Schematic** window will open:

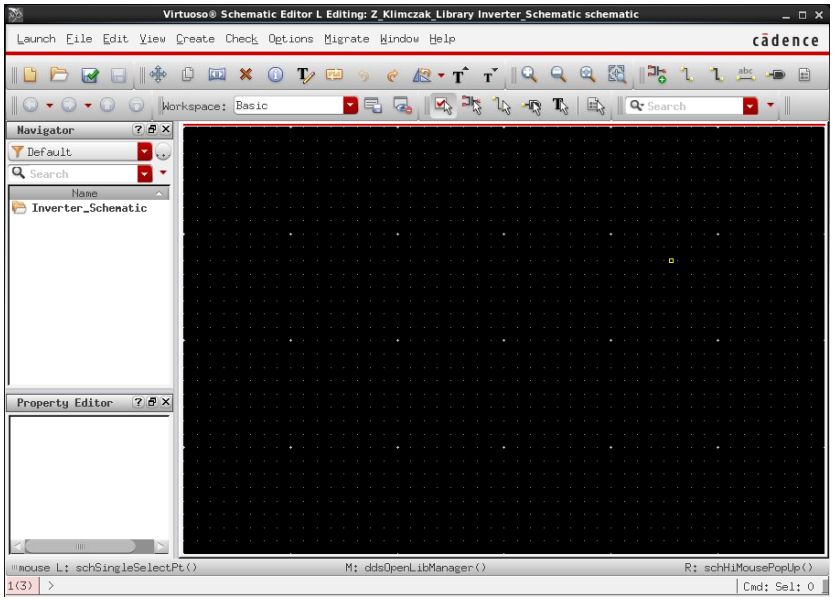


Figure 8: Schematic Design Window

The design environment has many tools that the user may find useful. While the details of these tools will not be covered in-depth within this tutorial, the tools are not overtly complicated, and the user should be able to pick up each tool's use with relative ease.

The user will be designing the following Inverter circuit:

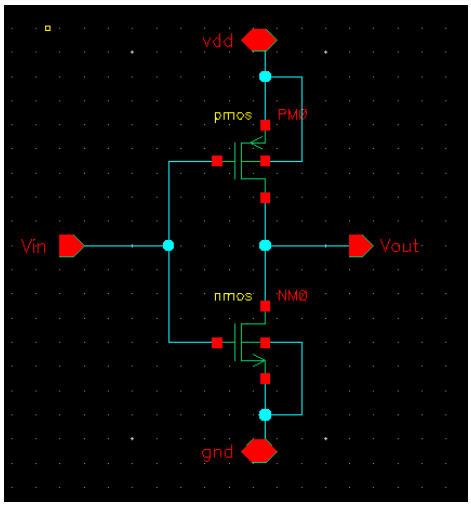


Figure 9: CMOS Inverter

To begin, the user should include two devices – a pMOS device and an nMOS device. To do this, the user should use the *i* shortcut key. The user should **Add Instance** window, similar to the figure below:

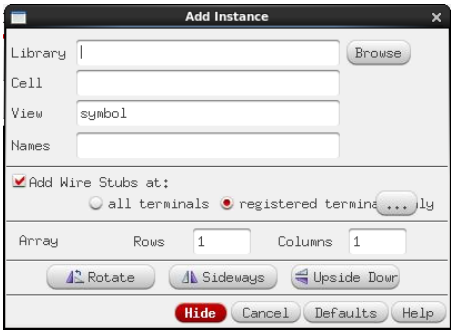


Figure 10: Add Instance Window

To navigate to the correct device, the user should select *browse.* The **Library Browser – Add Instance** window should be visible, similar to the figure below:

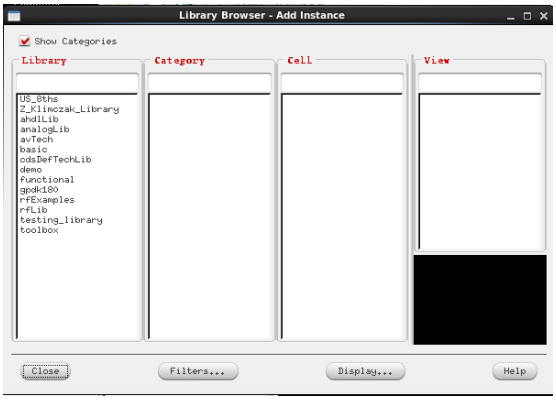


Figure 11: XXXX

From this, the user should select the *gpdk180* library located on the left hand window pane. The user should then select *pmos* as the desired device, located in the Everything category. The user should be sure to select *Symbol* in the view pane located on the right of the **Library Browser – Add Instance** window. The selected device will now appear over the design window when the user hovers the mouse over this area. The user should place the nMOS device wherever they wish. The following figure shows what the schematic will look like when the nMOS device is placed:

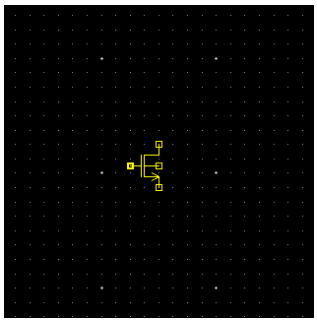


Figure 12: nMOS Device

The user should now add a pMOS device in the same manner from the same library. When these two devices are added, the schematic should now look like the figure below:

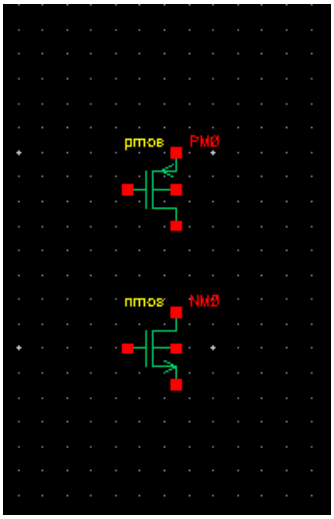


Figure 13: nMOS and pMOS devices

The user should now wire the devices together. A simple command for this is the *w* button, to draw wires. The user should then connect the wires between devices as follows:

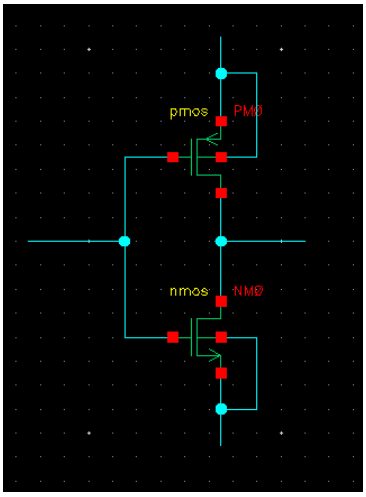


Figure 14: nMOS and pMOS with wired connections

The user can now set the pins (input/output) for this schematic, and designate their net names. To start, the user should press *p* to use the 'pin' command.

PLEASE NOTE: MULTIPLE PINS CAN BE SET AT ONE TIME. HOWEVER, ALL PINS SET AT ONE TIME WILL ALL BE INITIALLY OF THE SAME TYPE (INPUT, OUTPUT, BIDIRECTIONAL, ETC.).

The following **Add Pin** window should appear for the user:

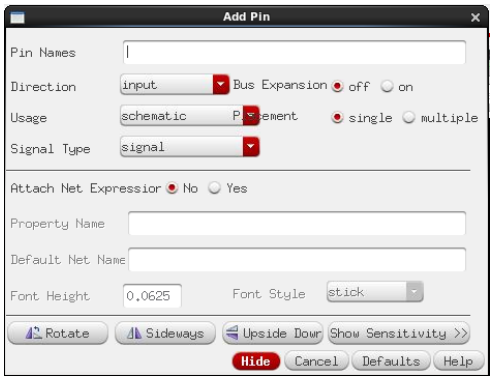


Figure 15: Add Pin Window

From this, the user should place two pins on the schematic, one for input, and one for output. The user can name these pins whatever they wish. For this demonstration, the author used 'Vin' and 'Vout' for these designators. The user should set these input and output pins on the input and output ports of the Inverter similar to figure 16 below. Likewise, the user should set two inputoutput pins for vdd and gnd. When finished, the user should then select the *Check and Save* button.

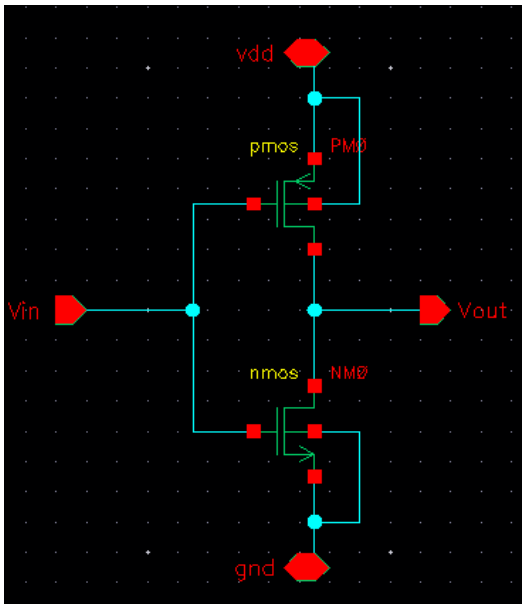


Figure 16: finished CMOS Inverter

If any errors were encountered during this phase, the user should follow the instructions printed out on the log window to ensure errors are corrected before proceeding.

Simulation

With the inverter design completed, the user can now proceed to simulating this device to ensure device functionality. Typically, inverters are meant to produce a complimentary signal – i.e. an output that is the opposite to its input. Thus, in a digital circuit, if a '0' is shown at the input, a '1' should be present at the output, and vice versa.

NOTE: HAVING A BASIC UNDERSTANDING OF EXPECTED CIRCUIT BEHAVIOR CAN BE EXTREMELY BENEFICIAL TO DEBUG WITHIN A DESIGN ENVIRONMENT.

To run the simulation environment, for this tutorial the user will be using ADE L. To select this, from the schematic window, the user should select *Launch* and then *ADE L*. Selecting this will bring up the following **Simulation** window:

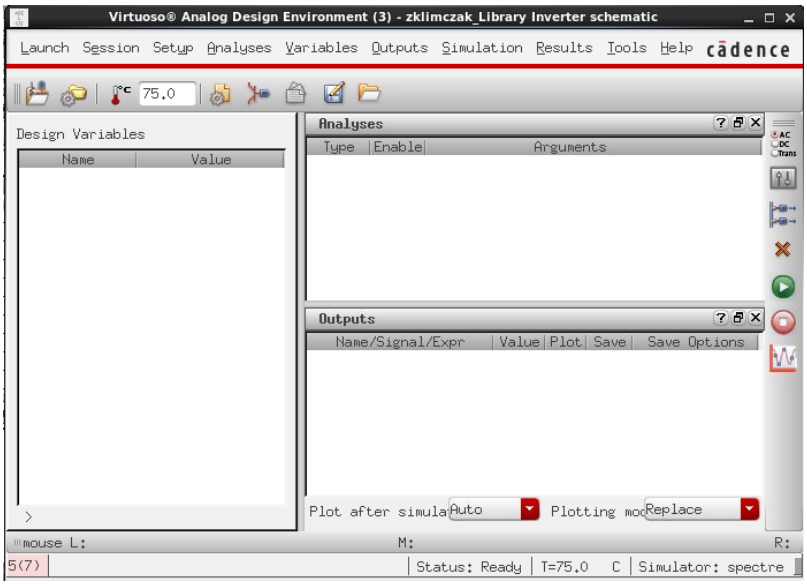


Figure 17: Simulation Window

To begin, the user must first select the type of stimuli that will be present at each of the associated pins within the schematic, as well as selecting the voltage level for any DC voltages present. To do this, the user needs to select *Setup* and then *Stimuli…*. This action will bring up the **Setup Analog Stimuli** window:

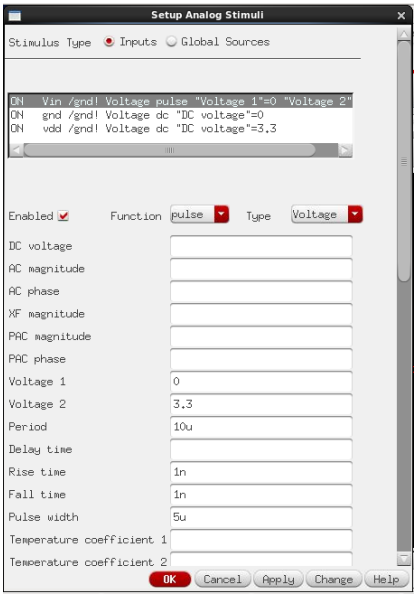


Figure 18: Analog Stimuli Window

There are two types of stimuli available within Cadence. The first is 'Inputs'. These are any input/bidirectional pins that have been placed on the schematic. The second is 'Global Sources'. These are any of the global VDD or VCC lines that have been setup on the schematic (not used in this design). For this tutorial, the inputs pin marked 'Vin', 'gnd', and 'vdd' show up on the list of available Inputs.

NOTE: INPUTS AND GLOBAL SOURCES ARE ALWAYS MARKED WITH RESPECT TO GROUND AS SHOWN BY THE NOTATION 'PIN_NAME' / gnd! WHERE 'gnd!' IS A UNIVERSAL NET.

The user must first select the *enable* button located on the sources window. As the input to this circuit will be a basic pulse train, the user should set the *Function* dropdown box to *Pulse*. The user should then set the following parameters within the window for inputs:

Table 1: Input Pulse Parameters

Parameter	Value
Voltage 1	0V
Voltage 2	3.3V
Rise time	1p
Fall time	1p
Pulse width	5u

For the *gnd* option, the student should ensure the *function* dropdown is set to *dc* and the value for *DC Voltage* is set to 0V. Likewise, a similar procedure should follow for the *vdd* option, only with a DC value of 3.3V setup.

The user can now click on *OK* to close this window. The user must now set up what type of simulation they want to run. In this case, since the input to this circuit is a pulse train, the user needs to run a transient simulation for the first three to five cycles of the input. To do this, the user should select *Analyses* and then *Choose…*. The following **Choosing Analyses** window should appear:

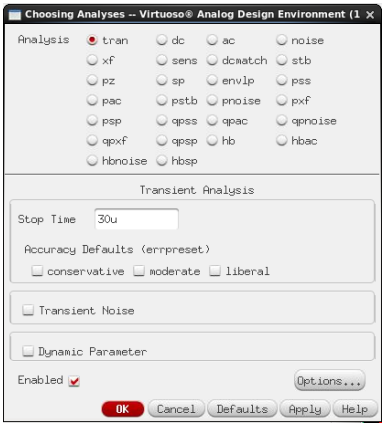


Figure 19: Analysis Window

The *tran* option should be highlighted. As this is the option the user wants, no other options should be selected. Since the input pulse to the circuit designed was given a time period of 10 µs, the user should set the *Stop Time* value to 30 µs. The user should then select the *enable* button before selecting *apply*, and then select the *ok* button.

The user should now see the type of simulation being run (in this case a transient simulation) in the top window of the **Simulation** window, similar to the figure below.

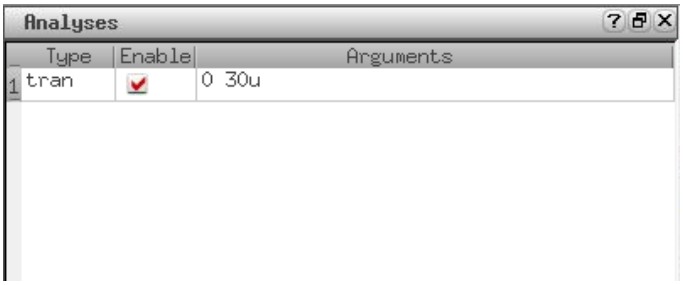


Figure 20: Transient Simulation Selected

In the event that multiple simulations needed to be run, the user could set multiple types of simulations, and then select which type of simulation needed to be run at any time. In this case, since the user is only running a transient simulation, only the *tran* simulation should be showing in the *Analyses* portion of the **Simulation** window.

The final step involves selecting the outputs that are to be plotted. To do this, the user should select *Outputs*, then *To be plotted*, then *Select on Schematic*. This will bring the user back to the cell view, where the user can now select the nodes to be plotted. In this case, to confirm the Inverter works in the way it is designated, the user should select both the input and the output nodes. To do this, the user should simply click on these pins. When selected, the pins and associated nodes should highlight red, similar to the figure below:

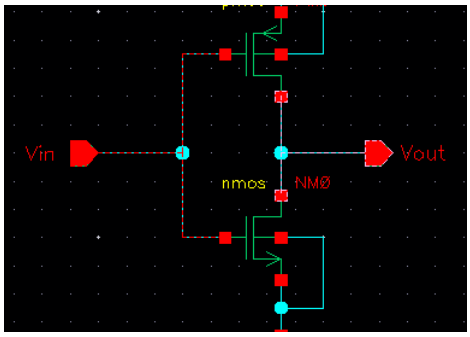


Figure 21: Highlighted Nodes confirming Simulation

Once all the nodes to be plotted are selected on the schematic, the user can now select the **Simulation** window again. Now that the desired outputs have been selected, the user should see both of these outputs selected in the *Outputs* frame of the **Simulation** window. Since the author has named these pins *Vin* and *Vout*, these can be seen in the figure below. The user should have something similar.

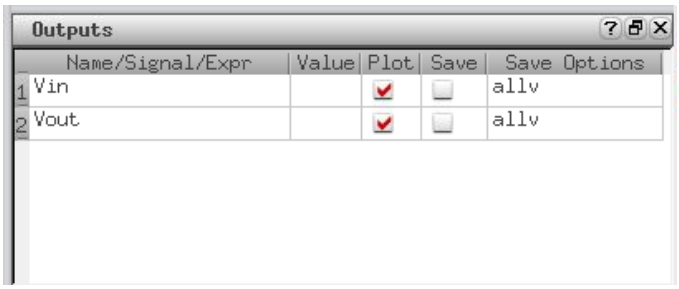


Figure 22: Outputs Pane

To simulate, the user should now select the *Netlist and Run* button on the right side of the simulation window. Selecting this option will generate a log window as Cadence runs through the simulation parameters, before generating the outputs on the screen.

NOTE: WHEN THE SIMULATION HAS FINISHED, ALL GRAPHS WILL BE PLOTTED ON THE SAME GRAPH, TOGETHER. TO SEPARATE THESE GRAPHS FOR EASE OF VISIBILITY, THE USER SHOULD SELECT THE GRAPH(S) THEY WISH TO MOVE, RIGHT CLICK AND SELECT 'MOVE TO', THEN 'NEW SUBWINDOW'. THIS WILL SEPARATE OUT THE GRAPHS SIMILAR TO THE FIGURE BELOW.

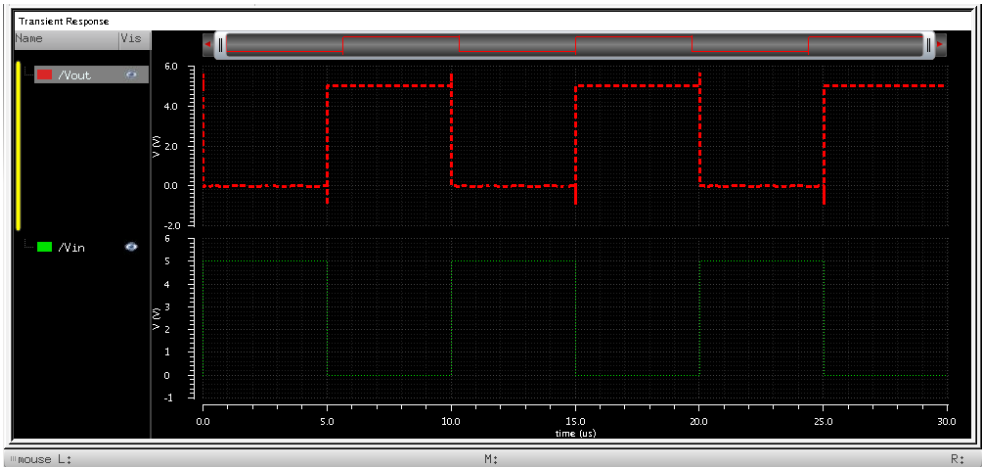


Figure 23: Completed Simulation of Inverter

This concludes the simulation portion for the Inverter. If the user is required to include screenshots of simulation results, the user should select 'File' then 'Save Image' to save the selected outputs in a number of different file types.

Layout

To begin layout the user should select *Launch*, then *Layout XL*. This will bring up the **Startup Option** window

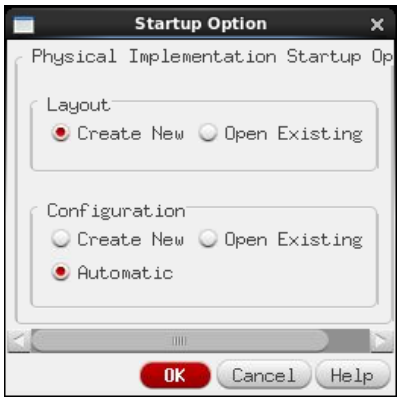


Figure 24: Layout Options Window

The user should select the two radio buttons marked 'create new' under both the layout and configuration sections and select ok. The **New File** window will appear:

Figure 25: New Layout File Window

The user should give this cell the same name that was given for the schematic, and ensure that the view type selected is 'layout' before selecting *ok*.

The user will then be given the following **Layout Design** window:

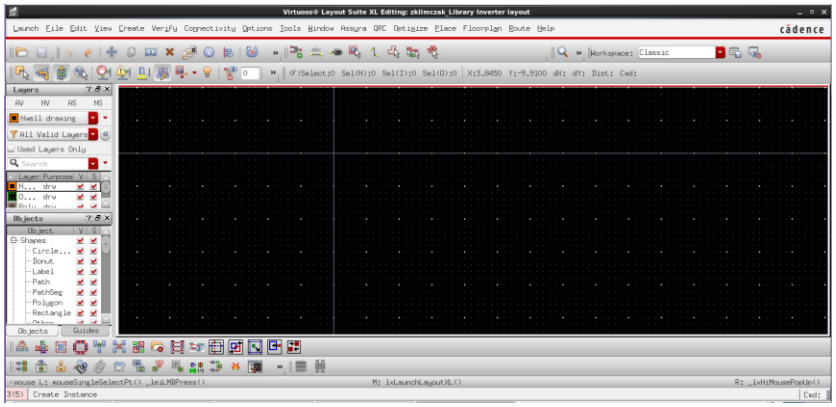


Figure 26: Layout Design Window

The user should take some time to familiarize themselves with the various layout options in this window before proceeding. The user should select the *Generate all from source* button, located in the lower left hand corner of the window, as seen below:

Figure 27: Generate all from source Button

Selecting this button will generate all of the cell views that were utilized in the schematic and transpose them to layouts, including the inputs and output. When this button is selected, the user should see the **Generate Layout** window:

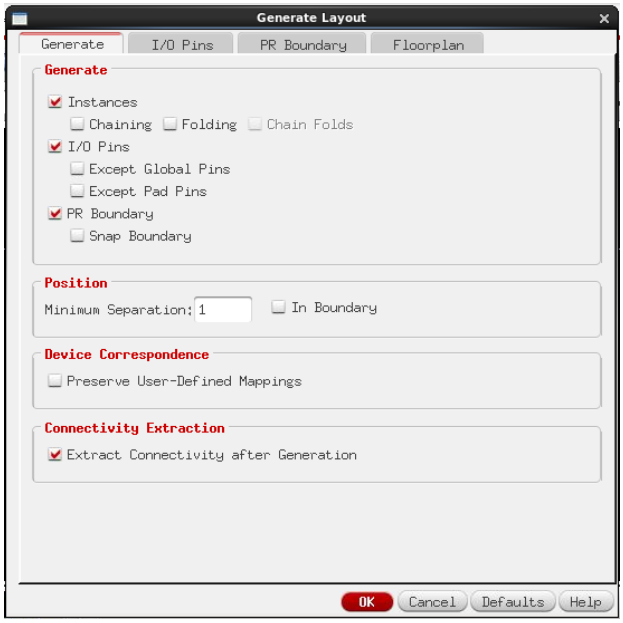


Figure 28: Generate Layout Window

The user should select the *I/O Pins* tab located on the top, and ensure that all of the pins that were established previously on the schematic are visible, this includes pins for VDD and GND, as well as Vin and Vout (though these will be dependent on what the user labeled these as). The user should then select *ok* and the layout cell views will be generated in the **Layout Design** window, as follows:

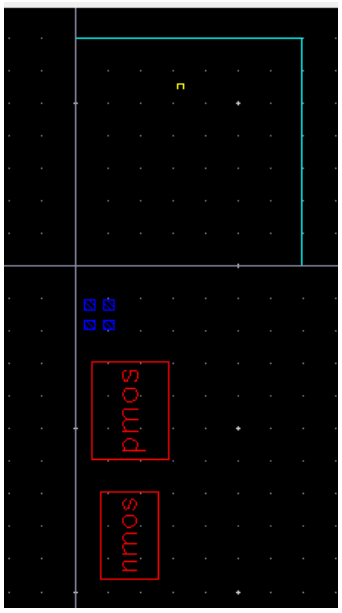


Figure 29: Layout Design Window with Layout Cells

The figure above shows the four I/O pins (in blue) as well as the nMOS and pMOS layout cells. In order for the user to see the various levels associated with the cell views, the user should select *Options*, and then *display* to bring up the **Display Options** window:

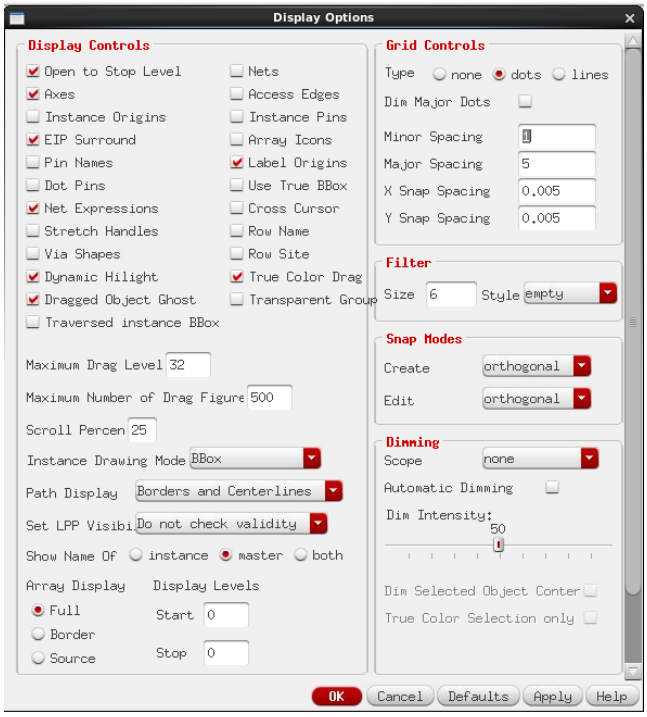


Figure 30: Display Options Window

Located at the bottom of this window under the 'display levels' heading, the user should set the *stop* textbox to 10. This will ensure that up to 10 different layers are shown, allowing the user to verify proper

connection when routing layout traces. When this is set, the user should select *ok* to return to the previous view, which should now include the following levels of detail:

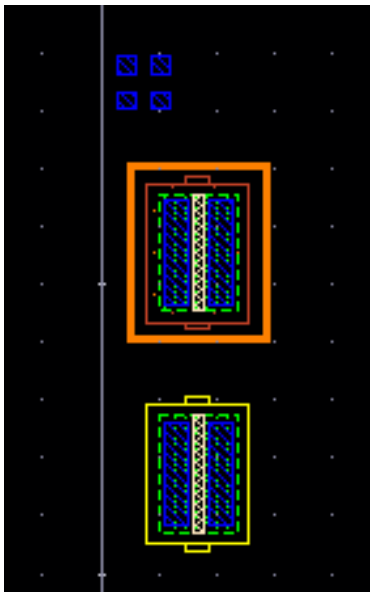


Figure 31: Layout with multiple Levels shown

This figure shows the various layers of the cell layout. The user can verify these different layers using the 'Layers' toolbox located on the left-hand side of the design window:

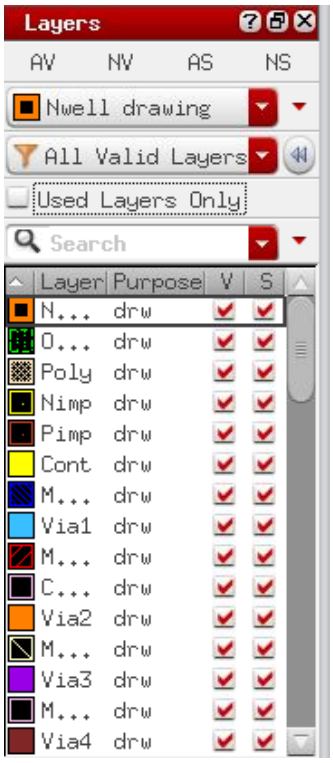


Figure 32: Layers toolbox

The user can now begin the layout process of routing proper traces. To begin, the user should erase the PR boundary box on the screen, this is the small box at the top. The author has highlighted this box in purple in the following figure:

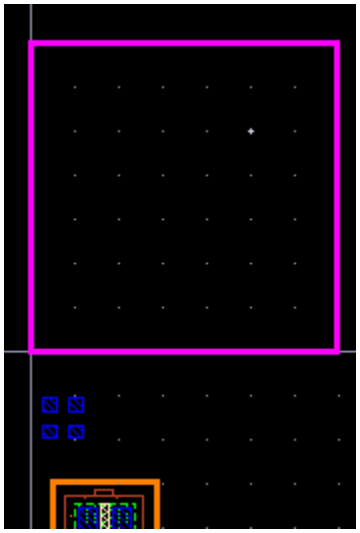


Figure 33: PR Boundary Box Highlight

When this box has been deleted, the user can now position the remaining six devices in the following layout configuration:

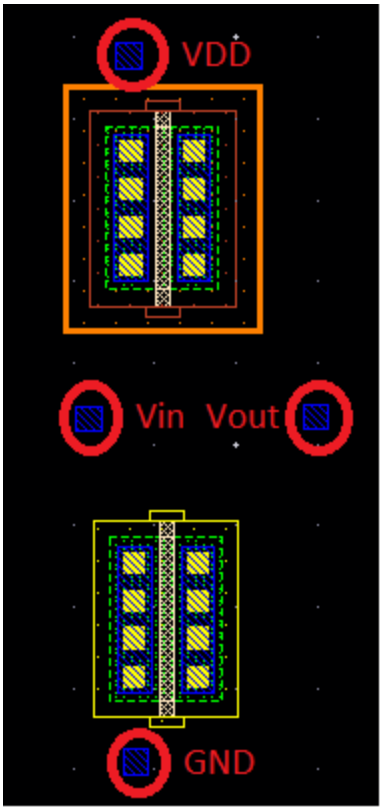


Figure 34: Positioned Layout Cells

The user can verify the pins by *right-clicking* each one and clicking *q* to bring up the **properties** window to verify these pin names. With these devices in place, the user should now select *Create*, then *Via* to bring up the **Create Via** window:

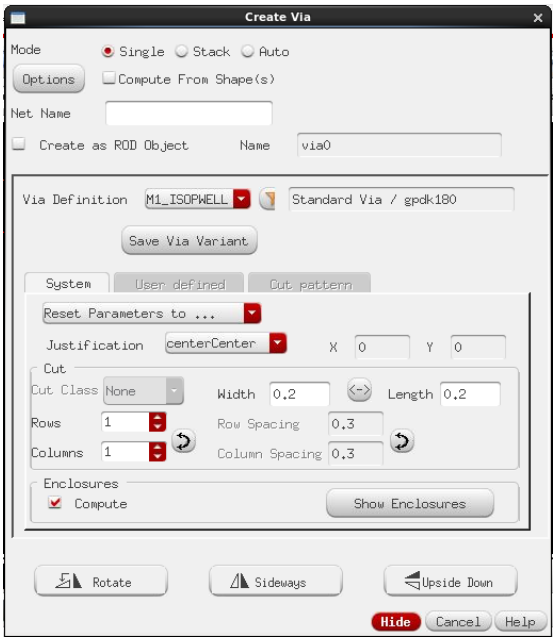


Figure 35: Create Via Window

The user should set the *Via Definition* Window to *M1_POLY1*. The user can now select the *Hide* option if desired; however in the design window the user should now see the following device on the screen:

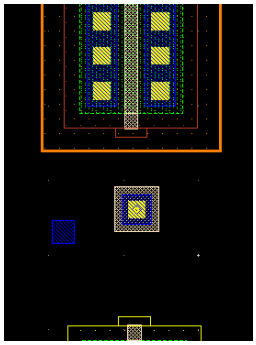


Figure 36: M1_POLY1 Via

This device is a Via. Similar to Printed Circuit Board Vias, it allows traces to run between multiple layers of the Integrated Circuit and is useful for interconnects (for example between Polysilicon and Metal Layer 1). The user should place two of these in the following locations:

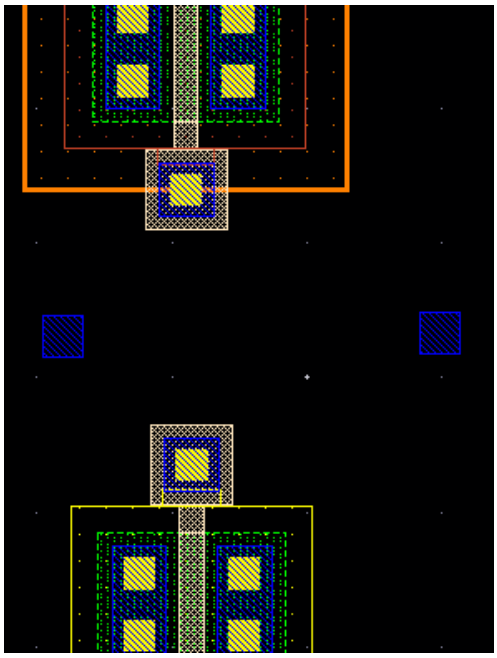


Figure 37: Placed Vias

The user should now align the nMOS and pMOS cells together based on these vias, such that they are in alignment, directly over one another. This will ensure that no design rule checks are broken later on. Likewise, this is also an opportunity for the user to condense the space between nmos and pmos cells – something that would traditionally be done in a modern process.

When these devices are aligned, the layout should look as follows:

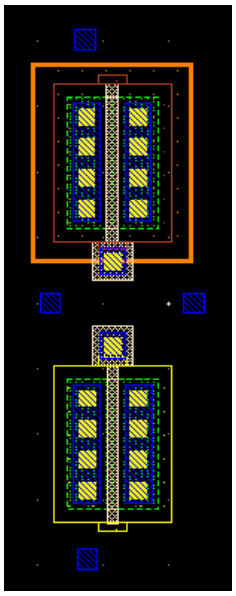


Figure 38: Condensed CMOS Layout

The last step to be completed is the bodydie attachment for the nMOS and pMOS cells. To complete this step, the user should select the *pMOS cell*, *right click*, and select *properties*, bringing up the **Edit Instance Properties** Window:

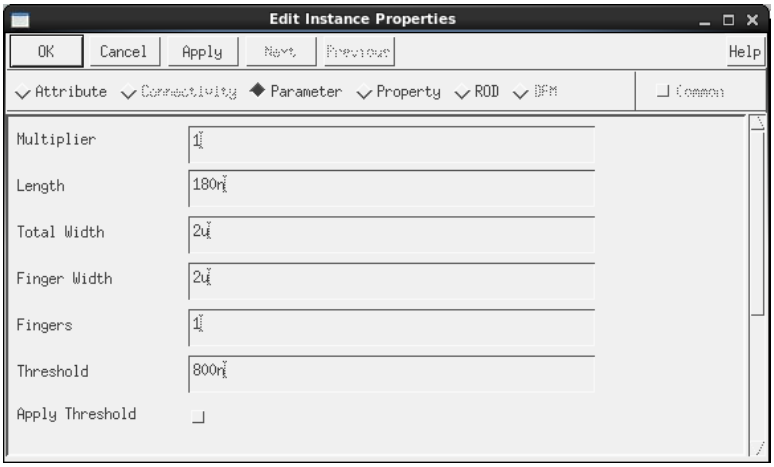


Figure 39: Edit Instance Properties Window

The user should select the *parameter* option, scroll down, and under the dropdown for Bodydie type, select the *Integrated* option. The user should repeat this for the nMOS cell as well. This will extend out the left-hand branch of the cell, and allows the user to make contact to the inputs/outputs. The user should now see the following on the design window:

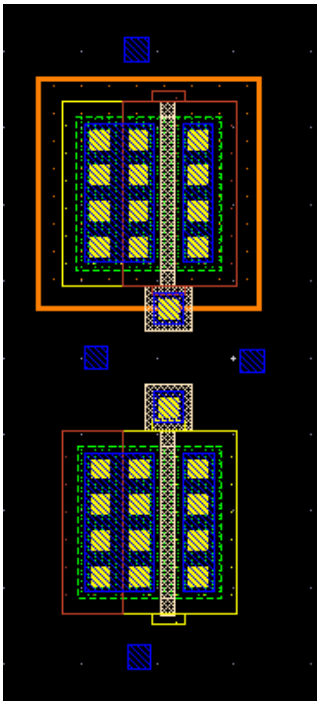


Figure 40: Cells with Bodydie attachment

With this layout, the user can begin routing traces between portions of the cell. To begin this process, the user should ensure that they have selected the *Metal1* option from the **Layers** window. The user should then select the *create wire* option:

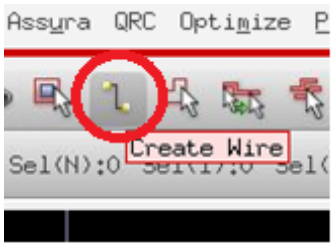


Figure 41: Create Wire Option

The user should now connect the Metal 1 layers together. To aid the user in this process, the author has shown this process graphically with the figures below

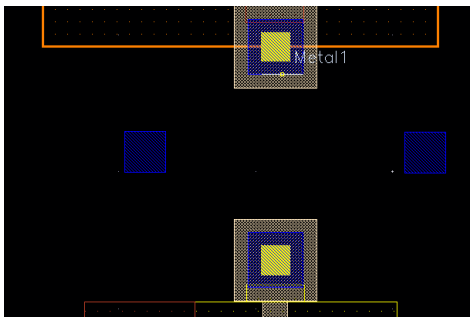


Figure 42: Begin Metal1 Connection between Vias

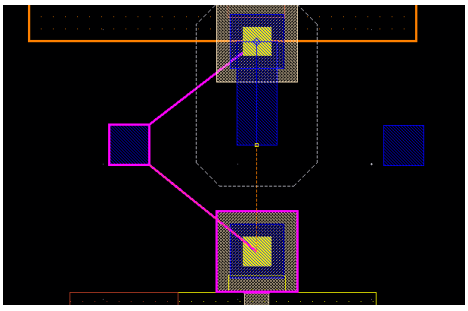


Figure 43: Continue Metal1 Connection between Vias

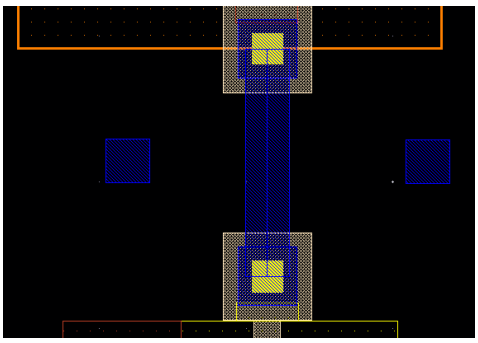


Figure 44: Finish Metal1 Connection between Vias

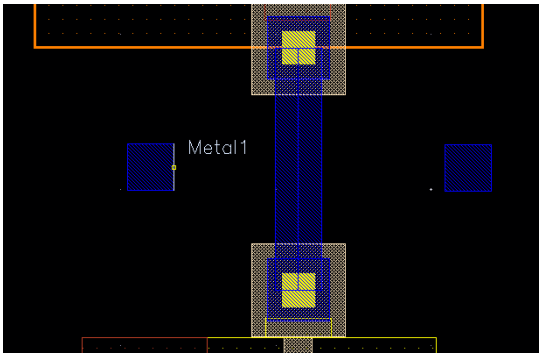


Figure 45: Vin begin connection to Metal1 Between Vias

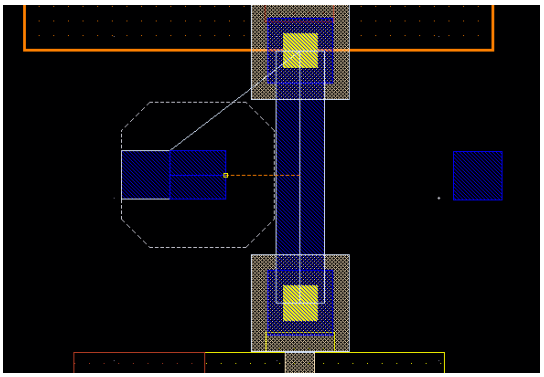


Figure 46: Vin continue connection to Metal1 Between Vias

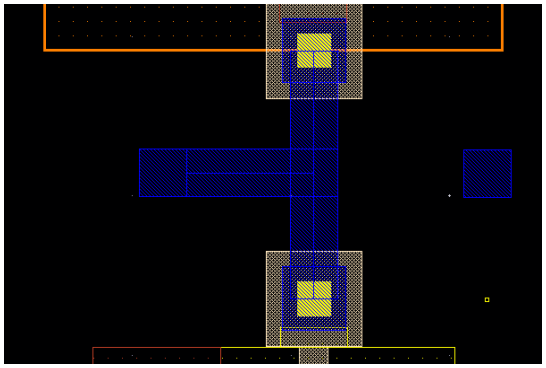


Figure 47: Vin finish connection to Metal1 Between Vias

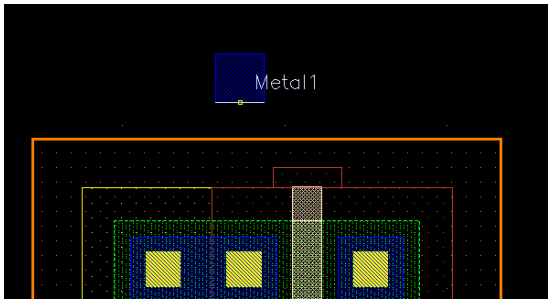


Figure 48: vdd Begin Metal1 Connectin to pMOS

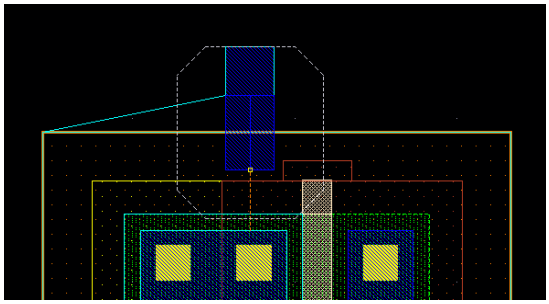


Figure 49: vdd continue Metal1 connection to pMOS

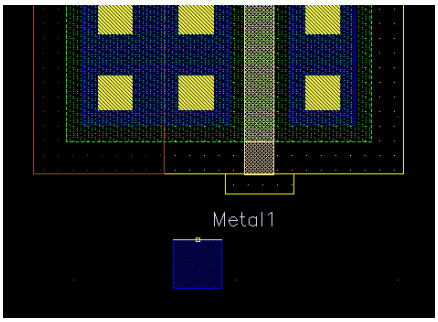


Figure 50: gnd begin Metal1 connection to nMOS

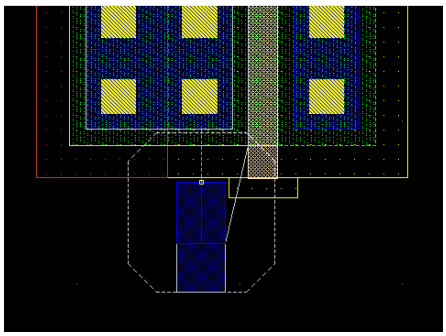


Figure 51: gnd continue Metal1 connection to nMOS

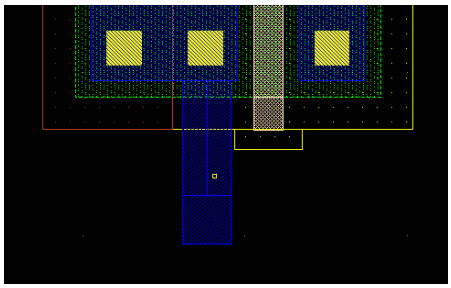


Figure 52: gnd finish Metal1 connection to nMOS

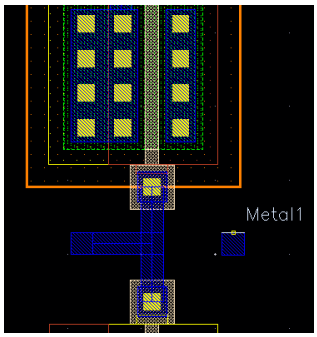


Figure 53: Vout begin Metal1 connection to pMOS

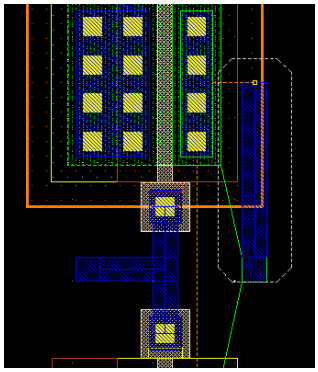


Figure 54: Vout continue Metal1 connection to pMOS

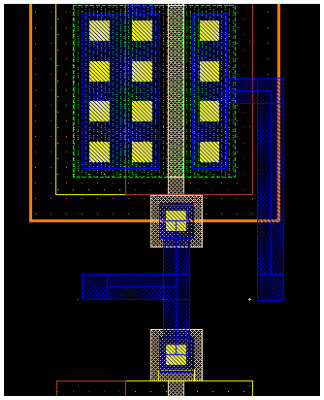


Figure 55: Vout finish Metal1 connection to pMOS

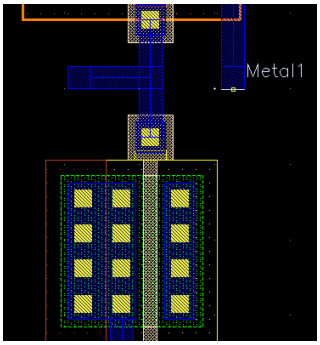


Figure 56: Vout begin Metal1 connection to nMOS

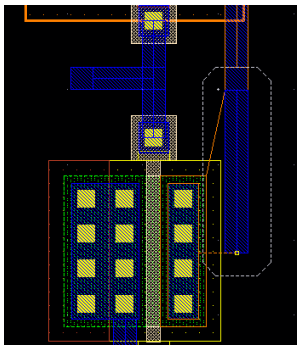


Figure 57: Vout continue Metal1 connection to nMOS

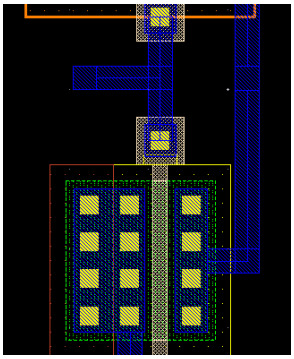


Figure 58: Vout finish Metal1 connection to nMOS

Once these steps have been completed, the user should see the following finalized layout:

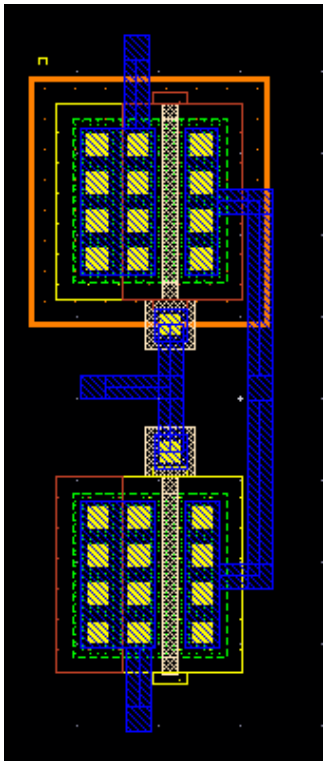


Figure 59: Finished Layout Design

With this layout complete, the user is required to run a Design Rule Check to ensure that this design has met layout requirements as per those specified in the library rules file. To do this, the user should select *Verify* then *DRC* to bring up the **DRC** Window

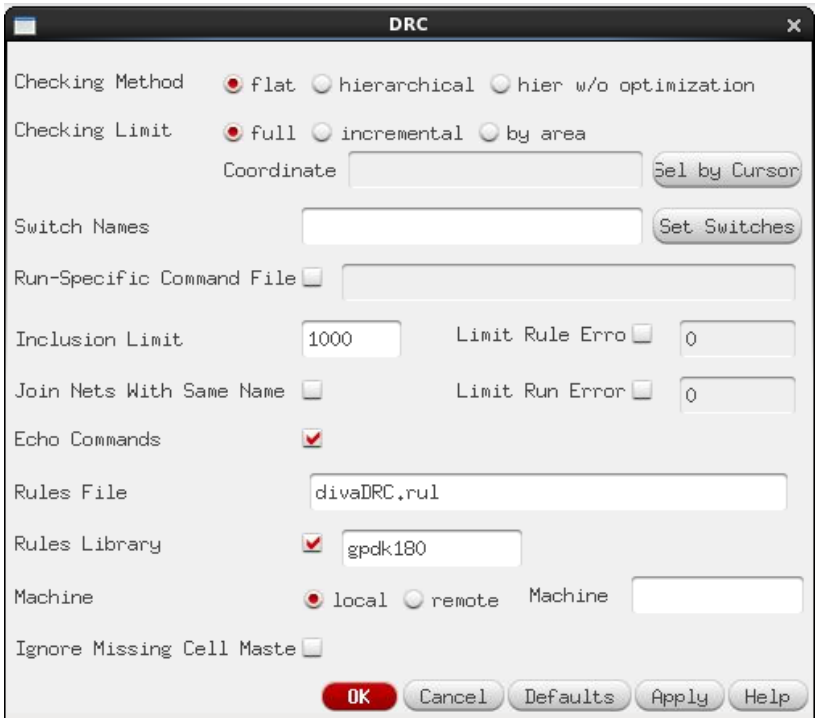


Figure 60: DRC Window

The user should then select *ok* to run a DRC.

Every user may have a different type of error associated with their layout. While not all possible errors can be covered in this tutorial, the user is advised to consult the cadence log window to ensure that all errors are accounted for. In this example, the author was given no errors when running DRC, showing no errors with the design.

However, in the event that errors did exist within the design, the following highlighted areas would be shown on the layout itself, similar to the figure below:

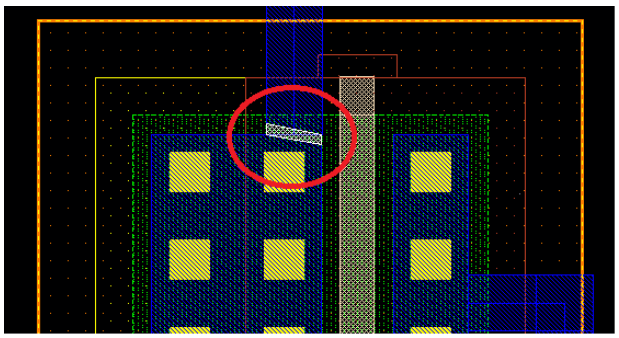


Figure 61: DRC Error in Layout Design

Likewise, an error message would be generated on the **Cadence Log** window, similar to the figure below:

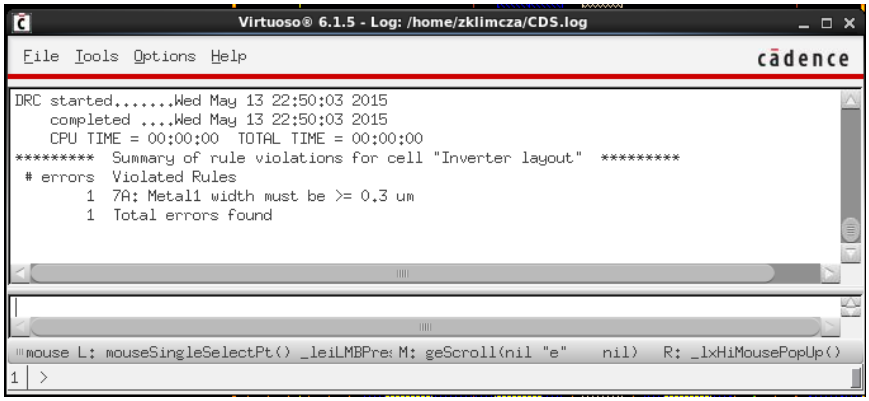


Figure 62: Cadence Error Log showing DRC Error

Conclusion

We hope that this tutorial has been enlightening and helpful in your progression with the Cadence Design Environment. While Cadence Virtuoso can be a complex tool, its use is prevalent in a number of Semiconductor Design Centers, and being able to utilize it to its fullest capabilities will enhance the skillset of any practicing Engineer or Engineering Student.

If you have any questions in regards to this tutorial, please contact its author Zach Klimczak at Zach.Klimczak@gmail.com for additional information or help.