# **Cadence Virtuoso Tutorial**

version 6.1

## **University of Southern California**

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## System Setup

#### **Basic setup**

Cadence can only run on the unix machines at USC (e.g., viterbi-scf1). You will need to remote login (XTerm) to these machines to run the tools.

- If you're using Windows, download X-Win32 2012 (for remote login) and Filezilla (for file transfer) from <u>http://software.usc.edu</u> (usc account login required)
- If you're using MAC or Ubuntu, use terminal command "ssh -X" for remote login and "scp" or "sftp" for file transfer. If you're not familiar, please read this tutorial for more information: <u>http://www.linuxtutorialblog.com/post/ssh-and-scp-howto-tips-tricks</u>

If you have any license issues when you run X-Win32, you can either try to connect to USC Wireless Plus (how-to link: <u>http://www.usc.edu/its/wireless/plus/</u>) or use USC VPN (how-to link: <u>http://www.usc.edu/its/vpn/anyconnect.html</u>).

#### a) X-Win32 Connection Setup

To remote login using X-Win32, select Manual and choose ssh:

. [	X-Win32 2012 Configuration	
N	🖓 Connections 📑 Window 🚇 Network 🔌 Input	Font 📢
Please so Conne	ISD CP	New Connection         Manual         Wizard         Edit         Remove         Shortcut         Passwords         Add Folder
	Next Cancel	Launch
	Other  Display On Startup  Exit when all connections have dosed	Defaults
	OK Cancel A	pply Help

Connection Name: (anything you like) Host: viterbi-scf1.usc.edu Login: (your my.usc.edu account name) Command: /usr/bin/xterm Password: (your my.usc.edu account password)

🔊 Edit Conr	ection (ssh)	- X-Config
General	Advanced	
Connection	Name:	viterbi-scf1
Host:		viterbi-scf1.usc.edu
Login:		siyuyue
		/usr/bin/xterm
Command:		
Password:		•••••
Confirm Pa	ssword:	•••••
Share F	Password	
Show Status		
Save		Test Cancel Help

Save your connection. Launch it:

X-Win32 2012 Configuration	
🖓 Connections 🏾 🖓 Window 🖉 Network 🦃 Input	Font 🛃
<ul> <li>My Connections         <ul> <li>Autostart</li> <li>Stripping</li> <li>aludra</li> <li>viterbi-scf1</li> </ul> </li> <li>Shared Sessions</li> </ul>	New Connection Manual Wizard Edit Remove Shortcut Passwords Add Folder Launch
Other	Defaults
OK Cancel Ap	ply Help

If you see the xterm window like below, congratulations your X-Win32 is all setup.



#### b) Filezilla Connection Setup

Open Filezilla, use **viterbi-scf1.usc.edu** as host and **22** as Port. The username and password are the same as your X-Win32 connection.

FileZilla				1	-		×
File Edit View Tran	isfer Server Bookmarks H	elp					
	2 😫 🖗 🏜 🌸 🛷 🔳	R & n					
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							-
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	PHED106						
	12-Spring Tesh						
😨 🍒 Resea	rch	=					
	rchDizhu						
	n Volume Information						
Filename	Filesize Filetype	Last modified	Filename	Filesize Filetype	Last modified	Permissions	0
📕 ]] examples	File folder	8/29/2012 14:55:28					
.cshrc	1,147 CSHRC File	8/29/2012 13:29:24		Not connected t	o any server		
201203_EE577b	104,235 Microsoft Wor						
examples.tar	40,448 WinRAR ????	8/29/2012 11:09:02					
			•	m			ŀ
3 files and 1 directory. To	tal size: 145,830 bytes		Not connected				
Server/Local file	Direction Remote f	ile	Size Prio	rity Status			
Oueued files Failed to	ransfers Successful transfers						_
Queded mes Praied o						1.	
					🚥 Queue:	empty •	

Navigate and choose files from the left window to upload and files from the right window to download.

5 sftp://siyuyue@viterb	si-scf1.usc.edu - FileZilla			-					×
File Edit View Tran	sfer Server Bookmarks	Help							
1 - 1000	🛃 😆 🕼 🔁 🗽 🛷 🗄	E 🕂 👎 🗥							
Status: Calcula Command: mtime Response: 13462 Status: Timezo	accd to viterbi-scf1.usc.edu ating timezone offset of server. "cds"					kconnect			( III )
Local site: C:\Users\Siyu	Yue\Documents\		•	Remote site: /ho	me/scf-03/siy	uyue			
<ul> <li>Desktop</li> <li>My Documents</li> <li>Skecycle.Bin</li> <li>Config.Msi</li> <li>Documents and Settings</li> </ul>									
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1 file and 8 directories. To	otal size: 402 bytes			27 files and 19 di	rectories. Tot	tal size: 197,30	i2 bytes		
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			_				🔒 🎰 Queue: e	empty 🔍	٠

#### **Cadence setup**

Before you start, familiarize yourself with the following linux commands:

ls	// List files	
pwd	// Show your current directory	
cd	<pre>// Navigate to some directory</pre>	
mv	// Move	
ср	// Сору	
rm	// Remove	
mkdir	// Create a directory	

You can find 'cshrc\_linux' ,tsmc.spice and 'vlsi\_tools.csh' from http://bits.usc.edu/ee209/ site. Note that the file entitled 'cshrc\_linux' should be renamed to 'cshrc' after uploading it in your home directory.

Download *.cshrc, tsmc.spice* and *vlsi\_tools.csh* from http://bits.usc.edu/ee209/ under Lab Tutorial. Use Filezilla (or scp) to upload these files to your home folder on viterbi-scf1. Make sure they are named .cshrc or vlsi\_tools.csh exactly.

Type command "Is –a" to list all files under your home directory:

Google them for more information about their usage if needed.

ls -a



If you need to rename those files to .cshrc or vlsi\_tools.csh, use command "mv", for example, to rename cshrc to .cshrc, you can say:

#### mv cshrc .cshrc

Convert the encoding of those two files by dos2unix command:

#### dos2unix .cshrc

#### dos2unix vlsi\_tools.csh

Create a folder named cds:

#### mkdir cds

Copy useful files to your cds directory:

#### cp ~ee577/design\_pdk/tsmc25/files/\* ./cds/

```
cp ~ee577/design_pdk/tsmc25/files/.cds* ./cds/
```

Check you have the following files in the cds folder:

Is -a ./cds/

.cdsinit // cadence initialized file

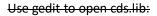
.cdsplotinit cds.lib schBindKeys.il tsmc25.spice leBindKeys.il // cadence printing setup file

- // cadence library setup file
- // Binding key files for shortcut keys
- // TSMC 25 spice parameters
- // Binding key files for shortcut keys

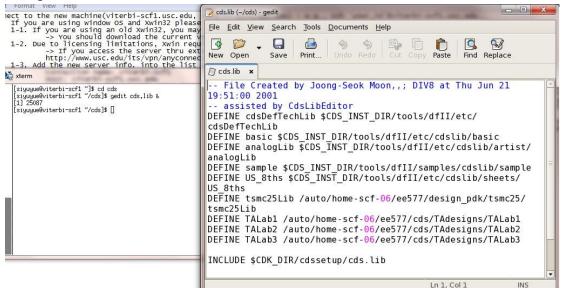
This step is no more necessary

Now go to the cds folder:

cd cds



#### gedit cds.lib



Add the following line to it; do not remove any existing content:

INCLUDE \$CDK\_DIR/cdssetup/cds.lib Go back to your home directory:

cd ..

Copy the cadence environment files to your cds working directory:

#### cp ~ee577/design\_pdk/ncsu-cdk-1.6.0.beta/cdssetup/cdsinit ./cds/.cdsinit

Copy the .simrc file to your cds directory:

cp ~ee577/design\_pdk/ncsu-cdk-1.6.0.beta/cdssetup/simrc ./cds/.simrc Then you can source .cshrc file:

#### source .cshrc

If nothing comes out, then you're successful:



Please remember that you need to source .cshrc every time you login before running virtuoso. You don't need to repeat other steps though.

To run virtuoso, now go to cds directory: (always run virtuoso in the cds directory)

#### cd cds

And open virtuoso: (by adding  $\pmb{\&}$  you can use virtuoso and xterm and the same time)

#### virtuoso &

	Si Library Manager: WorkArea: /home/scf-03/siyuyue/cds				
	Elle <u>E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp				
🔀 xterm	Show Categories Show Files	View			
[siyuudeViterbi=scf1 "]\$ source .cshrc [siyuudeViterbi=scf1 "]\$ od ds [siyuudeViterbi=scf1 "/cds]\$ virtuoso & [1] 24741 [siyuudeViterbi=scf1 "/cds]\$ []	NCSU_Analog_Parts       NCSU_Digital_Parts       NCSU_Tech.lb_ami06       NCSU_Tech.lb_nmi06       NCSU_Tech.lb_tsmc02       NCSU_Tech.lb_tsmc02d       NCSU_Tech.lb_tsmc03d       NCSU_Tech.lb_tsmc04_4M2P       US_6ths       analogl.lb       basic       cdsDerfech.Lib       demoe       lab       sample				
	Messages           Warning: The directory: '/auto/nome-scf-06/ee577/cds/TA/designs/TA/Lab3' does not exist but was defined in libFile '/home/scf-03/siyuyue/cds/cds/lb' for Lib 'TA/Lab3'.           Warning: The directory: '/auto/nome-scf-06/ee577/cds/TA/designs/TA/Lab2' does not exist but was defined in libFile '/home/scf-03/siyuyue/cds/cds lib' for Lib 'TA/Lab2'.           Warning: The directory: '/auto/nome-scf-06/ee577/cds/TA/designs/TA/Lab1' does not exist but was defined in libFile '/home/scf-03/siyuyue/cds/cds lib' for Lib 'TA/Lab2'.           Warning: The directory: '/auto/nome-scf-06/ee577/dssign_pdk/smc25fsmc25Lib' does not exist but was defined in libFile '/home/scf-03/siyuyue/cds/cds.lib' for Lib 'tsmc25Lib'.	st			
Г	ARNING* The directory: '/auto/home-scf-06/ee577/design_pdk/tsmc25/tsmc25Lib' but was defined in libFile '/home/scf-03/siyuyue/cds/cds.lib' for Li aloading MCSU_CDK_customizations. ading rte.cxt nouseL: M: >				

Make sure you can see those NCSU\_XX libraries and then you're all set!

.cdsplotinit	// cadence printing setup file
cds.lib	// cadence library setup file
schBindKeys.il	// Binding key files for shortcut keys
tsmc25.spice	// TSMC 25 spice parameters
leBindKeys.il	// Binding key files for shortcut keys

A. Make sure you can run cadence tool by typing.

#### % which virtuoso /usr/usc/cadence/2009/IC610/tools/dfII/bin/virtuoso

B. Go to your home directory, open your .cshrc file and add the following lines at the end of this file:

setenv CDK\_DIR /home/scf-06/ee577/design\_pdk/ncsu-cdk-1.6.0.beta setenv CDS\_Netlisting\_Mode Analog

- C. Close the .cshrc file and source this file by typing the following command:% source .cshrc
- D. Open the library file cds.lib which is located in your cds directory. Just add the following line to cds.lib. Do not remove existing contents in cds.lib:

#### INCLUDE \$CDK\_DIR/cdssetup/cds.lib

E. Go to your home directory. Copy the cadence environment files to your cds working directory by typing the following command while you are in your home directory:

%cp ~ee577/design\_pdk/ncsu-cdk-1.6.0.beta/cdssetup/cdsinit ./cds/.cdsinit

F. Stay at your home directory. Copy the .simrc file in your cds directory by typing the following command while you are in your home directory:

% cp ~ee577/design\_pdk/ncsu-cdk-1.6.0.beta/cdssetup/simrc ./cds/.simrc

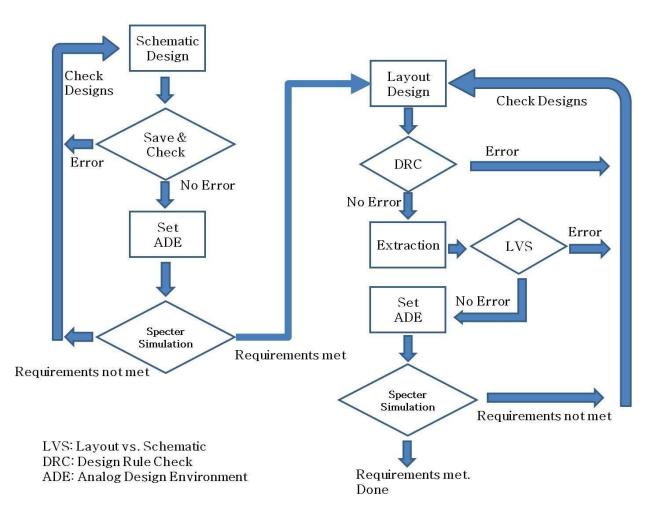
Note that the name of the file that you are accessing is "cdsinit" but you need to save it as ".cdsinit". Also note that you may already have a ".cdsinit" file from the past in your cds directory. In this case you still need to overwrite it by this new file.

G. Always invoke "virtuoso" in your ~/cds directory because all setup files are in this directory. Type virtuoso & at the command prompt. The "&" is for background execution, it is useful when we want to keep the command prompt in the same console.

## **Basic Design Flow**

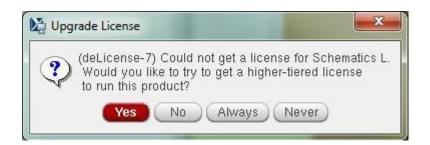
#### 1. Overall design flow

Following flow chart shows overall design flow.



#### 2. Create Library

For prompt to access for higher tiered license, click "always".



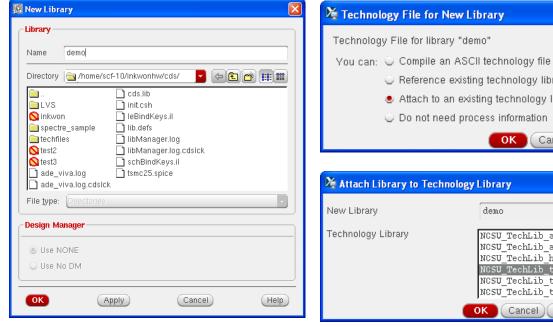
A. Tools  $\rightarrow$  Library Manager



B. File  $\rightarrow$  New  $\rightarrow$  Library

🐺 Library Manager: WorkArea: /home/scf-10/inkwoi	nhw/cds	
<u>File E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
New     Image: Library       Open     Ctrl+O       Open (Bead-Only)     Ctrl+R       Image: Local Defaults     Category       Save Defaults     Open Shell Window       Open Shell Window     Ctrl+R       NCSU_TechLib_tsmc03d     NCSU_TechLib_tsmc04_4M2P       analogLib     basic       cdbefferChLib     TortechLib_tsmc04	Cell O0_Complete_Index_00 Current_Sources_Index Diodes_Index H.Spice_Only_Index MOS_a2a MOS_d2a MCrowave_Parts_Index N_Transistors_Index Parasitic_Devices_Index Parasitic_Dev	- View
Messages Log file is "/home/scf-10/inkwonhw/cds/libManager.log".	1001	

C. Give a name and attach it to a technology library



	0,					
Reference existing technology libraries						
<ul> <li>Attach to ar</li> </ul>	<ul> <li>Attach to an existing technology library</li> </ul>					
Do not need process information						
OK Cancel Help						
🧏 Attach Library to Techno	ology Library 🛛 🔀					
New Library	demo					
Technology Library	NCSU_TechLib_ami06 NCSU_TechLib_ami16 NCSU_TechLib_hp06 NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d NCSU_TechLib_tsmc03					
OK Cancel Apply Help						

×

## 3. Schematic

## A. Create a cell view

select the library just created, File->new

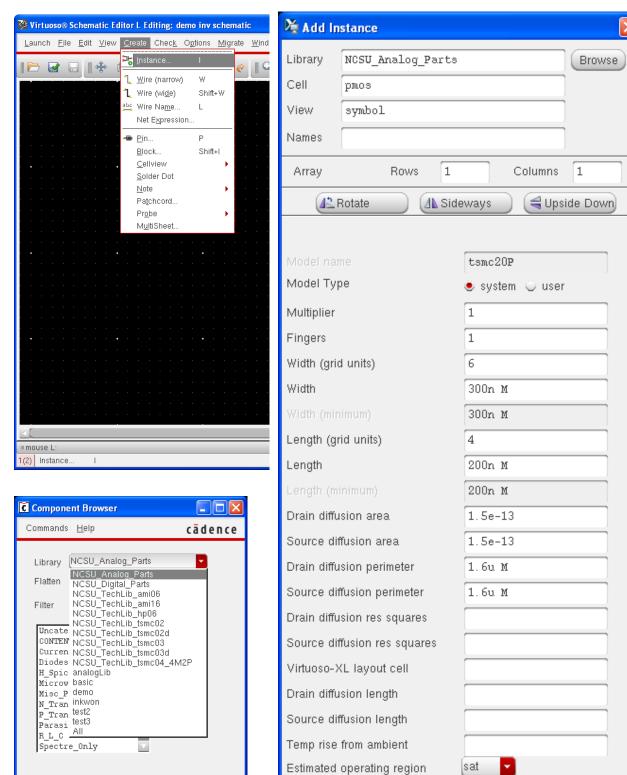
疑 Library Manager: WorkArea: /home/scf-10/inkwonhw	w/c ds	New File	
<u>File E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		-	
New Library	Cell	Library path file	demo
New Cell View			

B Library Manager: WorkArea: /home/scf-10/inkwor	ihw/c ds	
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demo	inv	schematic
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Messages		
Log file is "/home/scf-10/inkwonhw/cds/libManager.log". Created new library "demo" at /home/scf-10/inkwonhw/c DB was auto refreshed.		( III ) X

#### B. Draw a schematic

i. Add instances – pmos

You can modify Width of transistors. Don't modify length unless you have a special purpose. You should select a NCSU\_Analog\_Parts library.



(Hide)

Cancel ) Defa

Defaults (Help

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## ii. Add instances – nmos, vdd, and gnd

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We have for different types of direction. For schematics, we only use two types, input and output. InputOutput type is for supply changes, and it is necessary only for layout. We will discuss about this later.

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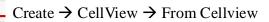
Check and save  $\rightarrow$  is to make sure there are no errors.

Now, we completed a schematic design.

## C. Create a symbol (Optional)

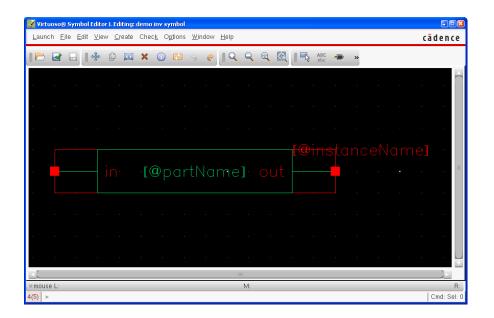
For hierarchical design, we may need to make symbols of designed circuits.

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Remember that when you use more than one symbol in schematic, they all will have common Vdd and Gnd even if there are one Gnd and Vdd for each symbol (in the original design). To design with symbols in layout, you should make sure that all of the Vdd and Gnds are connected.

### 4. Run Spectre simulation (Transient analysis)

We will run spectre simulation. This section is for **both** schematics and layouts. I will show an example for a schematic. You can do the same thing for a layout.

## A. Launch ADE (Analog Design Environment) L

#### Launch $\rightarrow$ ADE L

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#### B. Basic setup

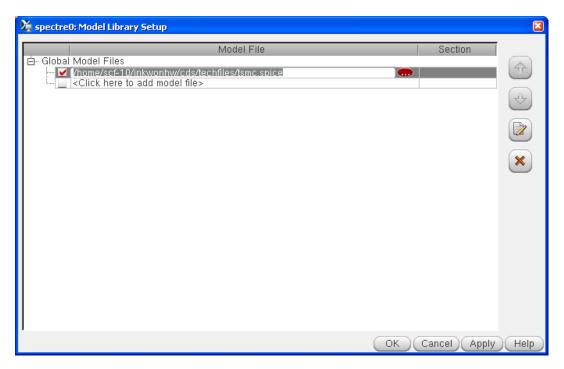
Check if your simulator is spectre. You can modify project directory.

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## C. Model Libraries

You can download a library file at the DEN blackboard. Put the tech file under /home/scf-10/your-user-name/cds/techfiles/

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Please only use the provided tsmc file because some tsmc files does not work correctly.

### D. Stimuli

Define input signals include supply nets (for layout, vdd! and gnd! are under inputs and both should be enabled.)

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#### Global sources

#### Input (change)

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DC voltage	1.5	DC voltage	
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AC phase		AC phase	
XF magnitude		XF magnitude	
PAC magnitude		PAC magnitude	
PAC phase		PAC phase	
Temperature coefficient 1		Voltage 1	0
Temperature coefficient 2		Voltage 2	1.5
Nominal temperature		Period	2n
Source type	dc	Delay time	0
Noise file name		Rise time	200p
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Noise 1		Temperature coefficient 1	
Freq 2		Temperature coefficient 2	
Noise 2		Nominal temperature	
Eron 3		Source tune	
	OK Cancel Apply (		OK Cancel Apply

Remember to check Enabled button and then press OK or APPLY otherwise you will lose the configured numbers.

#### E. Choose a type of analysis - transient

You can choose "dc" if you want to do dc analysis

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Analysis

#### A. Choose tran

- B. Give Stop time which means how long you want to simulate
- C. Select moderate as accuracy defaults
- D. Do not check Transient Noise

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Enabled ⊻	Options
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🎽 Choosing Analyses --- Virtuoso® Analog Design Environment (1)

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🛈 pss

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🛈 qpxf 🛈 qpsp

×

E. Check Enabled

#### F. Select signals to plot

Outputs  $\rightarrow$  To Be Plotted  $\rightarrow$  Select On Schematic

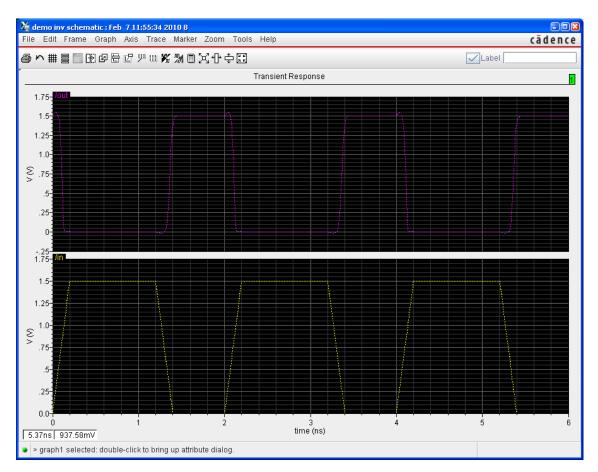
Click a signal (Pin) on a schematic/extracted. In Extracted try to use pins for signal that you need in the simulation because it is hard to select a net in the extracted view.

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<ul> <li>Plotting mode:</li> <li>Results in/scf-10/inkwonhw/cadence/simulation/inv/sg</li> <li>Select On Schematic</li> </ul>	Replace

## G. Run simulation

Simulation  $\rightarrow$  Run

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If you see a waveform like above picture, you followed every step properly. Good job!.

#### H. Measurement

The following steps describe the measurement of rise time. Using similar steps other parameters of delay, fall time can be estimated.

Invoke the calculator  $\square$  or tools-> calculator , select the Wave radio button:

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🚟 Virtuoso (R) Visualization & A	nalysis L Calc	ulator			
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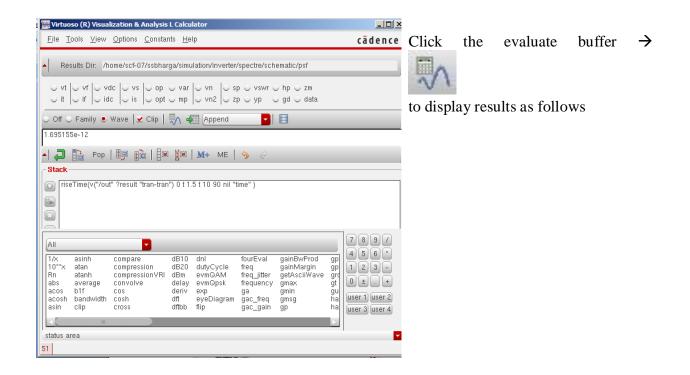
In the functions window – choose "all"

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⊖ vt ⊖ it	○ vf         ○ vdc         ○ vs         ○ op         ○ var         ○ vn         ○ sp         ○ vswr         ○ hp         ○ zm           ○ if         ○ idc         ○ is         ○ opt         ○ mp         ○ vn2         ○ zp         ○ yp         ○ gd         ○ data	
Off (	🔾 Family 🖲 Wave 🛛 🗹 Clip   🏹 🐗 Append 🔽 📘	
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	Signal	
li li	nitial Value Type (y at×	
	Initial Value 0	
	Final Value Type (y at x	<b>•</b>
	(Ok) (Apply) (Defaults) (Quit)	

Select the rise time option

Elle Tools View Options Constants Help         Results Dir:       /home/scf-10/hsunweih/cadence/simulation/inv/spectre/schematic/psf         Vt       vf       vdc       vs       op       var       vn       sp       vswr       hp       zm         it       vf       idc       is       opt       var       vn       sp       vswr       hp       zm         Off       Family       Wave       Clip       V       V       it       it	
Ovt Ovf Ovdc Ovs Op Ovar Ovn Osp Ovswr Ohp Ozm Ott Oif Off Ovdc Ois Opt Omp Ovn2 Ozp Oyp Ogd Odata Off OFamily ● Wave V Clip   ♥ ▲ Append III ●	
it   uif   uid:   uis   uopt cimp   up 2   up cipp cipd cidata Off C Family ● Wave   ⊻ Clip   🖏 🐗 Append 🔽   📑	10000
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All rise Time	789/ 456* 123-
Signal (v("/out" ?result "tran-tran")	0±.+
Initial Value 0	user 1 user 2
Final Value Type 🖉 🗖	user 3 user 4
Final Value 1.5	
Percent Low 10	
Percent High 90	1
Ok Apply Defaults Quit	]
Expression evaluation failed: Expression evaluates to nil	-
9	

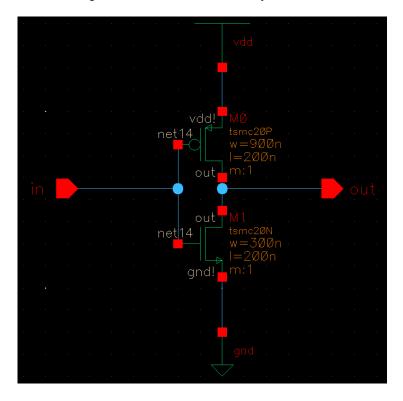
Select the signal from the waveform window whose rise time needs to be determined and click "OK":



You can also select a signal from calculator for example cos(Vin) as one of the plotted signals and you can see the results whenever you run the simulation.

Remember to save the simulation setup to use it later. You can do so by clicking on Session  $\rightarrow$  Save State in the ADE (Analog Design Environment) window. Next time you want to simulate the same cell, you can reload your configuration by clicking on Session  $\rightarrow$  Load State.

#### 5. Run Spectre simulation (DC analysis)



The following inverter schematic is already created

#### A. Voltage Source

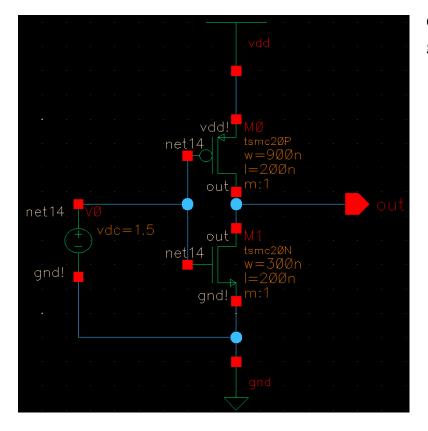
For DC analysis, the input pin "in" must be altered. The following are the steps to alter the pin "in" : Create→instance→NCSU analog parts→Voltage\_sources select Vdc

	na ana ana ana ana ana ana ana ana ana	
	M Edit Object Properties	×
	Apply To Only current 🔽 Instance 🔽	
	Show system 👱 user 👱 CDF	
• • • • • •	Browse Reset Instance Labels Display	
	Property Value	Display
	Library Name NCSU_Analog_Parts	off 🔽
	Cell Name vdc	off 🔽
het14 TVØ	View Name symbol	off 🔽
$\downarrow$ vdc=1.5	Instance Name	off 🔽
	Add Delete Modify	
	User Property Master Value Local Value	Display
.gnd! 📥	Ivsignore	off 🔽
	CDF Parameter Value	Display
	AC magnitude	off 🔽
	AC phase	off 🔽
	DC voltage 1.5 ¥	off 🔽
	Noise file name	off 🔽
	Number of noise/freq pairs 0	off 🔽
	Temperature coefficient 1	off 🔽
	Temperature coefficient 2	off 🔽
a a a a a a	Nominal temperature	off 🔽
	OK Cancel Apply Defaults Previous	Next Help

The DC voltage must be set to 1.5V as shown.

#### B. Replace Input Pin

The Input pin "in" must be replaced with the above voltage source as shown below



Check and Save (make sure you get no errors)

## C. Choosing Analyses

Launch ADE L, repeat steps A to D in section 3 of "Basic Design Flow" except that there is no "in" input signal this time.

🎽 Choosing Analyses Virtuoso® Analog Design Environment	(3)			
Analysis 🔾 tran 🖲 dc 🔾 ac 🔾 🔾 noise				
🔾 🛪 🔾 sens 🔾 domatch 🔾 stb				
⊖pz ⊖sp ⊖envlp ⊖pss				
🔾 pac 🔾 pstb 🔾 pnoise 🔾 pxf				
🔾 psp 🔾 qpss 🔾 qpac 🛛 qpnoise				
⊖ qpxf ⊖ qpsp				
DC Analysis				
Save DC Operating Point 📃				
Hysteresis Sweep				
Sweep Variable	]			
Component Name /₩0				
Design Variable     Select Component				
🖌 Component Parameter 🛛 Parameter Name 🛛 dc				
🔄 Model Parameter				
Sweep Range				
• Start-Stop Start 0 Stop 1.5				
⊖ Center-Span				
Sweep Type				
Step Size 0.01				
🔾 Number of Steps				
Add Specific Deinte				
Add Specific Points				
Enabled 🖌 Optic	ins)			
	ults Apply			

Go to Analyses  $\rightarrow$  Choose dc

Choose "Component Parameter",

Select Component, then the voltage source in the schematic, then choose 0 as Start, 1.5 as Stop and 0.01 as step .

Make sure that there are no other analyses selected apart from DC

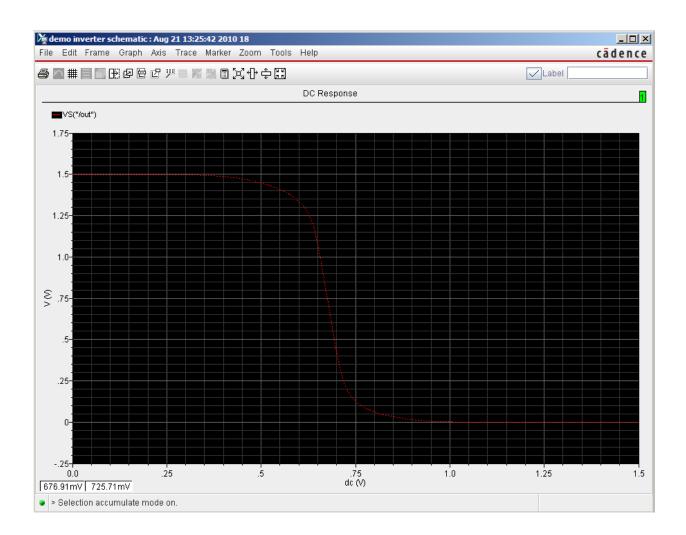
😲 Virtuoso® Analog Design Environment (3) - demo inverter schematic	<u> </u>
S <u>e</u> ssion Set <u>up</u> <u>A</u> nalyses <u>V</u> ariables <u>O</u> utputs <u>S</u> imulation <u>R</u> esults <u>T</u> ools <u>H</u> elp <b>cāde</b>	епсе
Ⅲ Status: Ready T=27 C Simulator: spectre	

#### D. Run Simulation

Do simulations  $\rightarrow$  netlist and run. On successful completion we get the following

Elle Help cadence reltol = 1e-03 abstol( $\Psi$ ) = 1 uV abstol(I) = 1 pA temp = 27 c troom = 27 c tempeffects = all gmin = 1 pS maxrsd = 0 0hm mos_method = s mos_vres = 50 mV dc: dc = 40 mV (2.67 %), step = 10 mV (667 m%) dc: dc = 120 mV (8 %), step = 10 mV (667 m%) dc: dc = 120 mV (12.7 %), step = 10 mV (667 m%) dc: dc = 270 mV (118 %), step = 10 mV (667 m%) dc: dc = 400 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 400 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 400 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 400 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 640 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 640 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 640 mV (52.7 %), step = 10 mV (667 m%) dc: dc = 640 mV (52.7 %), step = 10 mV (667 m%) dc: dc = 790 mV (52.7 %), step = 10 mV (667 m%) dc: dc = 1.02 V (68 %), step = 10 mV (667 m%) dc: dc = 1.02 V (68 %), step = 10 mV (667 m%) dc: dc = 1.17 V (78 %), step = 10 mV (667 m%) dc: dc = 1.24 V (82.7 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (32.7 %), step = 10 mV (667 m%) dc: dc = 1.32 V (32.7 %), step = 10 mV (667 m%) dc: dc = 1.32 V (32.7 %), step = 10 mV (667 m%) dc: dc = 1.32 V (32.7 %), step = 10 mV (667 m%) dc: dc = 1.32 V (32.7 %), step = 10 mV (667 m%) dc: dc = 1.32 V (32.7 %), step = 10 mV (667
abstol(V) = 1 uV abstol(I) = 1 pA temp = 27 c trom = 27 c tempeffects = all gmin = 1 pS maxrsd = 0 0hm mos_method = s mos_vres = 50 mV dc: dc = 40 mV (2.67 %), step = 10 mV (667 m%) dc: dc = 120 mV (12.7 %), step = 10 mV (667 m%) dc: dc = 270 mV (12.7 %), step = 10 mV (667 m%) dc: dc = 240 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 420 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 420 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 420 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 420 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 420 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 420 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 420 mV (22.7 %), step = 10 mV (667 m%) dc: dc = 720 mV (38 %), step = 10 mV (667 m%) dc: dc = 720 mV (58 %), step = 10 mV (667 m%) dc: dc = 700 mV (58 %), step = 10 mV (667 m%) dc: dc = 1.02 V (68 %), step = 10 mV (667 m%) dc: dc = 1.02 V (68 %), step = 10 mV (667 m%) dc: dc = 1.02 V (68 %), step = 10 mV (667 m%) dc: dc = 1.22 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.47 V (92.7 %), step = 10 mV (667 m%) dc: dc = 1.32 V (88 %), step = 10 mV (667 m%) dc: dc = 1.47 V (98 %), step = 10 mV (667 m%) dc: dc = 1.47 V (98 %), step = 10 mV (667 m%) dc: dc = 1.47 V (98 %), step = 10 mV (667 m%) dc: dc = 1.47 V me = 0 ms. Accumulated dc load time = 20 ms. Accumulated dc solve time = 10 ms. Total time required for dc analysis 'dc' was 50 ms. modelParameter: writing model parameter values to rawfile. element: writing instance parameter values to rawfile. element: writing instance parameter values to rawfile. element: writing nethist parameters to rawfile.
subckts: writing subcircuits to rawfile.

Now, go to the results  $\rightarrow$  Direct plot  $\rightarrow$  DC. Click on the output pin "out" on the schematic and ESC key to get the following VTC



#### 6. Layout

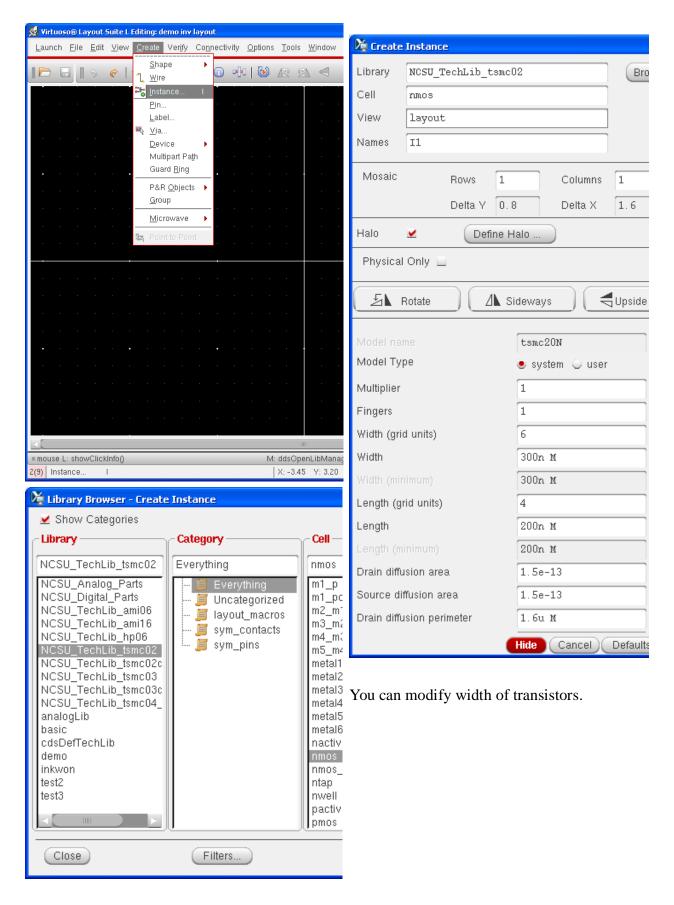
It's time to draw layout. Schematics are for verifying your design very roughly. They don't consider physical features like parasitic capacitances. After determining your design variables by schematics, you need to draw layouts.

Design flow of layouts is very similar to one of schematics, but it has additional step which is LVS check. It is for check if your layout is identical to the schematic or not. Hence, this step is very important. If your logic doesn't pass this step, you may lose significant points for that.

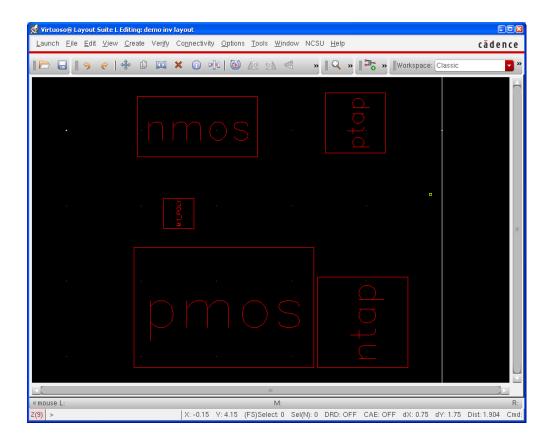
### A. Create a layout

😹 Library Manager: WorkArea: /home/scf-10/inkwor	nhw/cds	D	🍹 New File		
<u>File Edit View D</u> esign Manager <u>H</u> elp		ſ	- File		
New			Library	demo 🧧	
Open     Ctrl+O     Cell View     Open (Read-Only)     Ctrl+R     Category	Cell		Cell	inv	
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			Library path file	schematicSymbol	
Messages	~		/home/scf-10/in	text Veriloq	Ь
Log file is "/home/scf-10/inkwonhw/cds/libManager.log".				VerilogA	
Created new library "demo" at /home/scf-10/inkwonhw/c DB was auto refreshed.	ds/demo.			VerilogAMSText	
				vhdl VHDLAMSText	
	100				lel)(Help)
New Cell View					

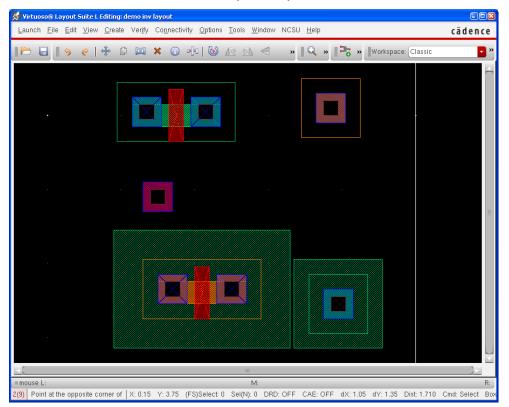
#### **B.** Add an instance - nmos



## C. Add more instances – pmos, ptap, ntap, and m1\_ploy



You can select alternate view of a layout. Try "Shift + f" and "Ctrl + f".

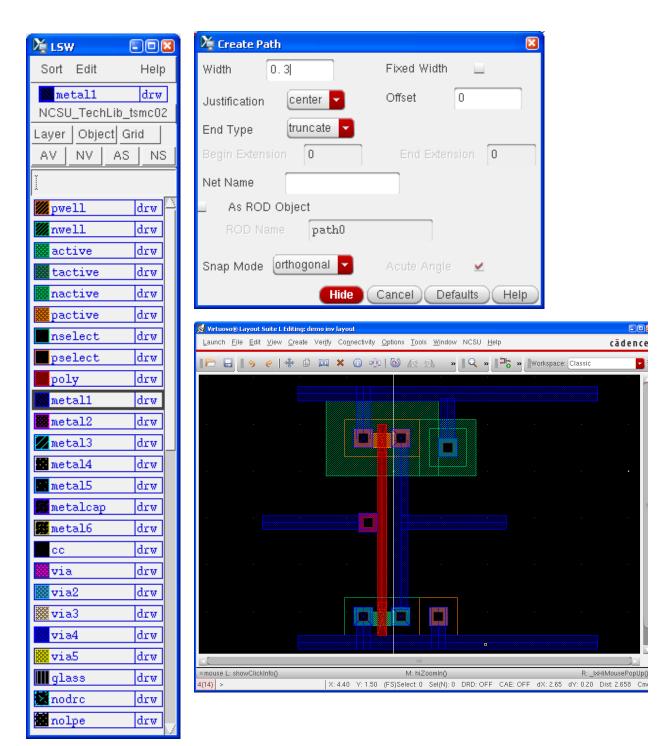


#### D. Draw metal1

There are few ways for drawing metal, but I recommend you use "path". It"s quite convenience than others.

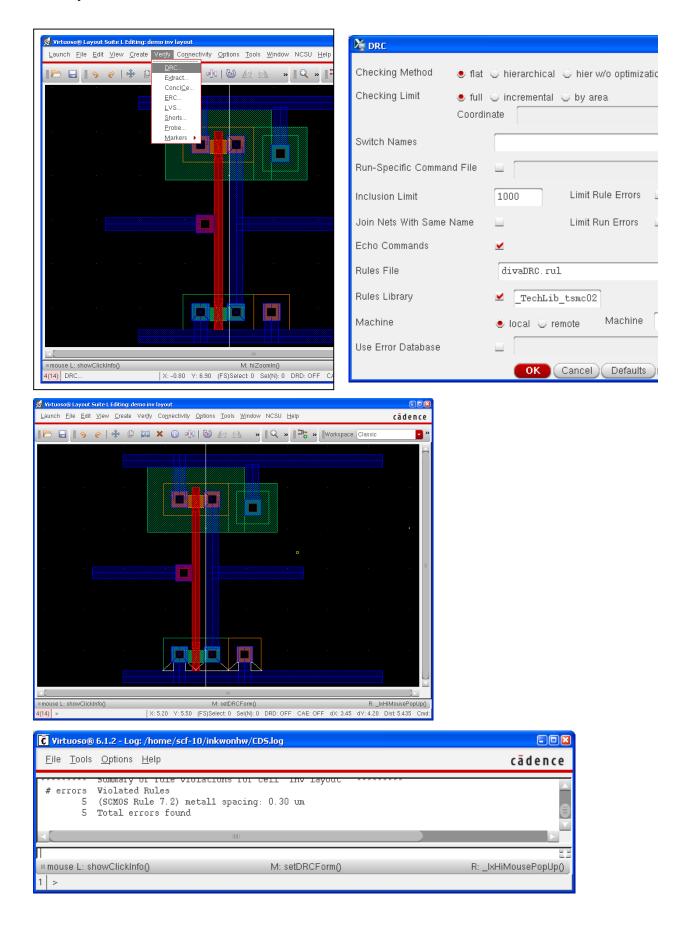
Create  $\rightarrow$  Shape  $\rightarrow$  Path

First of all, you should select metal1 on LSW window. Default width for metal1 is 0.3, which means 300nm (3  $\lambda$ ). You can draw metal layer simply by clicking

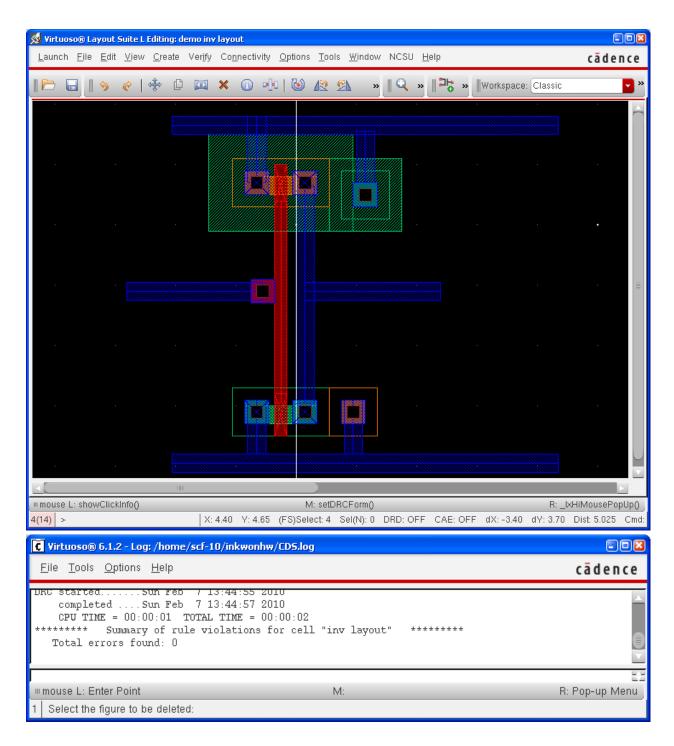


#### E. Run DRC

This step checks if your layout follows design rules. Verify  $\rightarrow$  DRC



We have five errors. It is because a gnd metal layer is too close to an nmos transistor. After modifying layout, run DRC again.



There is no error!!

### F. Add pins

We had two pins on a schematic, which are "in" and "out". Pins are for assigning signals to physical device, so we assign voltage level of gnd and vdd by using pins. Hence, we have 4 pins for the layout, which are "in", "out", "gnd!", and "vdd!".



🕺 Virtuoso® Layout Suite L	Editing: demo inv layout	隆 Create Shape Pin
Launch Eile Edit View	<u>Create Verify Con</u> nectivity Option Shape 1. <u>Wire</u> D. •]•0   € D. •]•0   € D	
· ·	Multipart Path Guard Ring P&R Objects • Group Microwave • Repoint to Point	Mode       ● rectangle ◯ dot ◯ polygon ◯         I/O Type       ◯ input ◯ output ● inputOutput         ◯ jumper ◯ unused ◯ tristate         Snap Mode       orthogonal ♥         Access Direction       ♥ Top ♥ Bottom ♥ Left ♥ Right         ♥ Any □ None
· ·		Check "Display Terminal Name" if you want t see pin name on the layout. Click "Display Terminal Option
		Terminal Name Display       Height     0.3       Font     stick
mouse L: showClickInfo() 4(14) >	X: -2.65 Y: 6.70 (FS)S	Text Options 🖌 Drafting Overbar Layer

🛈 Pin Layer

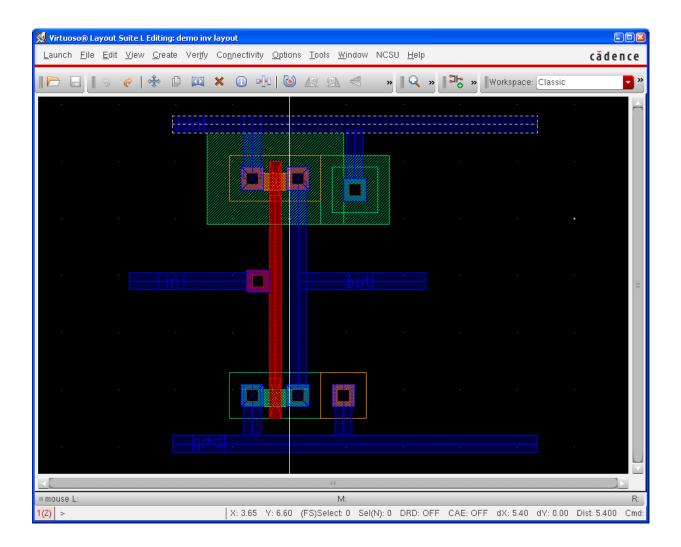
centerCenter

▲ Sideways

0K

Justification

🕗 Rotate



## G. Extract

A layout is just a picture. If you need to run simulation using the layout, you should convert it to the other format. It is done by extracting. It's something like compiling a code.

🕺 Virtuoso® Layout Suite L Editing: demo inv layout	N	
Launch File Edit View Create Verify Connectivity g	K Extractor	
	Extract Method 🛛 💩 flat	😳 macro cell 🤤 full hier 🙄 incremental
ERC	View Names Extracted	extracted Excell excel
<u>L</u> VS <u>S</u> horts	Switch Names	Extract_parasitic_caps Set
<u>P</u> robe Markers ▶	Run-Specific Command File	-
	Inclusion Limit	1000 Limit Rule Errors
	Join Nets With Same Name	Limit Run Errors
	Echo Commands	<b>⊻</b>
	Rules File	divaEXT. rul
	Rules Library	✓ _TechLib_tsmc02
	Machine	🖲 local 🤍 remote 🛛 Machine
	Use Error Database	
		OK Cancel Defaults Ap
	Select "Extract_parasti	c_cap" as a switch name,
	-	d design won't have parasitic
	capacitances.	
mouse L: showClickInfo()         M: hiZor           1(2)         Extract         X: 1.65         Y:		
Kibrary Manager: WorkArea: /home/scf-10/inkwonhw/cd	5	
<u>File E</u> dit <u>V</u> iew <u>D</u> esign Manager <u>H</u> elp		cādence
🔄 Show Categories 🔄 Show Files		
Library Cell	View	
demo inv	extracted	
NCSU_TechLib_ami16 inv NCSU_TechLib_hp06	extracted Tayout	
NCSU_TechLib_tsmc02 NCSU_TechLib_tsmc02d	schematic	
NCSU_TechLib_tsmc03 NCSU_TechLib_tsmc03d		
NCSU_TechLib_tsmc04_4M2P		
basic cdsDefTechLib		
~ Messages		
Log file is "/home/scf-10/inkwonhw/cds/libManager.log". DB was auto refreshed.		

#### H. Run LVS

As I mentioned before, this step is very important for your grading. More complicated design, more time will be required for debugging LVS.

Verify  $\rightarrow$  LVS

Keep in mind. You SHOULD compare your schematic with EXTRACTED.

🕺 Virtuoso® Analog Design Environment L Editing; demo inv e	C Artist LV5		
Launch Eile Edit View Create Verify Connectivity (	Commands <u>H</u> el	p	cāden
Extract	Run Directory	LVS	Brows
	Create Netlist	⊻ schematic	⊻ extracted
<u>S</u> horts	Library	demo	demo
Probe <u>P</u> robe → <u>M</u> arkers →	Cell	inv	inv
	View	schematic	extracted
		Browse Sel by Cursor	Browse Sel by Curs
	Rules File	divaLVS.rul	Brows
	Rules Library	✓ NCSU_TechLib_tsmc02	2
	LVS Options	⊻ Rewiring	📃 Device Fixing
		📃 Create Cross Reference	⊻ Terminals
	Correspondence	File 🔲 🔤 Ivs_corr_file	Creat
	Switch Names		
	Priority 0	Run background 🔽	
	Run	Output Error Display	Monitor Info
	Backannotate	Parasitic Probe Build	Analog Build Mixed
mouse L: showClickInfo() M: hiZo			
mouse L: showClickInfo()         M: hiZor           2(4)         LVS         X: -0.70         Y: 7.65         (F:	12		

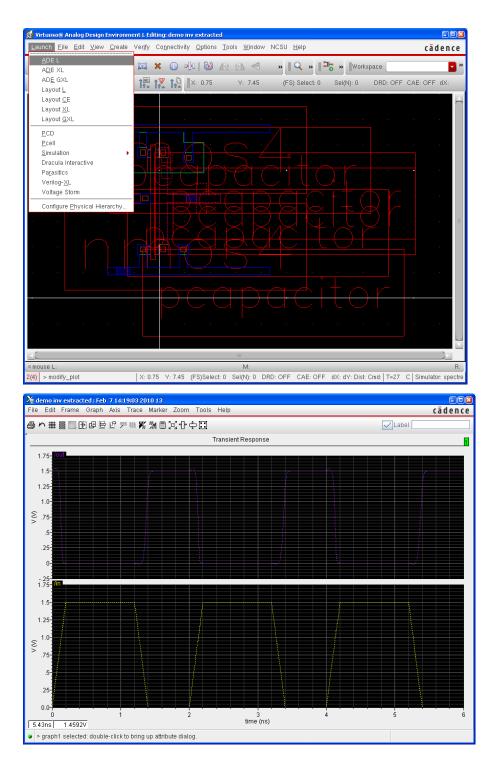
#### I hope all of you will see the following window.



If there are errors, you can check the results by clicking "Output" button. "Error Display" also might be helpful.

## I. Run Spectre simulation

It is same as schematics. Please follow the instructions for the schematics.



#### Congratulations!!

You followed all steps I prepared. Let's do the same thing for more complicated designs.

## \*Some useful information

## **Useful Links:**

http://www.edaboard.com/ http://www.eda.ncsu.edu/wiki/NCSU\_EDA\_Wiki http://www.cadence.com/community/forums/