Carbon Nanotube Field Effect Transistor- A Review

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Abstract— The greatest advances in Silicon based electronic technology have dominated the computation world for the past decades. The captivating performance of Si devices lies in sustainable scaling down of the physical dimensions, by that increasing device density and improved performance. But, the fundamental limitations due to physical, technological, economical and manufacture features restrict further miniaturization of Si based devices. The pit falls are due to scaling down of the devices such as process variation, short channel effects, high leakage currents and reliability concerns. To fix the above-said problems, it is needed either to follow a new concept that will manage the current hitches or to support the available concept with different materials. The new concept is to design spintronics, quantum computation or two terminal molecular devices,. Otherwise, presently used well known three terminal devices can be modified with different materials that suits to address the scaling down difficulties. The first approach will occupy in the far future since it needs considerable effort; the second path is a bright light towards the travel. Modelling paves way to know not only the current-voltage characteristics but also the performance of new devices. So, it is desirable to model a new device of suitable gate control and project the its abilities towards capability of handling high current, high power, high frequency, short delay and high velocity with excellent electronic and optical properties. Carbon nanotube became a thriving material to replace silicon in nano devices. A well-planned optimized utilization of the carbon material leads to many more advantages. The unique nature of this organic material allows the recent developments in almost all fields of applications from an automobile industry to medical science, especially in electronics field-on which the automation industry depends. More research works were being done in this area. This paper reviews the carbon nanotube field effect transistor with various gate configurations, number of channel element, CNT wall configurations and different modelling techniques.

Key words: Array of Channels, Carbon Nano Tube Field Effect Transistor, Gate Wrap Around Transistor, Modeling, Multi-Walled CNT, Single-Walled CNT

I. INTRODUCTION

FOR, the past four decades, Si technology governs the computing world by achieving defensible performance with the scaling down of physical dimensions and advanced device characteristics. But, the scaling trend is slowing down because of its physical, material as well as manufacturing restrictions. It is the right time to study the effects of aggressively downscaling and to explore the suitability of new device materials and design.

Carbon won its dominating place with its identical electrical, optical characteristics over Silicon. Recently more developments are reached in realization of nano electronic devices with carbon material like nano diodes, nano transistors, nano sensors and so on. Number of different structure had been proposed and analyzed so far. It is well-being to model a structure and to know its full behavior before fabricating in real time.

Nor Zaidi Haron et.al [1] in their paper discussed the above said challenges faced by CMOS silicon semiconductor technology. They also suggested another alternative - the non-CMOS nano devices to explore, to invent new high-performance and cost-effective alternatives.

Mark White et.al [2] in their work on scaling CMOS Technology stressed the limits of scaling down the physical dimension and their impact on circuits. The technological challenges towards a) new lithography techniques b) new transistor design c) sensitivity of current to radiation errors d) nano-scaled interconnections e)stability in circuits f)improved productive design g)density of devices adaptability of new materials and h) cost were addressed. Along with the impact on circuits, the management of leakage power, uncertainty and variation were included. The authors also add about the soft error problem due to radiation which is a serious issue while designing advanced processors.

Ban.P.Wong et.al [3] discussed the problems and challenges of scaling down the nano-CMOS and the necessary steps to be followed to face such difficulties. They included the manufacturing, lithographic issues, new physical design, new modelling, change in design methodology, process control and reliability.

Phaedon Avouris et.al [4] reviewed the progress electronics and optoelectronics of carbon nanotube. They stated that the discovery of integrated circuits led to the development of advances in Si-based industry. It was achieved by scaling of the physical dimension that reached its saturation and needs some other alternative to outperform the existing ones. In addition, Carbon nanotube (CNT) addresses the problems of aggressively downscaling of Si-devices. Single-walled carbon nanotube with its unique electronic and optical properties has more advantages along with its nanoscale dimension, the authors added. Soree B et.al [5] claimed that the nanodevices (nanowire and graphene devices) with their high functionality, outstanding electrostatic control, improved management of short-channel effects and ultra-high mobility could replace the existing CMOS.

Though carbon nanotube is a potential replacer of Si, one of the challenges is to study the electrical characteristics and to test low power nano scale devices. Jonathan Tucker [6] provided the methods, techniques of probing the nano meter measurements and to overcome any measurement errors. In CNTFETs, the channel is replaced with semiconducting carbon nanotube between the source and drain electrode instead of Si as in the conventional devices. The electron current flows when a positive or negative charge is on the gate

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for n- or p- type FET and the voltage exceeds the threshold as stated by Phaedon Avouris [7].Carbon nanotubes can be metals or semiconductor with respect to their chiralities. The aspect ratio is very large with its small diameter. Meanwhile, long length helps the CNTs to possess 1-D structure. This in turn led to the reduced carrier scattering and ballistic transport [7]. Yafei Zhang et.al [8] reviewed the advances in structures, principles and operation of nanodevices. Sensors, diodes, transistors, photovoltaic and light emitting devices could be developed using nanostructures. The CNTFET performs better, faster with less power consumption than conventional Silicon devices. Joerg Appenzeller [9] reviewed the understanding problems while developing high- performance carbon nanotube. The authors included 1. Optimum device design 2.Contact formation in CNTs 3. AC characteristics and capacitance considerations and 4. CNTFET-based ring oscillator in their work. Reviewing Carbon nanostructures, Ali Eatemadi et.al discussed their various structures, properties and applications in the field of medicine[10].

Satio.T in his work explained the hybridization of carbon materials and its electronic structure[11]. The synthesis, energy band, transport properties, phonon modes and Raman spectra of single-walled carbon nano tubes were discussed in detail. Single-walled carbon nanotube of 1nm diameter was synthesized by Sumio Iijima et.al[12]. They reported that with the single shell open at the ends resulted in free dangling bonds to capture the carbon atoms. Co-vapourising carbon and cobalt grow very small diameter CNTs of single atomic layer thickness reported Benthune et.al [13]. The unique electronics and magnetic properties of nanostructures, CNTs, inorganic nanowires, array of channels, detailed by Klaus D Sattler provided an overview of the material [14].

Mobility enhancement technique was reviewed by Yi Song et.al [15] along with the global, process-induced strain technology, new high-mobility channels and hybrid-orientation channels too were added in detail. The real-time applications of CNTs have its limitations such as the selection of most appropriate form of sp2. Composites, electronics, field emission and electrochemistry were four areas reviewed by John Robertson [16]. He stressed that among various methods of synthesis of nanotubes, Chemical vapour deposition is found to be the best fit with controllable purity during the CNT growing process.

II. Applications of Electrical Characteristics of CNTs

A. *CNT in Electronics*

CNTs perform remarkably in the field of electronics. Its 1D nature decreases the scattering phase space by that increasing the possibility of maximum bulk mobility in semiconducting CNT transistors resulting in high “on” current (> 1mA/µm). In addition, 1D electron confinement suppresses short-channel effects. Similarly, extremely high current densities (~19A/cm2) are generally handled by metallic CNTs since it has low scattering, good thermal conductivity and strong chemical bond. Also, as there are no dangling bond states in CNTs, it allows a choice of a wider range of gate insulator materials. CNTs provides the same effective mass for both p-type and n-type devices that suit better for CMOS. As CNTs can be both metallic and semiconductor, it fulfils the need of both interconnect and devices [17].

The physical properties of carbon nanotube could be controlled by doping carbon nanotube with non-metals, transition metal, alkali metals and clusters is found in the literature [18]. Electrical, magnetic, transport and optical properties of carbon nanotubes along with its applications in the fields like field spintronics, emission, nonlinear optics and chemical sensors were reviewed in detail.

Graphene nanoribbons (GNR) and carbon nanotube were compared for their transistor characteristics and made clear that CNTFET would head the future electronics. The reason for this prediction was that CNTFET proved its characteristics similar to the conventional Si-devices consuming low power. To study the electrical characteristics of a new device material it is necessary to examine its electronic structure and the nature of the band gap. Rashid Nizam et.al.[19] calculated the band gaps of the carbon nanotube (CNT) using tight-binding approximation. They observed that the band gaps decrease from 6 eV to 0 eV in zig-zag CNT with increase in its diameter. In contrast, armchair CNT maintains 0.011 eV for all diameters. In addition, the density of states in zig-zag becomes zero at 0eV which is not in the case of armchair. It is clear that zig-zag CNT(n,0) is semiconducting if n/3 is not an integer otherwise it is metal. The relation between the diameter and the band gap has been proved.

More improvements were possible in p-CNTs since oxygen-induced dipoles at the interface between the metal electrode and CNT allowed them to be available under ambient conditions, while n-CNTs need a controlled environment. Radosavljevic. M. et. al [20] fabricated vertically scaled potassium n-doped of high performance by exposing potassium vapour and device annealing in high vacuum. The energy barrier between the electrodes and carbon nanotube has to be addressed seriously as it is a severe limitation for the device conductance. This is overcome by contacting a high work function noble metal like palladium removes this barrier through the valence band of nanotubes Javey A et.al [21]. Palladium contact allows the ON states of semiconducting nanotubes to behave as ballistic metallic tubes and exhibits ballistic transport at room temperature. The device analysed by the square-law completely failed to reproduce device characteristics because the transport is closer to ballistic for the short tubes.

Yu-Ming et.al fabricated CNTFETs of electrostatic tunable n- or p-type with unipolar behavior and good OFF-state performance[22]. A controllable polarity for thin gate oxides results in pure p- or n- type enhancement-mode CNTFETs show the steepest sub-threshold slope. Regarding the integration with high ε-dielectrics it is easier for CNTs for the interface does not exist as in Si-SiO2 that needs passivation. The high physical, chemical stability and high conductivity of metallic CNT makes them use as good interconnects [4].

B. *CNTs as Field Effect Transistors*

Non-CMOS nano devices are categorized into electrical, magnetic and mechanical-dependent devices. Under electrical-dependent devices, the ballistic transport, tunneling and electrostatic operations are based upon either the ballistic current flow through the channel (medium with zero

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resistance, tunneling current due to quantum-mechanical process) or with the electron interaction due to electric field. Examples of such devices includes Carbon nano tube field-effect transistors (CNTFETs), semiconductor nanowire field effect transistors (NWFETs), resonant tunneling diodes (RTDs), single electron junctions(SEJs) and electrical quantum dot cellular automata Nor Zaidi Haron [1].

The magnetic dipole interactions and the spin-polarized electron transport manipulate electrons to carry the information in magnetic-dependent devices. The magnetic quantum dot cellular automata (MQCA) and spin field effect transistors (spinFETs) belong to such category of devices. In the case of mechanical dependent devices, the conductive polymers are restructured for any changes or movement to respond the input sources. The molecular memory and FPGA utilizes this phenomenon.

The basic concepts for analysing the various devices, circuits and systems were explained by Mark Lundstrom et.al [23]. The nature of ballistic nanotransistors, scattering theory of MOSFET, nanowire field effect transistors and the transistors at the modelling scale were detailed by the same authors. The book reveals the fundamentals to be learned for handling nano scale device. Phaedon Avouris et.al [17] reviewed the electronics and optoelectronics of carbon nanotube. The graphene sheet is folded to get 1-D structure of CNT and this structure is responsible for reducing phase space scattering and increasing bulk mobility of charge carriers resulting in high ON current in semiconducting CNTs. Also, chemical stability supports the carrier mobility without being affected by processing and roughness scattering as in conventional devices.

In addition, regarding the gate insulators, they have a wider choice because of its improved electrostatics [24]. The gate leakage current as in SiO2 thickness below 1nm is improved with its gate control as there is no dangling bond states at the surface of the tube. The combined impact of electrostatic and high ON current suggest applications of CNTs in optoelectronics. Role of diameter and gate oxide thickness in determining the electronic property of CNTs is vital [25]. Ambipolar CNTFETs can be used to produce a single gate-controlled light source.

An analytical model proposed by Yousefi.R et.al [26] and calculated the charge of the top of the channel barrier. Ali Javey [27] demonstrated that high-quality thin film high-k dielectric gate insulator with Pd- tube contacts and doped source/drain electrodes resulted in increased performance p-type CNTFETs. This structure allows aggressive vertical scaling down of FETs and provide good OFF state.

Numerical simulations were used to analyze the CNTFET with palladium contacts in the literature by Aron W. Cummings et.al [28]. It was found that the gate strongly modulate the contact properties that could be used for realizing excellent sub threshold swings for short channels high-performance CNTs. Scaling behavior also shows real improvement in this work.

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III. Various Gate Configurations

A. Double Gate Configurations

Schmitt-Landsiedel.D [29] introduced various innovative architectures in design perspective view. For devices beyond CMOS, circuits with FinFETs and multi-gate FETs reduce the leakage power while the switching speed and maximum ON current remain challenging were observed.

The electrical performance of double-gate (DG) CNTFET was optimized using a genetic algorithm in the research work by Toufik Bendib et.al [30]. In general, the nanoscale DG CNTFET face challenges to model as the coupling between the electrodes, quantum confinement transport and tunnelling of gate. The compact model proposed an efficient algorithm to maximize the electrical performance of DG CNTFET. Also, this model could be extended to other parameters like underlap, overlap and series resistances. This model could be used to study the nanoscale sensor devices. The newly developed dual gate CNTFET with the gate on top and underneath the channel gives conventional device characteristics with negatively biased silicon gate. The advantage of co-axially gated device over the dual-gate is that the former provides aggressive scaling down of channel length.

CNTs allows for aggressive channel length scaling due to its small dimension. Its intrinsic nature ensures high-ON current. The structure of CNTFET is similar to the conventional FET except the semiconducting CNT replaced for the channel. The reduction of device dimensions and improved material properties to increase the mobility of the charge carriers will increase the switching speed of the device. But, experts suggested that downscaling is at the expense of reduced channel mobility. Reducing gate oxide thickness leads to more gate leakage currents though high-k gate material will help. As ultra-thin body thickness in turn results in reduced mobility due to increasing in surface roughness scattering.

B. Gate Wrap around Transistor

The intrinsic advantage of gate all around transistor is said to be more due to high mobility and ultrathin body. Fig.1a shows Double-gated CNTFET while the Fig1b displays co-axially gate CNTFET, which allow the most aggressive gate length scaling with good channel control. The metal gate is wrapped around the channel and the parasitic effects due to overlap of the electrode contacts are significantly reduced because of the heavily doped, on-state low series resistance un gated portions. Fig .2 depicts the schematic device structure of multi-gate FETs viz.1) Double-gate, 2) triple-gate 3) quadruple-gate and 4) Pi-gate. Cross-section of various gate configurations is projected in Fig.3.Benjamin Iniguez et. al [31] proposed a compact model using 1-D Poisson's equation in the perpendicular direction of channel length for Multiple-Gate MOSFET. As scaling down of device dimension faces difficulties, the multi-gate structures proved to be a right solution for their good channel control that in turn reduces the short channel effects and a steep subthreshold swing. The noise and high-frequency performance were also been studied.

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The short channel effects of nanoscale MOSFETs were analysed for double-gate and surrounding gate. It was concluded that surrounding gate MOSFETs could be scaled 35% lesser than double-gate MOSFETs. In order to represent the accurate potential for the entire device channel, the 2-D electrostatic effects were analysed using evanescent-mode as per the report of Sang-Hyun et.al [32]. Bastien COUSIN et al [33] in their compact model for Gate-all around Si- nanowire transistor, analysed the quantum-mechanical effects. The new device CMOS structure is needed for handling the problems of device downscaling process and multi-gate relevantly provide the solution. The gate- all around structured transistor among the rest gives enhanced gate control to manage the short channel effect.

The Gate all around the structure is an ideal structure to maximize the gate control in FETs. For the first time, Zhihong Chen et.al [34] demonstrated functionalized tube as the channel in gate all around CNTFET surrounded by an Al2O3 as dielectric and WN as gate metal. The dielectric and gate metal is to wrap the CNT completely for a perfect GAA layout. Various annealing conditions were applied for improving the interface between the channel and the gate. The tungsten nitride and Al2O3 are removed from the other parts of the channel except the gate area. The contact points form at the ends of the source/drain electrodes and the rest of the uncovered portion of the tube are subjected to doping either chemically or electrostatically while, the gate part of the CNT remains undoped. Two arguments were put forth, first was the claim of the first demonstration of GAA CNTFET device configuration and the second was that the extent of response of the gate oxide charges for the device performance.

A compact model Landauer transmission theory for gate-all-around CNTFET is proposed by Jimenez.D et.al [35] at the ballistic limit. Semi-classical ballistic transport and zero transmission probabilities were assumed and the current was derived by means of Landauer approach. More charge was induced as a result of lowering of barrier height due to gate voltage. The model suits for circuit design and holds good for wide range of temperature, in all the operating regions. The doping concentration, the geometrical dimensions and source/drain extension of bulk gate-all-around nanowire were adjusted. It was done for optimized AC, DC characteristics by reducing the parasitic capacitance and resistance reported by Yi Song et.al [36]. It was concluded that smaller the nanowire cross section better the gate control and volume inversion.

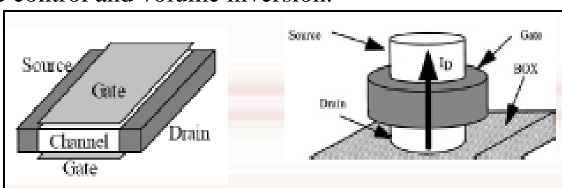

Fig. 1(a) Fig. 1(b)

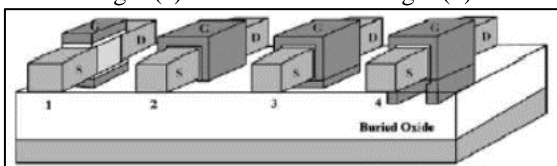

Fig. 2:

Bottom isolation, nanowire diameter control and Source/drain extension design were optimized so that the parasitic conduction of GAA MOSFET was suppressed and thereby the device behaviour could be improved [37]. This optimization supports for high device immunity against short channel effects and high ION/IOFF ratio. Biswajit Ray et.al [38] proposed a physics-based model of a GAA Nanowire Transistor and discussed its potential distribution. As GAA offers excellent channel control and zero corner effects, the work proposed a compact model for such devices so as to make it for integrated circuit design and simulation. Poisson's 2-D equation in cylindrical coordinate system was solved to find that at crossover point- where all the curves between body potential and gate voltages meet for equal lengths but various radii of the channel. The influence of body radius on the threshold voltage of undoped body multi-gate transistors had been explained.

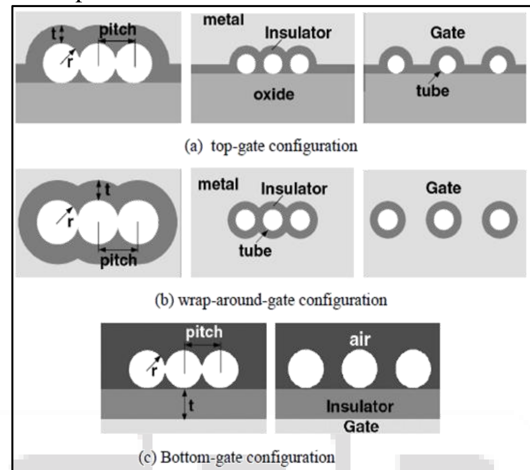

Fig. 3: Configuration

A self-consistent Schrodinger-Poisson solver was used and investigated for studying the electrostatic characteristics of different CNT transistors. It was found that due to the symmetry nature gate all around performed with good and efficient gate control by Marchi A et.al [39]. Surrounding Gate performs better than back-gated structure; an optimum design was proposed by Md. Shafayat Hossain et.al[40] through the study of electron transport in a ballistic regime. Md Shafayat Hossain et.al [41] also observed high performance carbon nanotube transistor with the high-k dielectric gate oxide.

IV. ARRAY OF CNT CONFIGURATIONS

CNTFETs need to be fabricated with a parallel array of channels between the Source/Drain electrodes in order to match the performance with the conventional Si-devices, as in the literature of Marchi A et.al[39]. Most current synthetic schemes evolve in fabricating SWCNTs as mixtures of metallic or semiconducting tubes that adheres themselves to form 'bundles' or 'ropes.' Using 'constructive destruction' [7] selectively destroyed m-CNTs alone leaving s-CNTs behind. Fig. 4 shows AFM image of an SWNT after removing metallic tubes. Fig. 5 illustrates an array of channels connecting source and drain electrodes.

To get more information about AC characteristics of the intrinsic channel, gated array of channels is proposed to enhance the total current by using the parallel nanotubes. This structure supports for increasing more gate capacitance and decreasing the impedance.

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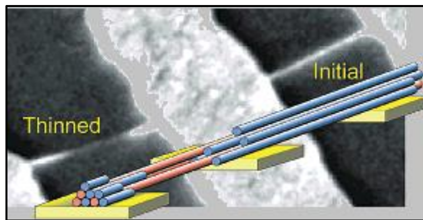

Fig. 4: CNTFETs

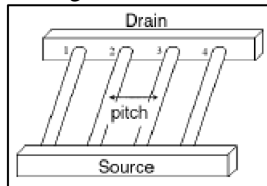

Fig. 5: CNTFETs

Ballistic self-aligned carbon nanotube FET with low contact resistance palladium electrodes and gate oxide electrode of high-k dielectric at room as well as at low temperature was demonstrated by Ali Javey et.al[27]. The advantages of array of channels allow for larger current were given importance. It is obvious that single channel provide little drive current and an array of CNTs are required to drive largely deriving capacitance as Xinlin Wang et.al[42] reported. Three configurations of gate electrodes were studied and the capacitance of CNT was calculated for the array. It was concluded that wrap-around gate configuration with array of channels provides largest capacitance. Also, the value of the pitch distance slightly larger than 2 (gate insulator thickness plus radius of the tube) provide larger gate to channel capacitance and in turn larger drive current.

Thin film CNT is one of the solutions to a deliver large current, but the large contact resistance between the CNTs restricts the selection of the same. Vertical array of channels performs lesser due to large top contact resistance and in-efficient gating. An ultra-short channel length, densely packed parallel array of non-overlap planar CNT had been preferred for inducing larger gate channel capacitance [43]. It was found that the pitch distance between the CNTs should be below 6nm to outperform the silicon devices. Impedance mismatch and more parasitic effects were experimental observations for individual CNTs and those were limited using aligned CNT arrays between the source/drain electrodes claims Zhenxing Wang et.al [44].

The high-frequency performance of the CNTFET is as important as the improved drain current performance. The intrinsic capacitance plays a major role in 1-D devices like CNTFET to reduce its throughput. This could be optimized by arranging an array of channels in the geometry of a single transistor. Then it enables Carbon nano tube field effect transistor to decrease the parasitic capacitance as reported in [45]. This work is useful in studying the high-frequency characteristics of CNTFET and assess it for RF applications.

Though it was proved that CNTFET excelled in its performance and predicted the device's suitability for high-frequency operation; it is still challenging because the scattering parameter measurement needs the impedance matching. Henri Happy [46] fabricated and found that the array of parallel tubes suitably improves impedance matching. Also, replacing semiconducting gate with the metal gate reduced the parasitic capacitance and increased density of channel resulted in high-frequency characteristics of CNTFET.

Single channel CNTFET lags in high –frequency performance because it suffers from the parasitic capacitance. This difficulty was overcome in the literature [47]. They utilized the self-consistent quantum simulations to disclose the high-frequency performance of the CNT. It was observed that denser the parallel channels lesser the parasitic effect that in turn resulted in a larger improvement of high- extrinsic frequency performance with sparse channels. The improvement was smaller with denser channels during which the extrinsic become equal to the intrinsic frequency. Yijian Ouyang et.al [43] assessed the performance of CNT array transistors under the non- ideal factors. They observed that CNTs performed lesser with non-ideal factors during fabrication. Fraction of metallic CNTs swept away the gate modulation of the current, and misalignment of CNT orientation disturbed the on- and off- currents.

A dual-output second-generation current conveyor was realized using a high-performance, wide bandwidth CNTFET The channel density, the diameter of the tube and the pitch distance are the parameters taken for the investigation by Ale Imran et.al[48]. The value of trans conductance increases with an increase in number of channels thus reducing the resistance. Closer the CNTs decreases the gate channel capacitance; the optimum choice of inter-CNT pitch distance being 16nm. The band gap energy and threshold voltage of the CNT is related to the diameter of the tube. It also affects the source/drain series resistance. Increasing the tube diameter decreases both gate channel capacitance and fringing capacitance due to screening effects of adjacent channels. Increase in diameter also reduces the resistance thus increasing the current but it deteriorates with more diameter value. A trade-off is involved and the optimum diameter had been chosen as 1.5nm with the chirality of (19, 0). Finally, it had been proved that the CNTFET possess excellent performance than its CMOS counterpart providing high-frequency response with low power supply. Andre DeHon [49] designed basic computing architecture systems for nano devices like CNTFET, Si- nanowire FETs and nano-scale FETs. This cross wire array architecture holds good for micro-to-nano scale interfacing.

V. VARIOUS CNT WALL CONFIGURATIONS

A. *Single-walled CNTFET (SWCNT FET)*

By wrapping a single graphite sheet into a tube, forms carbon nanotube. The density of states (DOS) is zero at the Fermi level of graphene, by which itself can be characterized into a zero-gap semiconductor or a metal. In turn it can be imparted into the carbon nanotube. Also, the electrical conduction in CNT depends on its chirality (way of rolling the graphite sheet) and the diameter. SWCNTs are almost with smaller diameter and longer length possessing very large aspect ratio resulting in 1D system

In switching industry molecular electronics, would lead to new miniaturization techniques. However, the electrical measurements are difficult to be realized. Sander. J Tans et.al [50] fabricated a single-wall carbon nanotube connecting to two electrodes at the end to form three-terminal switching transistor. Application of gate voltage switches the device from ON to OFF state. The importance of this work remains in the operation at room temperature.

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Zhen Yao et al [51] measured the intrinsic high-field transport in SWCNT and observed that with the increase in the bias voltage drops the conductance because of scattering of electrons.

In the hexagonal lattice arrangement of the carbon atoms, each atom is bonded with neighbouring three atoms via sp2 molecular orbitals. The fourth valence electron forms a localized π- band by hybridizing with all other pz orbitals. The electronic properties of carbon nanotube can be derived from that of the unique characteristics of the graphene sheet. The wrapping up connects two sites of graphene sheets called chiral vector, which is defined as C = na + mb ≡ (n, m). Here a,b are the unit vectors and n, m are integers. The rectangle formed by C and the 1D translational vector is defined as unit cell. As the unit cell has even number of carbon atoms resulting with even number of electrons, it consequently leads to the band structure that can be either a metal or semiconductor. In Fig. 6a and Fig. 6b, a tube of circumference C is formed if point B is brought to touch point A with n = 5 and m = 2 (5,2). If mod (n-m,3) = 1or 2, then the SWCNT is semiconducting otherwise, if mod(n-m, 3) =0 or if (n < m), then the SWCNT is metallic at room temperature. The case n=m denotes arm chair (Fig. 8) while on the contrary (n, 0) is zig-zag tubes (Fig. 7). Regarding the ohmic contacts in single-walled CNTs, David Mann et .al [52] found that Pd ohmic contacts performed better than the titanium (Ti). Mean free path in the CVD grown material for defect scattering was found to be from 1μm to 4μm.

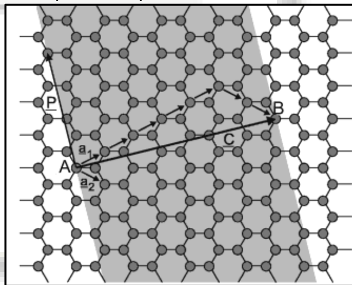

Fig. 6(a): Band structure

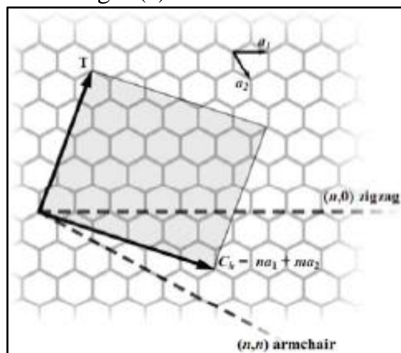

Fig. 6(b): Band structure

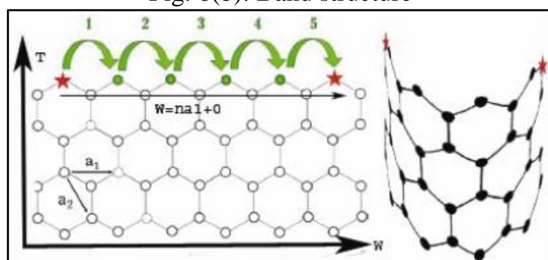

Fig. 7: Zig-zag tubes

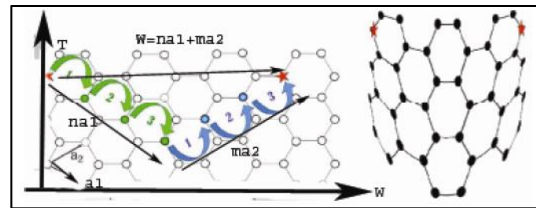

Fig. 8: ARM chair

B. Multi-walled CNTFET (MWCNT FET)

MWCNTs are scrolled graphite sheet of co-axial cylinders separated by a distance of ~0.34nm to form multiple layers in Russian doll model. Arc-discharge and CVD methods are used to grow the tubes of diameter from ~2nm to 100nm. Larger the diameter, larger the defects like vacancies [24].

As it is co-axial cylinders, alternatively the tubes are semiconducting and metallic. Inter cylinder interactions are very small but cannot be neglected for nano devices. If the cylinders are of different chiralities, total density of states will be the individual contribution of each cylinder [24]. Metallic MWCNTs can be a better interconnect with lesser signal delay and it is significant with technology scaling and long wires than Cu as shown by Li H et.al [53]. Being easier to fabricate, MWCNTs find its immediate utilization in VLSI and ULSI. Pu SN et.al [54] found that double-walled CNT interconnects reduces the crosstalk –induced time delay, particularly in long wires that were more significant.

Regarding MWCNTs, the cumulative resistance will affect the overall current performance of the device. Nihei M et.al [55] reduced it by parallel conduction of each inner tube. It was achieved by making the top layers in contact with the side of MWCNTs. The side contacts act as good ohmic contact between the top contact layer and MWCNTs. Thus by optimizing the interface structure between thick (>6nm) Ti bottom layers and MWCNTs, the resistance is lowered (the lowest being 0.7kΩ) below the ideal resistance (6.45kΩ) of SWCNTs.

Li HJ et.al [56] studied the transport properties of MWCNTs at room temperature and explored that each tube in the MWCNTs contribute individually to the current. It resulted in large driving current with low resistance that was greater than the cumulative current due to the same number of SWCNTs. Perfect ohmic contacts with the electrodes, large tube diameter and the individual tube contribution guarantees the high current capacity at low-bias gate voltage they added. BourlonB et.al explored the inter shell conduction in MWCNT [57]. He stated that based on the overlap between π orbitals of adjacent shells the intershell transport was mostly independent of temperature and consistent tunnel type. Also, the individual shells conduct along the walls in spite of the insulation from each other with the shorter shell separation.

The disorders and helicity in the transport lengths effects the position of Fermi level in the multishell intrinsic conduction [57]. The same point was stressed by [58] during the analysis of double-wall CNT that each channel contributes individually to the conduction in spite of any inequalities in the tube. The authors [59] of the book reviewed details regarding the structure of CNT, electrical, optical, transport properties of Single and Multi-Wall CNTs. It was stressed that with easier synthesis, MWCNT possesses high electrical and transport properties compared to that of SWCNT.

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Kaihui Liu et.al [60] claims that the advantages of double-walled CNTs are stronger than single-walled CNTs with their unique mechanical, thermal and structural properties. In general, multi-wall CNTs during fabrication introduce alternative electrical properties to the individual walls (i.e. Metallic (M)/semiconducting(S), S/M, M/S, M/M). The paper tested all the combination and found that DWCNTs of M/M and M/S combination shows no gate voltage modulation, S/S provides typical p-type semiconducting with (Ion/Ioff) ratio as high as 104. While in S/M DWCNTs the positive gate voltage suppresses the drain current.

VI. Modeling of CNTFET

Modeling of devices explores the capability towards the understanding its characteristics which provides the enough information including the utilization in various applications. The basic properties of CNTFET with its current-voltage characteristics was investigated and proposed an analytical model of CNTFET by [61]. The simulated results suit well with the results published earlier. Quasi 1-D was incorporated in the analytical modeling proposed by Desmond CY Chek [62]. High mobility model is compared with the low mobility model and the former shows three times greater on-off ratio in this work.

New perspective had been proposed by AdessiC et.al [63] to get fit for aggressively scaled BEYOND-CMOS devices. The different communities of computational modelling and quantum simulation were cross-fertilized to enhance the standard simulations tools. Gate oxide capacitance and the nanotube diameter were the factors are taken by Roberto Marani et.al to propose an analytical capacitance model[64]. Using a new procedure based on best-fitting, the simulated and the measured values were compared.

Array of channels results in parasitic capacitance due to screening effects. For less number of channels in the array and narrow gate widths 1- Devices were not performing better than 2-D devices. Approximations and methods for optimization to overcome such difficulties were discussed by [65]so that the advantages of 1-D devices could be used properly. The analytical model quantifies the metrics of optimized 1-D devices and enables the model for circuit analysis. Meanwhile, the DC operation of conventional CNTFET with high-k dielectric and similar behaviour of normal MOSFET is modelled by Maneux C et.al [66] which has ballistic electric transport. The helical angle and tube diameter are the key parameters to influence the drain current. The complex CNTFET circuits could be analysed logically or analogically using this proposed model.

Sebastien Fregonese et. al [67] proposed an analytical model for analysing conventional CNTFET. They manage a self-consistent loop: Vgs is modulated; VCNT is lowered by QCNT proportionately resulting in a voltage drop across the insulator (VG - VCNT).

As Carbon nano tube transistor is found to the alternate for conventional Si-device, it is time to put effect on circuit design. Yu Cao et al [68] discussed a non-interactive and SPICE compatible integrated model for CNTFET and CNT interconnect. They use zone-folding approximation to relate the parameters, derived the surface potential and studied the impact of Schottky barrier. Surface potential and QCNT are calculated self-consistently. It was found that the intrinsic capacitances control the total performance of the device and get dominated by the fringe capacitance and inter electrode capacitance.

Serhan Yamacli et. al [69] proposed a Spice compatible self- consistent model in Verilog for CNTFET and CNT interconnects and found that CNT possess saturation current characteristics above the threshold voltage. The gate capacitance and the electrical characteristics of CNTFET were numerically modeled for various configurations of the gate electrode like bottom gate, top gate, double gate and surrounding gate. From the study done by Chen PYet.al [70]it was concluded that though top gate could be preferred for easier fabrication and high device performance, surrounding gate configuration possess high gate control with highest gate capacitance. Array of channels are taken for understanding the screening effects, and the pitch distance between the channels were optimized in the work.

The difficulty of modelling the nanotransistor is that it operates in a far-from-equilibrium condition. This hardly describes the device neither by drift-diffusion nor pure ballistic model. 1-D CNTFET using semi-analytical model proposed by Paolo Michetti et.al [71] consider both the far – from equilibrium transport regime and SB contacts. The transition from barrier-limited to channel limited transport was well supported by this model. JieyingLuoet.al [72] reported a semi-analytical model based on virtual-source model for gate all around (GAA) CNTFET. The impact of tunnelling leakage current of the ultra-scaled devices could be studied in detailed with this proposed model. The irregular potential profile along the channel length was modelled including the parasitic capacitance, series resistance and tunnelling drain leakage current. Improvement of delay was through reducing the contact resistivity in CNTFET and tunnelling limits the gate length downscaling were the conclusion drawn from the research work.

Studying the influence of the capacitive effects in CNTFET, Cazind' Honincthun H et.al observed that the high fraction of ballistic transport was yielded by low driving electric field [73]. High ION/IOFF ratio and good intrinsic delay was achieved with the combination of electrostatic gate control and a high fraction of ballistic electrons. In [74] it was presented that the intrinsic transport in Gate All around CNTFET through the evaluation of the electron mean-free-path including electron-phonon scattering. High-level of operation could be expected to closer to quantum capacitance regime was observed with good ION/IOFF ratio and delay in the CNT-based devices.

VII. Conclusion

Carbon nanotube transistor had been reviewed with its modelling techniques including its competing property of CNT against the difficulties of scaling down BEYOND CMOS. Its unique physical, chemical, electrical and mechanical stability nature allows the material in almost all applications. If it is possible to grow enough CNTs using the non-disposable polymers, then in the future the biggest reason of global warming may find a solution. Only if the theoretical results are to be verified practically, the real-time applications will come in true.

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