M E M O R I A D I G I T A L
P A R A
O S C I L O S C O P I O

Tesis previa a la obtención del Título de Ingeniero en la especialización de Electrónica y Telecomunicaciones de la Escuela Politécnica Nacional.

JORGE VILLA GUEVARA

QUITO

MARZO DE 1.976

Certifico que este trabajo ha sido realizado en su totalidad por el señor JORGE VILLA G.

H Jacobson M

Ing. Herbert Jacobson

CONSULTOR DE TESIS

Quito, Marzo de 1.976

A M I S P A D R E S

A G R A D E C I M I E N T O

A los Profesores de la Escuela Politécnica Nacional que me han brindado los conocimientos de Ingeniería.

Al Ingeniero Herbert Jacobson, que guió la realización del presente trabajo.

Y a todas aquellas personas que, de una u otra forma, han contribuído para el logro de esta Tesis.

Quito, Marzo de 1.976

I N D I C E

I N T R O D U C C I O N

La necesidad que tiene el Ingeniero de optimizar los equipos que utiliza, sujeto a los condicionamientos del medio, hace que su actividad se dirija mayormente a la investigación, casos de países desarrollados, o dedique más tiempo a solventar esta desventaja, dotando de mayor utilidad y funcionalidad a los equipos que dispone.

El presente trabajo otorga a uno de los equipos más utilizados, el osciloscopio, una de las cualidades que la técnica ofrece: MEMORIA DIGITAL.

Por limitaciones de carácter económico, debe lograrse un diseño que permita su utilización en el mayor número de osciloscopios con que se cuenta en Laboratorio.

Esta tesis no trata de la teoría digital básica ni cubre áreas tratadas en trabajos similares.

El trabajo desarrollado en cada uno de los capítulos es el siguiente:

En el primer capítulo se trata de los objetivos del presente trabajo y se delimita sus alcances.

Un estudio teórico sobre la memoria se presenta en el segundo capítulo.

En el capítulo tercero se realiza el diseño detallado de la memoria.

C A P I T U L O I

OBJETIVOS DEL PRESENTE DISEÑO

1.1. GENERALIDADES

Uno de los equipos de mayor utilidad en laboratorio es el osciloscopio, por tanto merece especial atención. Será de mucho beneficio dotarle de cualidadee que hagan de este equipo más versátil, por ejemplo: incrementar su respuesta de frecuencia, dotarle de una memoria, etc.

El presente trabajo está orientado a lograr una de estas cualidades: dotar de una memoria digital a un osciloscopio. Para una mayor funcionalidad del diseño deberá ser enfocado en sentido mucho más general.

Actualmente existen diferentes técnicas para almacenamiento de información, tanto digital como analógica. Se prefiere pára el presente trabajo el almacenamiento digital por las ventajas -- que ofrece. El presente trabajo deberá constar de una etapa de - conversión analógico - Digital (A/D), la memoria digital, etapa de conversión digital - analógico (D/A) y el sistema de control.

El diseño debe incluir además la etapa de atenuación y el sistema de fuentes necesarias para su funcionamiento. Lo indicado se presenta en el diagrama de bloques de la figura Nº 1

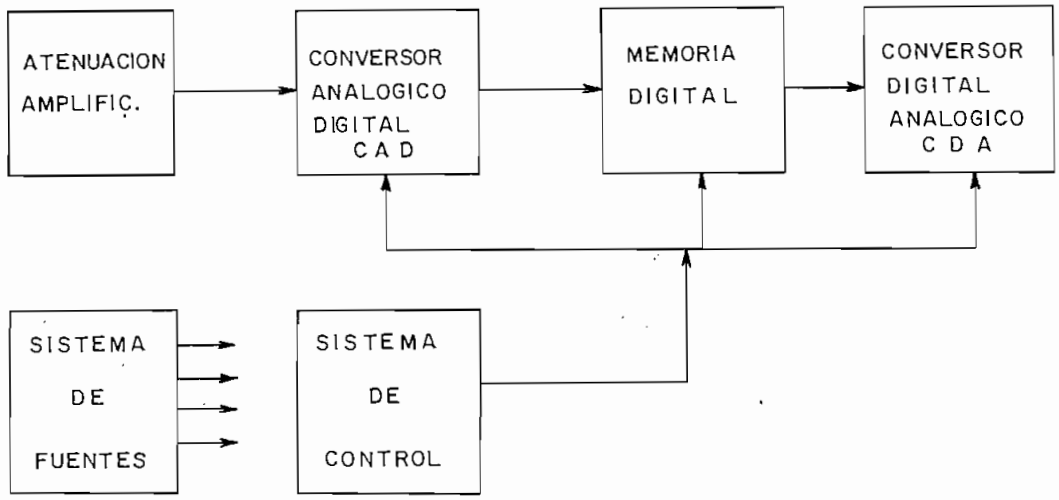


FIG. Nº I

La información a grabarse debe primero alcanzar los niveles de voltaje necesarios para procesarse normalmante, en la etapa de atenuación-amplificación. Posteriormente debe convertirse de su forma analógica a digital como será almacenada en la memoria. Para su presentación en el osciloscopio debe convertirse de su forma digital a analógico.

1.2 OBJETIVO TECNICO

El objetivo técnico del presente trabajo radica en dotar de memoria digital a uno de los osciloscopios que se dispone en laboratorio. Los que actualmente se disponen carecen de esta característica. En el Laboratorio de fuerza existe uno que presenta

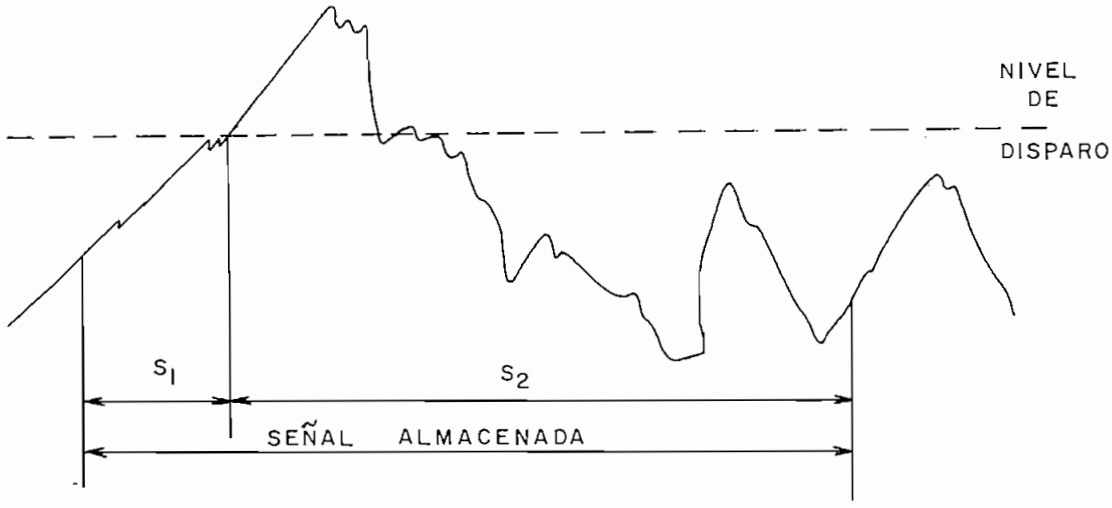
una mayor retentividad de la señal en la pantalla.

Por limitaciones técnicas se ha elegido la respuesta de - frecuencia: DC-100 KHz.

La memoria diseñada debe ser capaz de retener la información almacenada el mayor tiempo posible (teóricamente infinito, - posteriormente se verán las limitaciones existentes), debe responder en un rango de utilidad práctica aceptable a señales de diferentes amplitudes.

Uno de los problemas más frecuentes en las ramas de Ingeniería Eléctrica son los estados transitorios. Su estudio se torna un poco defícil por la dificultad de obtener mediciones durante esos intervalos.

Con este trabajo se presenta la posibilidad de obtener la señal en el momento mismo de producirse el estado transitorio. Se dispondrá da un circuito electrónico que al dispararse (cuando sobrepase la señal cierto nivel, regulable manualmente) grabará la señal desde un instante antes de producirse el disparo, como posterior al mismo. Esto se ilustra en la Figura Nº 2. Se evitarán - grabaciones posteriores.



S_1 : SEÑAL GRABADA ANTES DE PRODUCIRSE EL DISPARO

S_2 : SEÑAL GRABADA DESPUES DE PRODUCIRSE EL DISPARO

FIG. Nº 2

Al realizar estudios de señales sumamente lentas, telefonía telex, información de estudios geofísicos (desde menos de 1 - ciclo/seg. hasta 20 ciclos/seg.), al ser presentadas en el osci-- loscopio no pueden ser muy bien visualizadas por su baja frecuencia. Se hace factible con el presente diseño, grabar la señal a - una frecuencia baja y presentar en el osciloscopio a una frecuencia mayor, mejorando así su visualización.

En cuanto a señales que varían muy rápidamente, se logrará una expansión de las mismas seleccionando una frecuencia de berrido menor a la cual fue grabada.

1.3. OBJETIVO ECONOMICO

Algunos de los factores que delimitan la investigación a nivel universitario en nuestro país son: Versatilidad y calidad - del equipo disponible: limitaciones de carácter económico; poca o casi ninguna relación universidad-medios industriales de produc-- ción.

Un estudio detallado de los medios para solventar estos - inconvenientes abarcaría temas que salen del estudio de esta te-- sis.

Las limitaciones económicas permiten poca posibilidad de adquirir, con cierta frecuencia, equipos tecnológicamente más so- fisticados, que permitirían determinado tipo de investigación.

Debe la Universidad encaminar sus esfuerzos a solventar - este problema. Así por ejemplo se pueden hacer más funcionales a - los equipos disponibles implementando, optimizando sus caracterís ticas.

C A P I T U L O II

ESTUDIO TEORICO DE LA MEMORIA DIGITAL

2.1 DISEÑO A BLOQUES DE LA MEMORIA DIGITAL

2.1.a ATENUACION - AMPLIFICACION.

El sistema de conversión analógico-digital utilizado, opera con señales cuyos niveles de voltaje están comprendidos entre -4V y +4V. Si se aplican señales mayores el circuito resulta afectado notablemente. Con señales menores no responde satisfactoriamente, pues son habilitados muypocos niveles de cuantización.

La etapa de atenuación-amplificación debe satisfacer dos aspectos muy importantes:

a) Entregar la señal a grabarse dentro de los niveles de voltaje en los que opera el conversor analógico-digital.

b) Presentar una impedancia de entrada, constante en el rango de frecuencia utilizado, similar a la que presenta un osciloscopio.

El diagrama en bloques correspondiente a esta etapa se presenta en la figura Nº 3.

FIG. Nº3

La señal debe atravezar primero un circuito de acoplamiento AC/DC para eliminar componentes DC en señales alternas puras. Inmediatamente pasa al circuito de atenuación, el mismo que debe elegirse (con un conmutador) según los niveles del voltaje de la información.

El paso de amplificación además es necesario por que el muestreador, que constituye la siguiente etapa, necesita cargar el condensador de muestreo rápidamente con niveles de corriente relativamente altos, generalmente la información nó será capaz de satisfacer este requisito sin alterarse. Además es necesario independizar la señal de entrada del resto de el proceso.

2.1.8 MUESTREADOR

El sistema de conversión analógico-digital (CAD) que se utiliza requiere que la señal no varíe durante el proceso de conversión.

Para satisfacer esta necesidad se utiliza un sistema de Muestreo - Retención (SAMPLE - HOLD en Inglés). Consta de un sistema de interrupciones y un elemento de retención, como se ilustra en la figura Nº 4

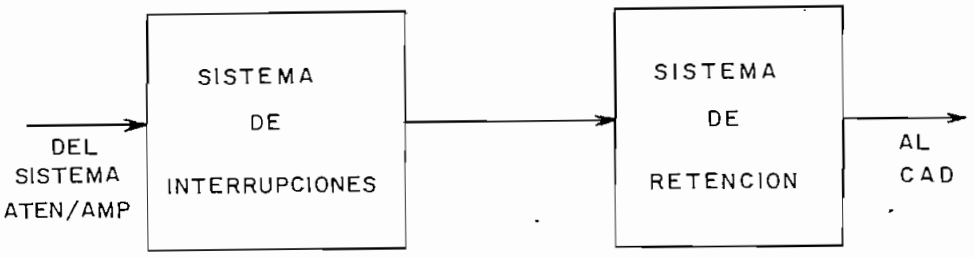


FIG. Nº 4

El sistema de interrupciones generalmente esta constituído por un FET, puente de diodos o un conmutador digital. Como elemento de retención se utiliza un condensador.

2.1.C C O N V E R S O R E S

Se utilizan dos tipos de conversores: analógico-digital - (CAD) y digital-analógico (CDA).

Los CAD transforman señales analógicas o contínuas, características en la mayoría de fenómenos físicos, en sus respectivas equivalencias digitales.

Los CDA son utilizados para devolver una señal analógica luego de haberla procesado como señal digital o discreta. Lo expuesto se presenta en la figura Nº 5.

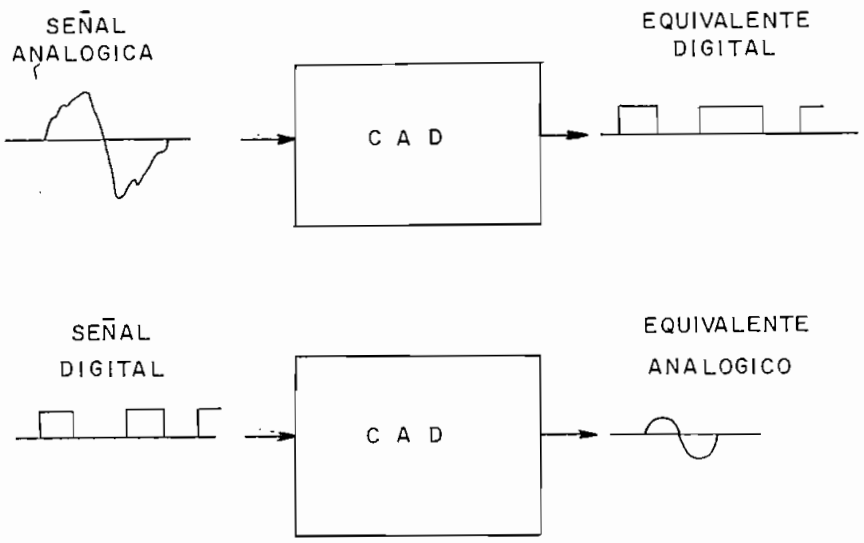


FIG. Nº 5

CANTIDADES ANALOGICAS.- Las señales analógicas que se utilizan como entrada generalmente son convertidas en voltajes o corrientes. Estas cantidades eléctricas aparecen como señales contínuas o alternas, moduladas o nó. Se obtienen por ejemplo de termocuplas, potenciómetros, computadores analógicos, etc.

Las señales analógicas que se obtienen de un CDA, sea como voltajes o corrientes, son analógicas puras.

CANTIDADES DIGITALES.- Las cantidades digitales están determinadas por la presencia o ausencia de niveles fijos de voltaje. Cada bit o unidad de información tiene uno de dos posibles estados: $^{1}_{L}$ (uno lógico), o $^{0}_{L}$ (cero lógico).

Una cantidad analógica puede ser representada, con precisión muy aceptable, con cantidades digitales. La precisión esta - directamente determinada por el número de bits que se utilizan para la representación.

2.1.D MEMORIA

La memoria digital consta de varios registros de desplazamiento, cada uno de los cuales puede almacenar hasta 1024 bits de datos en forma secuencial. Para su operación requiere de diferentes señales de comando.

2.1.E RELOJ Y SISTEMA DE CONTROL

La señal de reloj se obtiene de un oscilador de onda cuadrade. Esta sirve para obtener las señales de comando necesarias para que opere el sistema. Esto se esquematiza en la Figura Nº 6.

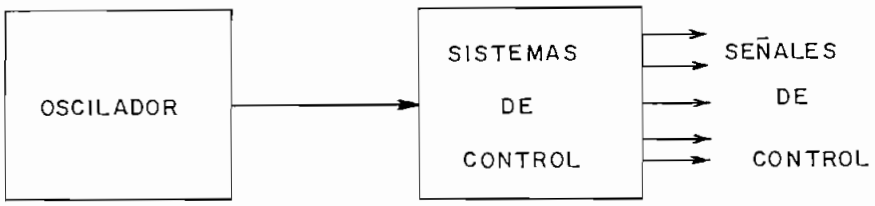


FIG. Nº 6

2.2. ANALISIS TECNICO DE LAS ETAPAS

2.2. A ETAPA DE ATENUACION

El sistema de atenuación debe diseñarse para una respuesta de frecuencia: DC-100KHz. Puede constar de una o varias etapas sin que esto modifique sus características. Debe presentar a la entrada una impedancia Z formada por una resistencia R_{eq} en paralelo con un condensador C_{eq} cuyos valores sean similares a los que presenta un osciloscopio. Consideremos el circuito de la Figura Nº 7.

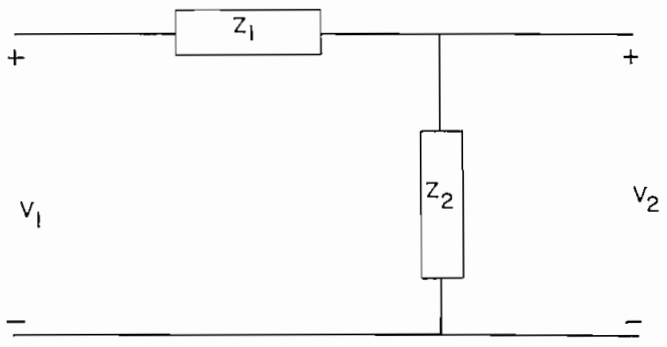


FIG. Nº 7

$$\frac{V_2}{V_1} = \frac{Z_2}{Z_1 + Z_2}$$

Si consideramos las impendancias formadas por una resistencia R en paralelo con un condensador C, como indica laFigura Nº 8.

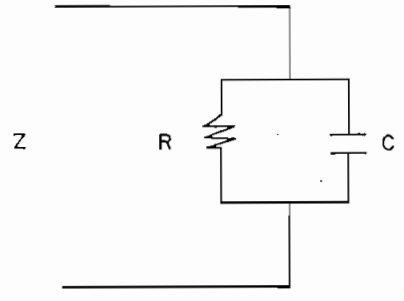


FIG. Nº 8

Tendremos que:

$$(2) \qquad Z = \frac{R}{1 + R\ S\ C}$$

en donde:

$$(3) \qquad S = j\omega = j\ 2\pi\ f$$

en la ecuación 1, reemplazando el valor de Z

$$(4) \qquad \frac{V_2}{V_1} = \frac{\dfrac{R_2}{1 + R_2\ S\ C2}}{\dfrac{R_1}{1 + R_1 SC_1} + \dfrac{R_2}{1 + R_2 SC_2}}$$

$$(5) \qquad \frac{V_2}{V_1} = \frac{R_2\ (\ 1 + R_1\ SC_1\ )}{R_1\ (\ 1 + R_2\ SC2) + R_2\ (\ 1 + R_1\ SC_1)}$$

Considerando el circuito de la Figura Nº 7, como unicamente resistivo, se tiene que:

$$(6) \qquad \frac{V_2}{V_1} = \frac{R_2}{R_1 + R_2}$$

y considerando, como circuito capacitivo:

$$(7) \qquad \frac{V_2}{V_1} = \frac{C_2}{C_1 + C_2}$$

Los capacitadores estan al mismo potencial que las resistencias:

$$\frac{R_2}{R_1 + R_2} = \frac{C_2}{C_1 + C_2}$$

$$(8) \qquad R_1 C_1 = R_2 C_2$$

Reemplazando en la ecuación Nº 5:

$$(9) \qquad \frac{V_2}{V_1} = \frac{R_2}{R_1 + R_2}$$

El circulo presentará características de transferencia independientes de la frecuencia, siempre que se cumpla la ecuación Nº 8.

En la práctica se puede construir un divisor de tensión resistivo. En el mismo existirán capacitancias parásitas, sean estas C_a, C_b, C_c. Como se indica en la figura Nº 9.

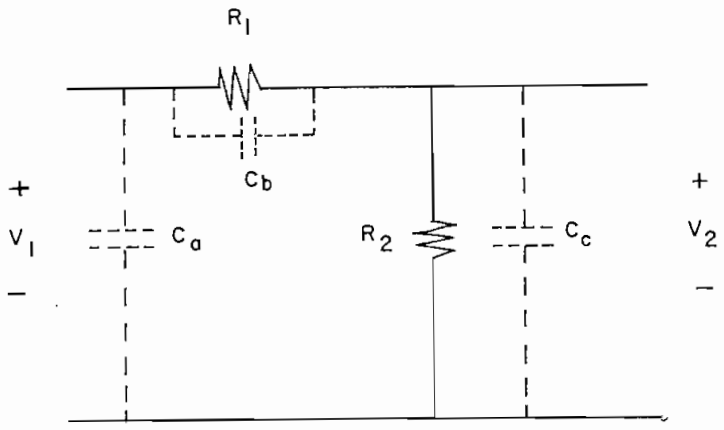


FIG. Nº 9

Si se colocan condensadores físicos C_1' y C_2' en paralelo con las capacitancias parásitas, el efecto capacitivo total será como se indica en las ecuaciones Nº 9 y 10.

(9) $$C_{T1} = C_1' + C_b$$

(10) $$C_{T2} = C_2' + C_c$$

Si en las ecuaciones 9 y 10 se cumple que:

(11) $$C_1' \gg C_b$$

(12) $$C_2' \gg C_c$$

Tendremos:

$$(13) \qquad C_{T1} = C_1'$$

$$(14) \qquad C_{T2} = C_2'$$

Se consigue disminuir notablemente el efecto de las capacitancias parásitas.

Sea:

$$(15) \qquad C_1 = C_{T1}$$

$$(16) \qquad C_2 = C_{T2}$$

Como se indica en la Figura Nº 10.

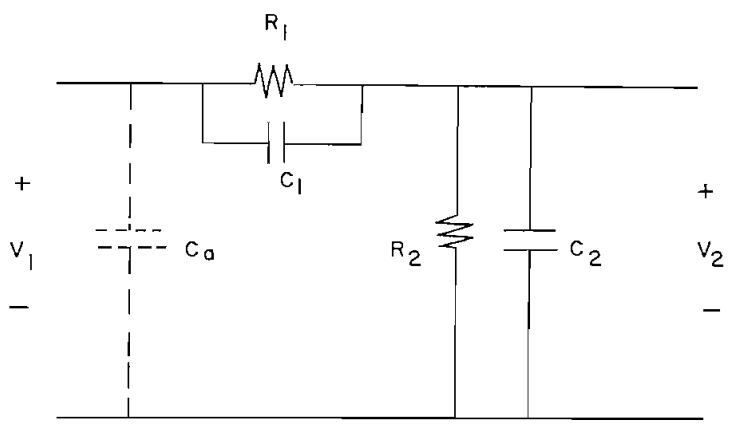


FIG. Nº 10

El valor de R_2 puede estar determinado por dos resistencias en paralelo, R_3 y R_4 como se indica en la Figura Nº 11. Al igualque $C_2 = C_3 // C_4$.

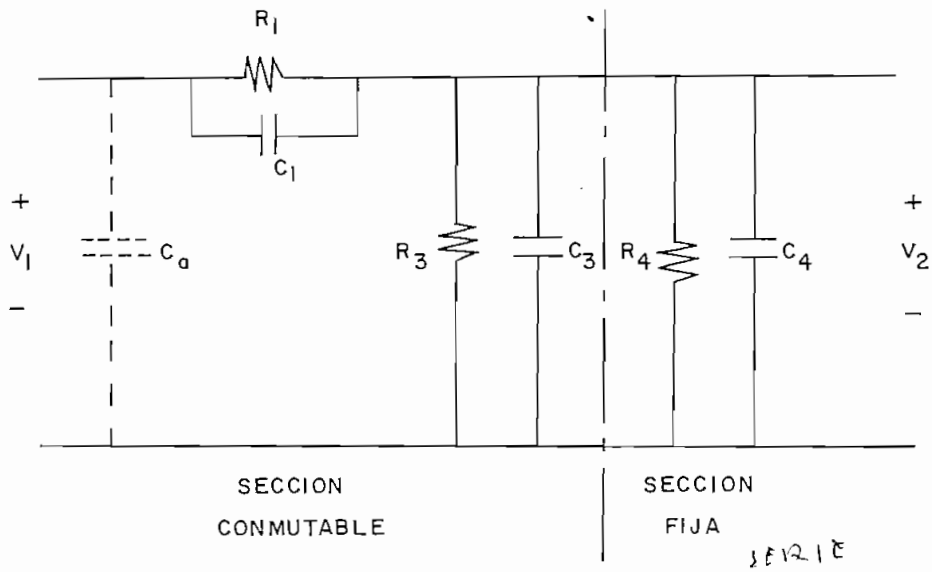


FIG. Nº II

$$(17) \qquad R_2 = \frac{R_3 R_4}{R_3 + R_4}$$

$$(18) \qquad C_2 = \frac{C_3 C_4}{C3 + C_4}$$

De este modo se consigue una sección de terminación fija y otra conmutable. Esto presenta algunas ventajas: Siempre se esta presentando une carga constante a la entrada. Pueden utilizarse varias etapas de atenuación en cascada, presentando a la entrada la misma impedancia a pesar de variar la atenuación.

La impedancia en los terminales de entrada (Zen) esta dada por la ecuación Nº 19.

$$(19) \qquad Zen = Z_1 + Z_2 = \frac{R_1}{1 + R_1 C_1 S} + \frac{R_2}{1 + R_2 C_2 S}$$

La misma debe ser similar a la que presenta un osciloscopio, una resistencia equivalente Req y una capacitancia equivalente Ceq en paralelo.

$$(20) \qquad Zen = \frac{Req.}{1 + Req\ Ceq\ S}$$

Igualando las ecuaciones 19 y 20, considerando la ecuación 8 se tiene:

$$(21) \qquad Req = R_1 + R_2$$

$$(22) \qquad Ceq = \frac{C_1 + C_2}{C_1 + C_2}$$

Como se indica en la Figura Nº 12.

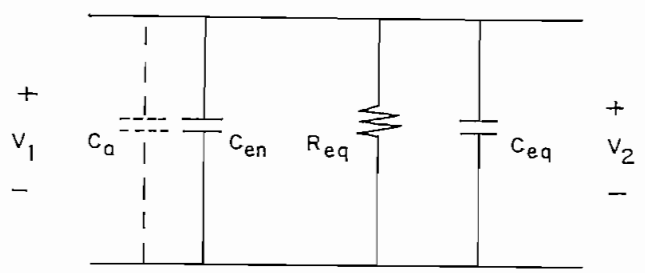


FIG. Nº 12

Con criterio similar, podemos colocar un condensador en paralelo a Ca, Sea este Cen cuyo valor sea:

$$(23) \qquad Cen \gg Ca$$

Entonces; Zen queda modificado a:

$$(24) \qquad Zen = \frac{Req}{1 + Req\ C'en\ S}$$

$$\therefore \quad C'en = \frac{Cen\ Ceq}{Cen + Ceq}$$

E T A P A D E C O N V E R S I O N A N A L O G I C O D I G I T A L

2.2.b C O N V E R S O R A/D

2.2.b.1 TEORIA DE CUANTIZACION.- El proceso de cuantización de una señal se ilustra con la función de transferencia de cuantización de la Figura Nº 13.

La cuantización es el proceso que permite convertir una señal analógica o cóntínua en una serie de niveles discretos. En el gráfico se presenta la señal analógica en el eje horizontal y los niveles discretos en el eje vertical. Los valores discretos

pueden identificarse con una serie de números, código binario por - ejemplo.

Los procesos de cuantización y codificación representan la operación básica de una conversión analógica - digital.

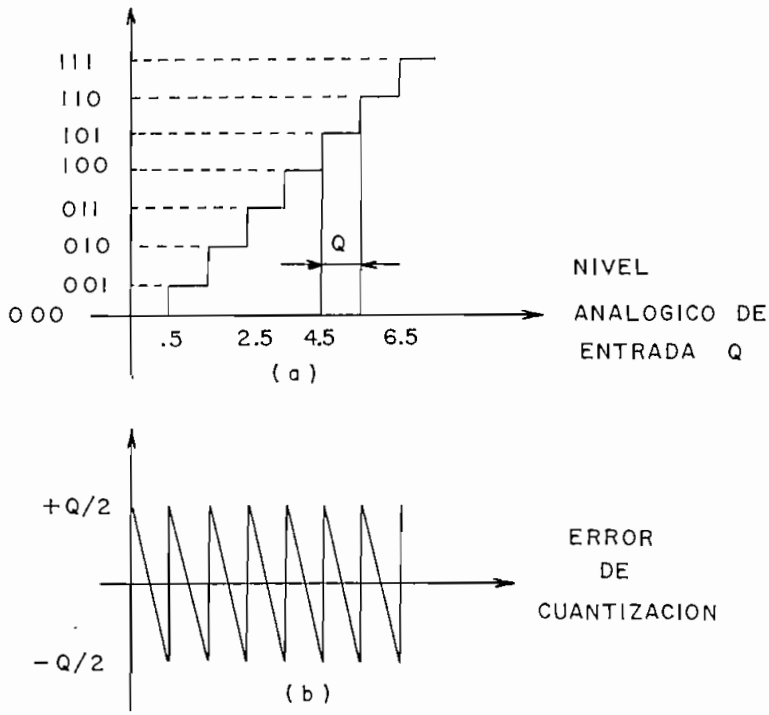


FIG. Nº 13

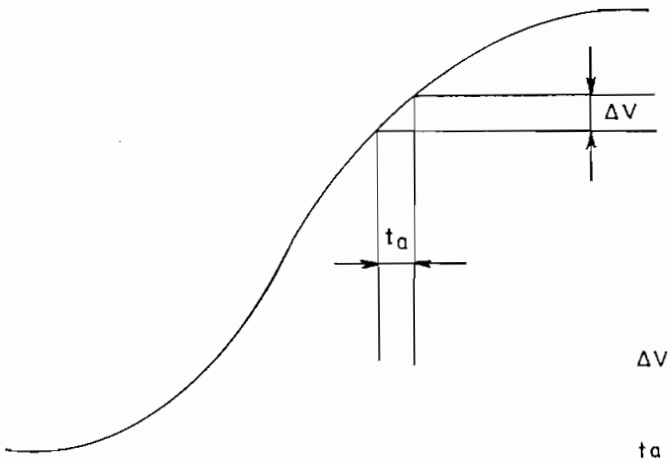
La función indicada es ideal con decisión para niveles -- analógicos: 0.5 , 1.5 , 2.5 , etc.

Los niveles de decisión son una serie de valores los mismos que determinan los niveles verdaderos. En otras palabras, una entrada analógica de valor unitario corresponderá a un nivel binario de 001. El nivel analógico 1 está entre los niveles de deci--

sión 0.5 y 1.5; luego una cantidad analógica cuyo valor sea 1 ± 0.5 será interpretada en forma digital como 001. Si se llama Q a la - distancia entre los niveles de decisión, tamaño de cuantización o tamaño del bit, un cuantizador con un código binario de salida -- tiene 2^n niveles de salida discretos con $2^n - 1$ niveles de decisión analógicas. Los niveles de decisión en el cuantizador no pueden - ser exactos pero deben tener su tolerancia alrededor de los mismos.

Si se varía la entrada del cuantizador en todo su rango - de valores y luego se sustraen los niveles discretos de salida, se tendrá una señal de error. Este error se denomina "error de cuantización", es un error inevitable en un proceso de cuantización y depende del número de niveles de cuantización o resolución del -- cuantizador. Al grafizar el error de cuantización se tiene una onda "diente de sierra" con un valor pico-pico igual a Q, como se - presenta en la Figura Nº 13b. El error de cuantización es cero -- únicamente a la mitad entre los niveles de decisión.

En conversores A/D los procesos de cuantización y codificación de la señal se realizan en un tiempo finito. Este depende tanto de la resolución del conversor como del método de conversión utilizado. La velocidad de conversión depende de la variación de la información en el tiempo y de la resolución que se requiere. El tiempo que se requiere para realizar la conversión generalmente se denomina "tiempo de apertura".



$$\Delta V = \frac{dV(t)}{dt}\, ta \qquad (25)$$

ta : TIEMPO DE APERTURA

ΔV : VARIACION DE AMPLITUD

FIG. Nº 14

Como se indica en la figura Nº 14 el tiempo de apertura y la variación de amplitud estan relacionados por las variaciones de la señal en el tiempo. Pare el caso particular de una onde sinusoidal la máxima relación de cambio ocurre en la intersección - con cero y la veriación de amplitud está dada por:

$$\Delta V = \frac{d}{dt}\,(V \operatorname{sen} \omega t)_{t=o} \rightarrow ta = V\omega\, ta$$

De donde:

$$\frac{\Delta V}{V} = \omega ta = 2\pi f\, ta$$

El tiempo de conversión que se requiere para codificar - una señal de 10 KHz con 8 bits de resolución, esto es una resolución de une parte de 2^8, (un 0.4%), utilizando la ecuación anterior se tiene:

$$t_a = \frac{\Delta V}{V} \frac{1}{2\pi f} = \frac{.004}{6.28\ 10^4} = 63.7\ 10^{-9}$$

Se requiere un tiempo de conversión de 63.7 nanosegundos - para mantener con un bit de resolución la relación del cambio de - la señal. Para convertir señales que no varían rápidamente, con - niveles moderados de resolución se requieren conversores relativa mente rápidos. Si sa utilizan circuitos de Muestreo — retención se puede aceptar un tiempo de conversión mayor, tomando rápidamente una muestra de la señal y reteníendo su valor durante la conversión.

2.2.b.2 T E O R I A D E M U E S T R E O

Una señal se muestrea sin perder información si la fre-- cuencia de muestreo es por lo menos dos veces la máxima frecuen-- cia de las componentes de la información, considerando el teorema de muestreo: " Si una señal contínua de ancho de bande limitado - no contiene componentes de frecuencia mayores que f_m. Entonces la señal original puede ser completamente recuperada, sin distorción, si es muestreada en no menos de f_m muestras por segundo".

El teorema de muestreo puede demostrarse con ayuda del teo rema de convolución en frecuencia. Sea la señal $f_x(t)$ de banda li

mitada que no presenta componentes espectrales mayores que fm ciclos por segundo. Esto significa que $F_{(w)}$, la transformada de Fourier de $f_{(t)}$ es cero para $|w| > w_m$, $(w_m = 2\pi f_m)$. Si se multiplica la función $f_{(t)}$ por una función periódica de impulsos $\delta_T(t)$. El producto es una secuencia de impulsos localizados a intervalos regulares de T segundos y con amplitudes iguales al valor de f (t) en el instante correspondiente. El producto $F(t)\ \delta_T(t)$ representa a la función f(t) muestreada a intervalos uniformes de T segundos. Si llamamos fs(t) la función muestreada de f(t), tendremos:

$$f_s(t) = f(t)\ \delta_T(t) \qquad (26)$$

Sea F(w) el espectro de frecuencia de f(t), la transformada de Fourier para una función periódica de impulsos $\delta_T(t)$ es también una función periódica de impulsos $\omega_o \delta_{\omega o}(\omega)$. Los impulsos están separados a intervalos: $\omega_o = 2\pi/T$.

$$\delta_T(t) \longleftrightarrow \omega_o \delta_{\omega o}(\omega) \qquad (27)$$

La transformada de Fourier de f(t) $\delta_T(t)$, según el teorema de convolución en frecuencia, está dado por la convolución de F(w) con $\omega_o\ \delta_{\omega_o}(\omega)$.

$$f_s(t) \longleftrightarrow \frac{1}{2\pi}\left[F(\omega) * \omega_o\ \delta_{\omega_o}(\omega)\right] \qquad (28)$$

Sustituyendo $\omega_o = \frac{2\pi}{T}$

$$f_s(t) \longleftrightarrow \frac{1}{T}\left[F(\omega) * \delta_{\omega_o}(\omega)\right] \qquad (29)$$

Se demuestra que el espectro de la señal muestreada fs(t) está dado por la convolución de F(w) con un tren de impulsos. Esto se presenta gráficamente en la figura Nº 15.

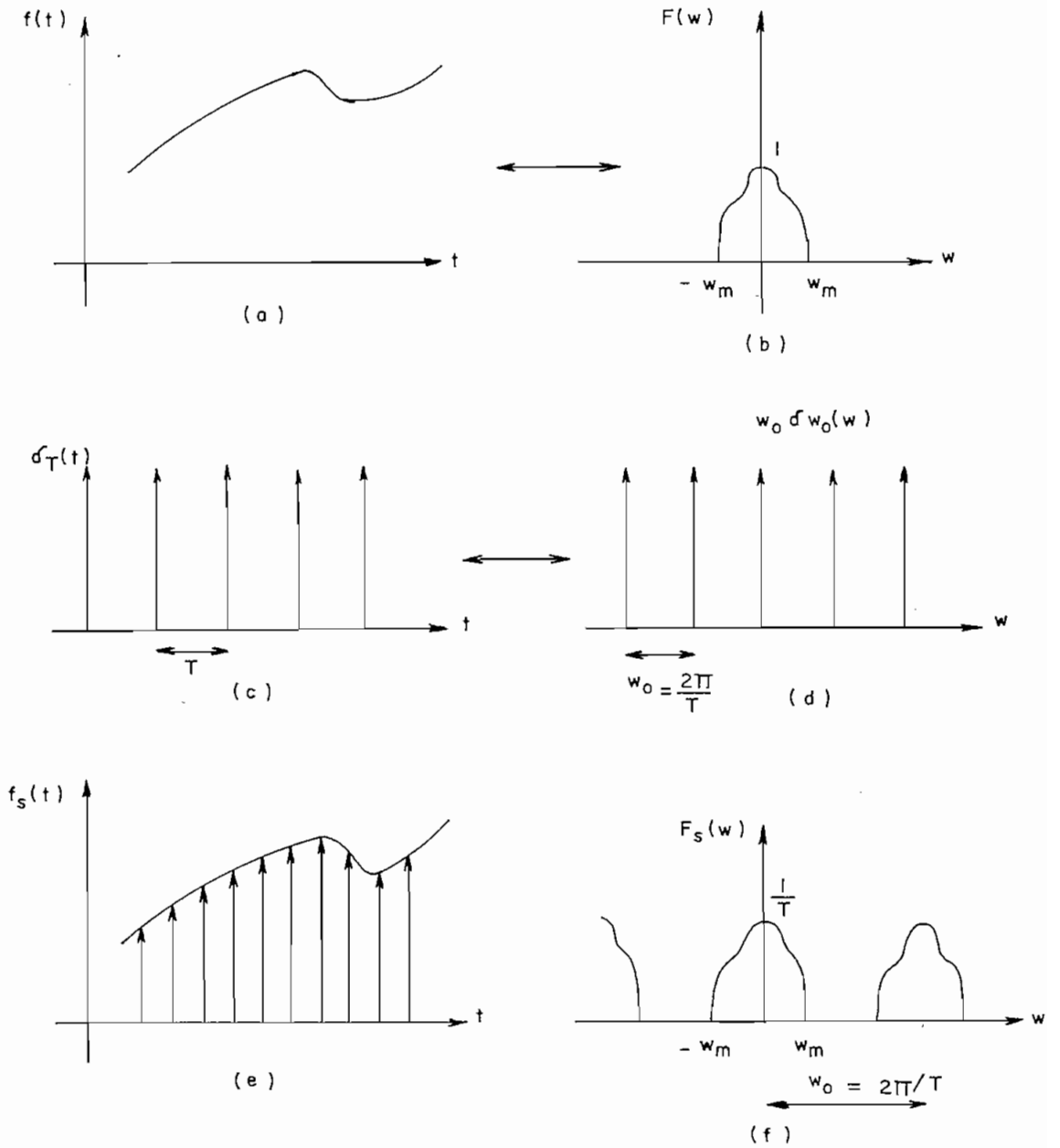


FIG. Nº 15

Como se observa en la parte (f) de la figura, F(w) se repite periódicamente sin que existen superposiciones siempre que:

esto es que: $\frac{2\pi}{T} \geq 2(2\pi f_m)$ (30)

$$\therefore \quad T \leq \frac{1}{2 f_m}$$

Que comprueba el teorema de muestreo.

El proceso de muestreo se presenta en la figura Nº16, en la misma se presente la señal analógica y un tren de pulsos periódicos de muestreo.

Los pulsos representan un conmutador rápido que conecta - la señal analógica por un instante y el resto del período permanece abierto. La señal modulada resultante se presenta en la parte (c).

Si el conmutador de muestreo se reemplaza por un conmutador y un capacitor, la señal se muestrea y se retiene hasta el -- próximo pulso de muestreo, obteniéndose una figura como la indicada en la parte (d) de la figura Nº 16. Este tipo de muestreador - se denomina de Muestreo - retención.

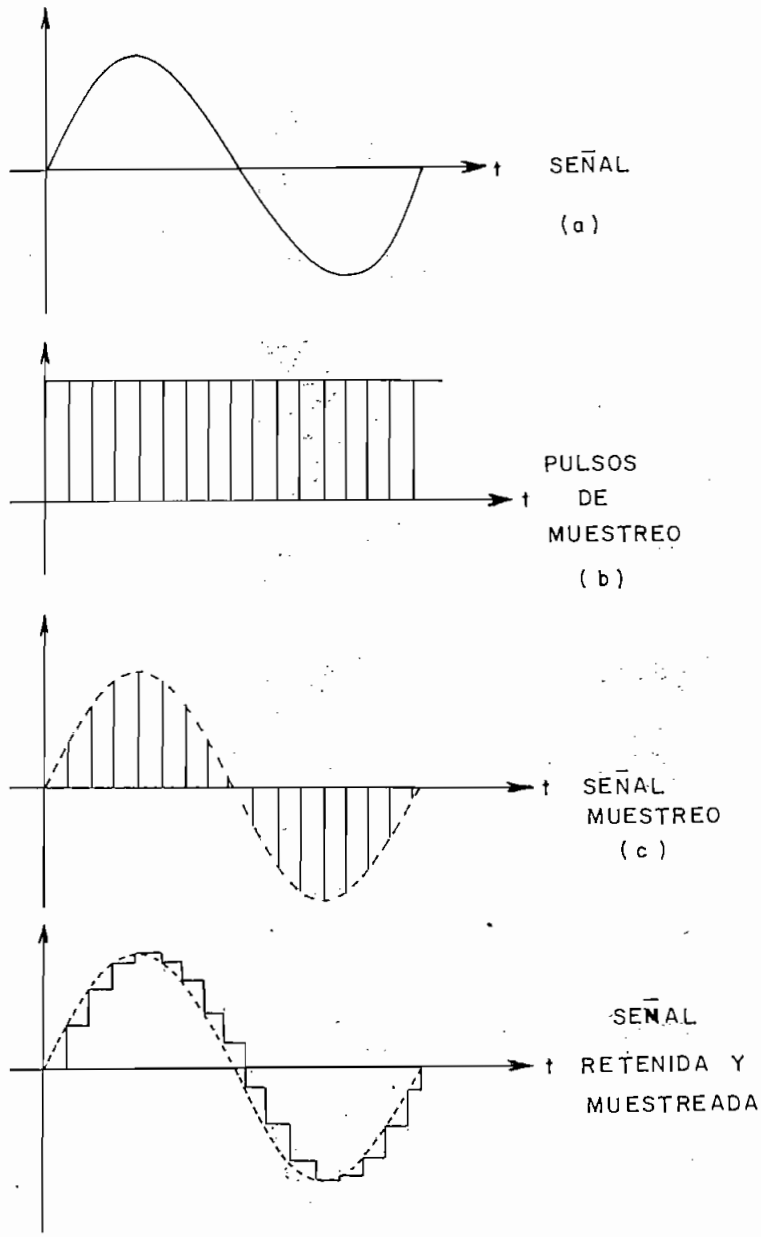

t
SEÑAL
(a)
PULSOS
DE
MUESTREO
t
(b)
t
SEÑAL
MUESTREO
(c)
SEÑAL
RETENIDA Y
MUESTREADA
t

FIG. Nº 16

El teorema de muestreo puede ser ilustrado con el epectro de ? frecuencia que se presenta en la figura Nº 17. La parte (a)- presenta el espectro de una señal contínua con componentes de frecuencia menores que fm. Al muestrear esta sañal a una frecuencia de muestreo fs, se obtiene un espectro de la señal como se indica en la parte (b). Si la frecuencia de muestreo no es lo suficientemente mayor que la frecuencia de la señal, aparecen algunas componentes de mayor frecuencia. Este afecto se denomina "frecuencia - fantasma".

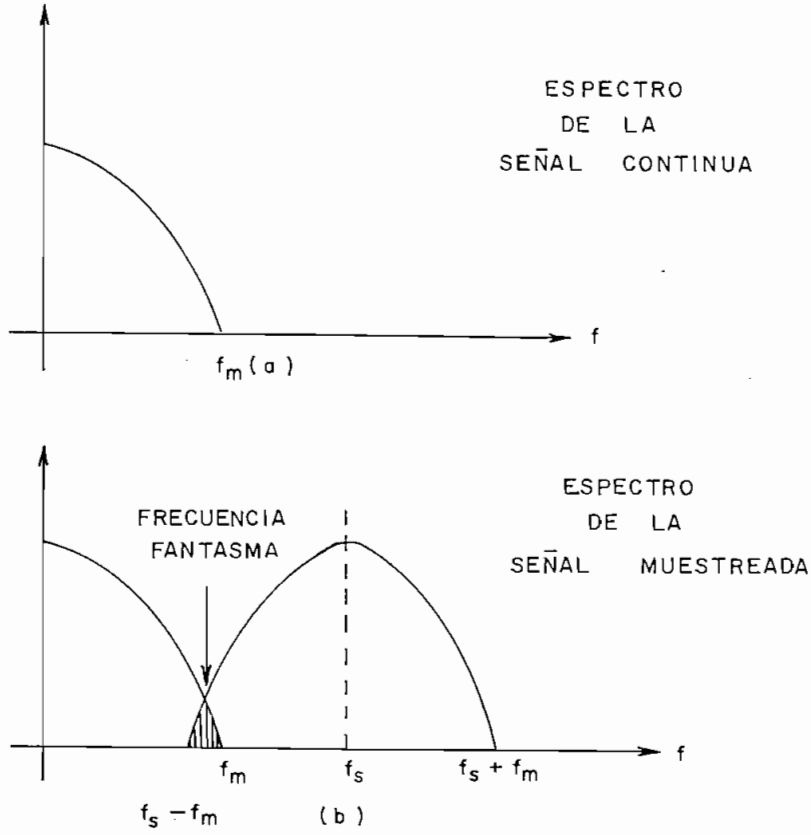


FIG. Nº 17

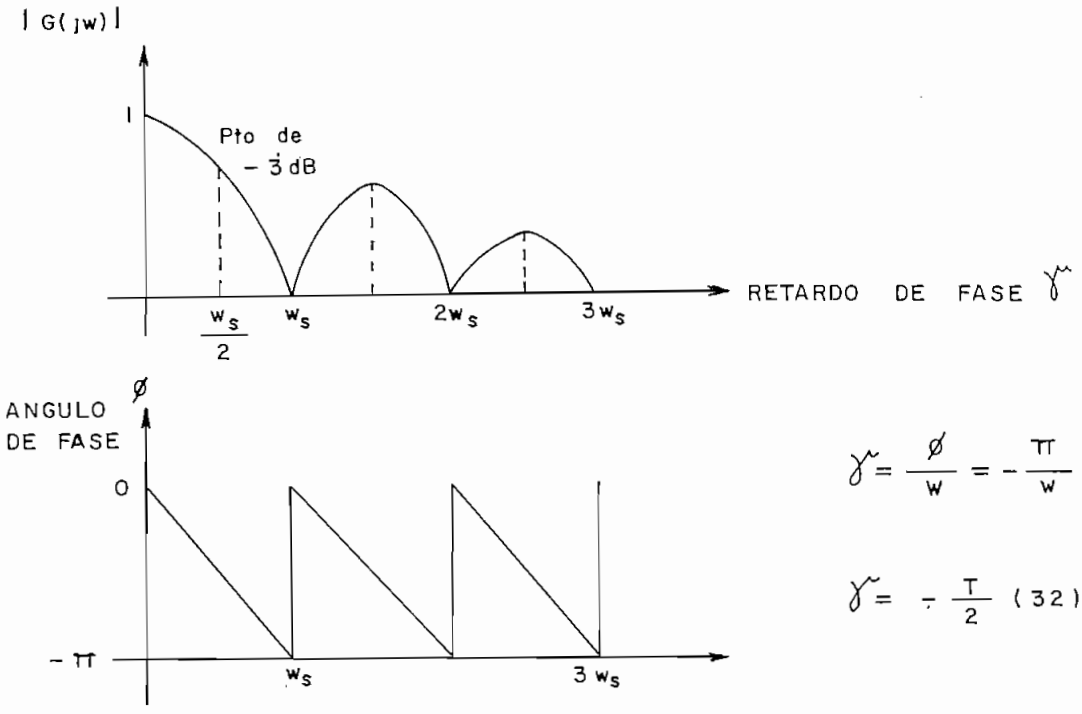
Al recobrar la señal original, los componentes de frecuencia fantasma causan distorsión y no pueden ser distinguidas o separadas de la información.

Las frecuencias fantasmas son eliminadas si la frecuencia de muestreo se hace mayor o pasando la señal original por filtros pasa-bajos.

Un circuito ideal de muestreo-retención toma una muestra en un tiempo igual a cero y es capaz de retener su valor por un tiempo infinito con mucha exactitud. Dispositivos reales toman una muestra en períodos de tiempo muy cortos comparados con el tiempo que retienen la misma. El efecto de este proceso con señales analógicas contínuas puede determinarse al encontrar la función de transferencia del circuito de muestreo-retención. Utilizando la transformada de Laplace se ancuentra que la función de transferencia es:

$$G(j\omega) = \frac{1 - e^{-j\omega T}}{j\omega} = \frac{2\pi}{\omega_s} \frac{\operatorname{sen} \pi\omega/\omega_s}{\pi\omega/\omega_s} e^{-j\pi\left(\frac{\omega}{\omega_s}\right)} \qquad (31)$$

En donde T es el período de muestreo y ws = 2π,fs la frecuencia de muestreo. Al grafizar se obtienen las representaciones de la Figura Nº 18. Puede observarse que un circuito muestreo-retención actúa como un filtro pasa-bajos con una frecuencia de corte igual a fs/2 y un retardo de fase T/2ó un semiperíodo de muestreo.



$$\gamma = \frac{\phi}{w} = -\frac{\pi}{w}$$

$$\gamma = -\frac{T}{2} \quad (32)$$

FIG. Nº 18

MUESTREADOR

Si se aplica una onda sinusoidal a un muestreador, se obtendrá una señal como la indicada en la figura Nº 19.

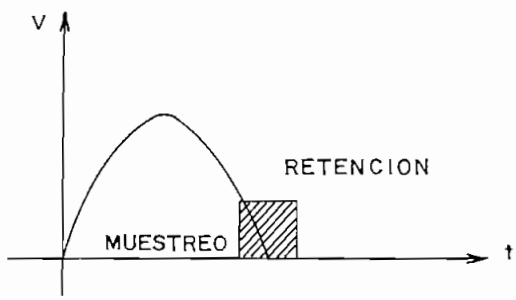


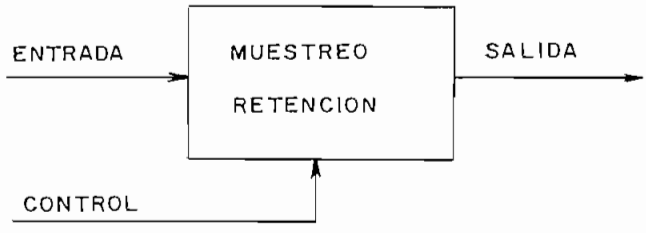
FIG. Nº 19

El muestreador entrega al conversor A/D un voltaje de igual al valor instantáneo de la información pocos nsegundos después de que la señal de comando ha sido dada. Esta señal es liberada automáticamente después que se ha realizado el proceso de conversión, continuandose el muestreo de la información.

El muestreador es un dispositivo que posee una señal de entrada, una de salida y otra de control. Tiene dos estados de operación: Muestreo (sample en inglés) durante el cual adquiere la señal de entrada tan rápidamente como sea posible y sigue la señal hasta que llega el comando de retensión (hold en inglés), tiempo al cual retiene el último valor adquirido de la señal de entrada.

Generalmente tiene ganancia unitaria sin inversión,

Las señales de control son operadas con niveles lógicos standard y tienen compatibilidad con la técnica TTL. Un nivel lógicoíes generalmente utilizado para muestreo y un nivel lógico -- "0" para el comando de retensión como se aprecia en la figura -- Nº 20.



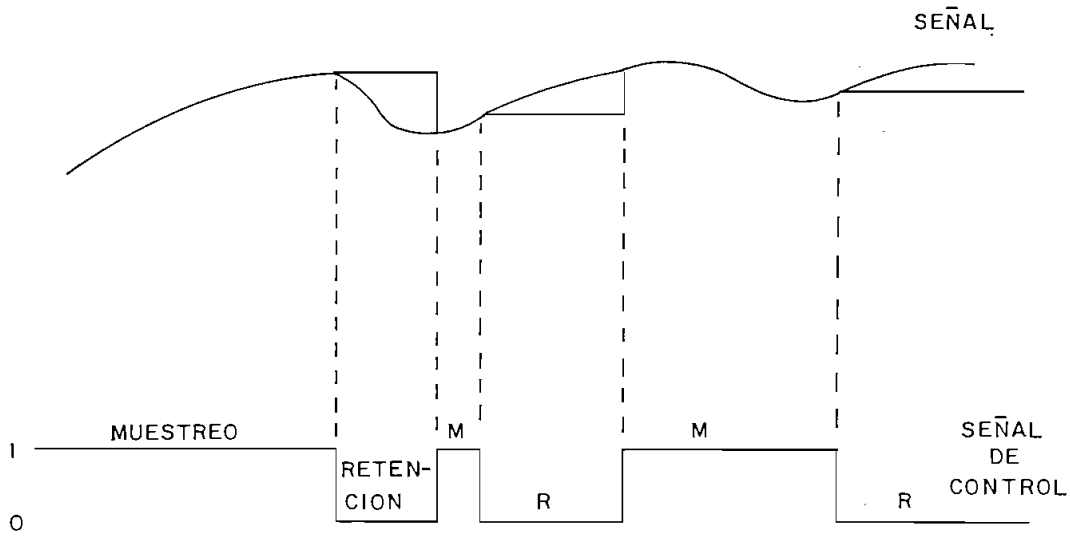


FIG. Nº 20

El gráfico se refiere a un dispositivo ideal, sin errores en el muestreo y con conmutaciones instantáneas, además de un tiempo infinito de espera. Las unidades que comercialmente pueden obtenerse especifican términos para diferenciar de un dispositivo -- ideal. Es necesario conocer estos términos antes de profundizar - su estudio. Por el momento nos preocuparemos de las principales características que suceden durante sus cuatro estados: Muestreo, - transición de muestreo a retención, retención y transición de retención a muestreo.

2.2.b.3 D U R A N T E E L M U E S T R E O

(Figura Nº 21).

OFFSET.- Señal que debe ponerse a la entrada para que la salida sea igual a cero.

NONLINEARITY.- (Nolinealidad) Cantidad en que la señal de salida difiere de la de entrada.

SCALE FACTOR ERROR.- (Error de Factor de Escala) Valor en el cual difiere la salida considerando una ganancia específica (generalmente unitaria).

SETTLING TIME.- (Tiempo de respuesta) Tiempo que requiere la salida para alcanzar el valor final, cuando a la entrada se ha aplicado una función paso a escala completa.

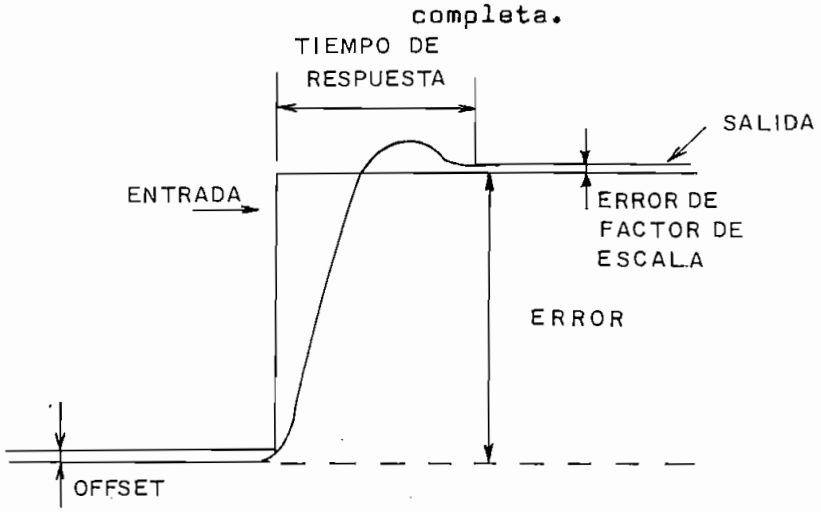


FIG. Nº 21

En este estado, el dispositivo se comporta como un seguidor de voltaje con ganancia unitaria.

2.2.b.4 TRANSICION DE MUESTREO A RETENCION
(Figura Nº 22)

APERTURE TIME.- (Tiempo de apertura) El tiempo comprendido entre la señal de comando y el comando mismo.

SAMPLE - TO - HOLD OFFSET.- (Error de Transición) Error que ocurre a la iniciación de una señal de espera causado por una descarga del condensador de almacenamiento através de la capacitancia entre el circuito de control y el lado del condensador hacia el switch. Esto no ocurre en unidades que tienen una señalización digital.

SETTLING TIME.- (Tiempo de respuesta) El intervalo requerido por la salida para alcanzar el valor final.

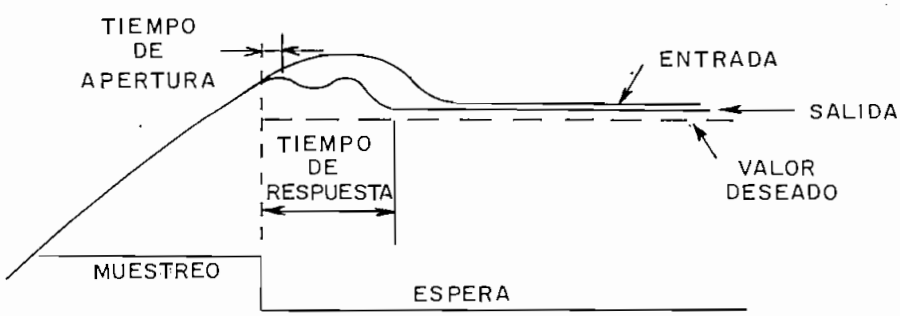


FIG. Nº 22

2.2.b.5 DURANTE LA RETENCION
(Figura Nº 23)

DROOP.- (Decaimiento) Un desplazamiento de la salida en una relación aproximadamente constante, debido a la corriente que circula atravéz del condensador de almacenamiento. Puede ser positivo o negativo.

FEEDTHROUGH.- (Factor de transferencia en retención) Fracción de la señal de entrada que aparece a la salida durante la espera, causado especialmente por la capacitancia entre los terminales del conmutador. Generalmente se mide aplicando una señal sinusoidal a escala completa en la entrada, y observando su salida.

DIELECTRIC ABSORPTION.- (Absorción dieléctrica) Tendencia de las cargas en el capacitor para redistribuirse en un período de tiempo, por lo cual resulta un "crecimiento" a un nuevo nivel que a la postre puede producir rápidas variaciones.

La impedancia de salida de un dispositivo Muestreo-Retención debe ser baja y de rápida recuperación para minimizar las transiciones causadas por cargas dinámicas, tales como entradas de dispositicos A/D.

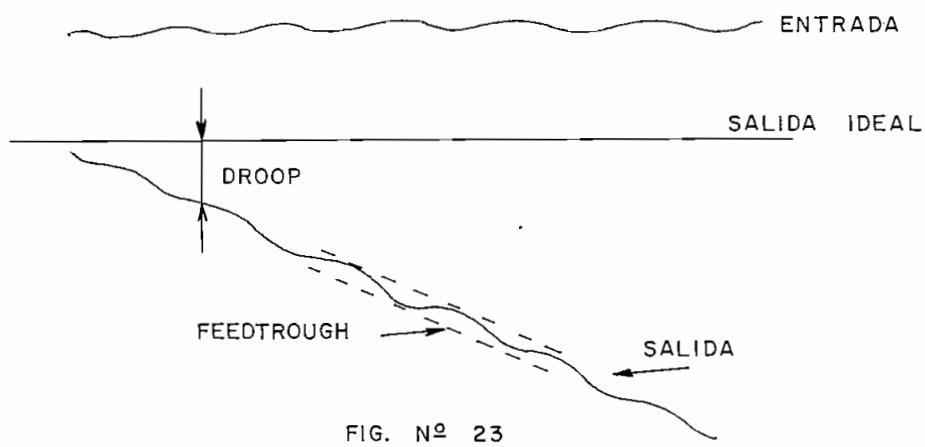


FIG. Nº 23

2.2.b.6 TRANSICION DE ESPERA A RETENCION
(Figura Nº 24)

ACQUISITION TIME.- (Tiempo de adquisición) Tiempo necesario que la señal requiere ser aplicada para un muestreo con la exactitud deseada.

HOLD-TO-SAMPLE TRANSIENTS.- (Transición de retención a muestreo) Voltajes transitorios que ocurren entre el comando de muestreo y la señal final. Resulta sumamente importante en algunas aplicaciones en las cuales los impulsos resultan ser comparables.

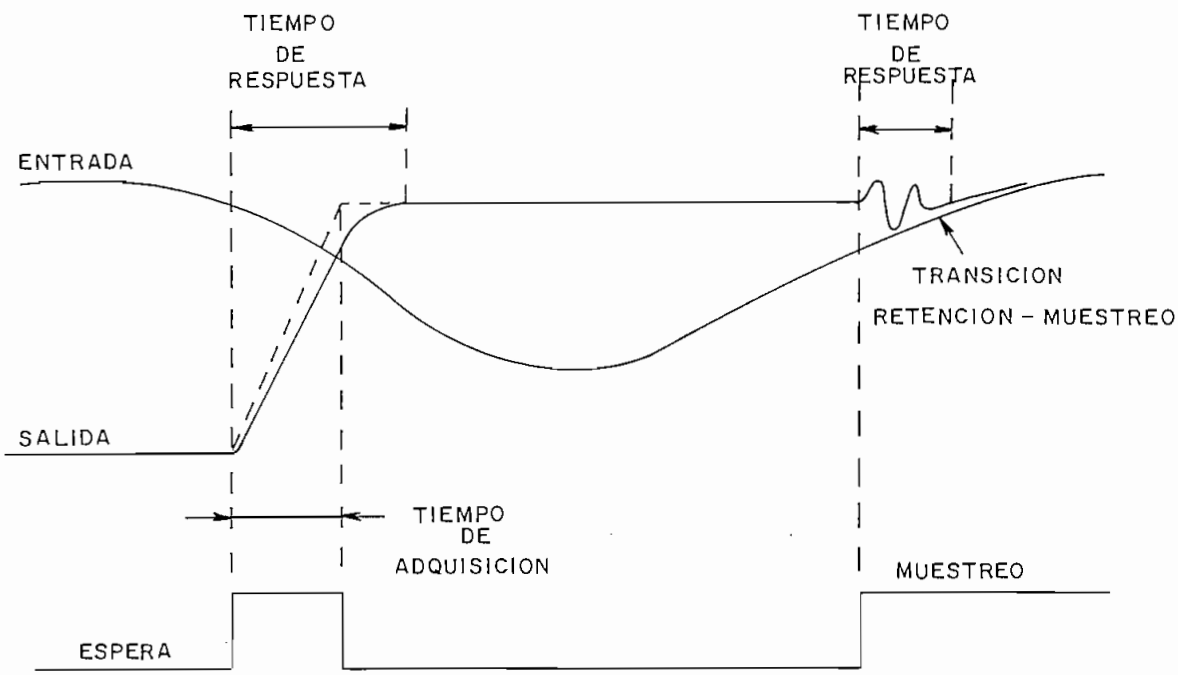


FIG. Nº 24

A L G U N O S C I R C U I T O S T I P I C O S

El tipo de elemento de almacenamiento divide en dos categorías a los circuitos S/H. El más convencional, popular y de muy - bajo costo emplea un condensador para almacenamiento (almacenamiento analógico). El otro método utiliza un conversor A/D y registros para almacenamiento, obteniéndose la salida através de un conversor D/A, que de cualquier manera resulta mucho más complejo y cos

toso. Se utiliza unicamente cuando se necesita mucha precisión, además presenta un tiempo muy grande de espera.

2.2.b.7 SEGUIDOR DE LAZO ABIERTO

Es el circuito básico que se presenta en la figura Nº 25. Cuando el conmutador está cerrado el capacitor se carga exponencialmente al voltaje de entrada, y la salida del amplificador "sigue" al voltaje del condensador. Cuando se abre el conmutador, la carga permanece en el condensador.

El tiempo de adquisición del capacitor depende de la resistencia en serie y también de la corriente disponible para cargar esa capacitancia. Una vez que se ha cargado el conmutador debe abrirse, sin que esto afecte al valor final. El tiempo que debe permanecer cerrado el conmutador, para mantener un margen de error de 0.1%, es 7RC.

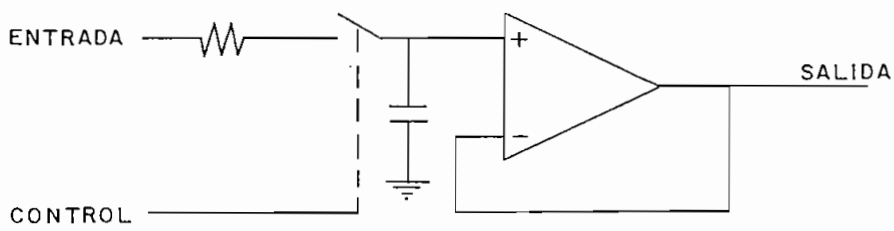


FIG. Nº 25

Un dispositivo muy utilizado como conmutador es un FET, y el amplificador con entrada tipo FET. Este circuito tiene la desventaja que el capacitor se carga desde la entrada, lo cual puede producir una oscilación a la vez que la corriente no es suficiente para cargar al condensador con la rapidez deseada. Esto se soluciona si utilizamos un seguidor de voltaje, tal como se indica en la figura Nº 26.

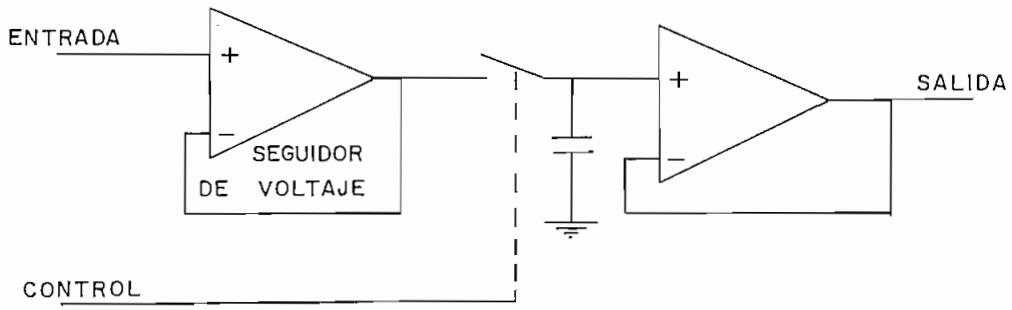


FIG. Nº 26

Cuando se desean respuestas muy rápidas en este circuito, a la vez que aceptables, puede utilizarse un puente de diodos como se indica en la figura Nº 27. La fuente de corriente está controlada por un mando para cargar el capacitor. Si el puente y la fuente de corriente son convenientemente balanceadas, la corriente fluíra hasta el capacitor miéntras el voltaje en el mismo no -

sea igual al de la entrada.

Durante el muestreo este circuito presenta mayor offset,- esto depende del balanceo que existe en los diodos del puente. Las características de los mismos deberían ser idénticas para minimizar este efecto. El error de transición en el paso de muestreo a retención es menor.

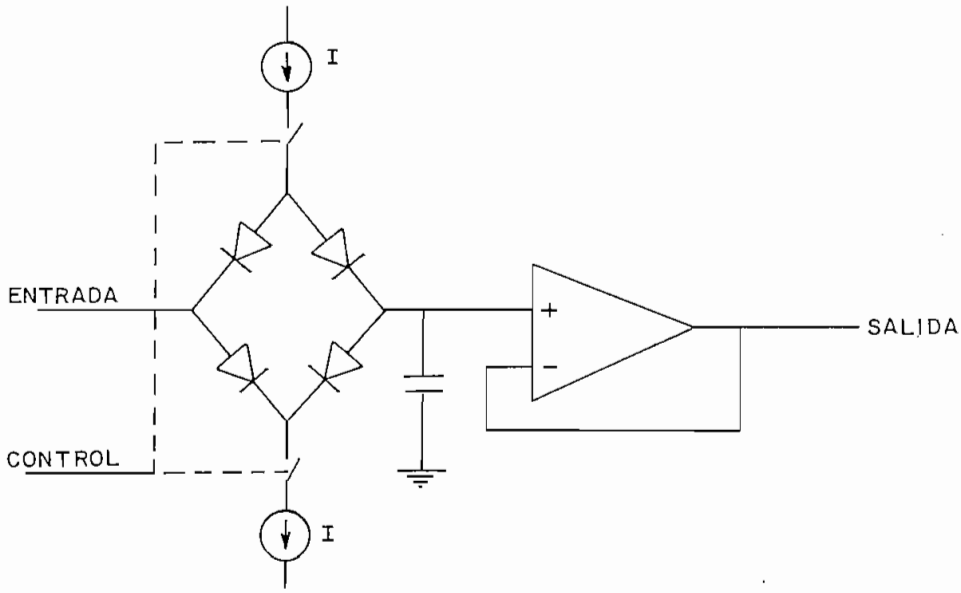


FIG. Nº 27

2.2.b.8 CIRCUITOS CON REALIMENTACION

Los circuitos anteriormente presentados tienen la gran ventaja de su rápida respuesta, pero son circuitos de lazo abierto.- En señales de baja frecuencia la exactitud en el muestreo es más importante que la velocidad de respuesta. En la figura Nº 28 se - tiene un circuito en el cual el seguidor de voltaje se ha susti--

tuído por un amplificador de diferencia de alta ganancia. Al cerrar el conmutador, la salida (que representa la carga en el capacitor) es forzada a muestrear la entrada, además se tiene la corriente de exitación que entrega el amplificador de entrada.

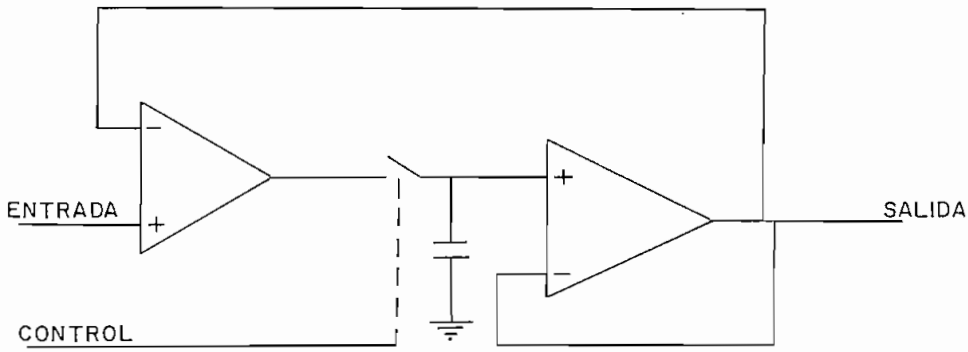


FIG. Nº 28

Los errores de modo común y de desviación (offset) en la salida del seguidor son automáticamente compensados al ajustarse la carga en el capacitor. Cuando el conmutador está abierto la salida retiene el valor final.

En la figura Nº 29 se utiliza un integrador, permitiendo así al conmutador operar con un potencial a tierra, simplificando los probles de fuga.

En los circuitos de las figuras Nos. 28 y 29 debido a que

la carga en el capacitor es controlada tanto por la salida como - por la entrada los tiempos de adquisición y de respuesta son idén ticos.

Si el circuito de la figura Nº 28 se cambia a retención - antes de que la salida alcance el valor de la entrada, el muestreo se realizará con error.

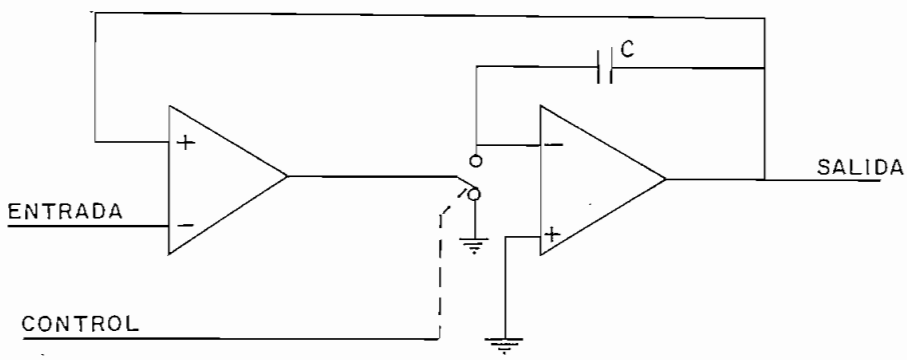
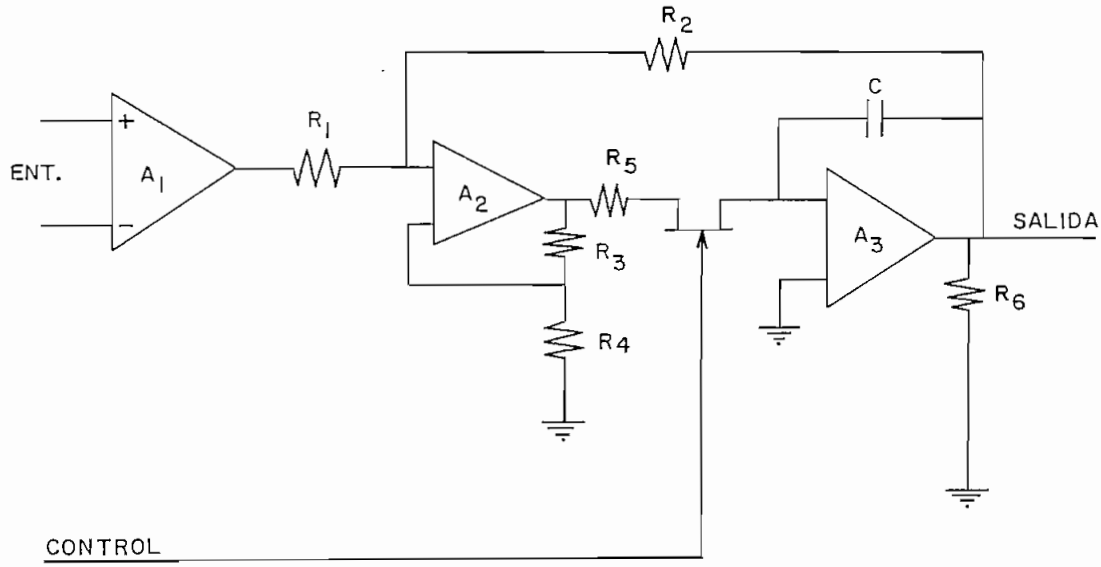


FIG. Nº 29

Un diagrama más completo se presenta en la figura Nº 30 - en el mismo se utiliza un FET como elemento de conmutación ya que este elemento presenta buenas características para esta operación.



A_1 : AMPLIFICADOR DE ENTRADA

A_2 : AMPLIFICADOR DE EXITACION

A_3 : AMPLIFICADOR DE MUESTREO

FIG. Nº 30

Durante el muestreo, el FET debe estar cerrado y la carga del condensador sigue a la señal de entrada. Cuando llega un comando para cambio de condición (muestreo a retención) el FET se abre y el voltaje del condensador permanece con el voltaje instantáneo que hubo a la entrada. Al terminarse el período de conversión el FET se cerrará y continuará el proceso.

La rapidéz de este método está determinado por el amplificador de exitación. El lazo de realimentación con los dos amplifi

cadores debe ser seleccionado de modo que se tenga ganancia unitaria.

Cuando se requieren circuitos muestreadores de alta velocidad, debe seleccionarse un conmutador analógico con control digital, pues su técnica ofrece resultados más garantizados.

Un conmutador teóricamente no presenta resistencia en su estado de conducción, en la práctica tiene su resistencia intrínsica que le llamaremos $R_{DS(ON)}$. Será de mejores carácteristicas aquel que presente una variación lineal de esta resistencia.

De las tecnologías utilizadas para la construcción de los conmutadores CMOS, PMOS, JFET, es esta última la que presenta características más lineales.

En cuanto a circuitos muestreadores con conmutadores analógicos con control digital existen diferentes, mencionaremos algunos:

a) Circuito muestreador, con inversión.

b) Circuito compensado con inversión.

c) Circuito muestreador sin inversión.

d) Circuito muestreador compensado con inversión.

2.2.b.9 CIRCUITO MUESTREADOR CON INVERSION

Presenta algunas ventajas con respecto a los otros circuitos. Opera con voltajes constantes por lo cual se reduce considerablemente la inestabilidad en el tiempo de apertura, por su configuración reduce notablemente las sobretensiones. La desventaja de este circuito radica en cuanto necesita más elementos externos para su funcionamiento aceptable. Este circuito se presenta en la Figura Nº 31

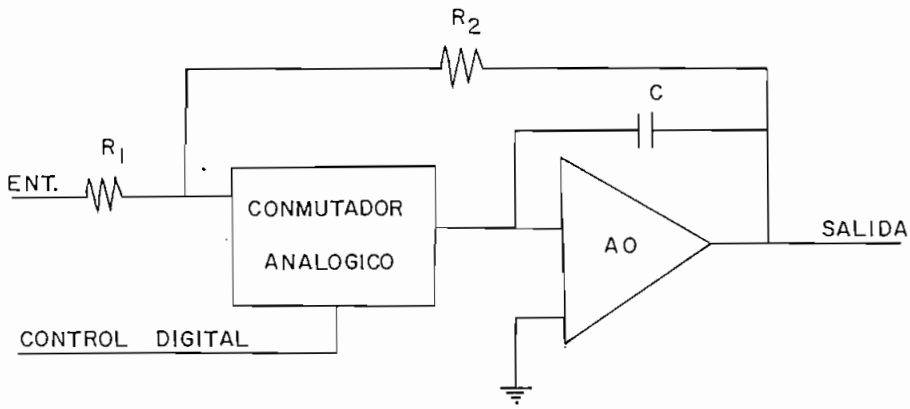


FIG. Nº 31

2.2.b.10 CIRCUITO MUESTREADOR COMPENSADO CON INVERSION

Cuando existen errores en la transferencia de carga de modo que estos llegan a interferir notoriamente, puede optarse por -

diferentes métodos de modo que se disminuya su efecto. Un método inicial consiste en incrementar el valor del condensador de carga, pero esto implica una pérdida de exactitud y velocidad. Un segundo método consiste en disminuir la complejidad del conmutador, lo -- cual hace que se incremente la resistencia en estado de conducción $R_{DS(ON)}$. Este método también involucra la relación exactitud-velocidad.

Un tercer método, más práctico, consiste en compensar la transferencia de carga. Entre estos circuitos existen algunos que simplemente al variar un capacitor se logra el efecto deseado.

Este circuito se muestra en la Figura Nº 32.

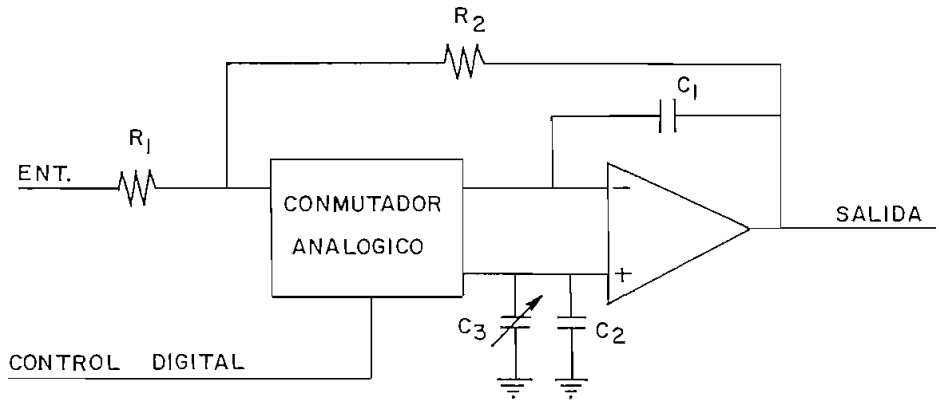


FIG. Nº 32

2.2.b.11 CIRCUITO MUESTREADOR SIN INVERSION

Para circuitos mucho más rápidos, puede emplearse una mejor combinación de velocidad y exactitud en la transferencia de la carga. Un circuito de estos se muestra en la Figura Nº 33.

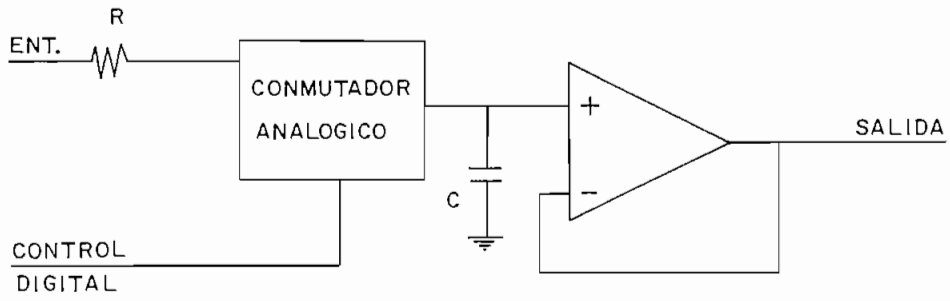


FIG. Nº 33

La desventaja de este circuito radica en que puede ser afectado por sobre-tensiones. Sus características son notables cuando se consigue una impedancia de la etapa anterior muy baja, y si el amplificador operacional es capáz de seguir la carga del condensador en óptimas condiciones.

2.2.b.12 CIRCUITO MUESTREADOR COMPENSADO SIN INVERSION

Es una sofisticación del circuito muestreador con inversión que se vió anteriormente. Dado que la transferencia de carga se incrementa proporcionalmente con el aumento de la impedancia de la etapa excitadora, es posible eliminar el condensador variable y hacer los ajustes necesarios con un potenciómetro, como se presenta en la figura Nº 34.

Este ajuste requiere esencialmente una etapa de excitación de impedancia muy baja.

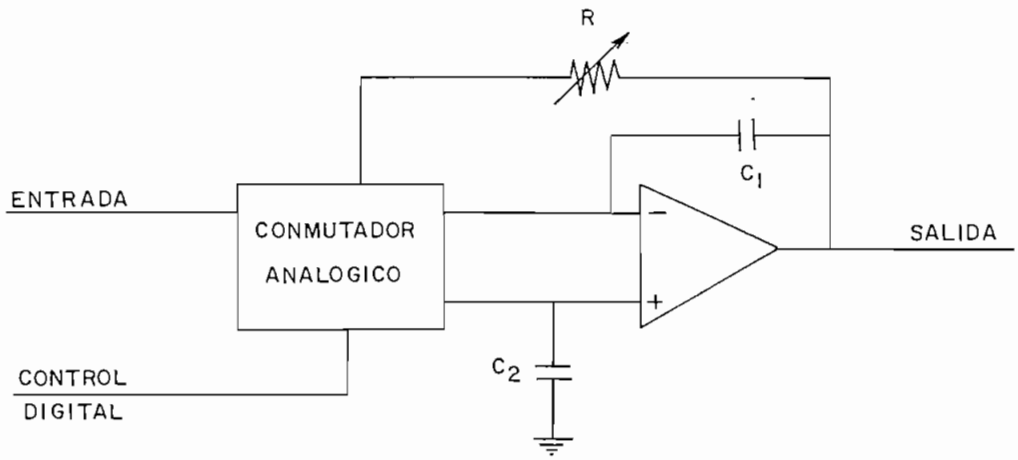


FIG. Nº 34

La señal de offset se ajusta a cero con una señal analógica de cera a la entrada.

En general para circuitos muestreadores mucha más rápidos se utiliza la técnica sin inversión, la transferencia de carga debe ser ajustada a cero a un voltaje solamente. La compensación en circuitos muestreadores con inversión prove mejores características offset en función de una disminución de velocidad. Los conmutadores analógicos JFET proveen mejor combinación de baja resistencia en conducción ($R_{DS(ON)}$) con la velocidad y baja transferencia de carga con exactitud.

2.2.c C O N V E R S O R E S

Existen diferentes tipos de conversores A/D siendo los más utilizados:

a.- Aproximaciones sucesivas.

b.- Integración.

c.- Contadores.

d.- Paralelo.

Cada tipo presenta sus características lo cual determina las posibles aplicaciones, considerando su velocidad, exactitud,-

versatilidad y costo.

2.2.c.1 APROXIMACIONES SUCESIVAS

Los conversores A/D por aproximaciones sucesivas son ampliamente utilizados especialmente por su alta velocidad y resolución. En este tipo de conversores, el tiempo de conversión es fijo, independiente de la magnitud de la señal de voltaje o corriente utilizada como entrada. Cada conversión es única e independiente de los resultados obtenidos en conversiones previas, debido a la lógica interna.

La técnica de conversión consiste en la comparación de una entrada desconocida con un voltaje o corriente bien determinado, que se ha generado internamente a la salida de el conversor D/A, como parte del proceso. La entrada del conversor D/A consiste en señales digitales provenientes del registro de aproximación sucesiva. El proceso de conversión es muy similar al proceso de pesaje utilizado en una balanza de precisión, como las utilizadas en laboratorio, cuando se cuenta con un juego binario de n pesas (por ejemplo: 1/2 lb, 1/4 lb, 1/8 lb. .....).

Luego de haber aplicado el comando para la conversión, el MSB (bit más significante igual 1/2 escala completa) de la salida del conversor D/A es comparada con la entrada. Si la entrada es -

mayor que el MSB, este es retenido, (aplicando un "1" a la salida del registro, por ejemplo), y al próximo bit menos significante (1/4 de la escala completa) es procesado. Si por el contrario la entrada es menor que el MSB, este es descartado ("0" a la salida del registro), de igual manera se procesa el siguiente bit menos significante. El proceso continua an orden descendente,hasta que se haya considerado el bit menos significante (LSB). Entonces se ha completado el proceso, la señal qua indica el estado del proceso cambia su condición para indicar que el valor a la salida del registro constituye una conversión válida. En estas condiciones la señal a la salida del registro constituye un código binario - digital equivalente a la señal de entrada. El proceso se indica en la Figura Nº 35

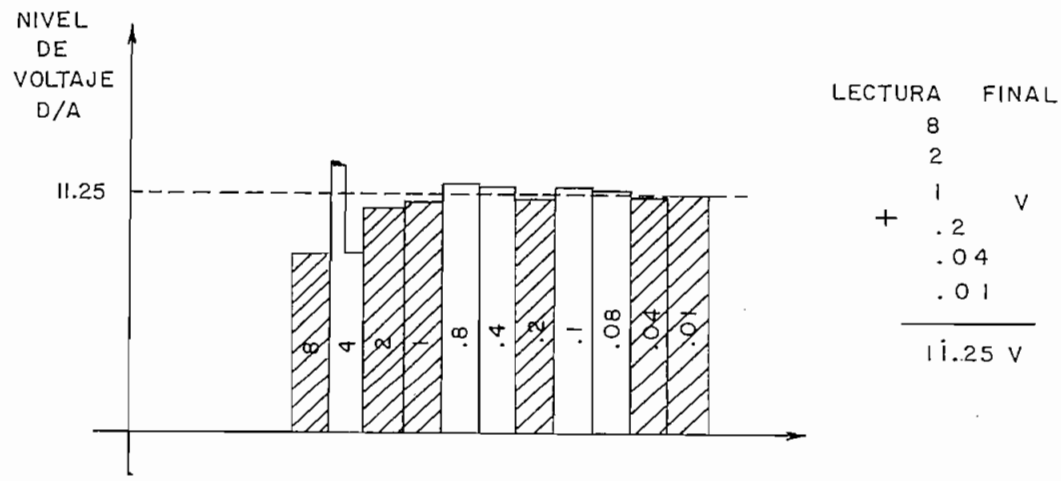


FIG. Nº 35

Método de aproximaciones sucesivas para convertir 11.25 - voltios en su equivalente digital utilizando una secuencia: 8, 4, 2, 1.

El gráfico de la Figura Nº 36 constituye un diagrama en - bloques de un conversor A/D por aproximaciones sucesivas.

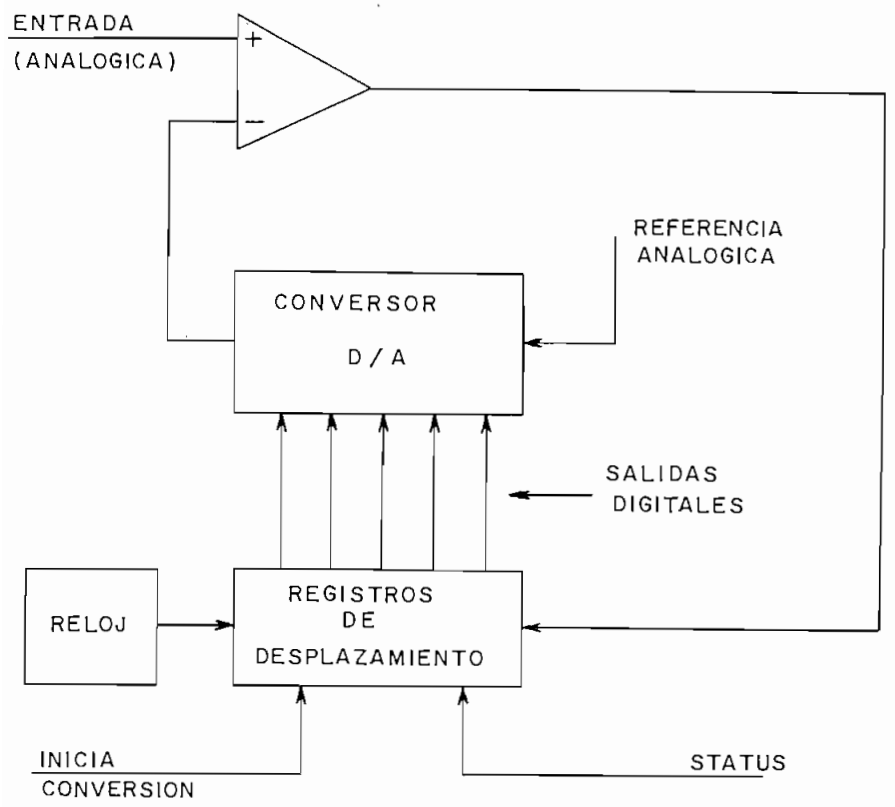


FIG. Nº 36

Los datos obtenidos en forma paralela no son válidos miéntras no concluye todo el proceso. Al obtenerse en forma serial los datos, debe considerarse que cada bit sea válido, que haya sido aceptado o rechazado correctamente.

En este método de conversión el comparador ideal tiene una ganancia infinita y un tiempo para la comparación igual a cero, los comparadoras reales están limitados por parámetros similares a los que limitan a los amplificadores operacionales: ganacia a lazo abierto, ancho de banda y sus características para señales contínuas y alternas.

El comparador puede relacionarse con un amplificador operacional realimentado. Opera con un producto ganacia x ancho de banda muy alto y tiene una compensación por realimentación mínima. Señales parásitas muy pequeñas en la realimentación, muy cerca al dispositivo o atravéz de la fuente de polarización pueden inducir oscilaciones. Generalmente estas oscilaciones son causadas por la disposición física de los conductores, esto puede apreciarse en puntos en los cuales se relaciona una señal de salida que varia muy rápidamenta con una etapa cuya impedancia de entrada sea muy alta.

En un sistema de conversión A/D, el efecto más notorio de la oscilación está dado en cuanto la señal analógica de entrada se aproxima a su nivelde cuantización, el equivalente digital que

se obtiene no es puro y presenta una señal sin un comportamiento definido. Así por ejemplo, un incremento de la señal analógica de entraga suficiente para incrementar al equivalente digital en un LSB, hará que el proceso sea erróneo.

Un comparador puede utilizarse básicamente de dos formas, para comparar voltajes o corrientes. En el proceso de conversión se utiliza para comparar corrientes, una desconocida con otra que sirve de referencia y que se ha generado internamente como parte de el proceso.

2.2.d MEMORIA CON REGISTROS DE DESPLAZAMIENTO

Actualmente existen diferentes tipos de memorias, sus características las hacen más apropiadas para una u otra aplicación. Las memorias con registros de desplazamiento que utilizan para su construcción la tecnología MOS, constituyen una de estas variedades Dos propiedades de la tecnología MOS en circuitos integrados, hacen de estos registros muy compatibles para el diseño de memorias con registros de desplazamiento: La alta impedancia asociada con los circuitos compuerta permiten un almacenamiento temporal de carga en las capacidades parásitas. Con las compuertas de transferencia un modo de compuertas puede muy facilmente conectarse o desconectarse de otros puntos del circuito.

Por su estructura utilizan muy pocas interconecciones y - para su funcionamiento no requieren de otros dispositivos electrónicos, constituyendo una de las memorias de semiconductores más - baratas en el mercado.

Estas memorias son utilizadas en terminales de computadoras con presentación visual de las intercomunicaciones. Los datos a ser presentados recirculan a través de la memoria en sincronismo con la presentación en el tubo de rayos catódicos. Además este tipo de memoria as muy utilizado en una amplia variedad de calculadoras.

En general son utilizados en circuitos con memorias de baja velocidad de acceso, especialmente cuando los datos pueden ser utilizados en al mismo orden de almacenamiento. No resultan muy - útiles para memorias de acceso aleatorio.

PRINCIPIOS DE OPERACION

Existen muchas variaciones en los circuitos básicos de -- los registros de desplazamiento. Tomemos un tipo canal P, para explicar su funcionamiento, como el que se presenta en la figura †- Nº 37.

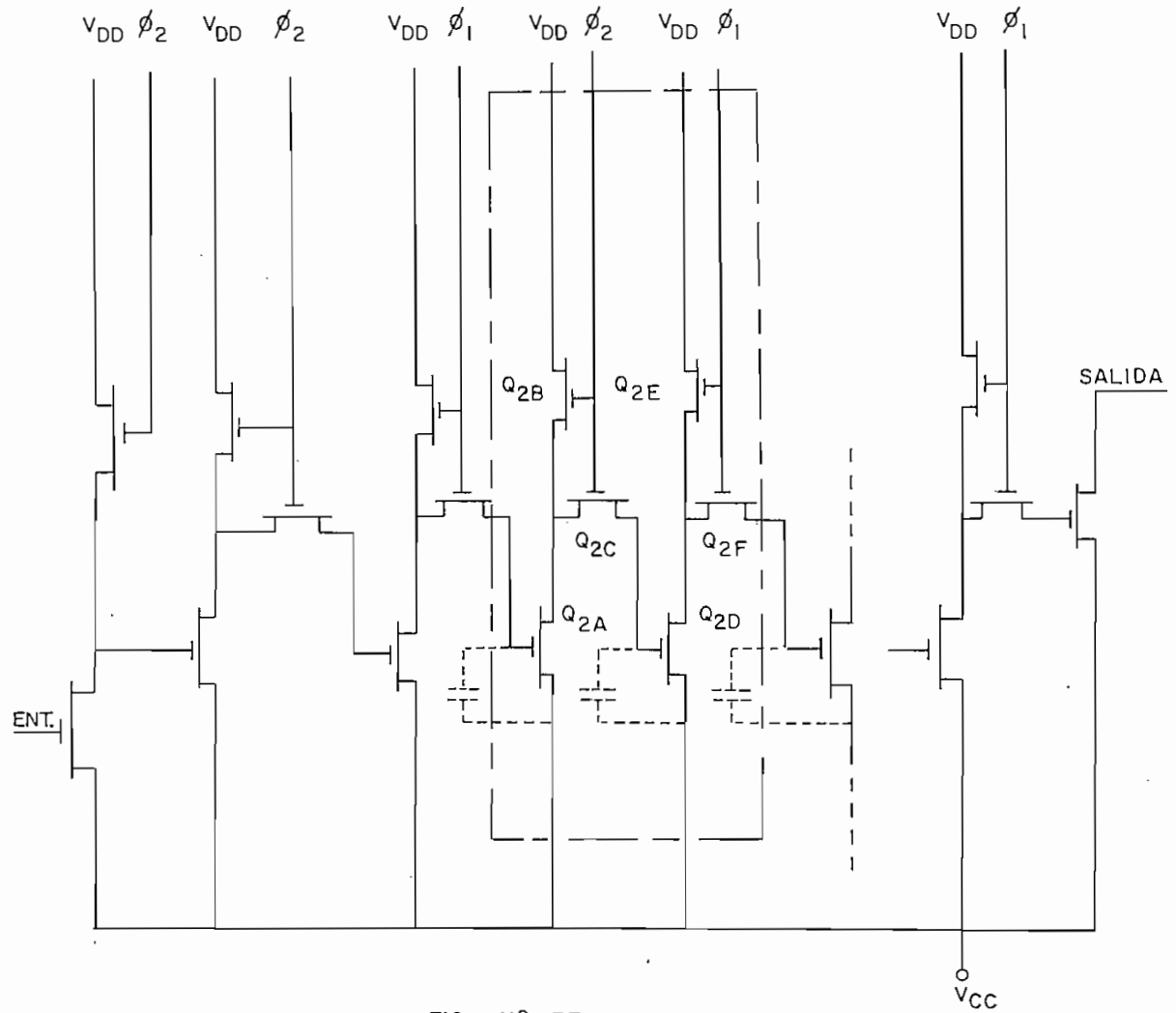


FIG. Nº 37

Cada bit de los registros de desplazamiento requiere de - seis dispositivos MOS. Veamos lo que sucede en uno de estos bits, por ejemplo el segundo, se han danominado Q_{2A}, Q_{2B}, ..., Q_{2F} a - los dispositivos MOS.

Al ingresar un dato proveniente del bit anterior se carga

la capacitancia parásita de Q_{2A}. Cuando el ciclo del reloj ϕ_2 -- (controla el ingreso de datos)hace su transición negativa (para - dispositivos de canal P), Q_{2A} y Q_{2B} forman un estado inverso.

Si la carga en la compuerta de Q_{2A} es suficientemente negativa para producir una conducción fuerte de Q_{2A}, el nodo común de Q_{2A}, Q_{2B} y Q_{2C} se aproximarán al nivel de voltaje positivo Vcc. De lo contrario, si la carga en la compuerta de Q_{2A} es lo suficientemente positiva para poner en corte a Q_{2A} al producirse la transición negativa de ϕ_2, el nodo común alcanza el voltaje V_{DD} a través de Q_{2B}. El nodo común alcanza un voltaje inverso al del dato. Simultáneamente con la transición negativa de ϕ_2 Q_{2C} conduce cargado la capacitancia parásita de Q_{2D} al mismo potencial del nodo común.

Luego de la transición de ϕ_2, Q_{2D} retiene el potencial adquirido. La transición negativa de ϕ_1 (controla la salida de datos). Transfiere el dato al siguiente bit, utilizando Q_{2E} y Q_{2D} para producir una inversión de la polaridad del dato y Q_{2F} como - elemento de transferencia.

La ventaja de este diseño radica en no perder la carga del dato. Si la información varía en su magnitud la siguiente etapa - tendrá la suficiente ganancia para normalizar los niveles. Cuando existen varias etapas es necesario que cada una tenga una ganancia ligeramente mayor que uno para compensar las pérdidas. Se uti

lizan los invertidores que cargan las capacitancias parásitas con esta ganancia.

C A P I T U L O III

D I S E Ñ O Y C O N S T R U C C I O N D E L E Q U I P O

El procedimiento a seguirse para grabar una señal será el siguiente: Dependiendo de la magnitud de la señal esta debe pasar por la etapa de atenuación-amplificación.

El valor máximo pico-pico para que la señal de entrada no sea atenuada debe ser de 800mV. Señales mayores deben pasar por una escala de atenuación de modo que su valor quede comprendido en este rango.

Luego de la etapa de atenuación la señal es amplificada y alcanza valores $\pm$ 4V. Posteriormente de su forma analógica es convertida a su equivalente digital, forma en la que es almacenada en la memoria.

Para obtener la señal debe pasar por un conversor D/A antes de ser presentada en el osciloscopio.

Se ilustra en el diagrama de bloques en la figura Nº 38.

Se dispondrá de un circuito que permita la grabación automática de la señal cuando esta supere cierto nivel relativo (graduable manualmente) con respecto al valor máximo de la escala utilizada.

Se realizará la grabación de la señal desde un instante antes de producirse el disparo como posterior al mismo.

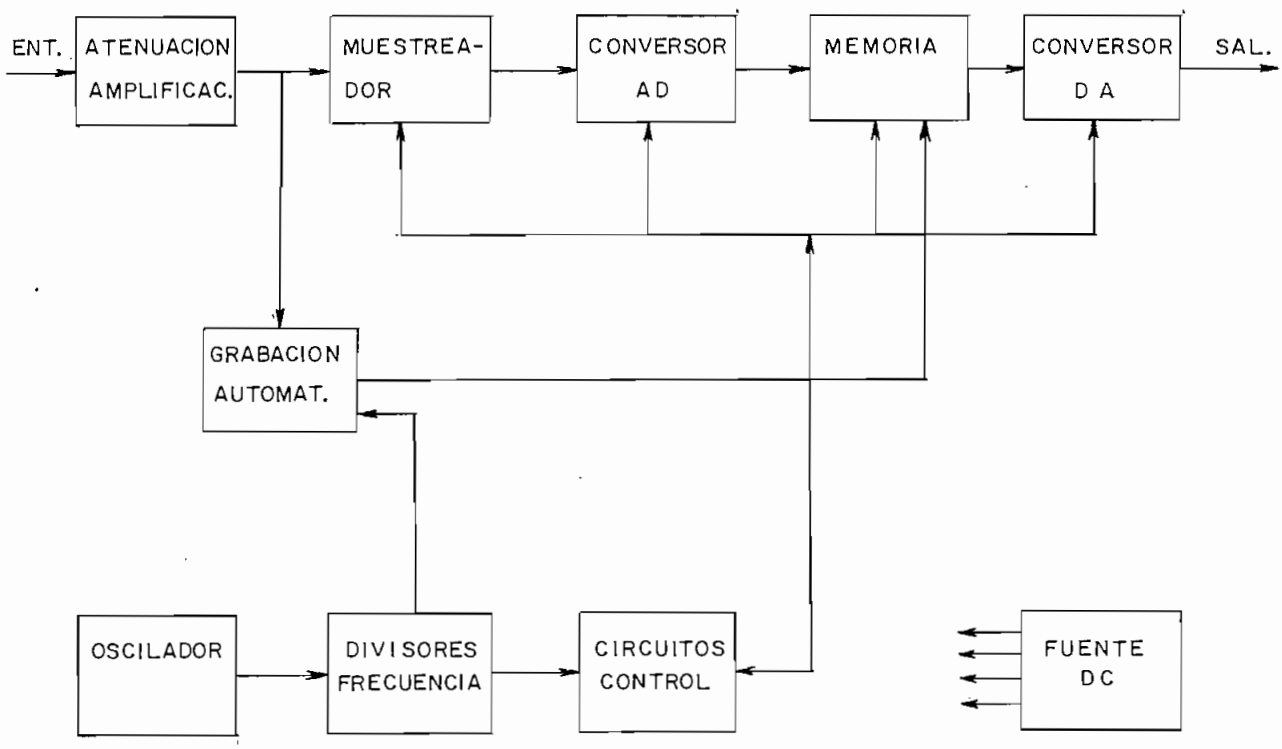


DIAGRAMA EN BLOQUES DE LA MEMORIA DIGITAL

FIG. Nº 38

DISEÑO DE CADA UNA DE LAS PARTES

3.1.a.1 ETAPA DE ATENUACION

Debe presentar una impedancia de 1MΩy 20pF. La disposición básica de los elementos se indica en la figura Nº 39 y desarrollada en el capítulo II.

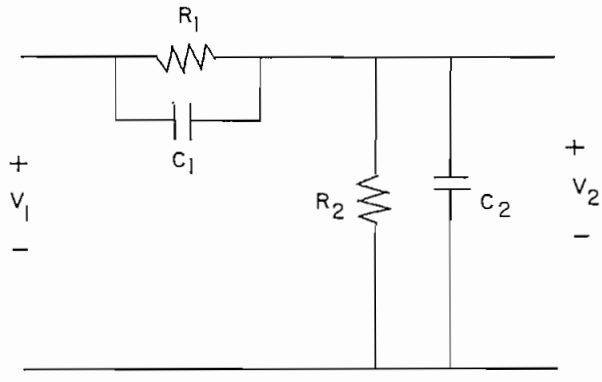


FIG. Nº 39

Según la ecuación Nº 9 se tiene:

(1) $$\frac{V_2}{V_1} = \frac{R_2}{R_1 + R_2}$$

Siempre que:

(2) $$R_1 C_1 = R_2 C_2$$

En donde:

(3) $C_1 = C' \; C_b$

C' : capacitancia conectada en paralelo con R_1

C_b : capacitancia parásita en los terminales de R_1

(4) $C_2 = C' + C_c$

C' : capacitancia conectada en paralelo con R_2

C_c : capacitancia parásita en los terminales de R_2

Con estos valores se tiene que:

(5) $$Z_{eq} \cong \frac{R_{eq}}{1 + R_{eq} C_{eq} S}$$

En donde:

(6) $R_{eq} = R_1 + R_2$

(7) $$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

ATENUACION 1 :

La señal debe pasar directamente hacia la siguiente etapa. Se tendrá un circuito como se indica en la figura Nº 40

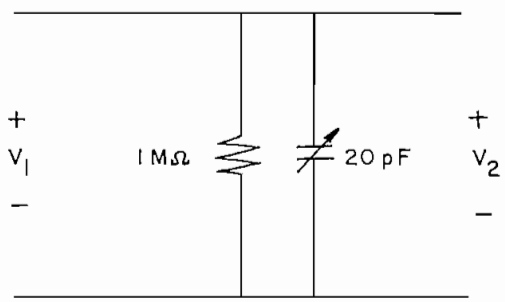


FIG. Nº 40

ATENUACION 2 : Considerando el circuito de la figura Nº 41 y las ecuaciones anteriores:

$$(8) \qquad \frac{V_2}{V_1} = \frac{R_2}{R_1 + R_2} = \frac{1}{2}$$

$$\therefore \quad (9) \qquad R_1 + R_2 = 10^3 \text{ K}$$

de (8) y (9)

$$2R_1 = 10^3 \text{ K}$$

$$R_1 = 500 \text{ K}$$

de la ecuación (2)

$$R_1 C_1 = R_2 C_2$$

$$C_1 = C_2$$

$$C_1 = C_2 = 20pF$$

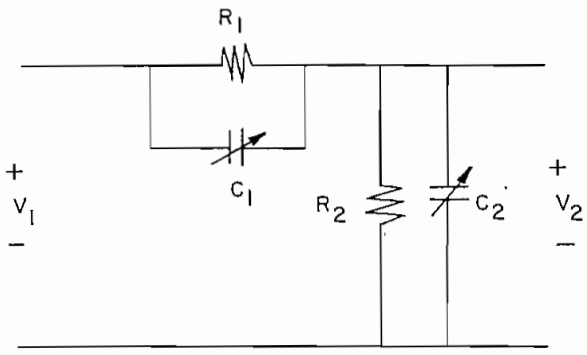
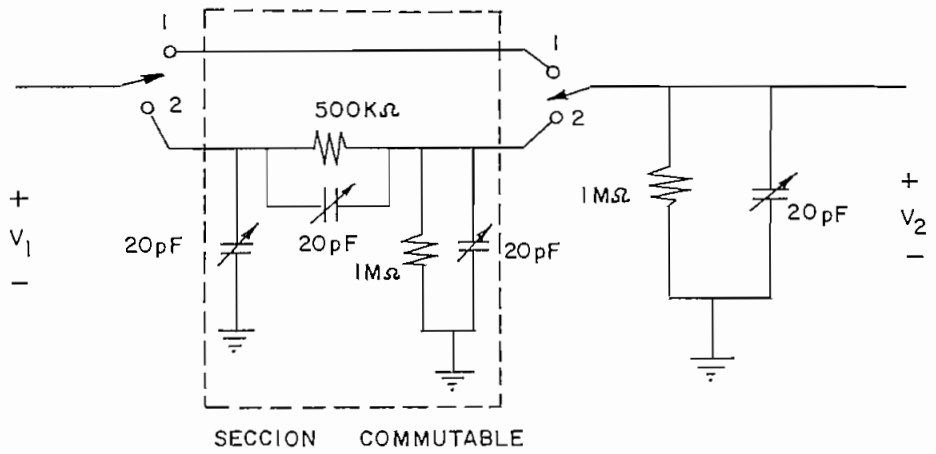


FIG. Nº 41

$$R_1 = R_2 = 500\ K\Omega$$

$$C_1 = C_2 = 20\ pF$$

Es conveniente tener una parte conmutable y otra fija, como se presenta en la figura Nº 42.



POSICION	FACTOR ATEN(V_2/V_1)
1	1
2	2

FIG. Nº 42

Entonces R_2 se modifica de la siguiente manera:

$$R_2 = 500\ K = 1M \,//\, R_2'$$

$$\therefore \quad R_2' = 1M$$

Los valores de C_2, C_1 y C_{en} deben encontrarse experimen - talmente ajustando los valores de los condensadores variables, --

hasta conseguir los valores calculados.

Esta etapa debe utilizarse para señales menores de 1600 - mV p-p.

Con un procedimiento similar puede diseñarse el resto de etapas como se indica a continuación.

ATENUACION POR 5

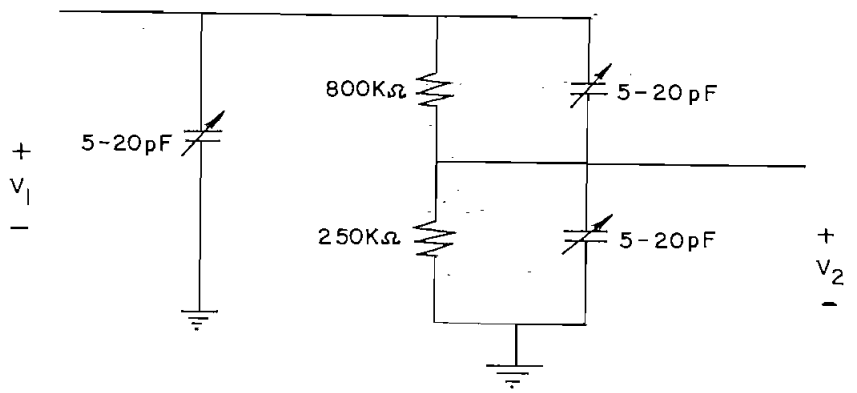


FIG. Nº 43

Se utilizará para señales menores que 4 Vp-p.

ATENUACION POR 10

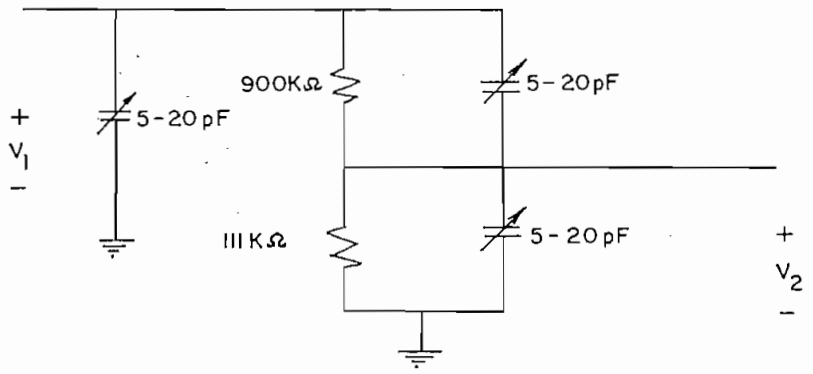


FIG. Nº 44

Debe utilizarse para señales menores que 8Vp-p.

ATENUACION POR 100

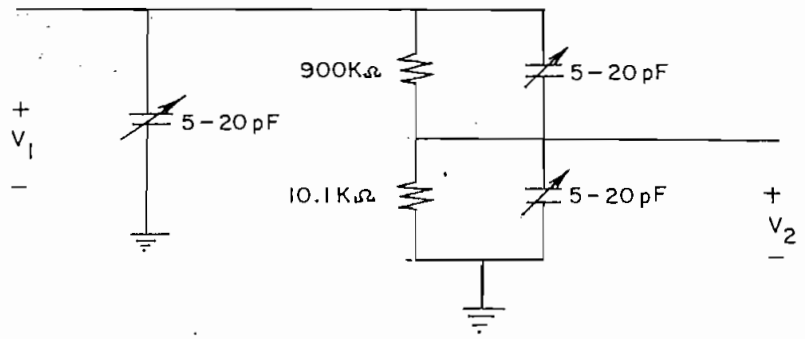


FIG. Nº 45

Debe utilizarse para señales menores que 80 Vp-p.

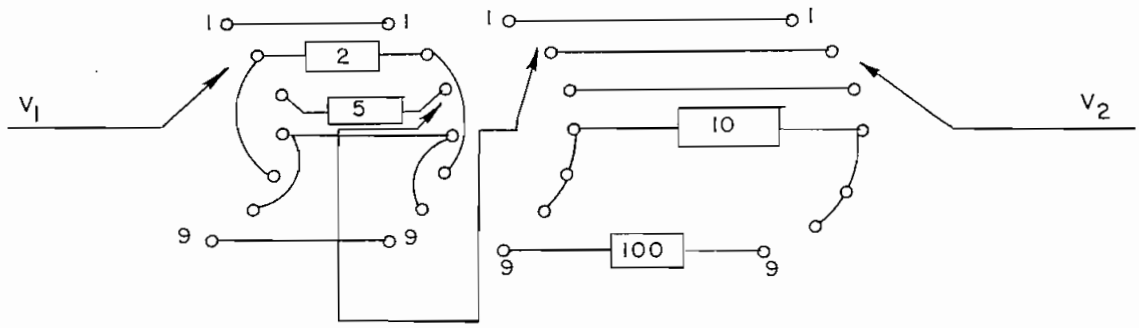
Con una combinación de estos pasos de atenuación pueden - conseguirse nuevos pasos de atenuación, por ejemplo al colocar en cascada el circuito de atenuación por 2 con el de atenuación por 10 se conseguirá una atenuación total por 20.

Se consiguen los valores indicados en la tabla de la Figura Nº 46

FACTOR ATENUA.	ENTRADA MAX. Vp-p (V)	ENTRADA MAX. V / DIV.
1	.8	.1
2	1.6	.2
5	4.0	.5
10	8.0	1.0
20	16.	2
50	40.	10
100	80.	20

FIG. Nº 46

El sistema de conmutación de la figura Nº 47 permite lograr estos factores de atenuación.



POSICION	FACTOR ATE.
1	1
2	2
3	5
4	10
5	20
6	50
7	100

FIG. Nº 47

Es necesario tener como paso previo a la sección de atenuación un circuito que elimine componentes DC en señales alternas puras, esto se consigue con el circuito de la figura Nº 48.

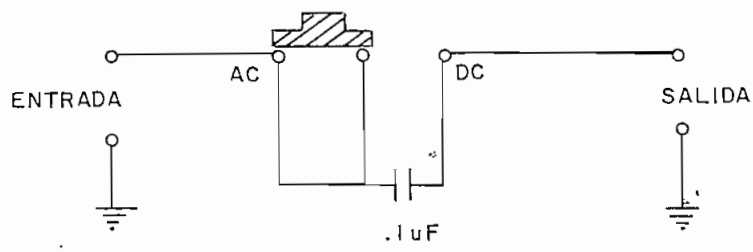


FIG. Nº 48

3.1.a.2 AMPLIFICADOR DE ENTRADA

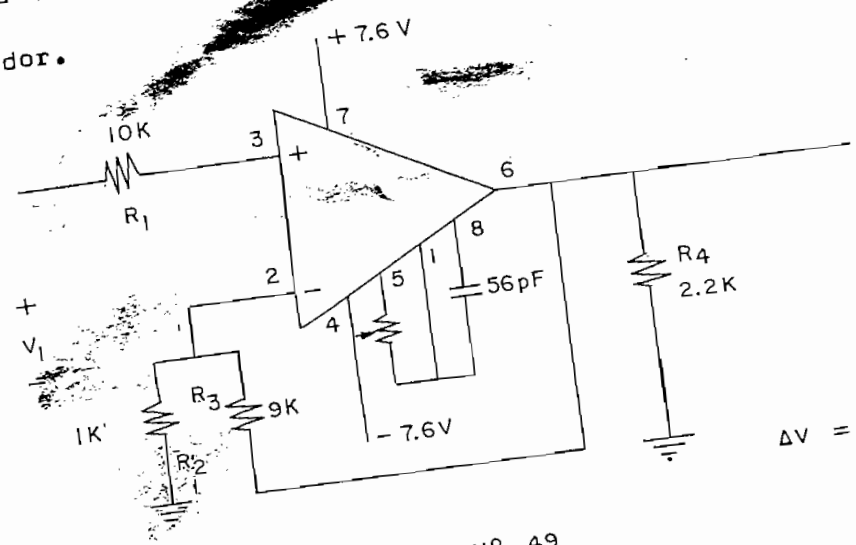
El circuito muestreador, por su naturaleza (carga de un - condensador), necesitará valores de corriente de exitación relativamente altos; al tomar directamente la exitación desde la entrada se introducirán errores que pueden hacer variar la señal de entrada. Los circuitos muestreadores presentan mejores características cuando operan con señales relativamente altas (algunos voltios) y de baja impedancia, esto limitaría su utilización a señales con - estas características. Es necesario utilizar un dispositivo que - independice la entrada del muestreador, a la vez que sea capáz de suministrar altas corrientes (pocas decenas de mA), con corrien--

tes de exitación muy pequeñas (pocos pA) y además con una baja - impedancia.

Pueden satisfacerse estos requerimientos con un amplificador. El desarrollo técnico ofrece muchas facilidades para estos casos, encontrándose en el mercado elementos que satisfacen plenamente.

Para el presente trabajo se toma el amplificador operacional CA3130S, cuyas características son muy afines. Puede observarse en las hojas de datos en el compedio de este trabajo.

En la figura Nº 49 se presenta el circuito que permite utilizar este elemento. Para señales de entrada menores de 400 mV, con una corriente de excitación de 2pA se obtiene una señal de -- hasta 4 V con 20 mA, que servirá como señal de excitación del mueatreador.



$$\Delta V = \frac{R_3 + R_2}{R_2} \quad (33)$$

FIG. Nº 49

tes de exitación muy pequeñas (pocos pA) y además con una baja - impedancia.

Pueden satisfacerse estos requerimientos con un amplificador. El desarrollo técnico ofrece muchas facilidades para estos casos, encontrándose en el mercado elementos que satisfacen plenamente.

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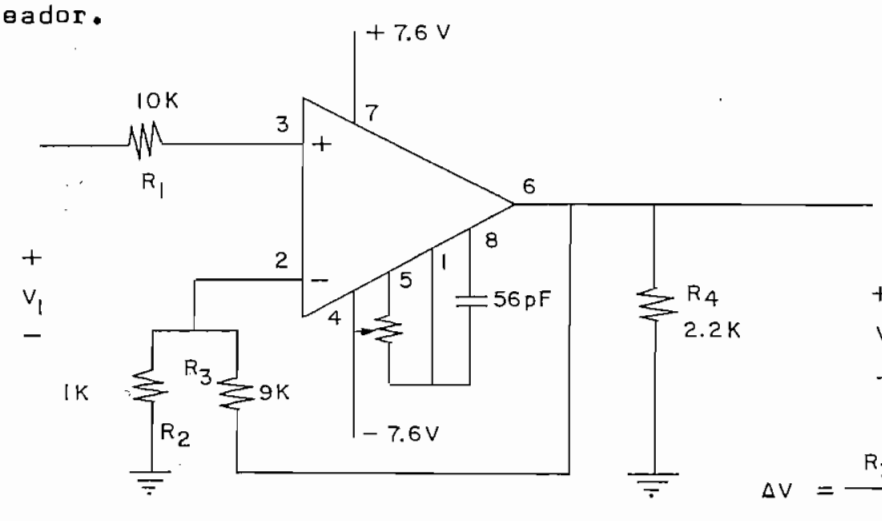


$$\Delta V = \frac{R_3 + R_2}{R_2} \qquad (33)$$

FIG. Nº 49

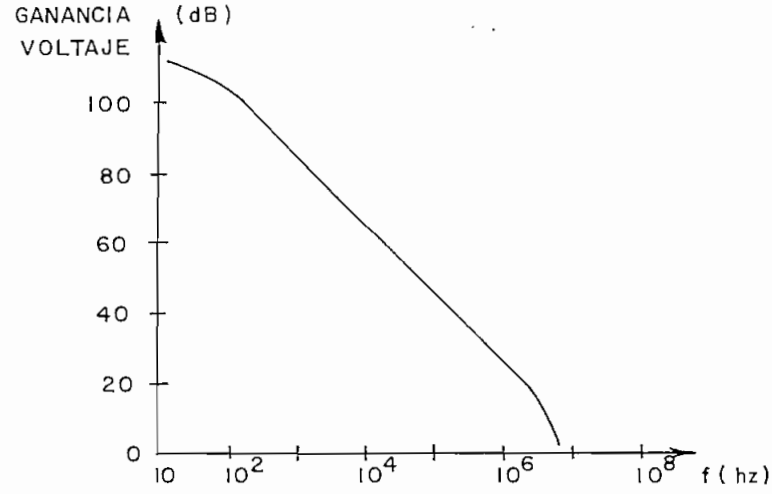
La amplificación de voltaje está dada por la ecuación Nº33

$$Av = \frac{R_3 + R_2}{R_2} = \frac{9 + 1}{1} = 10 = \frac{V_2}{V_1}$$

Esta configuración no produce inversión de la señal y presenta una impedancia de entrada muy grande.

La resistencia R_1 se ha considerado para limitaciones de corrientes de las señales. Una señal de corriente muy grande (algunos mA) destruiría el amplificador peracional.

Este amplificador operacional, que funciona en clase A tiene otra ventaja en cuanto con un condensador conectado entre los terminales 1 y 8 se pueden controlar las variaciones de fase, entre la señal de salida y de la entrada. En cuanto a su ganancia de voltaje en lazo abierto con respecto a la frecuencia podemos observar el gráfico de la figura Nº 50



3.1.b M U E S T R E A D O R

Para el presente diseño se ha seleccionado el circuito muestreador compensado sin inversión. Se requiere un circuito muestreador rápido, capaz de responder satisfactoriamente a señales con frecuencias de muestreo de hasta 250 KHz.

De los diferentes elementos de conmutación que existen en el mercado se ha preferido el DG 181BA, pues sus características dinámicas como, tiempo de repuesta del elemento (tiempo en el cual el dispositivo está listo para operar) de 180 ns (t_{ON} = 180 ns; - t_{OFF} = 150 ns); resistencia en estado de conducción ($R_{DS(ON)}$=50 ohm) rango de respuestaen cuanto a voltajes ± 7.5V; lo hacen muy compatible.

El emplificador operacional que debe utilizarse en el muestreador, debe poseer características como ser capaz de "seguir" el voltaje almacenado en el condensador, con mucha facilidad, además su señal de offset debe ser pequeña. la impedancia de entrada debe ser alta para que la información se mantenge en el condensador el tiempo necesario para el proceso de conversión, su corriente de excitación debe ser pequeña, la señal de salida debe tener un rango de corriente suficiente para excitar a la siguiente etapa. Estas consideraciones son satisfechas por el amplificador operacional CA3130S.

El circuito utilizado para muestreo-retención se presenta en la figura Nº 51.

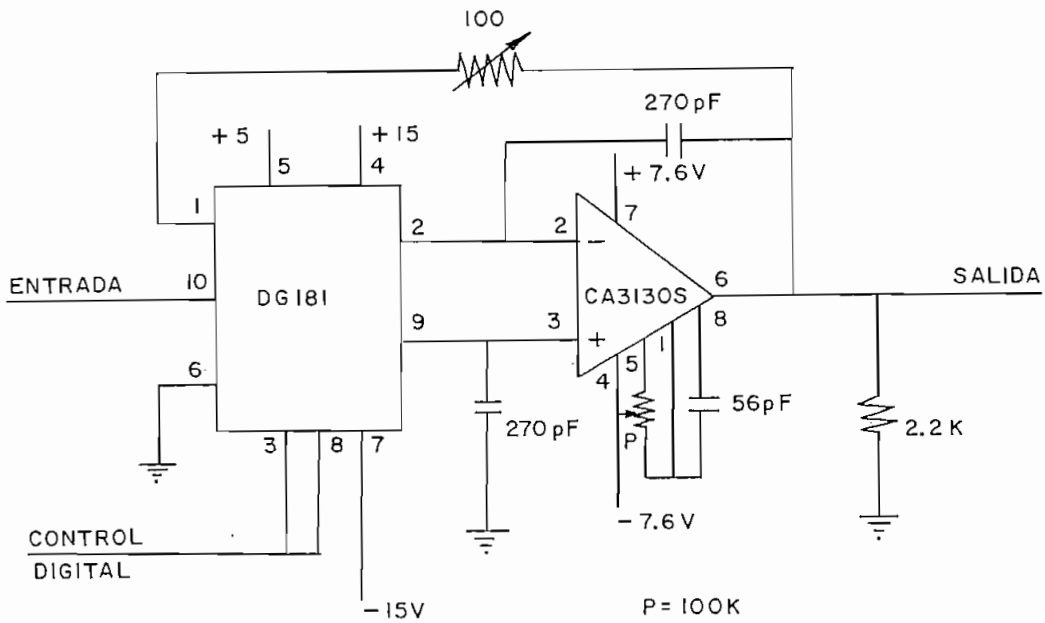


FIG. Nº 51

Considerando el preamplificador y el muestreador el circuito queda como se indica en la Figura Nº 52.

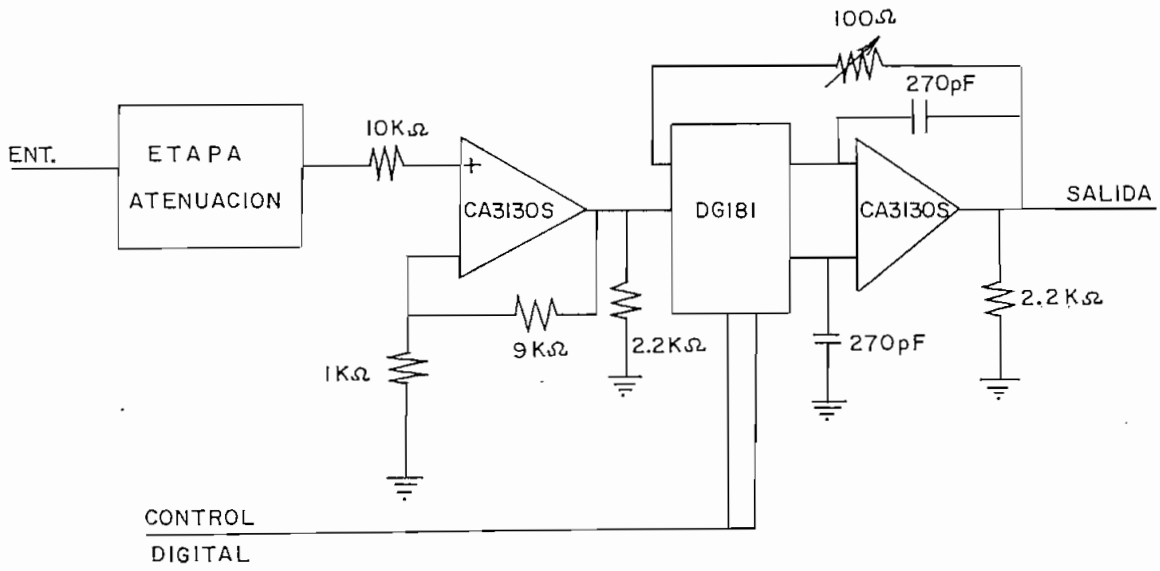


FIG. Nº 52

3.1.c.1 CONVERSOR ANALOGICO DIGITAL

La etapa de conversión A/D debe ser de alta velocidad con un tiempo de conversión fijo e independiente de la magnitud de la entrada. Cada conversión debe ser única e independiente de los resultados anteriores. Estas características son satisfechas por un conversor por aproximaciones sucesivas. Además presenta la ven

taja de ser económicamente más barato. El circuito se presenta en la figura Nº 53

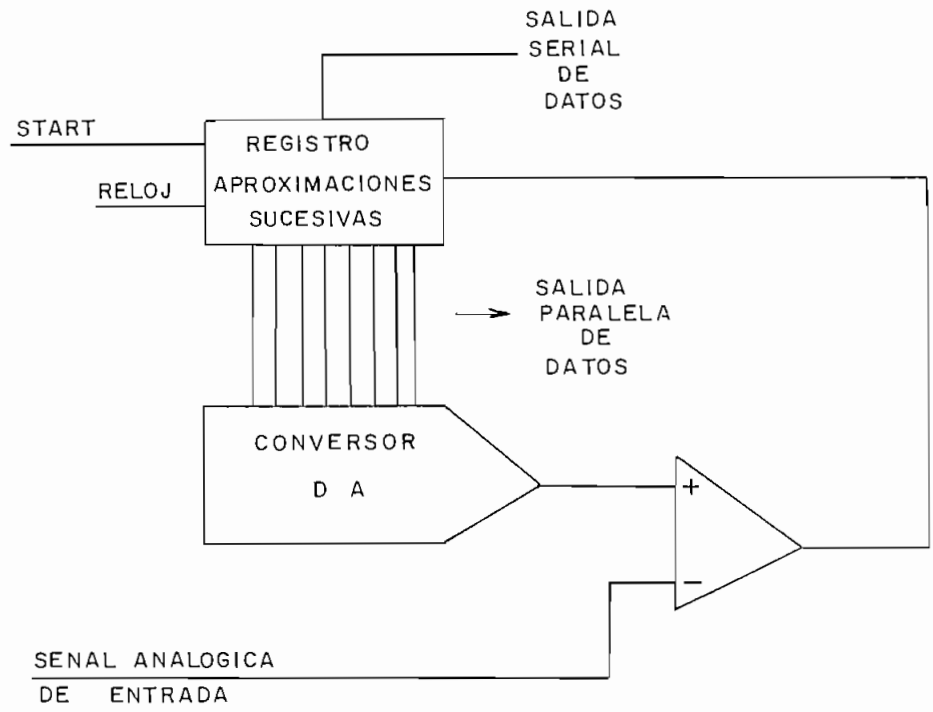


FIG. Nº 53

La conversión esta controlada por una señal de reloj y otra que indica cuando debe comenzar y terminar el proceso (START).

Se han elegido los siguientes elementos para el diseño de la presente etapa: Registro de aproximaciones sucesivas Am 2502, Conversor digital-analógico CMP01CJ, que con la configuración que se presenta en la figura Nº 54 ofrece resultados satisfactorios.

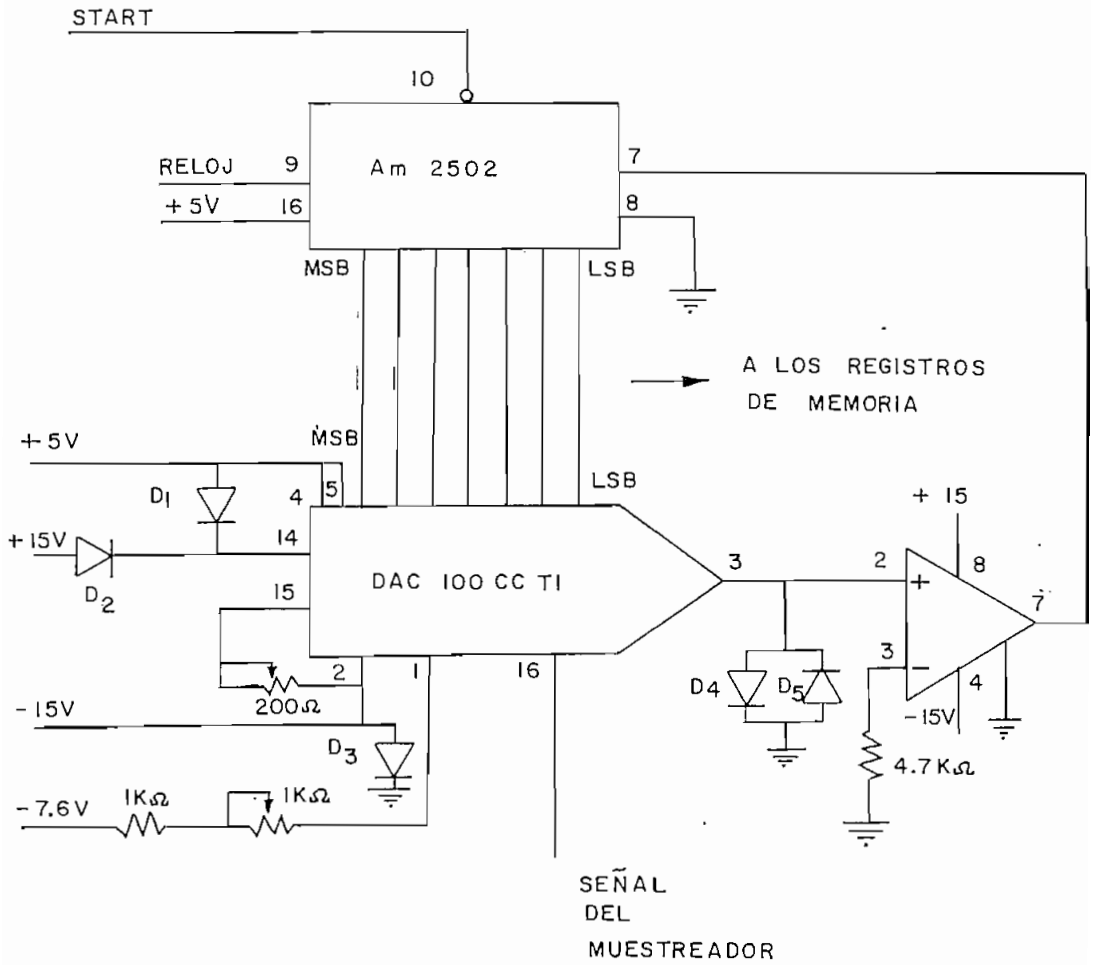

START
10
RELOJ
9
+5V
16
Am 2502
7
8
MSB
LSB
A LOS REGISTROS
DE MEMORIA
+5V
MSB
D1
4
5
LSB
+15V
14
D2
DAC 100 CC TI
3
+15
2
8
15
7
2
1
16
D4
D5
3
4
-15V
200Ω
-15V
D3
4.7KΩ
-7.6V
1KΩ
1KΩ
SEÑAL
DEL
MUESTREADOR

FIG. Nº 54

3.1.c.2 REGISTRO DE APROXIMACIONES SUCESIVAS

El registro de aproximaciones sucesivas (RAS) que se ha elegido, (250PC) es un registro de 8 bits. Contiene los controles y memorias digitales neceserios para una conversión analógico-digital por aproximaciones sucesivas.

Los niveles lógicos de entrada estan comprendidos en valores que utiliza la técnica digital TTL.

Este elemento consiste de una serie de registros maestro que actúan como elementos de control y cambian de estado cuando el reloj de entrada esta en 0_L, y una serie de registros esclavo que retienen los datos y varían con la transición positiva del reloj de entrada. Externamente este dispositivo actúa como un conversor serie-paralelo de propósito especial.

Acepta los datos por el terminal de entrada D y envía a - los registros esclavo. Simultáneamente con la entrada de datos,el bit próximo menos significante es puesto a nivel 0_L listo para su próximo iteración.

El registro es restablecido (condiciones lógicas iniciales) al poner la señal de comienzo S (START) en un nivel bajo - 0_L durante una transición positiva del reloj. Simultáneamente la salida del bit más significante (MSB Q_7) es puesto a 0_L miéntras

las otras entradas permanecen en 1_L. La señal S debe permanecer - con este valor hasta que se produzca la transición positiva del reloj, una vez efectuada esta, puede variar o no.

Con la próxima transición positiva del reloj el dato de - la entrada D es almacenado en el registro del MSB y el próximo ciclo del reloj. Con la siguiente transición positiva del reloj el dato ingresa al registro continúandose el proceso hasta considerar el bit menos significante (LSB). El registro no aceptará más datos hasta que la señal S varíe nuevamente. Esto se indica en la figura Nº 55.

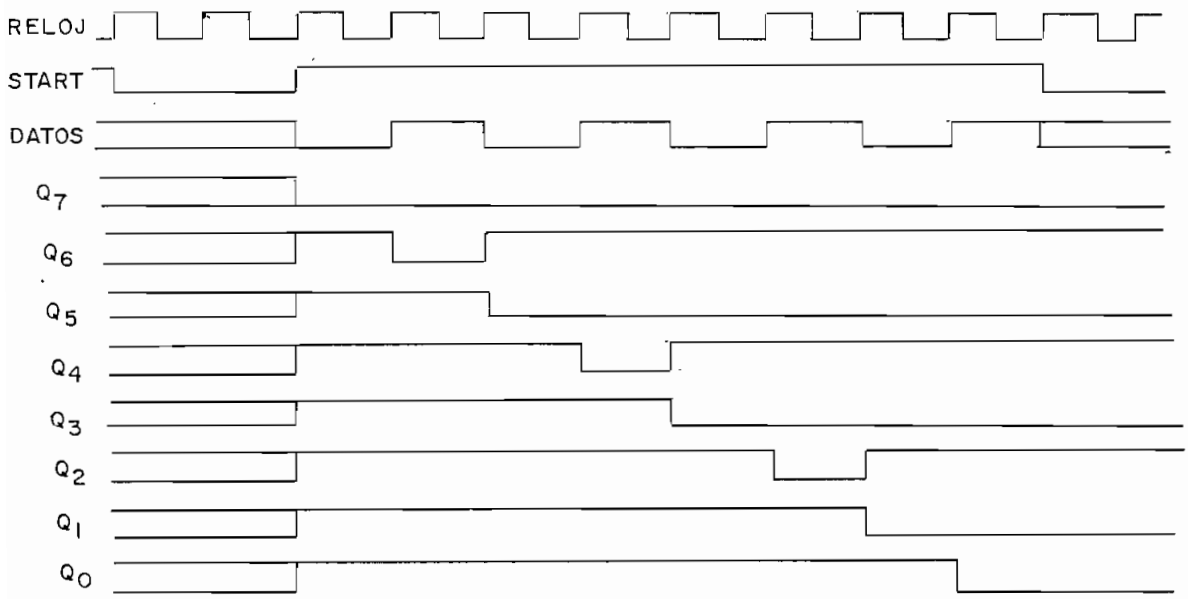


FIG. Nº 55

Lo anotado anteriormente puede resumirse en la tabla de estados de la figura Nº 56

TIEMP.	ENTRADAS			SALIDAS								
tn	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	X	B	B	X	X	X	X	X	X	X	X	X
1	D_7	A	B	X	B	A	A	A	A	A	A	A
2	D_6	A	B	D_7	D_7	B	A	A	A	A	A	A
3	D_5	A	B	D6	D_7	D	B	A	A	A	A	A
4	D_4	A	B	D_5	D_7	D_6	D_5	B	A	A	A	A
5	D_3	A	B	D_4	D_7	D_6	D_5	D_4	B	A	A	A
6	D_2	A	B	D_3	D_7	D_6	D_5	D_4	D_3	B	A	A
7	D_1	A	B	D_2	D_7	D_6	D_5	D_4	D_3	D_2	B	A
8	D	A	B	D	D	D	D	D	D	D	D	B

B : 0_L

A : 1_L

X : NO IMPORTA SU ESTADO

FIG. Nº 56

3.1.c.3 CONVERSOR DIGITAL ANALOGICO

El conversor digital-analógico DAC 100CCT1, opera con 10 entradas digitales, con precisión garantizada para 8 bits, tiene una muy buena respuesta en el tiempo (375 ns), presenta en un ter

minal de salida una señal analógica máxima de 11.1 y mínima de 10 v, con amplificador operacional externo, para escala completa. Otras características pueden observarse en el capítulo correspondiente, al final del presente trabajo.

Debido a que el registro de aproximaciones sucesivas trabaja con 8 bits, tomamos los 8 bits con precisión garantizada del DAC100CT1. Las entradas lógicas no utilizadas, que corresponden a los bits menos significantes, se polarizan a nivel lógico 1.

Una particularidad muy importante que presenta este conversor en su diseño es su salida de corriente. Opera en óptimas condiciones cuando su salida es próxima a ± 0.7 v. Tiene una resistencia interna de 4.88 kΩ conectada entre el terminal de salida y un terminal de entrada analógica. De esta manera se evita que variaciones indeseadas del voltaje en el terminal de salida afecten el proceso. Variaciones relativamente grandes de voltaje pueden producir daños irreparables.

El nivel óptimo de funcionamiento (± 0.7 v) implica la conección de un par de diodos limitadores (D_4 y D_5).

Debe tenerse especial cuidado en las fuentes de polarización, laa mismas que deben conectarse simultáneamente, de lo contrario su funcionamiento puede no ser normal o inclusive causar daños permanentes. Especialmente con las fuentes de voltaje positivo, si estas son ectivadas 300 ms luego de haberse aplicado la

señal analógica, su daño será definitivo, por esta circunstancia se ha conectado D_1, para el caso en que la fuente de +5v sea activada antes que la de +15v. Primero debe activarse la parte analógica luego la digital. El nivel de corriente a la salida puede ser contralado conectando un potenciómetro de 200Ω entre el terminal para ajuste a escala completa (FSA) y el terminal de voltaje negativo. Este ajuste debe realizarse con los niveles lógicos de entrada 0_L. El diodo D_3 se ha colocado para prevenir errores de polarización.

C O M P A R A D O R

Este elemento es muy crítico en esta etapa. Debe elegirse un elemento cuyas señales de offset tanto para corriente como para voltaje sean muy pequeñas, y que responda satisfactoriamente a variaciones algo rápida en su entrada.

Se ha elegido el comparador OP-01CJ con resultados experimentales muy satisfactorios.

3.1.d MEMORIA DE DESPLAZAMIENTO INTERNO

Se emplean los registros Am 2808PC (2525 según la Signetics), cuya fabricación se ha realizado con la tecnológía MOS (canal P). Son registros directamente compatibles con la tecnología TTL, con excepción de la señal de reloj.

Presentan compatibilidad tanto en sus características dc como en las dinámicas, además de su bajo costo. Por ser registros de recirculación interna no requieren 'refrescar' los datos como sucede en otros tipos de memorias.

La recirculación interna no requiere control, pero sí necesita comandos para que el registro acepte datos o los entregue (READ Y WRITE respectivamente). El diagrama de tiempos se presenta en la figura Nº 58

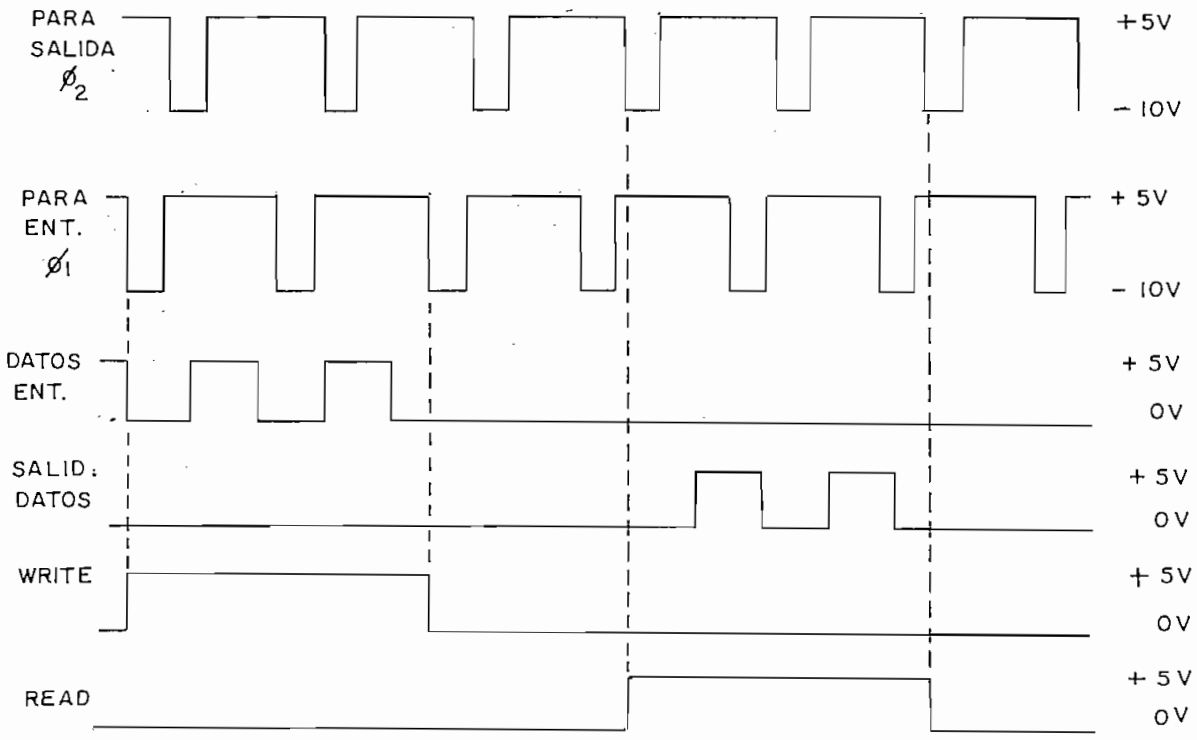


FIG. Nº 58

En cuanto a los tiempos de referencia puede observarse la Figura Nº 59.

	MIN	MAX	UNIDAD
FRECUENCIA	.0005	3	Mhz
TRANS. PULSO	10	1000	ns
TRANSICION READ-WRITE	0		ns
TRANSICION WRITE-READ	0		ns

FIG. Nº 59

Debe notarse que los niveles lógicos de reloj tanto para la entrada de datos ($\emptyset_2$), como para la salida de los mismos ($\emptyset_1$) tienen + 5 v. para el nivel superior y - 10 v. para el nivel lógico inferior. Las señales para $\emptyset_1$ y $\emptyset_2$ pueden conseguirse con registros JK, NAND, etc., pero se conseguirán estas con niveles lógicos estandard. Para conseguirse los niveles apropiados se u-

tiliza un amplificador de aplicación especial, el MH0026C, que con una polarización adecuada nos permite alcanzar tales niveles. El circuito se presenta en la figura Nº 60, por ser un elemento dual las conecciones se limitan considerablemente.

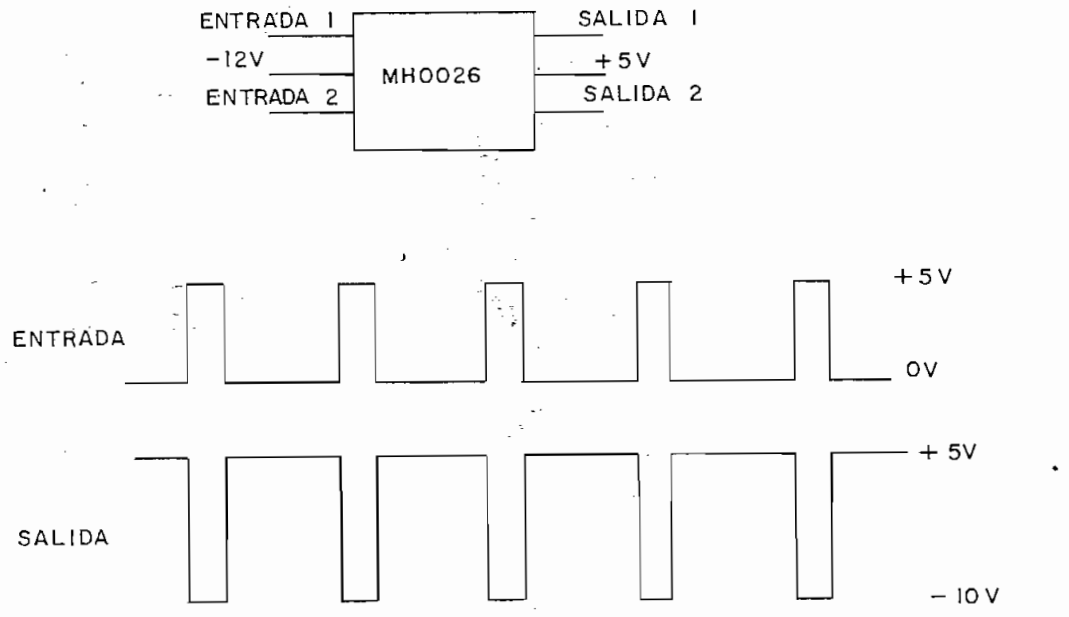


FIG. Nº 60

Este amplificador produce una inversión de la señal, característica que se detalla en la sección correspondiente al sistema de control.

La tabla de estados para control de entrada-salida se -

presenta en la figura Nº 61. Existen cuatro posibilidades, sinembargo necesitamos únicamente dos en el presente trabajo, consiguiendose de esta manera simplificar el diseño y el costo total.

WRITE	READ	FUNCION
0	0	RECIR. SAL. '0'
0	1	RECIR. SAL. DATO
1	0	ESCRIT. SAL. '0'
1	1	LECTURA SAL. '0'

FIG. Nº 61

Cada pulso de reloj $\emptyset_2$ para la entrada de datos, permite el ingreso de un bit-dato, miéntras el comando WRITE permanezca en 1_L. Si WRITE es igual a 0_L, los datos ya presentes en el registro son recirculados. La señal READ habilita la salida (sincronizado por $\emptyset_1$) sin afectar la recirculación.

Los registros tienen capacidad para 1024 bits, cada uno. Se utilizan 8 registros de memoria (uno por cada bit de la etapa de conversión analógico-digital). La memoria del presente trabajo tiene una capacidad de 8192 bits datos.

Una vez almacenados los datos, para presentarse al osciloscopio deben cambiar de su forma digital a analógica. La última etapa constituye la etapa de conversión digital-analógico.

3.1.c.4 CONVERSOR DIGITAL ANALOGICO DE SALIDA

Como elemento conversor de esta etapa se trató de utilizar el DAC100CCT1, pero el realizar pruebas previas de montaje resultó afectado definitivamente. Un buen sustituto es el MC1408 , con el circuito presentado en la figura Nº 62.

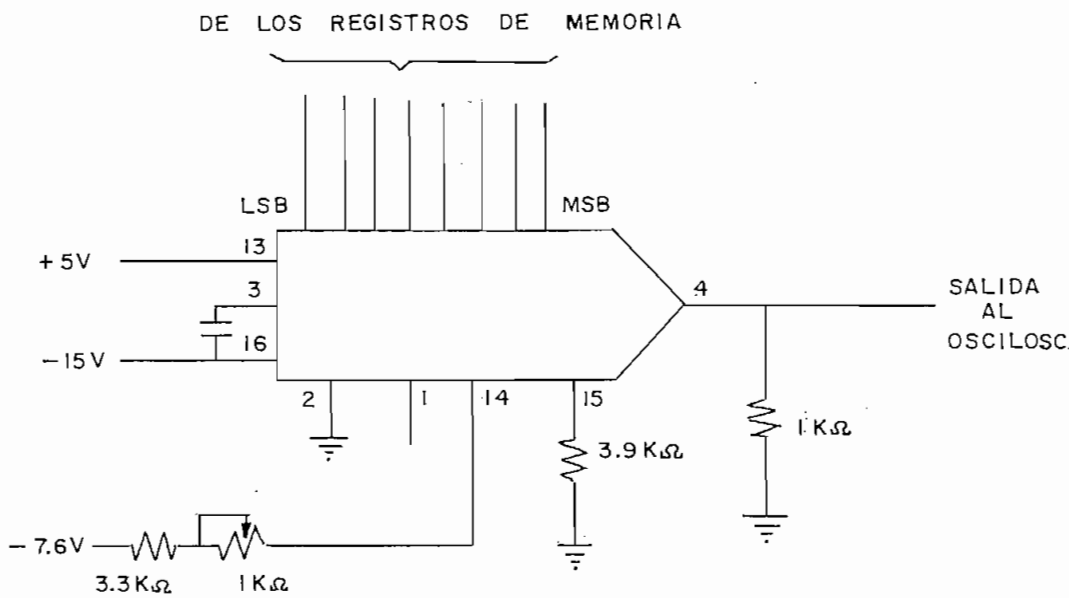


FIG. Nº 62

De las hojas de datos, sabemos que el rango de voltaje a la salida depende de la polarización, así se obtiene de -o.6v a + o.5 v conectando el pin 1 a tierra, y una salida de -5v a + o.5 v dejando este pin. En ambos casos se limita el voltaje positivo a + o.5 V; respecto al voltaje negativo conviene optar por el mayor rango pues de este modo se obtendrá una señal de mayor amplitud. La salida de esta etapa pasa directamente a presentarse en el osciloscopio. Será conveniente mantener la escala para vertical del osciloscopio en 25o mv/división, para que la salida a escala completa cubra la pantalla en toda su amplitud.

3.1.e S I S T E M A D E L R E L O J

3.1.e.1 FRECUENCIA DE MUESTREO

La grabación debe realizarse según la rápidez con que varíe la información, desde una variación lenta hasta algo rápida.

La frecuencia máxima de muestreo está limitada por los circuitos digitales y de conversión. Para el presente trabajo las demoras están dadas por el convertidor DA (200 ns), el comparador (200 ns) y el registro de aproximaciones sucesivas (30 ns) El tiempo para la conversión de un bit es aproximadamente 0.5 us. Se tiene 8 bits por lo que el tiempo total para cada conversión

es de 4 us. A éste debe agregarse el tiempo que emplea el proceso de muestreo 1 us. Luego para cada muestra:

$$t_{convers./muestra} = 8 \times 0.5 + 1 = 5 \text{ us.}$$

La frecuencia máxima de muestreo será:

$$f_{Máx\ muestreo} = 200 \text{ KHz.}$$

Señales de entrada de hasta 100 KHz pueden ser recuperadas sin pérdida de información.

Considerando que se toman 1000 muestras en cada barrido del osciloscopio se tiene para esta frecuencia un tiempo de grabación de 5 ms. por barrido.

Con una frecuencia mínima de reloj de 500 Hz, tendremos:

$$f_{Mín\ reloj} = 0.5 \text{ KHz.}$$

$$t_{conv./muestra} = 2 \text{ ms.}$$

El tiempo de grabación será de 2 seg./barrido.

Este rango resulta muy conveniente para el estudio de transitorios en sistema de potencia. La presentación de los datos en el osciloscopio debe parecer estable, ésto se consigue si se tienen una presentación de 200 barridos/seg. se presentan 1000 mues-

tras por barrido entonces:

200 barr/seg x 1000 muest/barrido = 200000 mues
tras/seg.

La frecuencia de reloj esta determinada por la frecuencia de muestreo. Se necesitan 8 pulsos de reloj para cada conversión, y uno o dos pulsos para cambio de estado en el RAS, si consideramos dos pulsos se tendrán 10 pulsos de reloj para cada conversión.

$$f_{reloj} = 10 \times f_{muestreo}.$$

Se necesita un oscilador de onda cuadrada, con una frecuencia como la indicada anteriormente. Existen diferentes tipos de circuitos que nos permiten conseguirlo, con elementos discretos o con circuitos integrados. Los niveles de voltaje, deben estar comprendidos en los rangos standard de la técnica TTL : 0 v. para el nivel inferior y + 5v. para su nivel superior.

El circuito presentado en la figura Nº 63 que utiliza -- circuitos NAND presenta resultados muy satisfactorios.

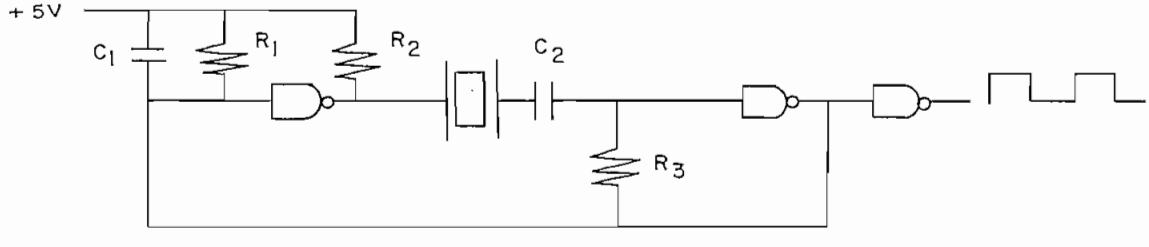
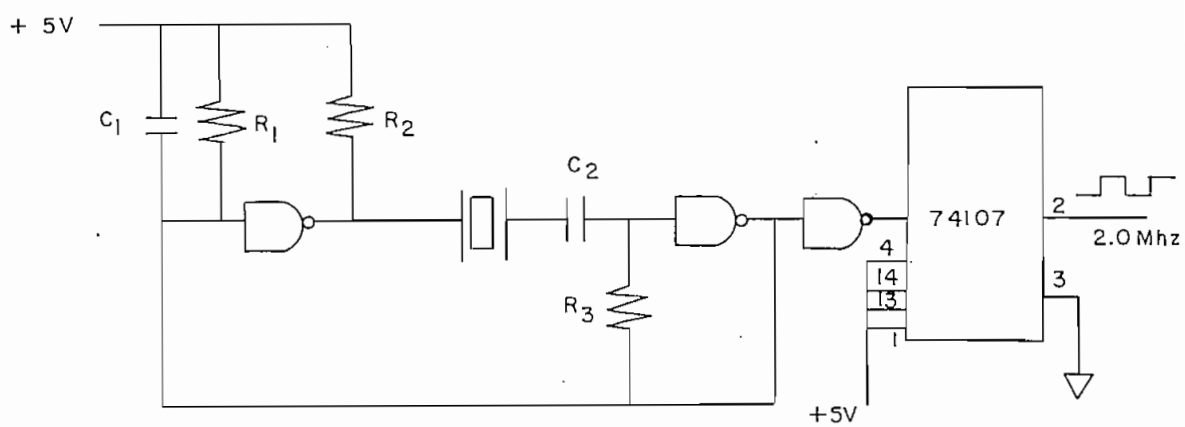


FIG. Nº 63

Es un oscilador controlado por cristal que estabiliza la frecuencia de oscilación. El cristal debe tener una frecuencia - de oscilación igual al valor calculado o muy próximo. Para el - presente trabajo no se pudo contar con un cristal de tal frecuencia, se disponía de un cristal con una frecuencia de oscilación de 4.018 MHz (el más aproximado). Utilizan un divisor de frecuencia por dos (SN74107) con el circuito que se presenta en la figura Nº 64 experimentalmente se consiguió una frecuencia de 2.0MHz, valor muy aceptable para el presente trabajo.



C_1 = .001 uF

C_2 = 120 pF

R_1 = 560Ω 1/2 W

R_2 = 280Ω 1/2 W

R_3 = 100Ω 1/2 W

CRISTAL f = 4018 Khz

FIG. Nº 64

La corriente que consume este circuito es de 30 mA. La - disipación en las resistencias es muy baja por lo que se tomaron resistencia de 1/4 de watt por facilidad de conseguirse en el mercado local.

Para señales que no varíen muy rápidamente en el tiempo, no se necesitará una frecuencia de muestreo de este orden, sino valores menores, los mismos que pueden conseguirse con una etapa de división de frecuencia.

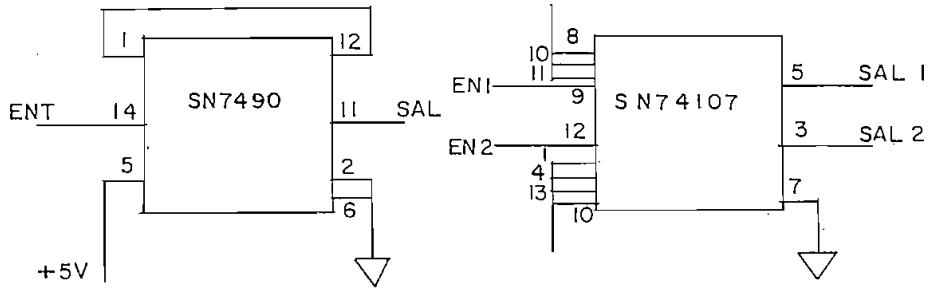
Una escala de valores como se indica en la figura Nº 65 - resulta muy conveniente, pues son valores muy familiares para un usuario del osciloscopio.

f reloj (Khz)	f muest.(Khz)	t reloj (ms)	t muest.(ms)	barri-ms/div
2000	200	.5	5	.5
1000	100	1	10	1
500	50	2	20	2
200	20	5	50	5
100	10	10	100	10
50	5	20	200	20
20	2	50	500	50
10	1	100	1000	100
5	.5	200	2000	200

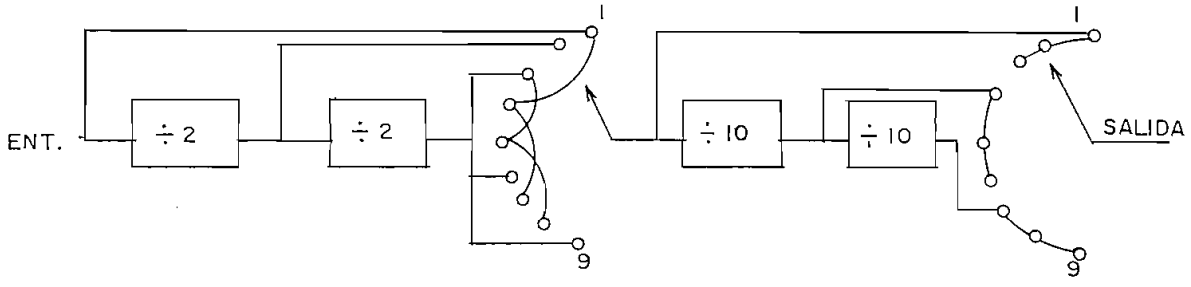
FIG. Nº 65

Los factores de división indicados pueden conseguirse con dos divisores por 10 y dos divisores por 2. De los diferentes divisores que existen en el mercado se eligió para divisor por 10 el SN 7490A y como divisores por 2 el SN 74107 (circuito dual),- sus características son muy compatibles al presente diseño.

El circuito que permite su funcionamiento se presenta en la figura Nº 29. Además se requiere un sistema de conmutación, el mismo se presenta en la figura Nº 66.



(a)



POSICION	BARR.ms/div
1	.5
2	1
3	2
4	5
5	10
6	20
7	50
8	100
9	200

FIG. Nº 66

3.1.c.2 DIVISOR DE FRECUENCIA

De la señal de reloj que se tiene, se obtienen las otras señales de control:

a) Control para el proceso de conversión A/D

b) Control para el sistema de muestreo.

c) Control para I/O de datos de la memoria.

SEÑAL DE CONTROL PARA EL PROCESO DE CONVERSION A/D.-

Esta señal debe controlar el registro de aproximaciones sucesivas (Am 2502) con las características que se presenta en - la figura Nº 67.

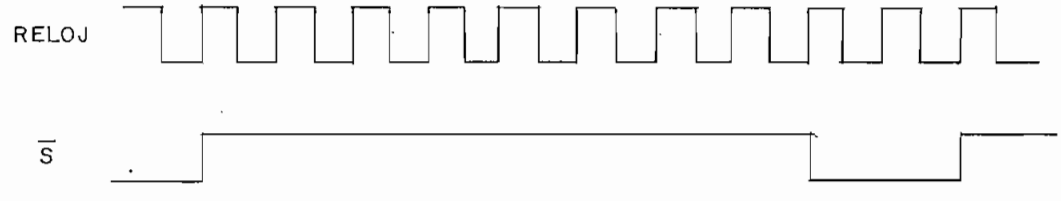


FIG. Nº 67

El registro Am 2502 produce una inversión de la señal S, debe entregarse al registro la señal $\bar{S}$. (complemento de S).

Esta señal puede obtenerse muy fácilmente con un contador módulo 10 por las características que presenta el SN7490 resulta muy apropiado, el circuito utilizado que se presenta en la figura Nº 68.

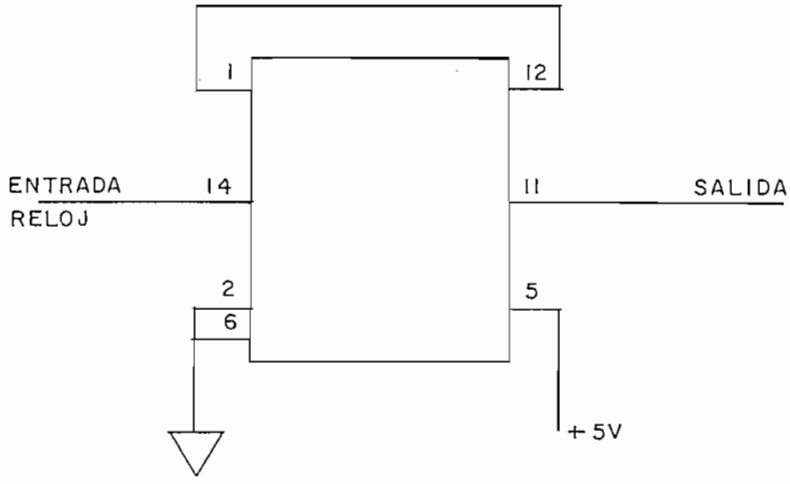
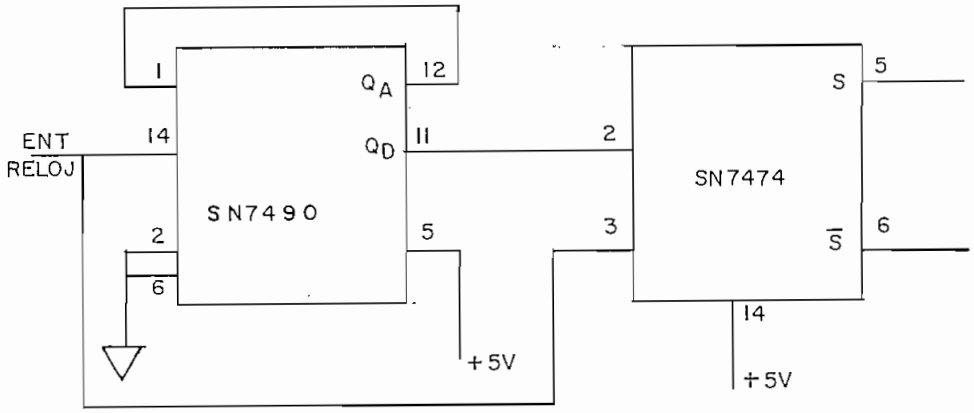
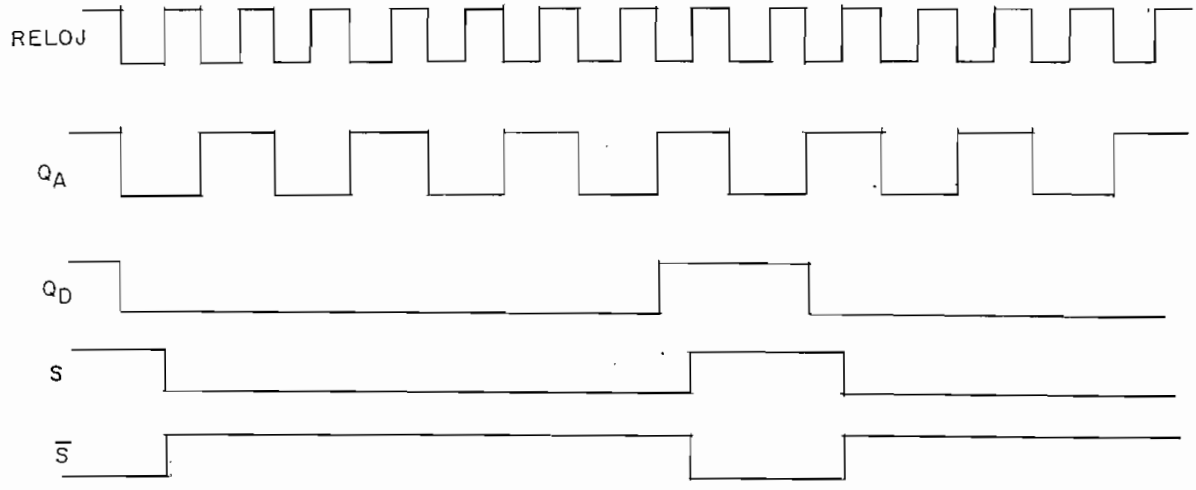


FIG. Nº 68

Esta señal debe retrasarse 1/2 pulso de reloj,para esto se utiliza un SN7474 (dispositivo dual) con la conección que se presenta en la figura Nº 69.



(a)



(b)

FIG. Nº 69

En la parte (b) de la figura Nº 32 se presentan las señales que se considerarán posteriormente. De este circuito se obtiene la señal $\overline{S}$.

CONTROLES PARA E/S DE DATOS DE LA MEMORIA.

Son necesarios 4 controles: dos para ingreso de datos y dos para salida de los mismos.

Uno de los controles para ingreso de datos es $\emptyset_2$, con cada pulso de este reloj ingresa un dato a la memoria, mientras el otro control para entrada permanece en su nivel alto (WRITE). -- Las transiciones de la señal WRITE deben realizarse durante las transiciones negativas de $\emptyset_2$.

Para la salida de datos, similarmente existen una señal de reloj, cada pulso de la misma permite la salida de un dato, - mientras la otra señal permanece en su nivel alto (READ). Ante-- riormente se indicó la conveniencia de mantener la señal de control READ en un voltaje fijo alto 1_L.

Se concretará el estudio a las señales $\emptyset_1$, $\emptyset_2$ y WRITE. - Por cada conversión A/D de una muestra se obtienen 8 bits, estos deben almacenarse en los registros de memoria (1 por cada bit).

Las señales de control para entrada y salida de datos -- de la memoria deben ser aplicadas simultáneamente a los 8 registros.

Las señales necesarias para $\bar{S}$, $\emptyset_1$, $\emptyset_2$ se indican en la - figura Nº 70.

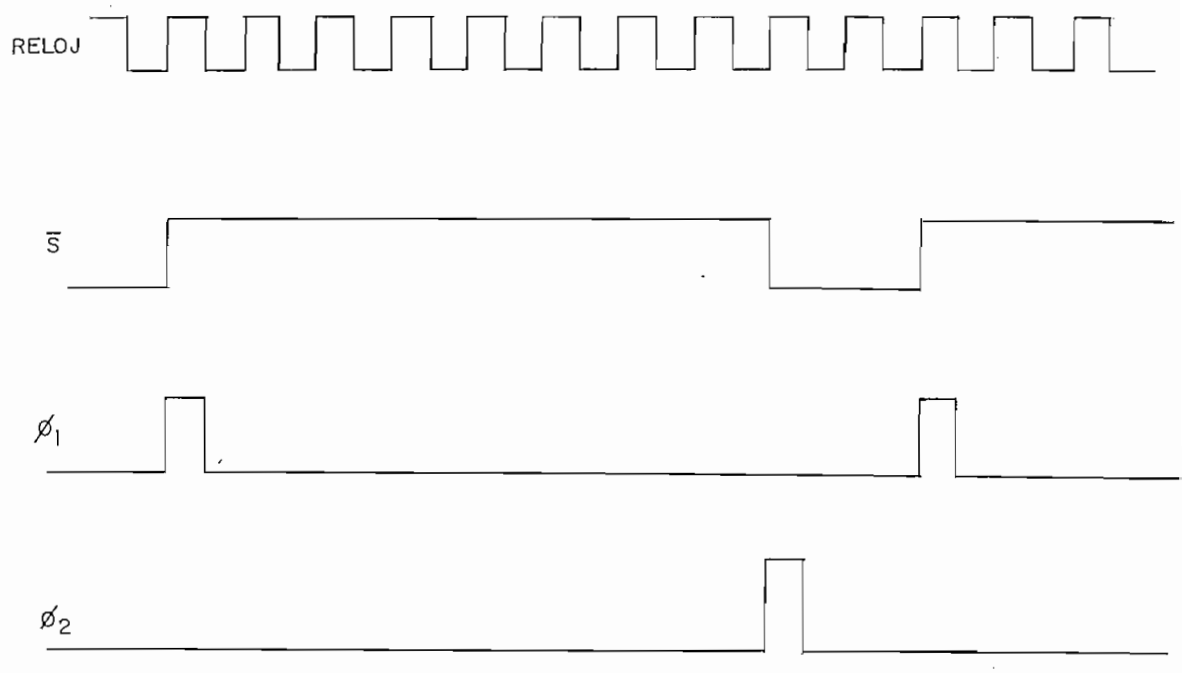


FIG. Nº 70

Para obtener ϕ_1 y ϕ_2 se dispone de las señales indicadas en la figura Nº 69 si además de estas disponemos de T y $\bar{T}$ como se indica en la figura Nº 74, podemos obtener $\phi_1 = \bar{S} \times T$ y -- $\phi_2 = S \times T$.

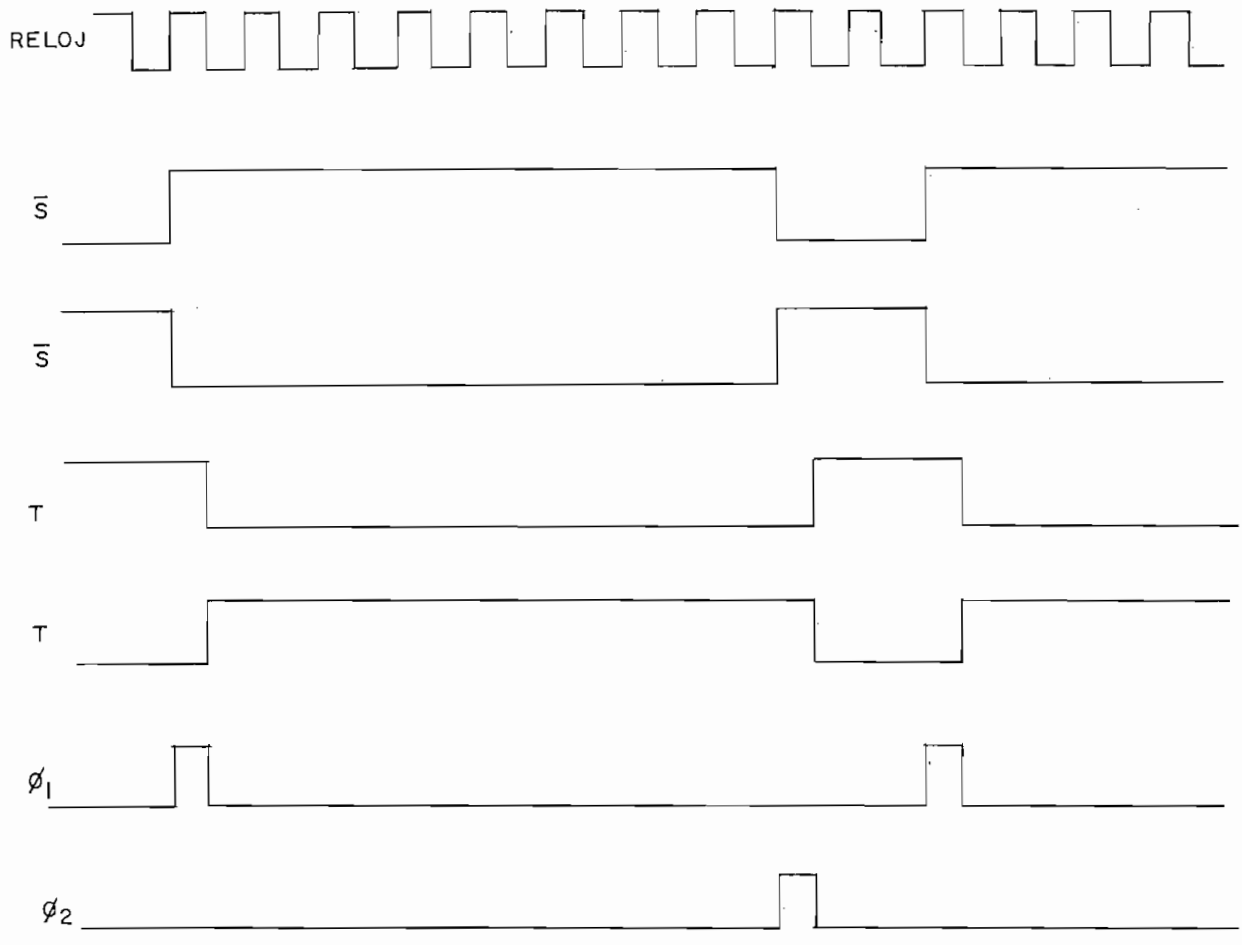
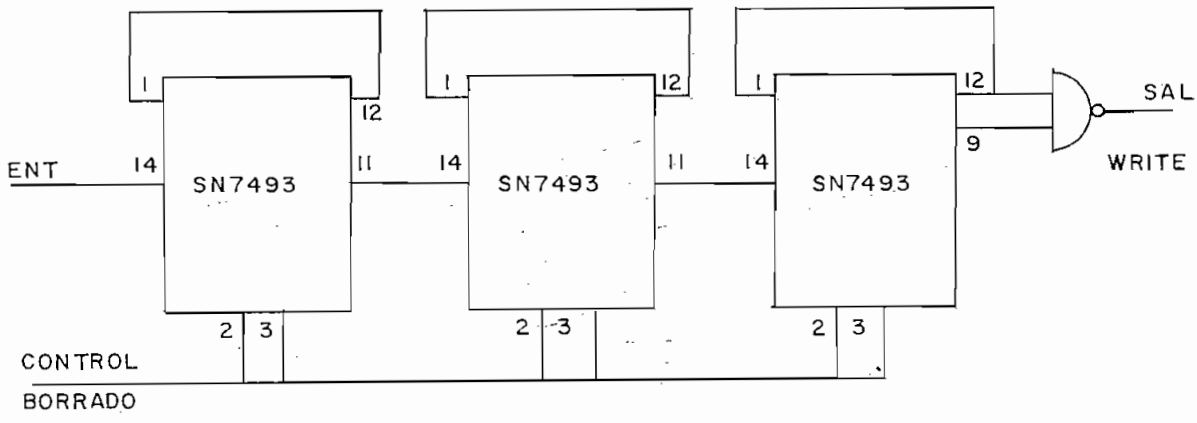


FIG. Nº 74

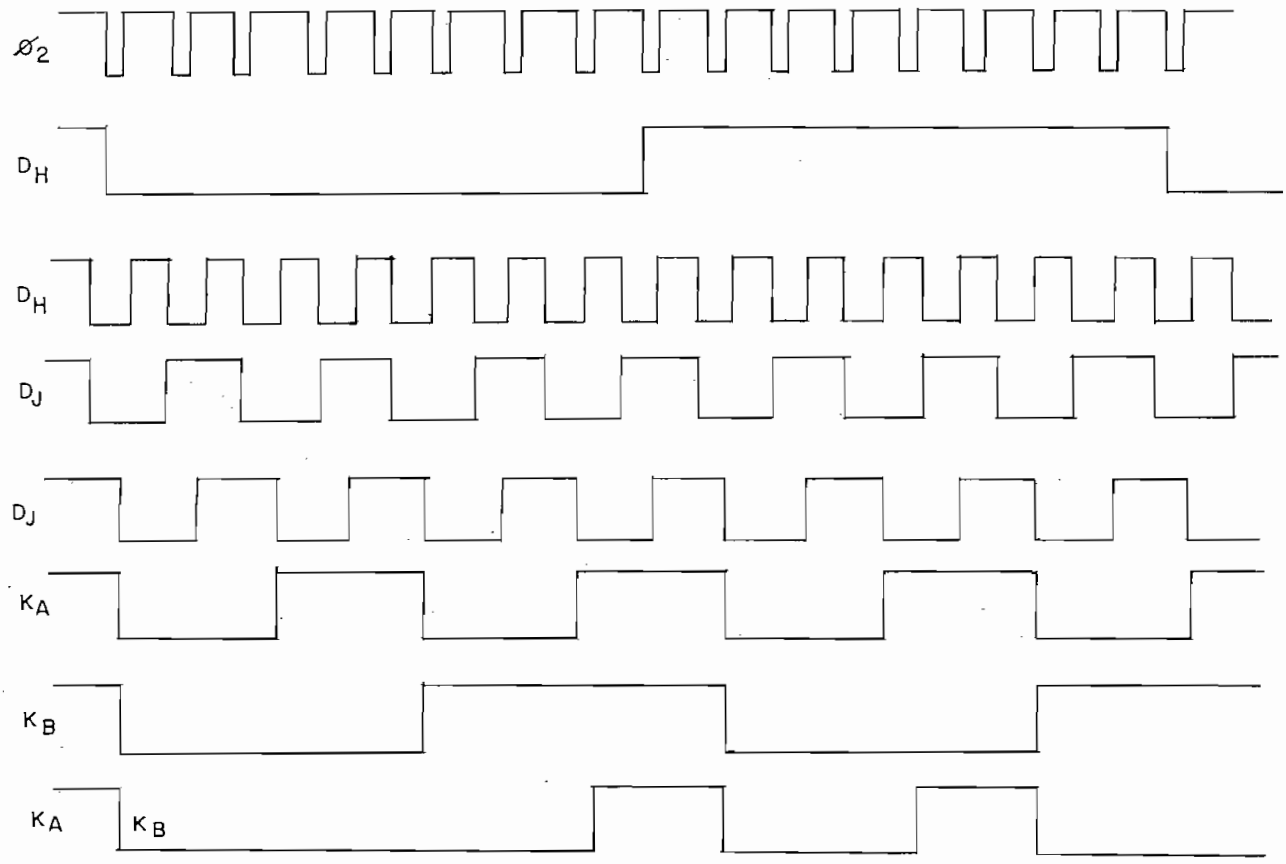
Las señales T y $\overline{T}$ se obtienen con un circuito SN 7474, como se indica en la figura Nº 72.

Este es un elemento dual y el un registro se utilizó anteriormente.

dulo 4. El circuito se presenta en la figura Nº 74 (a) y el diagrama de tiempos en la parte (b).



(a)



(b) FIG. Nº 74

trada está determinada por el ancho del pulso de salida. De los datos proporcionados, para el presente caso se necesita un con-- densador de 500 pF. El diagrama se presenta en la figura Nº 73.

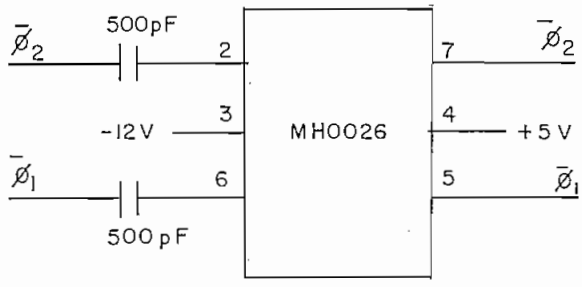


FIG. Nº 73

La señal de control WRITE que permite el ingreso de datos cuando se mantiene en su nivel alto (impide cuando está en su nivel inferior) ingresando un dato con cada pulso de reloj ϕ_2. Los registros de memoria tienen una capacidad para 1024 bits, y la - señal WRITE debe permanecer durante ese intervalo en su nivel superior (1_L). Se utilizan dos contadores de 16 y un contador de 4.

Como contadores módulo 16 se utliza los SN7493, con una conección adecuada se puede utilizar este mismo contador como mó

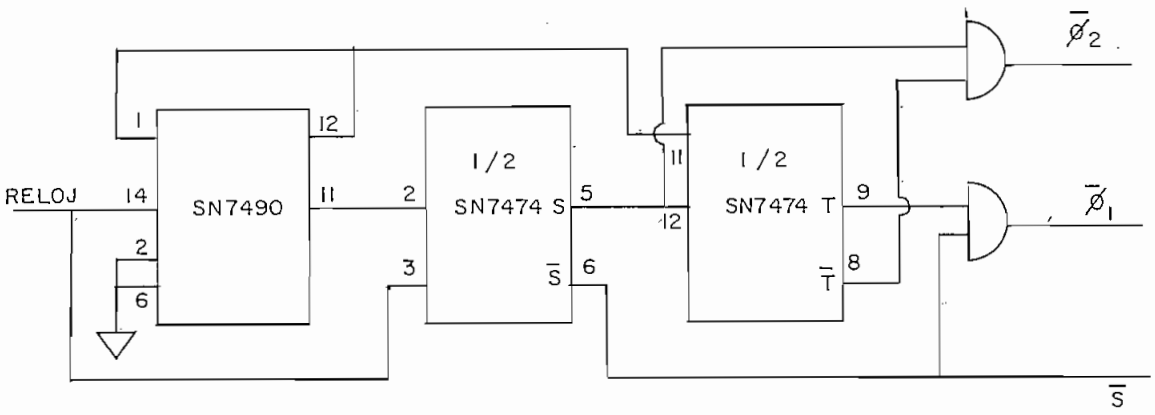


FIG. Nº 72

Las señales de control que se han obtenido, tienen niveles de voltaje correspondientes a la lógica positiva. Los registros de memoria requieren que las señales de reloj ϕ_1 y ϕ_2 tengan un nivel superior de voltaje comprendido entre + 4.0 v y +5.3 y el nivel inferior entre -12.0 v y -10.0v. Para lograr esto se utiliza un amplificador dual de propósito especial el MH0026. Con una polarización de V_{cc} = + 5v y V_{ee} = - 12v se obtienen niveles de salida de + 4.3 y - 11.5 v. para las señales de reloj.

El fabricante aconseja para valores negativos de V_{ee} un acoplamiento ac capacitivo. La selección de este capacitor de en

En cuanto al control automático de grabación de la señal debe grabarse la misma, en cuanto esta supere determinado nivel relativo graduable manualmente.

Para conseguir esto debe tomarse la señal de entrada y -- compararla con un voltaje de referencia. Para la comparación es - conveniente tomar la señal luego de la etapa de atenuación-amplificación porque presenta niveles adecuados por operarse (-4v, - + 4v). Por el rango de variación de esta conviene compararla con un voltaje dentro del mismo rango, por ejemplo + 5v que se utiliza para polarización de la parte digital.

El elemento de comparación debe ser muy confiable y que presente compatibilidad con el trabajo efectuado. Anteriormente se utilizó con bueno resultados el CMP01CJ, se utilizará este -- elemento en esta etapa. Este circuito de disparo debe controlar la señal WRITE. Es posible que se presenten más de una variación - de la señal capáz de producir un disparo, unicamente la primera - variación debe activar el dispositivo. Se utiliza un circuito eliminador de rebotes diseñado con dos NAND como se indica en la figura Nº 75.

Se presenta tanto el control para grabación como los circuitos que permiten obtener la señal de comando WRITE.

La grabación de la señal se realiza en forma contínua, -

cuando se activa la señal de disparo, se permite el ingreso de - 768 bits a cada registro de desplazamiento (768 muestras). Las - 256 muestras anteriores son consideradas como parte de la señal grabada.

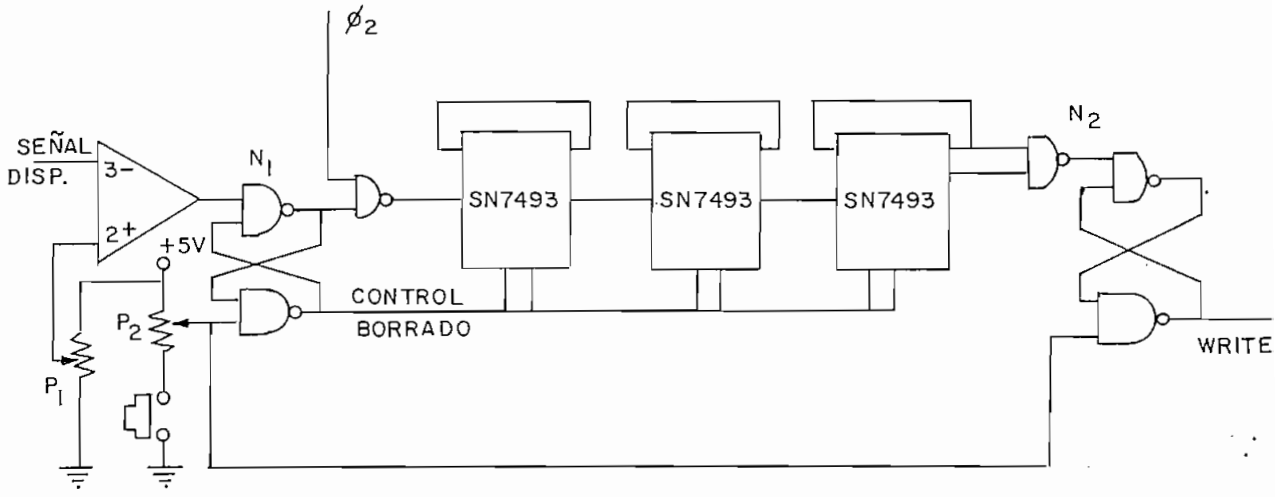


FIG. Nº 75

El ponteciómetro P_1 proporciona el nivel de referencia regulable manualmente entre 0 v y 5 V. Del comparador se obtiene un nivel correspondiente a 0_L o a 1_L según la señal ha superado o nó el nivel de referencia. El otro potenciómetro P_2 permite un - ajuste para el correcto funcionamiento del dispositivo, el pulsador permite iniciar el conteo para generar el comando WRITE.

El eliminador de rebotes N_1 controla el paso de ϕ 2 a los contadores. Se presenta en la figura Nº 76.

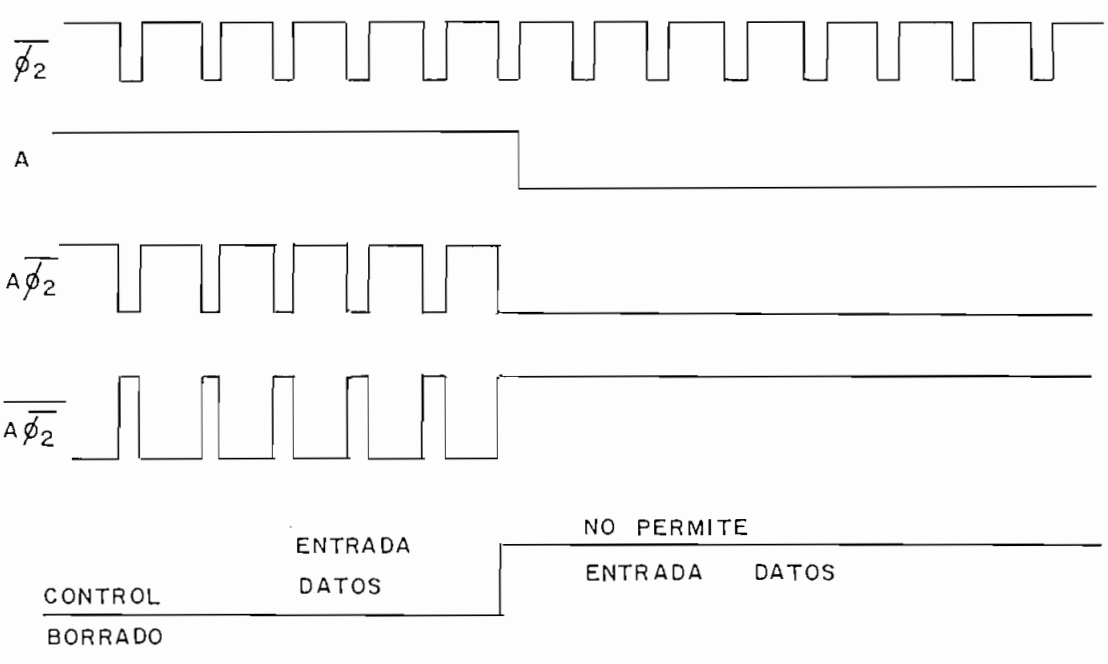


FIG. Nº 76

La señal de control para borrado pone las salidas a nivel 0_L con Ro(1) y Ro(2) en 1_L, la señal para este control se obtiene de la otra salida del eliminador de rebote N_1.

Considerando K_A K_B de la figura (b) del segundo eliminador de rebote, se obtiene la señal de comando WRITE, como se indi

ca en la figura Nº 77.

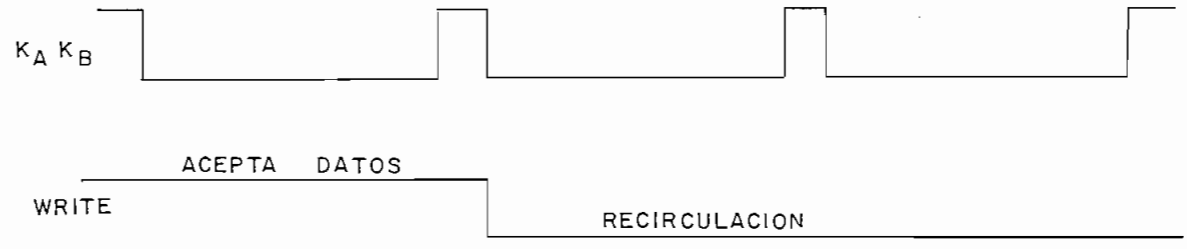


FIG. Nº 77

De la otra salida del eliminador de rebotes, se toma la señal que servirá para sincronisar la señal en el osciloscopio.

3.3. CONSIDERACIONES PRACTICAS DE DISEÑO

La disposición física de los elementos es muy importante, es necesario distribuir los mismos de modo que su interferencia sea mínima.

Las fuentes de alimentación deben ser aisladas no solo - físicamente sino eléctricamente. El espacio que contenga dichas fuentes debe blindarse. El sistema de atenuación es muy susceptible a interferencias por lo que será conveniente aislarle física mente del resto del sistema.

En cuanto a la distribución física de los elementos, debe realizarse de modo que no se tengan partes analógicas y digitales indistintamente colocadas.

Es conveniente disponerlos lo más separados e independientes posibles y tratar de que sus conecciones no se intercepten.

Las conecciones a tierra tanto de la parte analógica como de la digital no debe ser comunes excepto en un solo punto en el chasis.

El amplificador de entrada tenía la siguiente configuración:

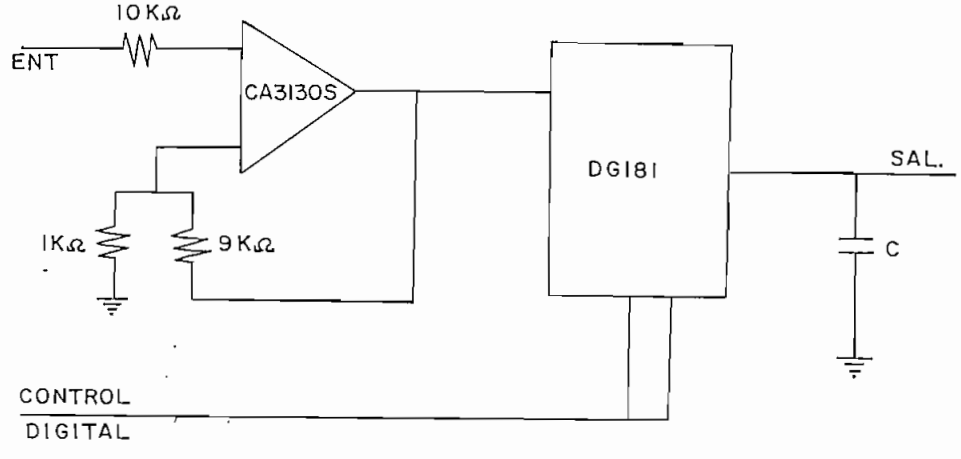


FIG. Nº 78

La corriente suministrada por el amplificador operacional CA3130S no es suficiente para cargar el condensador de muestreo rápidamente. Esto implica errores en el muestreo. Para solventar este problema se utiliza un seguidor de emisor como el que se presenta en la figura Nº 79.

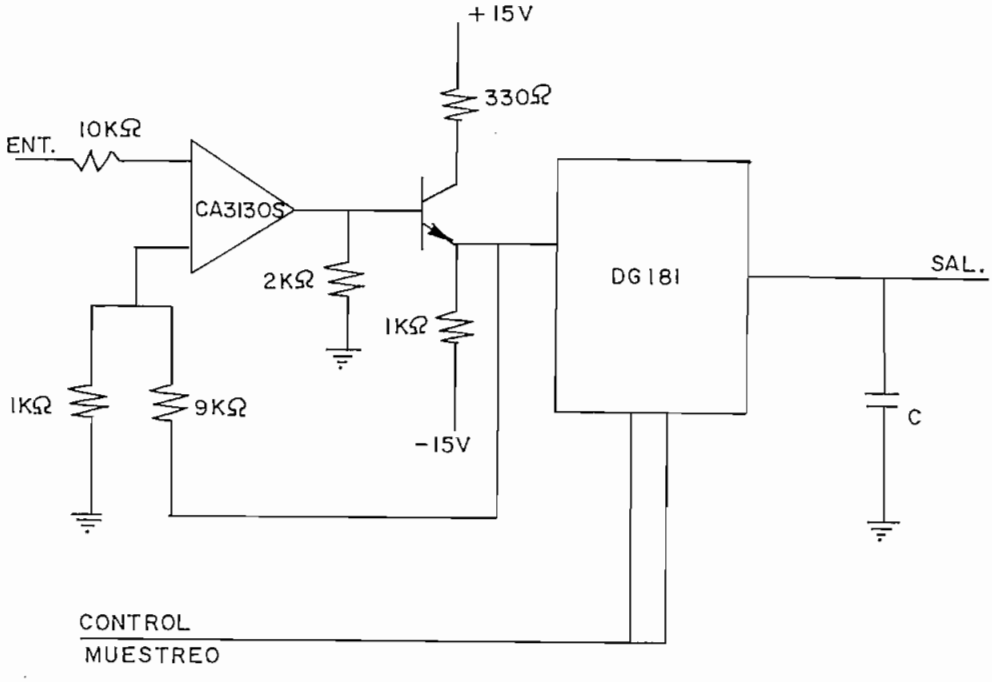


FIG. Nº 79

El circuito utilizado no dió resultados satisfactorios. Fue necesario diseñar un circuito más completo. El mismo que se indica en la siguiente figura.

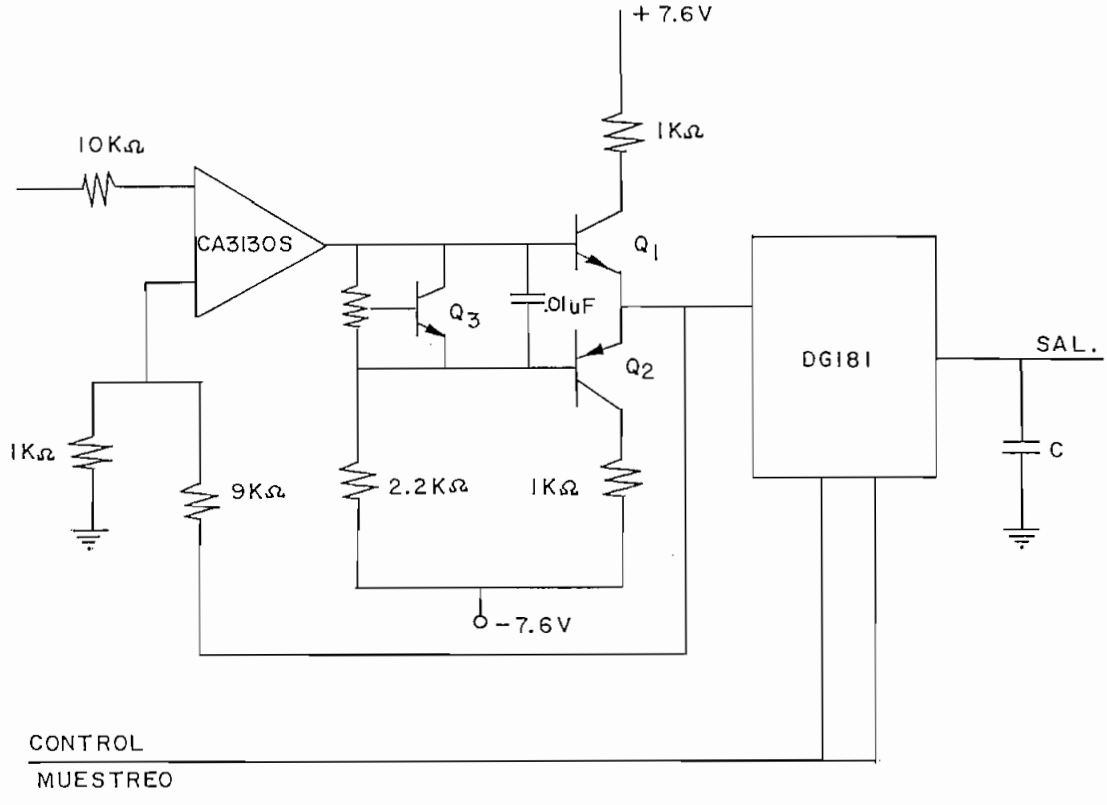


FIG. Nº 80

En este circuito, que opera como seguidor de emisor, la salida presenta una impedancia muy baja. Los transistores Q_1 y Q_2 operan alternativamente con la señal Q_1 durante los hemiciclos positivos y Q_2 en los negativos. Deben ser transistores simétricos complementarios. Para su funcionamiento correcto, la diferencia de potencial entre las bases de Q_1 y Q_2 debe ser $2V_{BE}$ = 1.2 v. Variaciones en la temperatura ambiente no debe alterarlo.

Para mantener esta diferencia de potencial se utiliza Q_3 y el potenciómetro. Para un mejor resultado Q_3 debe ir físicamente pegado a Q_1 ó Q_2.

Un incremento de temperatura ambiente, hace que circule mayor corriente por el emisor (Q_1 y/ó Q_2), a su vez V_{BE} disminuye. Simultáneamente se incrementará la corriente el emisor de Q_3, disminuyendo V_{CE} de Q_3, esto es la diferencia de potencial entre las bases de Q_1 y Q_2, lo cual impide un incremento de corriente en tales transistores.

La salida del seguidor de emisor no debe contener componentes DC, para no alterar la información, o sea:

$$V_{E1} = V_{V2} = 0 v$$

Utilizando transistores de Si.

$$V_{BE} = 0.6 v$$

Asumiendo $V_{CE} = V_{CC}/2$ para que los transistores operen en región lineal.

$$V_{CE} = 3.8 v$$

Es necesario limitar la corriente de Q_1, a uno 4 mA.

$$R_{C1} = 3.8/4 \text{ mA} = 0.95 K\Omega$$

$$R_{C1} = 1\ K \quad 10\%$$

Similarmente

$$R_{C2} = 1K \quad 10\%$$

Para polarizar la base de Q_2, se emplea R_{B2}. Asumiendo - $I2 = 3$ mA.

$$R_{B2} = \frac{7.6 - 0.6}{3\ mA} = 2.3\ K$$

$$R_{B2} = 2.2.\ K \qquad 10\%$$

La oorriente a travéz del potenciómetro P_1 debe ser muy - pequeña, en el orden de uno 0.3 mA.

$$P_1 = \frac{1.2\ v}{0.3\ mA} = 4\ K\Omega$$

La base de Q_3 debe conectarse aproximadamente a la mitad del potenciómetro.

El condensador de 0.01 μF se utiliza para evitar la interferencia de componentes de mayor frecuencia.

Se utilizan fuentes balanceadas para procurar mayor estabilidad térmica.

El circuito diseñado es capáz de suministrar la suficiente corriente para cargar el condensador de muestreo rápidamente.

Se comprobó que el conmutador analógico DG 181 no funcionaba por fallas de fabricación. El tiempo que se tardó en conseguir este elemento (6 meses), implica el diseño de un circuito muestreador con elementos discretos disponibles.

Un circuito utilizado para muestreo en frecuencia intermedias, está constituído por un puente de diodos y un sistema de - control para activar el puente durante los tiempos de muestreo. El circuito utilizado se presenta en la siguiente figura.

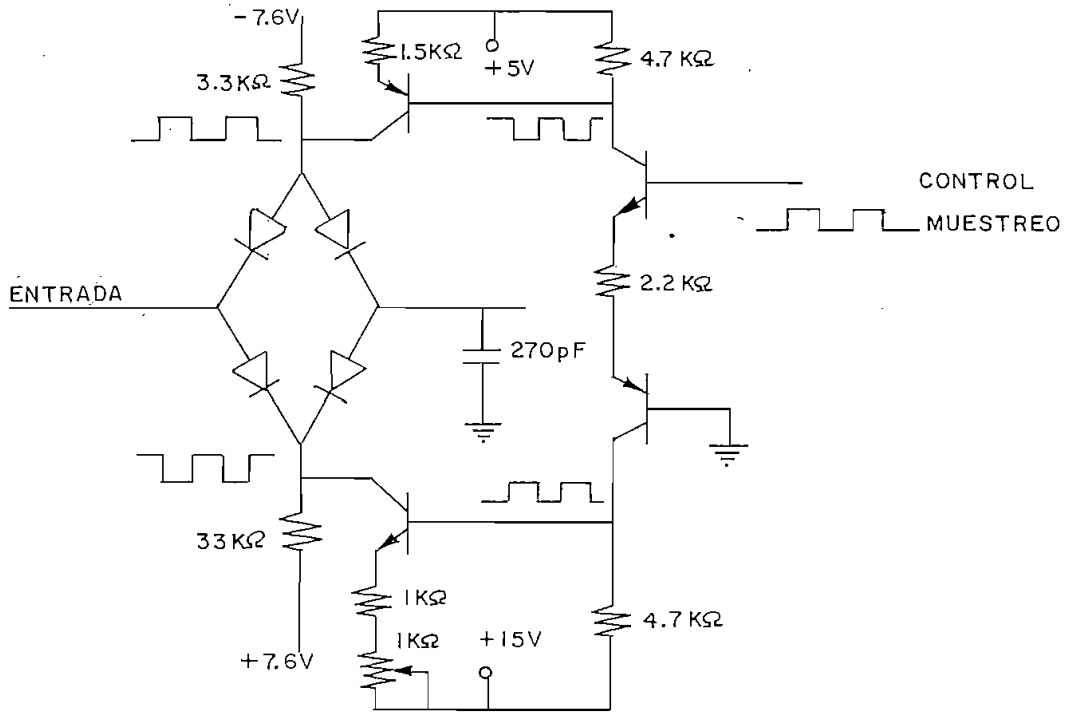


FIG. Nº 81

El circuito básico de conmutación está dado por un puente de diodos. Para activar los mismos deben entregarse pulsos para control de muestro, como se indica en la figura que sigue:

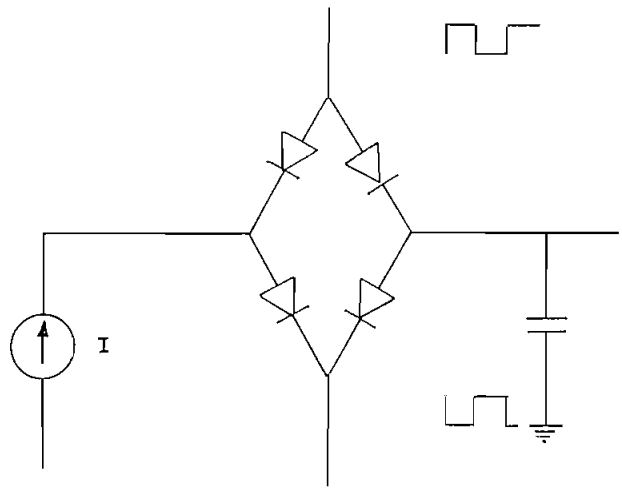


FIG. Nº 82

Las señales para control de muestreo pueden obtenerse de los circuitos integrados utilizados para el efecto. Esta señal no es entregada con la suficiente corriente como para controlar el puente.

Un circuito que nos permite amplificar estos pulsos se presenta en la figura que sigue:

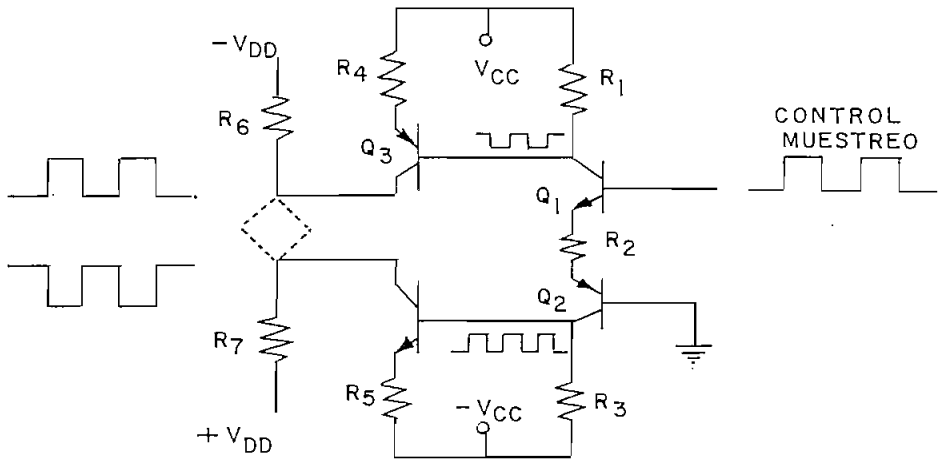


FIG. Nº 83

Es un circuito amplificador-inversor de los pulsos para el control de muestreo, formado por dos transistores simétricos

complementarios Q_1 y Q_2 que actúan como interruptores controlados. Los transistores Q_3 y Q_4 actúan como amplificadores de los pulsos positivos y negativos respectivamente. Se han elegido los transistores npn 2ñ3704 y pnp 2N3702, considerando su simetría en cuanto a β , hi y respuesta a variaciones rápidas en las señales.

La señal de control se obtiene de circuitos TTL standard, con una amplitud de voltaje aproximado de 3.5 v. Los pulsos que deben activar el puente deben ser simétricos y de sentidos opuestos.

Si se limta $I_1 = 1$ mA

Considerando los pulsos de reloj, con una amplitud de 3.5v

$$V_{B1\ (MAX)} = V_{BE1} + V_{BE2} + I_1 R_2 = 3.5 \text{ v}$$

$$V_{BE1} = V_{BE2} = 0.6 \text{ v}$$

$$R_2 = \frac{3.5 - 1.2}{1 \text{ mA}} = 2.3$$

$$R_2 = 2.2.\ \text{K}\Omega \quad 5\%$$

Asumiendo $V_{CE} \simeq 8$ v

$$R_1 = \frac{V_{cc} - (V_{BE1} + V_{E1})}{I_1}$$

$$R_1 = \frac{15 - (8 + 2.8)}{1 \text{ mA}} = 4.2$$

$$R_1 = 4.7\ K\Omega\ \ 5\%$$

De igual manera:

$$R_3 = 4.7\ K\Omega\ 5\%$$

Las resistencias R_4 y R_5 se utilizan como limitadoras de corriente. Asumamos $I_4 = 3$ mA.

$$R_4 = \frac{3.5 - .6}{3\ mA} = \frac{2.9}{3} = 1\ K$$

$$R_4 = R_5 = 1\ K\Omega \qquad 10\%$$

Las resistencias R_6 y R_7 se utilizan para mantener los diodos inversamente polarizados mientras los pulsos de control estan en el nivel inferior. En el mismo instante sirven para descargar rápidamente la capacitancia parásita de los diodos.

El amplificador operacional CA3130S que se utilizó como seguidor de voltaje del condensador de muestreo, no entregaba la suficiente corriente para operar el CAD. Fue necesario colocar un seguidor de emisor a la salida del amplificador operacional, como el que se indica en la siguiente figura.

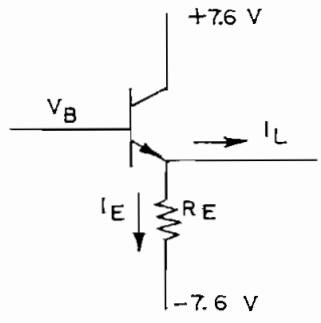


FIG. Nº 84

La salida debe entregarse sin componente DC, luego:

$$V_E = 0v$$

$$V_{BE} = 0.6\ v$$

Para que opere en clase A

$$V_{CE} = 7.6\ v$$

Asumiendo $I_E = 10\ mA$

$$R_E = 7.6/10\ mA = 760\Omega$$

$$R_E = 780\Omega \quad 5\%$$

El CDA de salida no responde satisfactoriamente a señales que varían rápidamente (60 KHz). La variación correspondiente al bit más significante no es muy bien transformada apareciendo una espiga en la señal analógica de salida, con una amplitud aproximada de 0.25 v. Para eliminar la misma se utiliza un filtro pasa bajos como el que se presenta en lafigura que sigue.

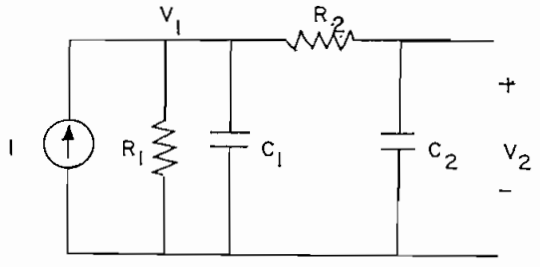


FIG. Nº85

Planteando las ecuaciones de nodos:

$$V_1 \left(\frac{1}{R_1} + \frac{1}{R_2} + S C_1 \right) - V_2 \frac{1}{R_2} = I$$

$$- V_1 \frac{1}{R_2} + V_2 \left(\frac{1}{R_2} + SC_2 \right) = 0$$

$$V_2 = \frac{I \frac{1}{R2} R_1 R_2}{1 + S (C_1 R_1 + C_2 R_2) + SC_2 R_1 + S^2 C_1 R_1 C_2 R_2}$$

$$\frac{V_2}{I} = \frac{R_1}{1 + S (C_1 R_1 + C_2 R_2 + C_2 R_1) + S^2 C_1 R_1 C_2 R_2}$$

La función característica de un filtro de segundo orden:

$$\frac{V}{I} = \frac{R_1}{1 + 2 \rho \left(\frac{S}{\omega}\right) + \left(\frac{S}{\omega}\right)^2}$$

ρ: Factor de amortiguamiento.

Para el filtro calculado

$$C_1 R_1 = C_2 R_2 = \frac{1}{\omega}$$

$$\frac{V_2}{I} = \frac{R_1}{1 + \frac{2\,S}{\omega}\left(1 + \frac{R_1}{2\,R_2}\right) + \left(\frac{S}{\omega}\right)^2}$$

Factor de amortiguamiento

$$\rho = 1 + \frac{R_1}{2\,R_2}$$

El CAD entrega la señal en corriente 2 mA. Tomando R_1 = 1 K R para tener una señal de salida de 2 v.

La frecuencia de corte consideramos para 100 KH_2.

$$R_1\,C_1 = R_2\,C_2 = \frac{1}{\omega}$$

$$2\,R_2 \gg R_1$$

$$R_1\,C_1 = \frac{1}{2\,\pi\,10^5}$$

$$C_1 = \frac{1}{2\,\pi\,10^8} \qquad C_1 = 1600\ p\,F$$

$$R_2 = 5\ K\Omega$$

$$C_2 = \frac{1}{2\,\pi\,10^8} = .318\ 10^{-9}$$

$$C_2 = 318\ p\,F$$

C A P I T U L O IV

C O N S T R U C C I O N D E L E Q U I P O

En el montaje del equipo se dispusierón los elementos de las diferentes etapas de la memoria de manera que sú interferencia sea mínima. Sinembargo fue necesario realizar algunas modificaciones tanto en el diseño como en la distribución de los elementos.

Para la etapa de atenuación no se pudieron conseguir todos los elementos de precisión. Para alcanzar tales valores fue necesario tomar una resistencia no de precisión y experimentalmente alcanzar el valor calculado, combinando con otra resistencia.

La etapa con factor de atenuación 10 utiliza 111 KΩ , se consigúió dicho valor con una resistencia de 100 KΩ en serie con otra de 10 KΩ .

Para la etapa de atenuación por 100, la resistencia de 990 KΩ se consiguió de una resistencia de 1 MΩ 10% .

En la etapa de conversión analógico-digital, las salidas del registro de aproximaciones sucesivas no entregaban la suficiente corriente, en el nivel lógico superior, a las entradas del DAC100CT. Se colocaron resistencias de 1 KΩ 10%, entre dichas entradas y la fuente de polarización + 5v.

Un problema similar se presentó entre las salidas de los registros de desplazamiento y el CDA de salida. Se procedió como

en el caso anterior.

El problema incial de mayor importancia que debió afrontarse estuvo relacionado con ruidos,tanto por inducción como por acoplamiento a través de las conecciones de tierra.

Inicialmente a la entrada del amplificador de entrada -- (manteniendo desconectada la etapa de atenuación), se tenía una relación señal/ruido = 0.2 .

A pesar de tener un rizado en las fuentes de polarización inferior a un 5%, el ruido presente en los elementos impedía resultado alguno.

El ruido provenía en parte a través de los conductores de polarización, por inducción. Se colocaron condensadores de 0.1μF entre cada punto de polarización de los elementos y tierra. Considerando que las conecciones a tierra sean a la analógica o digital según corresponda. Esta consideración resultó insuficiente, se mantenía una señal considerable de ruido en los puntos de polarización de los elementos.

Se colocaron condensadores electrolíticos de 47μF en paralelo con condensadores de cerámica de 0.1μF a la entrada de - la señal de polarización a cada una de las tarjetas, como se presenta en la figura que sigue.

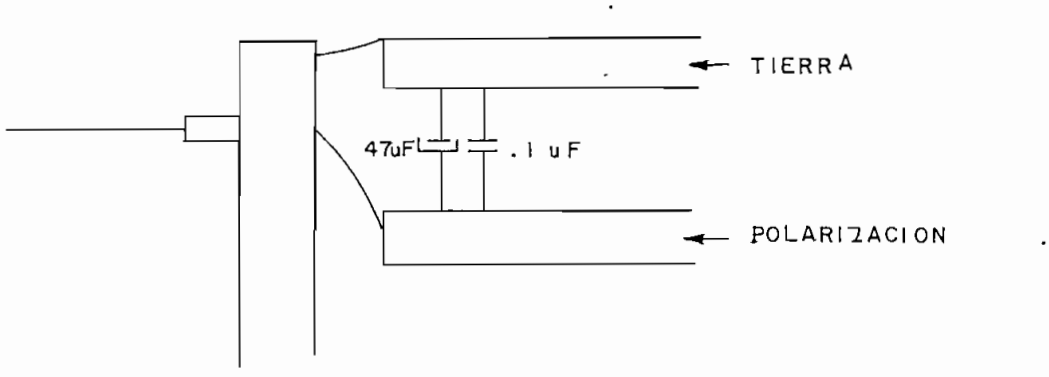


FIG. Nº 86

La señal de ruido se mantenía considerablemente. Debían bloquearse las señales de RF inducidas en los conductores de polarización. Se utilizarón choques, empleando núcleos de ferrita de 100 μH, como se ilustra en la siguiente figura.

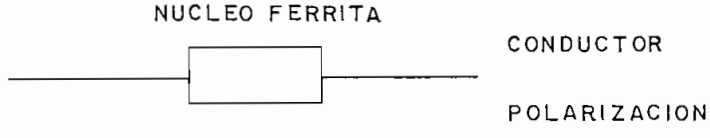


FIG. Nº 87

En estas condiciones se consigue una relación señal/ruido = 1.5. Es posible realizar algunas mediciones para mejorar esta relación. Observando con el osciloscopio dos puntos de tie-

rra, distantes entre sí unos 3 cm se observa una señal de 0.8v pico-pico. Presenta picos más salientes a intervalos regulares coincidentes con el período de las señales de reloj ϕ_2.

El elemento que se utiliza para amplificar las señales de reloj ϕ_1 y ϕ_2, (controlan la entrada y salida de datos a los registros de desplazamiento) debe suministrar las mismas con niveles de corriente relativamente altos. Durante su operación envia pulsos de corriente que llegan a tierra, además los conductores constituyen muy buenas antenas para radiar estas señeles. El primer paso constituye colocar a este elemento físicamente lo más - cerca a los registros de desplazamiento. Esto redujo a 0.5v la - señal medida en las condiciones anteriores.

Debe evitarse que esta señal llegue a la conección de tierra. Para esto los condensadores que inicialmente se conectaron a tierra (de los puntos de polarización de los registros de desplazamiento y del amplificador MH0026), se conectan a las barras de polarización como se indica en la figura que sigue.

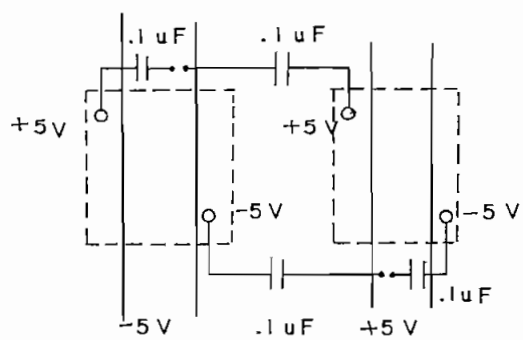


FIG. Nº 88

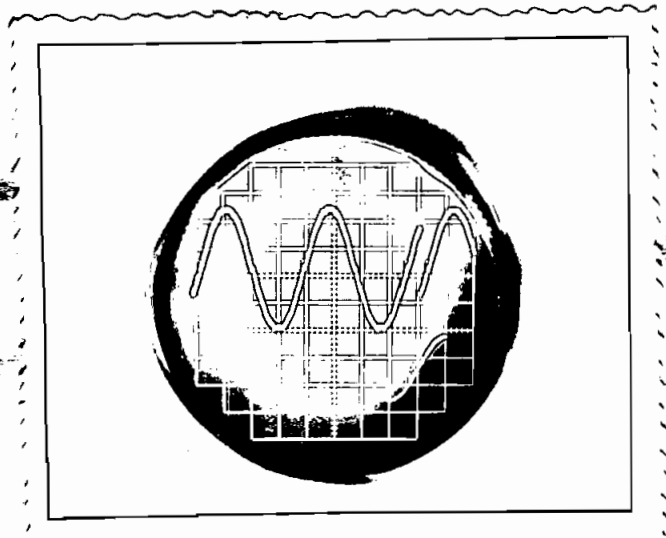
De esta manera se consigue formar anillos dentro de los cuales la señal circula pasando a tierra en una mínima propor-- ción. El conjunto se acopló a tierra con un condensador de cerámica de 0.1μF.

La señal medida en las condiciones anteriores se redujo a 0.01 v.

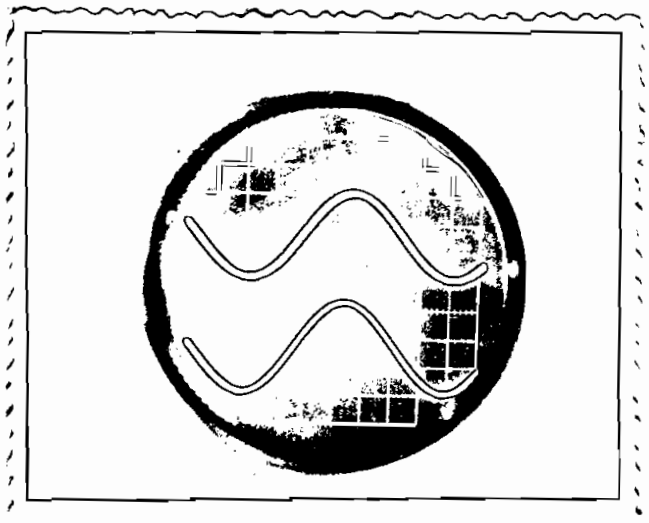
P R U E B A S

Se realizaron diferentes pruebas las mismas que se vieron limitadas por la disponibilidad de equipo en laboratorio.

f_s: FRECUENCIA DE LA SEÑAL
f_e: FRECUENCIA DE GRABACION
f_p: FRECUENCIA DE PRESENTACION



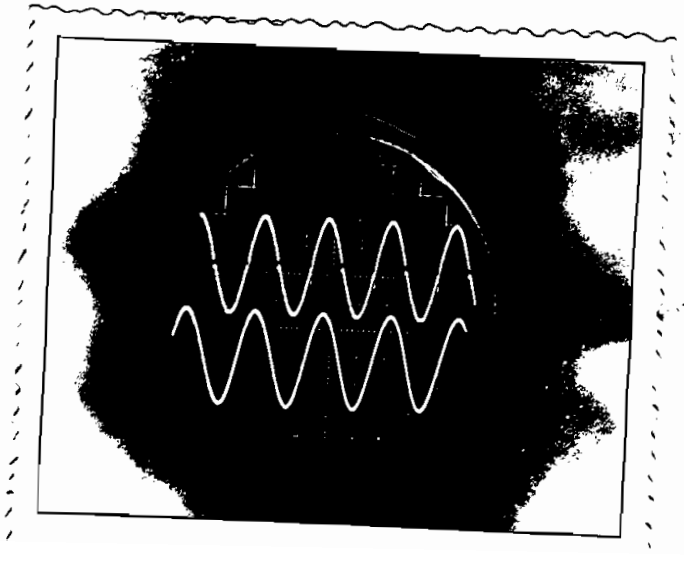
f_s: 5 Hz.
f_e: 500 Hz
f_p: 200 Hz



f_s: 5 KHZ

f_c: 100 KHZ

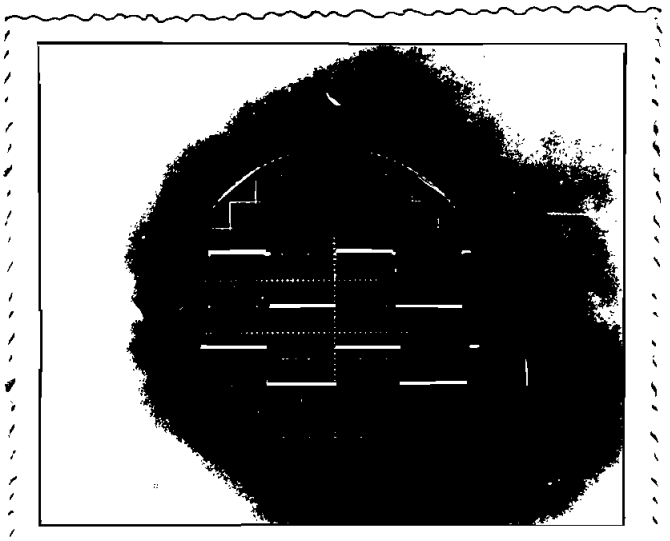
f_p: 200 KHZ



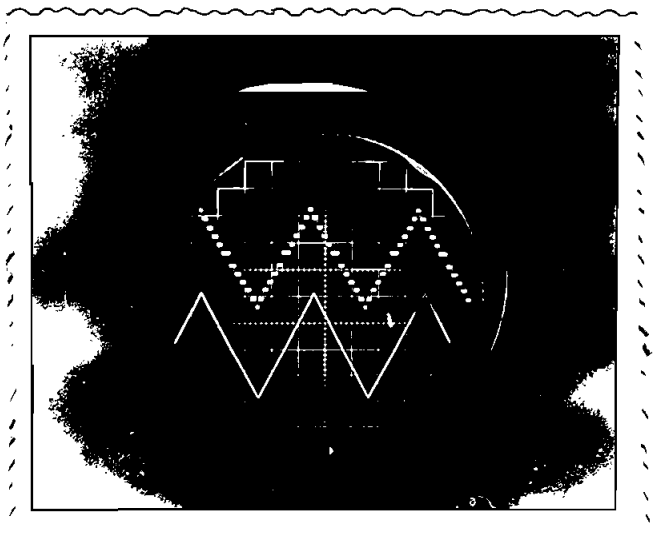
f_s: 35 KHZ

f_c: 100 KHZ

f_p: 200 KHZ



f_s: 20 KHZ
f_c: 100 KHZ
f_p: 200 KHZ



f_s: 15 KHZ
f_c: 100 KHZ
f_p: 200 KHZ

SISTEMA DE FUENTES

La alimentación general se toma de la red de 110 v, 60 Hz Deben obtenerse fuentes para un voltaje DC: ± 5v, ± 15v, ± 7.6v, - 12v.

Se diseñan como fuentes básicas: ± 5v, ± 15 v. De las fuentes de ± 15v se obtendrán los valores de polarización: ± 7.6 v, - 12v.

Las corrientes que deben suministrar estas fuentes son:

+ 5 v	700 mA
- 5 v	100 mA
+ 15v	200 mA
1 15v	200 mA

Las fuentes se diseñaron para valores de corriente iguales a dos veces los indicados, dejando la posibilidad de añadir memoria para otro canal.

El sistema básico de rectificación se realiza con diodos, como se indica en la figura que sigue:

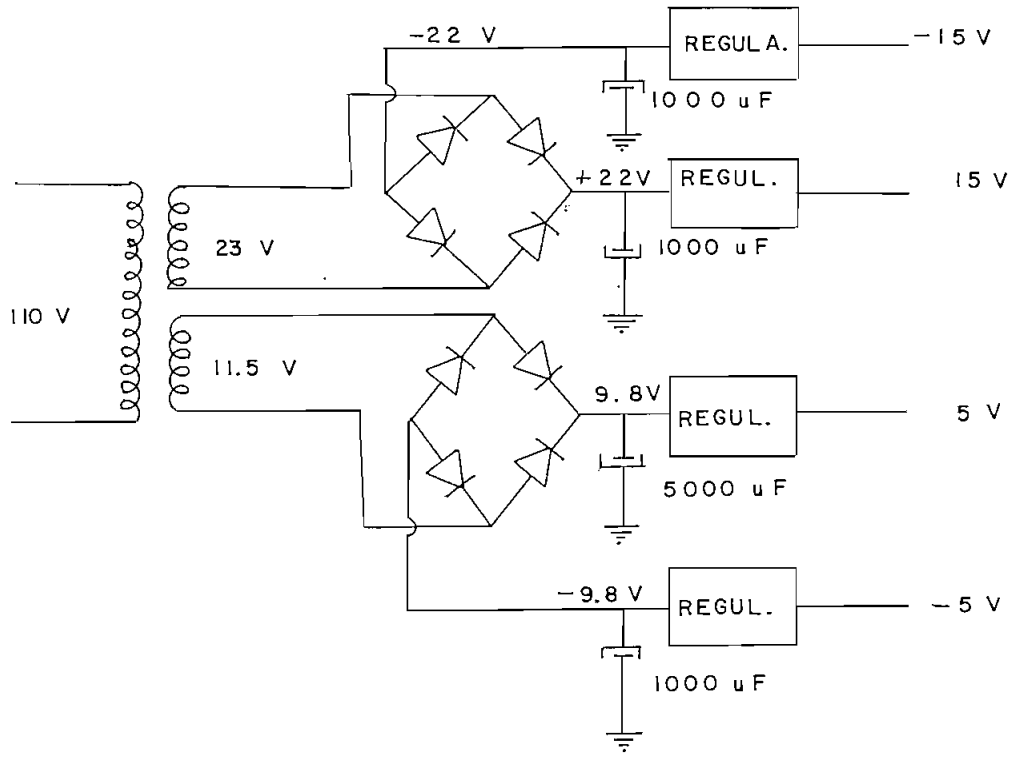


FIG. Nº 89

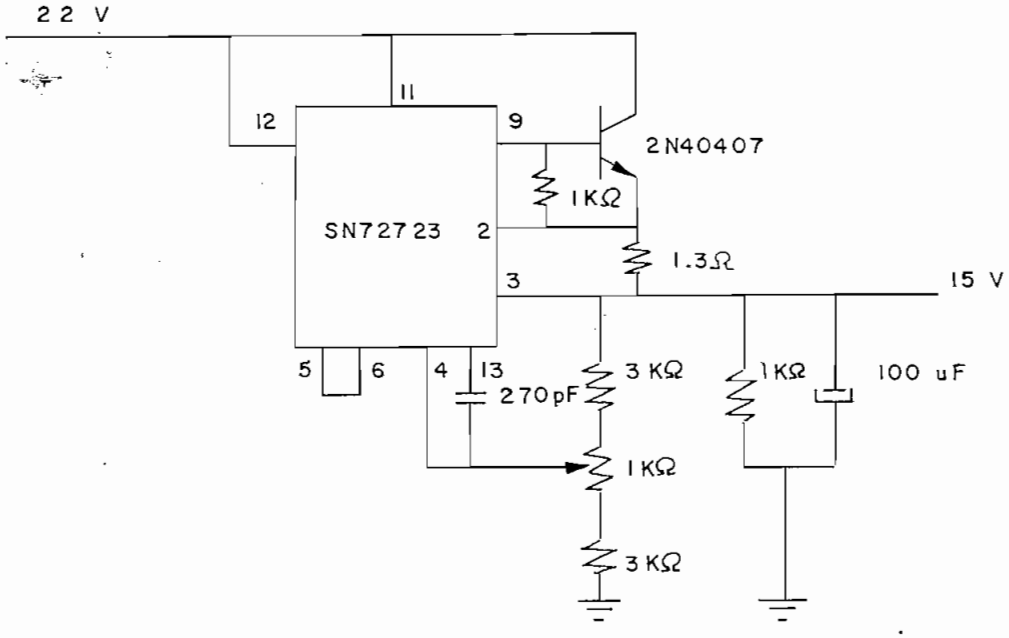
Como elemento de regulación se tomó el circuito integrado SN72723.

Se considerarón posibles variaciones de 10% en el voltaje de la red, Las fuentes se diseñaron considerando las notas de aplicación del fabricante.

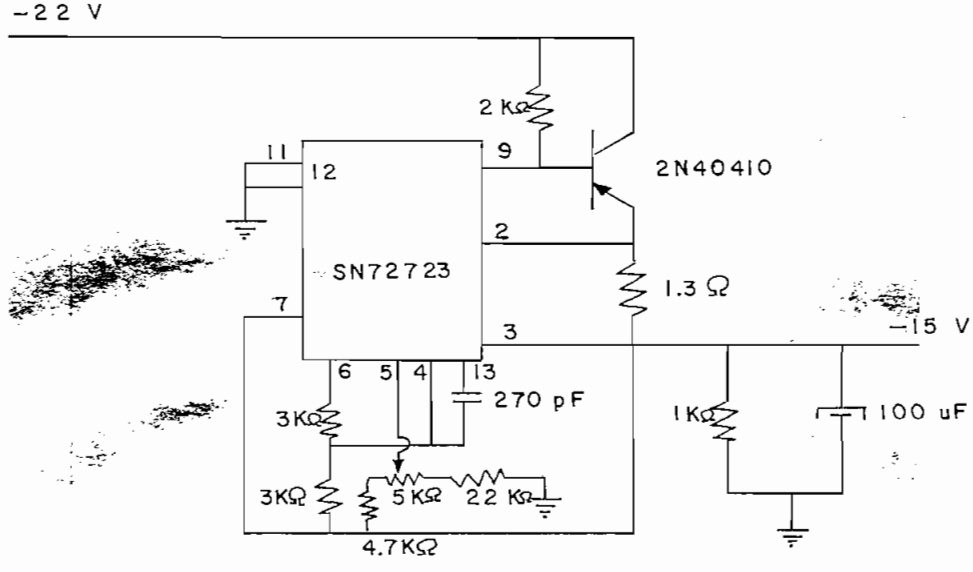
Se dispone de limitadores de corriente para protección de corto circuito.

Los circuitos y valores obtenidos se presentan a continuación:

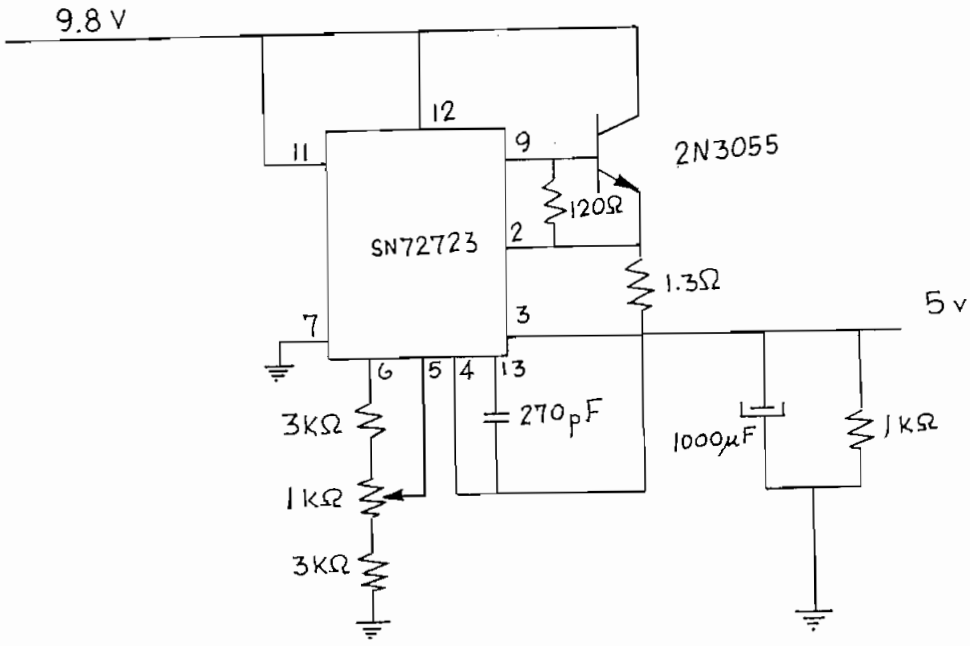
Fuente + 15v



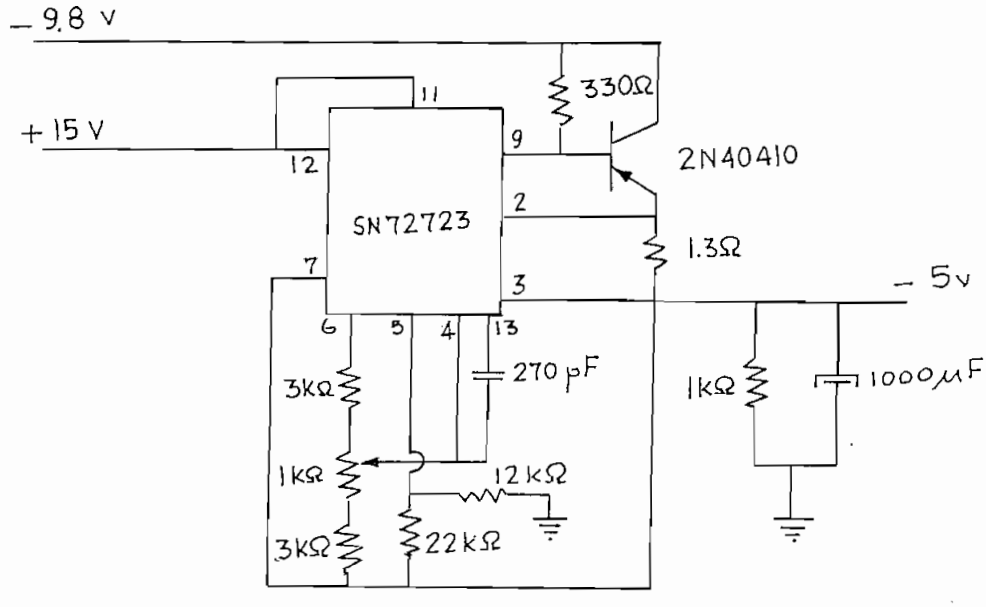
Fuente - 15v



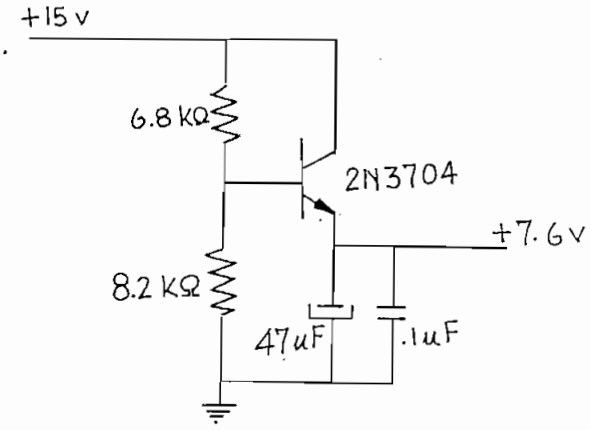
FUENTE 5 V



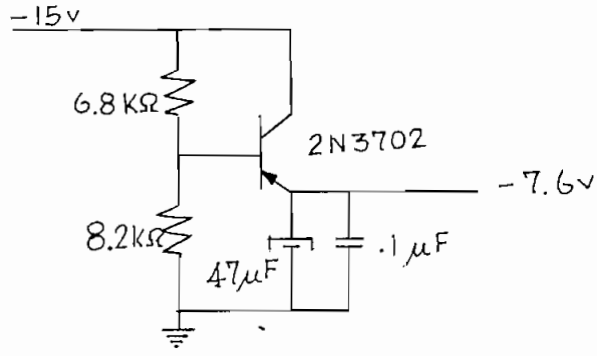
FUENTE -5 V



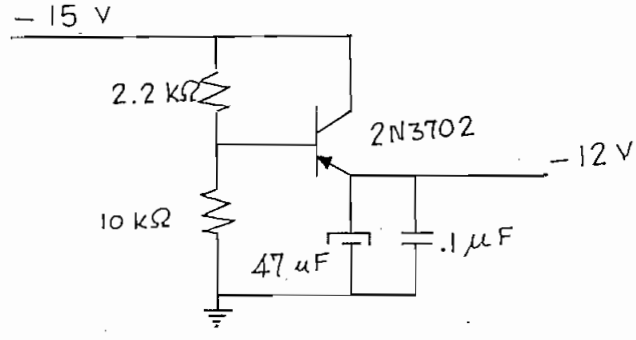
7.6 V 1 mA



- 7.6 V 1 mA



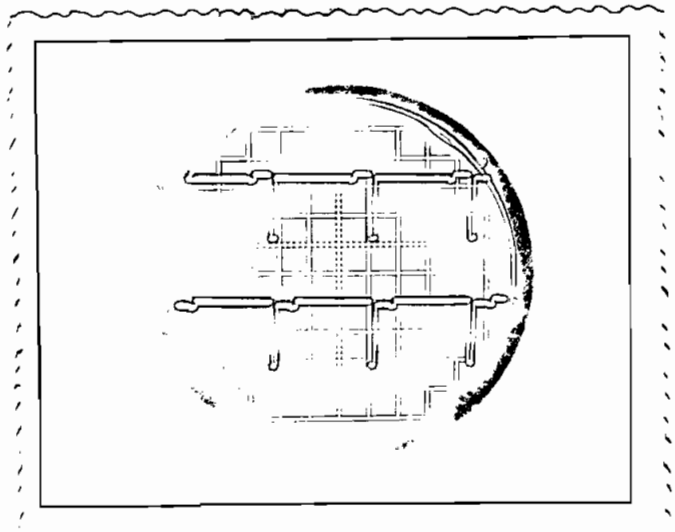
- 12 V 1 mA

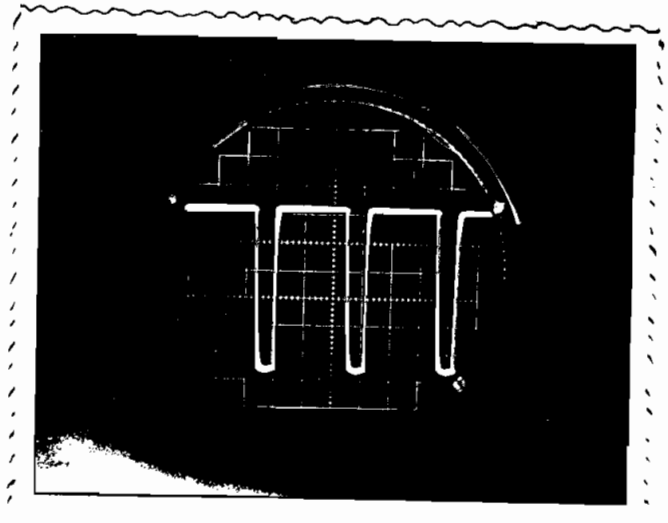


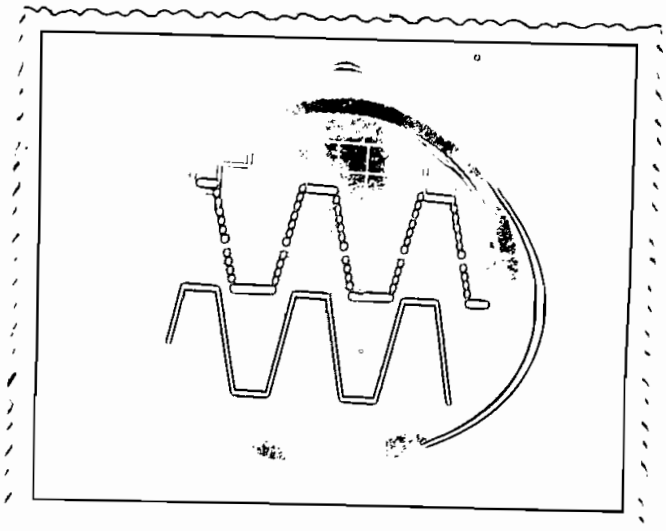
C A P I T U L O V

RESULTADOS CONCLUSIONES RECOMENDACIONES

Los resultados experimentales obtenidos se presentan a continuación:





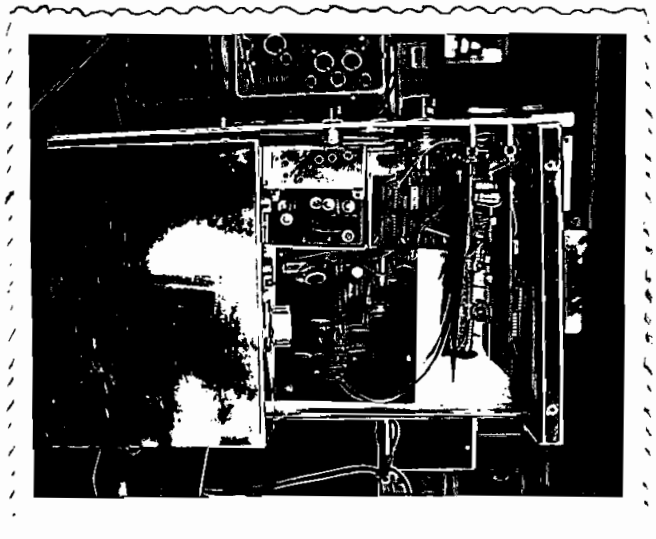


f_s: 30 KHZ

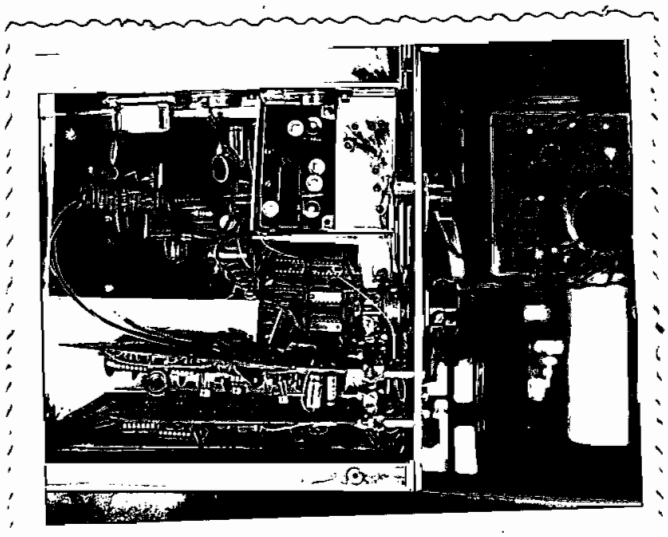
f_G: 100 KHZ

f_p: 200 KHZ

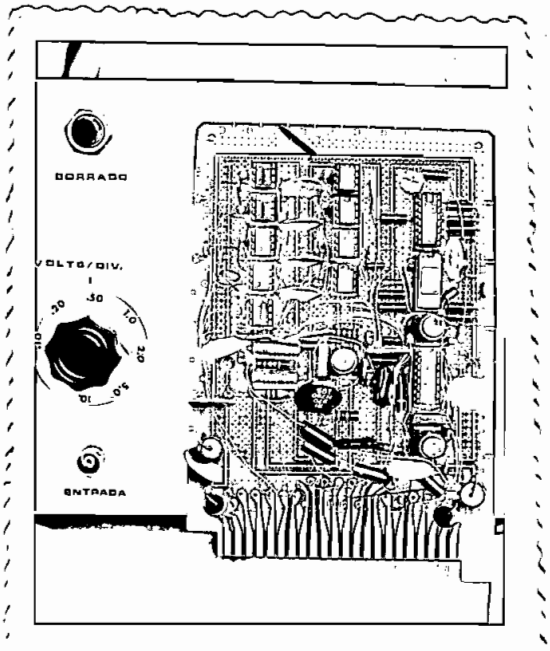
PRESENTACION DEL EQUIPO



VISTA SUPERIOR

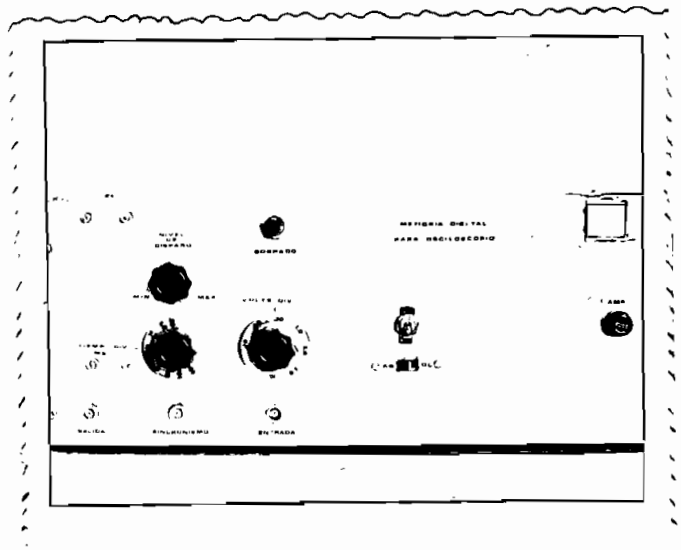


SISTEMA PRINCIPAL



TARJETAS UTILIZADAS

Las dimensiones físicas del equipo son: 32 x 23 x 17 cm.



VISTA FRONTAL

5.2 CONCLUSIONES RECOMENDACIONES

Considerando que ha sido necesario modificar el diseño de algunas de las etapas de la Memoria Digital, utilizando elementos discretos en vez de los circuitos integrados propuestos, los resulta

dos obtenidos son muy satisfactorios.

El circuito muestreador que se utiliza, trabaja bien si se considera que los diodos no son equilibrados. Si se emplean diodos schottky los resultados para este mismo circuito serán mucho mejores.

El CDA que se utiliza a la salida no responde satisfactoriamente con señales que varían rápidamente. Presenta a la salida una "espiga", la misma que pudo disminuirse con un filtro a la salida. Se puede utilizar un CDA más rápido.

Sería de mucho beneficio implementar la memoria digital con otro canal. Se puede utilizar un diseño dual o emplear retenedores (LATCH) que permitirían utilizar los mismos registros de memoria. Los otros elementos podrían ser compartidos.

Si se utilizan elementos más rápidos (especialmente los conversores), se pueden obtener resultados muy satisfactorios para frecuencias mayores. Los elementos más rápidos que están actualmente disponibles permitirían aumentar la frecuencia de muestreo hasta aproximadamente 1 MKz.

B I B L I O G R A F I A

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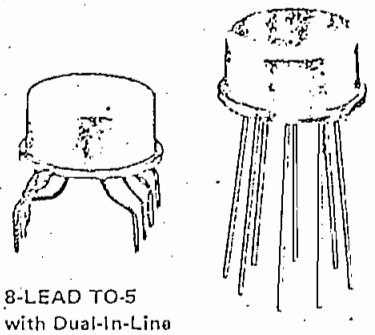
Linear Integrated Circuits

Monolithic Silicon

CA3130BT, CA3130BS
CA3130AT, CA3130AS
CA3130T, CA3130S



8-LEAD TO-5 with Dual-In-Line Formed Leads (S suffix) H-1787

8-LEAD TO-5 (T suffix) H-1528

COS/MOS Operational Amplifiers

With MOS/FET Input

Features:

- MOS/FET input stage provides:
  very high Z_I = 1.5 TΩ (1.5 x 10^{12} Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  2 pA typ. at 5 V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- COS/MOS output stage permits signal swing to either (or both) supply rails

} Ideal for single-supply applications

- Low V_{IO}: 2 mV max. (CA3130B)
- Wide BW: 15 MHz typ. (unity-gain crossover)
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Compensation with single external capacitor

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators (ideal interface with digital COS/MOS)
- High-input-impedance wideband amplifiers
- Voltage followers (e.g., follower for single-supply D/A converter)
- Voltage regulators (permits control of output voltage down to zero volts)
- Peak detectors
- Single-supply full-wave precision rectifiers
- Photo-diode sensor amplifiers

RCA-CA3130T, CA3130S, CA3130AT, CA3130AS, CA-3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor pair, capable of swinging the output voltage to within millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in either the standard 8-lead TO-5-style package (T suffix) or in the 8-lead dual-in-line formed-lead TO-5-style package "DIL-CAN" (S suffix) and operates over the full military-temperature range of −55°C to +125°C. The CA3130B is intended for applications requiring premium-grade specifications and with limits established for: input current, temperature coefficient of input-offset voltage, and gain over the range of −55°C to +125°C. The CA3130A offers superior input characteristics over those of the CA3130.

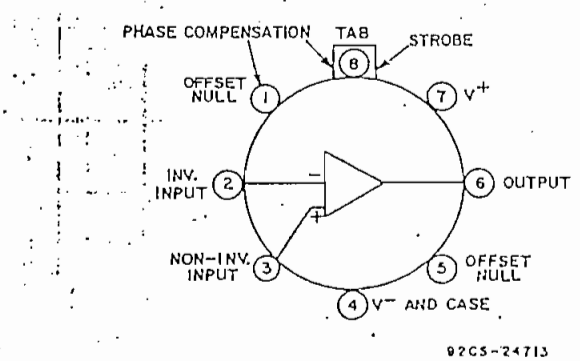


Fig. 1—Functional diagram of the CA3130 Series.

Printed in USA/8-74

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC INPUT VOLTAGE ..... V^+ to (V^--0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK—
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK—
UP TO 55°C ..... 418 mW
ABOVE 55°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING ..... −55 to +125°C
STORAGE ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
FROM CASE FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS — For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS (V^+=15 V, V^-=0 V, T_A=25°C (Unless Specified Otherwise)	CA3130B			CA3130A			CA3130			UNITS	FIG. NO.
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Offset Voltage	$\|V_{IO}\|$	$V^{\pm}$=±7.5 V	—	0.8	2	—	2	5	—	8	15	mV	—
Input Offset Current	$\|I_{IO}\|$	$V^{\pm}$=±7.5 V	—	0.5	10	—	0.5	20	—	0.5	30	pA	—
Input Current	I_I	$V^{\pm}$=±7.5 V	—	5	20	—	5	30	—	5	50	pA	—
Large-Signal Voltage Gain	A_{OL}	V_O=10 V_{p-p}, R_L=2 kΩ	100 k	320 k	—	50 k	320 k	—	50 k	320 k	—	V/V	4,5
			100	110	—	94	110	—	94	110	—	dB	
Common-Mode Rejection Ratio	CMRR		86	100	—	80	90	—	70	90	—	dB	—
Common-Mode Input-Voltage Range	V_{ICR}		0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V	—
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	$V^{\pm}$=±7.5 V	100	32	—	150	32	—	320	32	—	μV/V	—
	$\Delta V_{IO}/\Delta V^-$		100	32	—	150	32	—	320	32	—		
Maximum Output Voltage	V_{OM}^+	R_L=2 kΩ	12	13.3	—	12	13.3	—	12	13.3	—	V	9
	V_{OM}^-		—	0.002	0.01	—	0.002	0.01	—	0.002	0.01		10
	$\|V_{OM}^+\|$	R_L=∞	14.99	15	—	14.99	15	—	14.99	15	—		9
	$\|V_{OM}^-\|$		—	0	0.01	—	0	0.01	—	0	0.01		10
Maximum Output Current: Source	I_{OM}^+	V_O=0 V	12	22	45	12	22	45	12	22	45	mA	9
Sink	I_{OM}^-	V_O=15 V	12	20	45	12	20	45	12	20	45		10
Supply Current	I^+	V_O=7.5 V, R_L=∞	—	10	15	—	10	15	—	10	15	mA	7,8
		V_O=0 V, R_L=∞	—	2	3	—	2	3	—	2	3		
Input Current	I_I	T_A=−55 to 125°C ▲, $V^{\pm}$=±7.5 V, V_O=10 V_{p-p}, R_L=2 kΩ	—	Fig. 11	15	—	Fig. 11	—	—	Fig. 11	—	nA	—
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		—	5	15	—	10	—	—	10	—	μV/°C	—
Large-Signal Voltage Gain	A_{OL}		50 k	320 k	—	—	320 k	—	—	320 k	—	V/V	5
			94	110	—	—	110	—	—	110	—	dB	

* Applies only to A_{OL}.

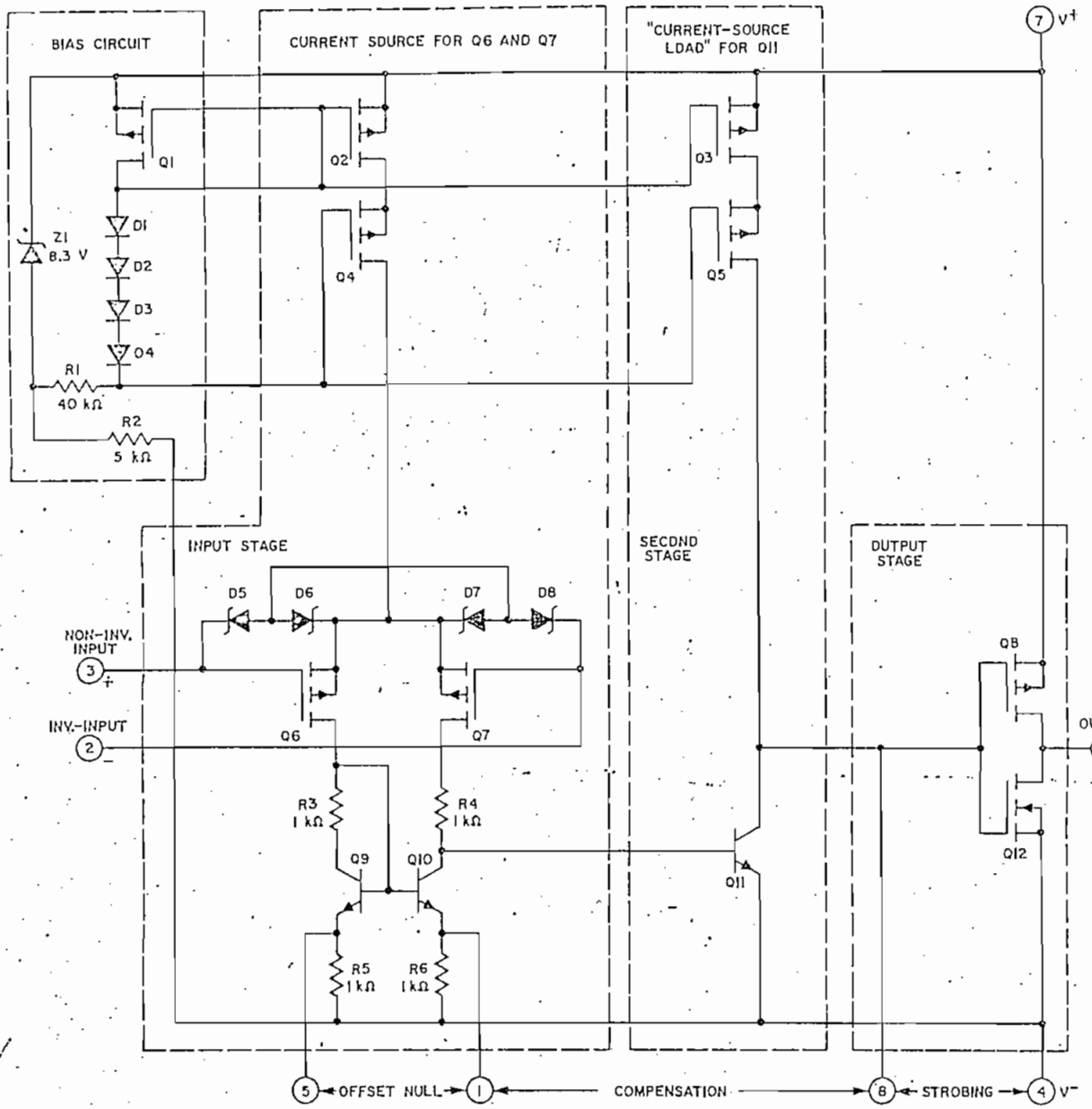
▲ Applies only to I_I and $\Delta V_{IO}/\Delta T$.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	SYMBOL	TEST CONDITIONS (V^+=+7.5 V, V^-=−7.5 V, T_A=25°C (Unless Specified Otherwise)	CA3130B	CA3130A	CA3130	UNITS	FIG. NO.
Input Offset Voltage Adjustment Range		10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	±22	mV	—
Input Resistance	R_I		1.5	1.5	1.5	TΩ	—
Input Capacitance	C_I	f = 1 MHz	4.3	4.3	4.3	pF	—
Equivalent Input Noise	e_n	BW=0.2 MHz, R_S=1 MΩ*	23	23	23	μV	14
Unity Gain Crossover Frequency	f_T	C_C = 0	15	15	15	MHz	4,15
		C_C = 47 pF	4	4	4		
Slew Rate: Open Loop	SR	C_C = 0	30	30	30	V/μs	—
Closed Loop		C_C = 56 pF	10	10	10		15
Transient Response: Rise Time	t_r	C_C = 56 pF, C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)	0.09	0.09	0.09	μs	15
Overshoot			10	10	10	%	15
Settling Time (4 Vp-p Input to <0.1%)			1.2	1.2	1.2	μs	15

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for sources of R_S up to 10 MΩ.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS (V^+ = 5 V, V^- = 0 V, T_A = 25°C (Unless Specified Otherwise)	CA3130B	CA3130A	CA3130	UNITS	FIG. NO.
Input Offset Voltage	V_{IO}		1	2	8	mV	—
Input Offset Current	I_{IO}		0.1	0.1	0.1	pA	—
Input Current	I_I		2	2	2	pA	—
Common-Mode Rejection Ratio	CMRR		100	90	80	dB	—
Large-Signal Voltage Gain	A_{OL}	V_O = 4 Vp-p, R_L = 5 kΩ	100 k	100 k	100 k	V/V	—
			100	100	100	dB	—
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V	—
Supply Current	I^+	V_O = 5 V, R_L = ∞	300	300	300	μA	7,8
		V_O=2.5 V, R_L = ∞	500	500	500		
Power Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V	—



NOTE:
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

92CL-24714

Fig. 2—Schematic diagram of the CA3130 Series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages—The circuit of the CA3130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS

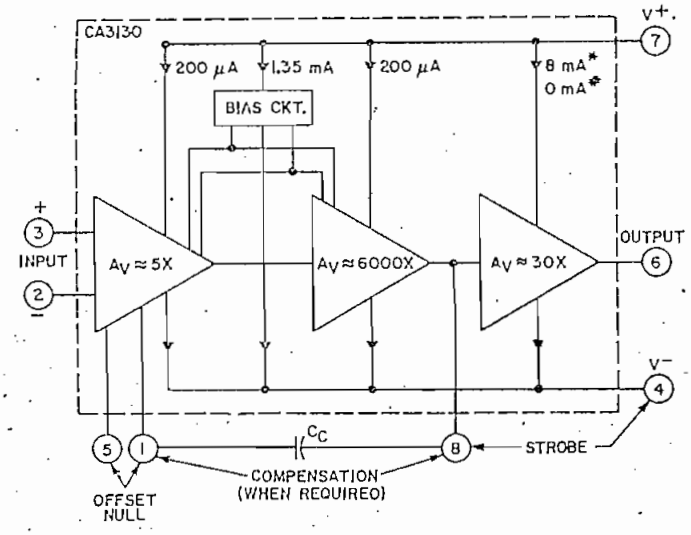


Fig. 3—Block diagram of the CA3130 Series.

transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g. including static electricity during handling for Q6 and Q7.

Second Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

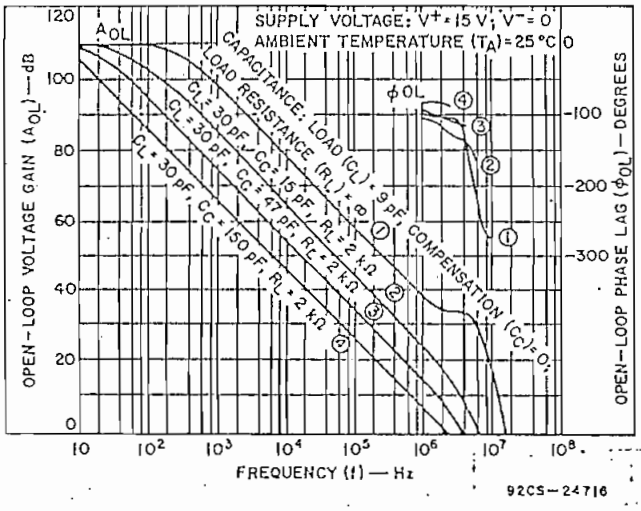


Fig. 4—Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

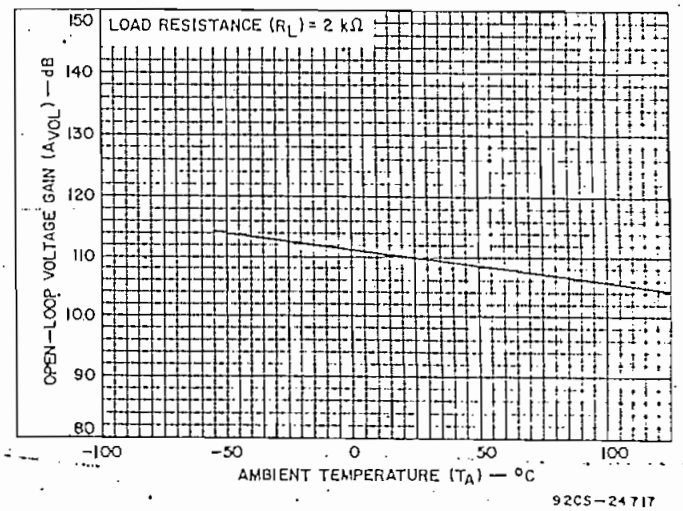


Fig. 5—Open-loop gain vs. temperature.

†For general information on the characteristics of COS/MOS transistor pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array."

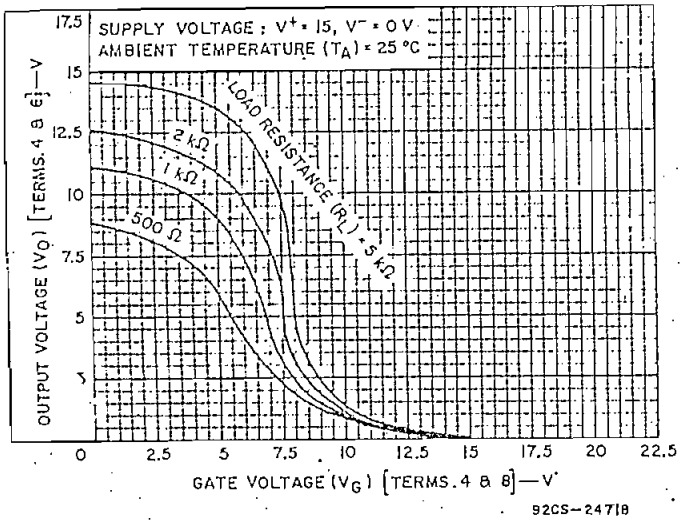


Fig. 6—Voltage transfer characteristics of COS/MOS output stage.

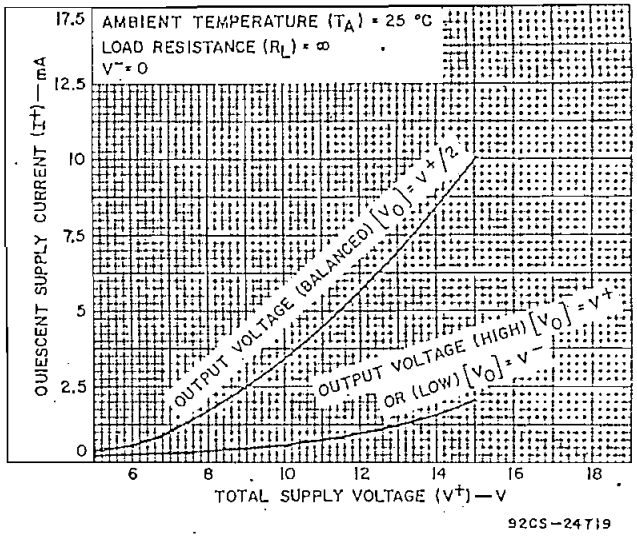


Fig. 7—Quiescent supply current vs. supply voltage.

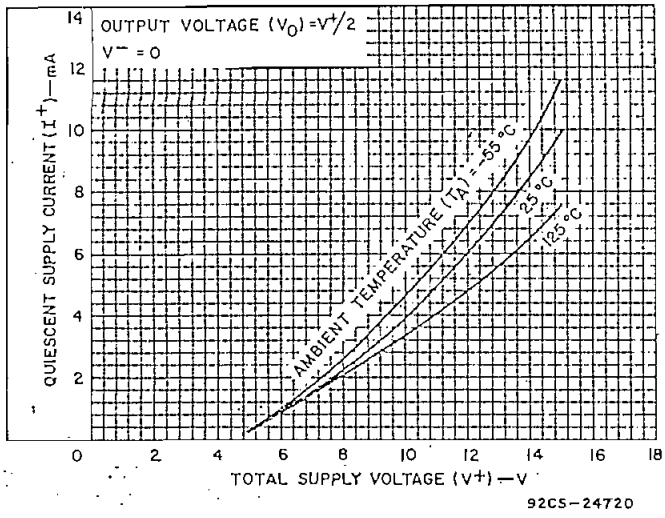


Fig. 8—Quiescent supply current vs. supply voltage at several temperatures.

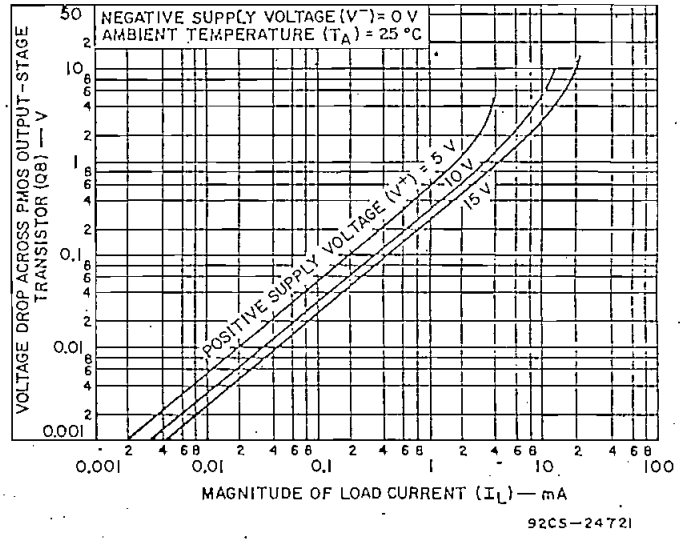


Fig. 9—Voltage across PMOS output transistor (Q8) vs. load current.

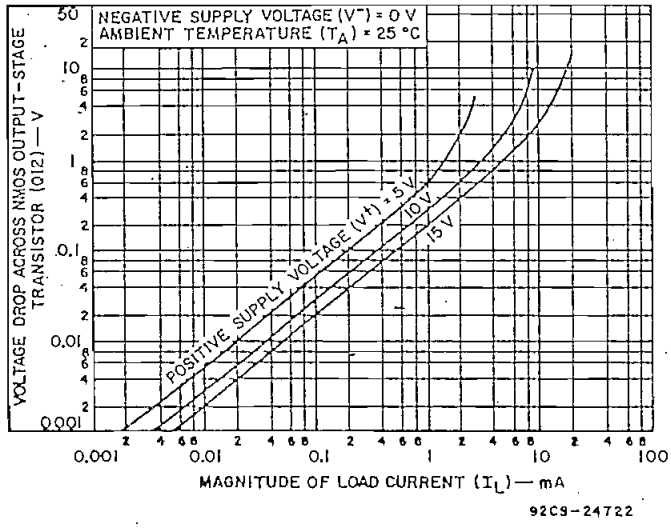


Fig. 10—Voltage across NMOS output transistor (Q12) vs. load current.

HANDLING AND OPERATING CONSIDERATIONS

Handling Considerations

The CA3130 uses MOS field-effect transistors in the input circuit. Because MOS/FET's have extremely high input resistances, they are susceptible to damage when exposed to extremely high static electrical charges. To minimize the possibilities of damaging the input stage transistors, Q6 and Q7, the CA3130 utilizes a protective diode network in the input stage. Nevertheless, it is good practice that the following precautions be observed during handling, testing, and actual operation of the CA3130 devices to minimize exposure to damage-inducing hazards:

1. Soldering-iron tips, metal parts of fixtures, tools, and handling facilities should be grounded.
2. Devices should not be inserted into or removed from circuits with the power ON because transient voltages may cause damage.
3. Signals should not be applied to the input (Terms. 2 and 3) when the device power supply is OFF. Input-terminal currents should not exceed 1 mA.
4. After CA3130 devices have been mounted on circuit boards, proper handling precautions should still be observed if the input terminals are unterminated. It is good practice during board-processing operations to return Terms. 2 and 3 to Term. 4 by jumping the appropriate conductors.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 11 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

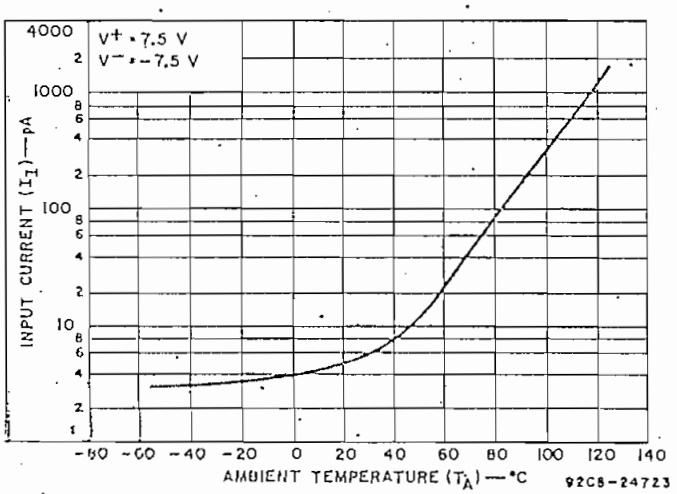


Fig. 11—Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig. 12 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices during life testing. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

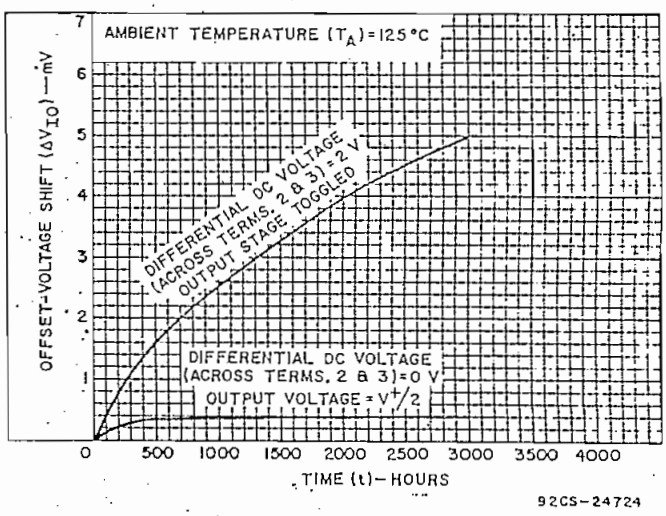


Fig. 12—Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single and dual-supply service. Figs. 13a and 13b show the CA3130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

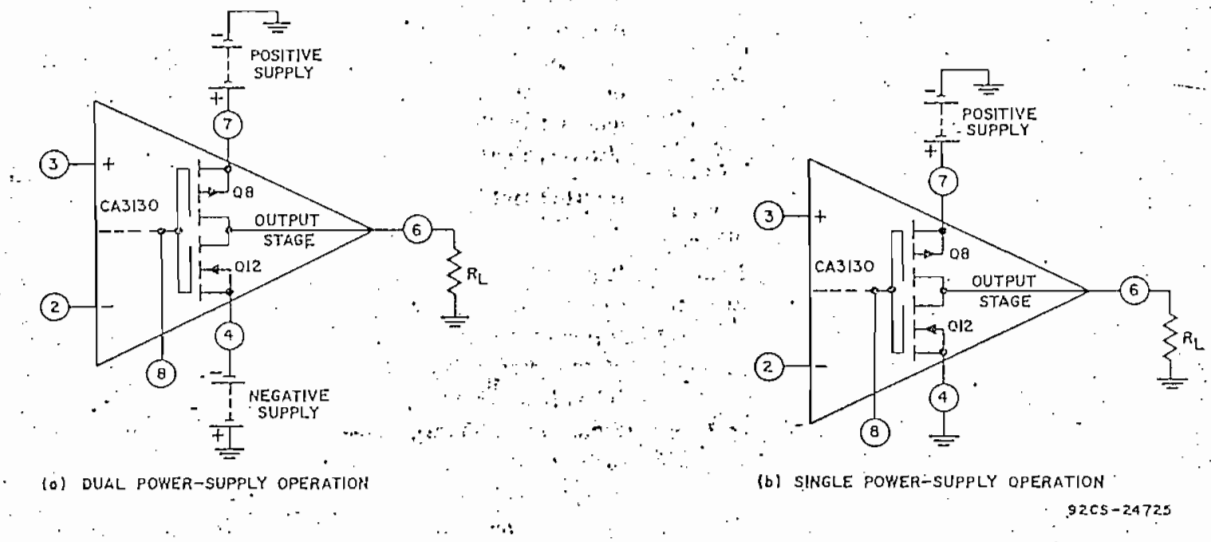


Fig. 13—CA3130 output stage in dual and single power-supply operation.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 13a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig. 13b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 14 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

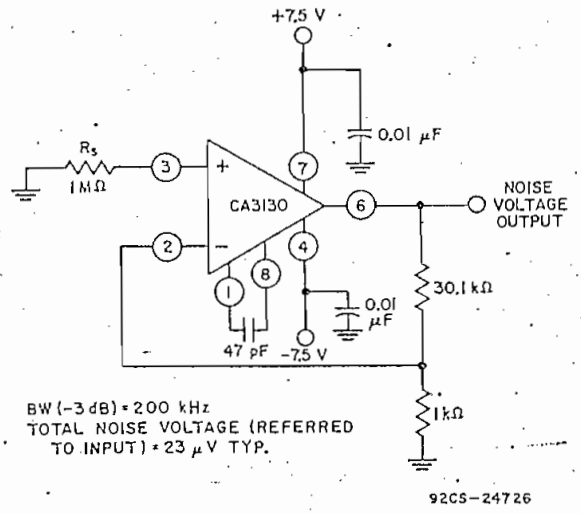
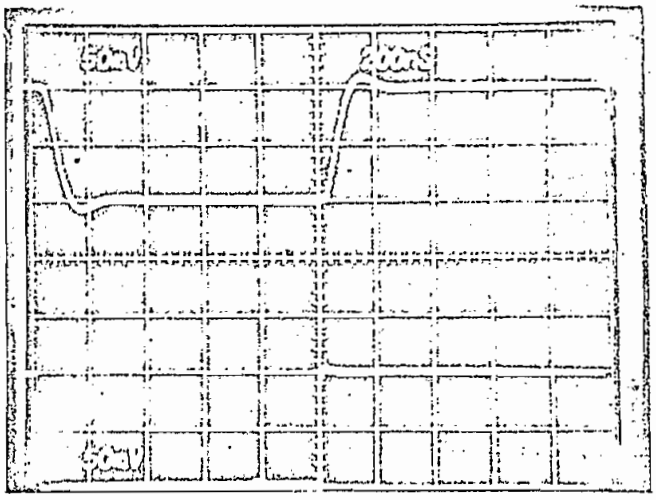
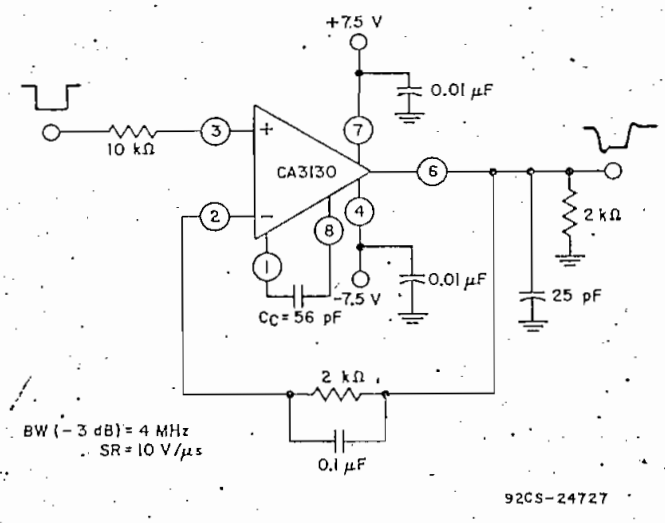


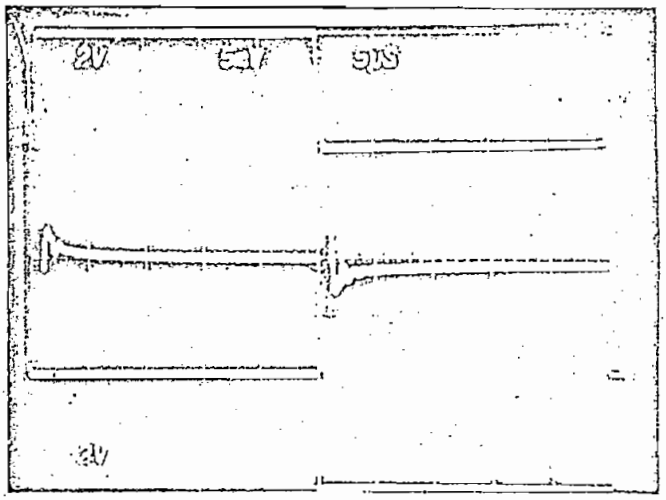
Fig. 14—Test-circuit amplifier (30-dB gain) used for wideband noise measurements.



Top Trace: Output
Bottom Trace: Input

(a) Small-signal response (50 mV/div. and 200 ns/div.)





Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)

(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

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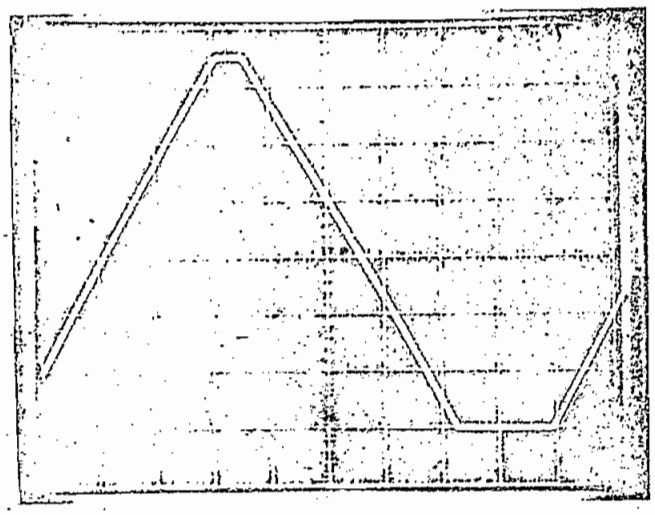
Fig. 15—Split-supply voltage follower with associated waveforms.

TYPICAL APPLICATIONS

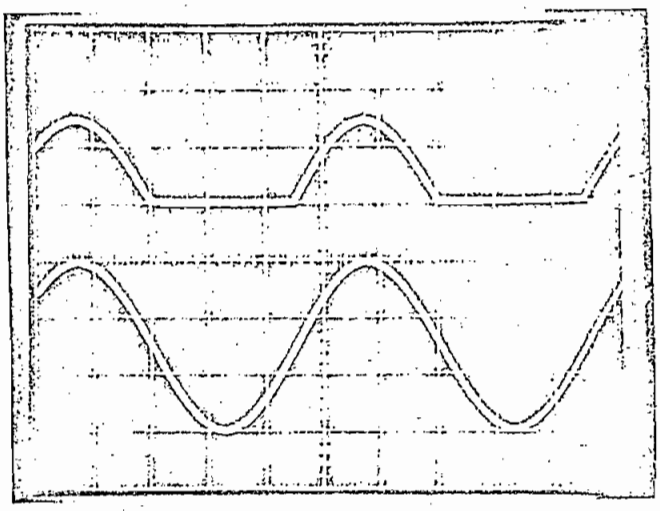
Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 15 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 16, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 16a with input-signal ramping. The waveforms in Fig. 16b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 16b also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.



(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)

(b) Output-waveform with ground-reference sine-wave input

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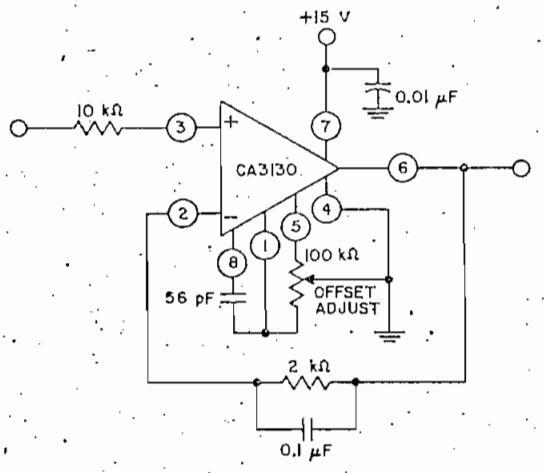

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Fig. 16—Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

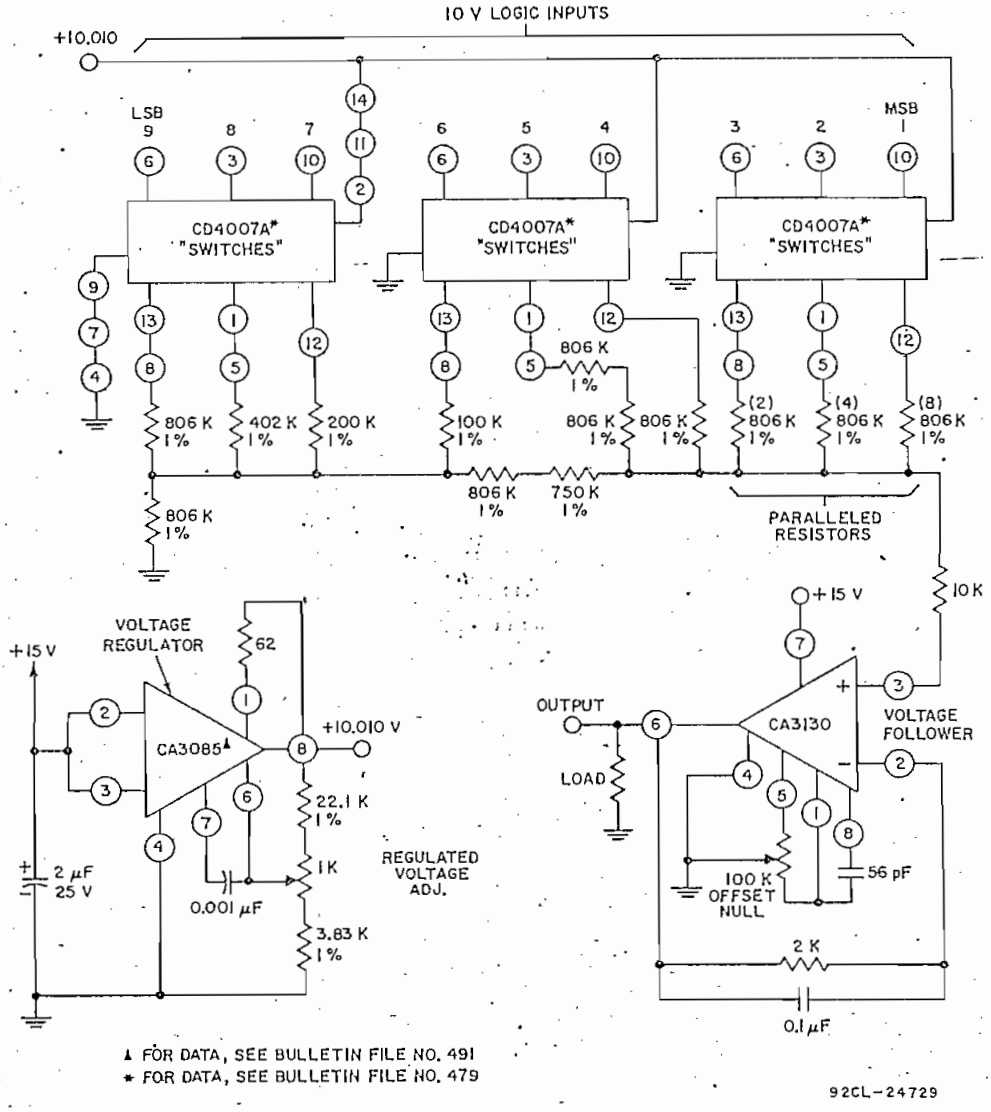
9-BIT COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig. 17. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op-amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 17.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output

*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC," Application Note ICAN-6080.



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

Fig. 17—9-bit DAC using COS/MOS digital switches and CA3130.

control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

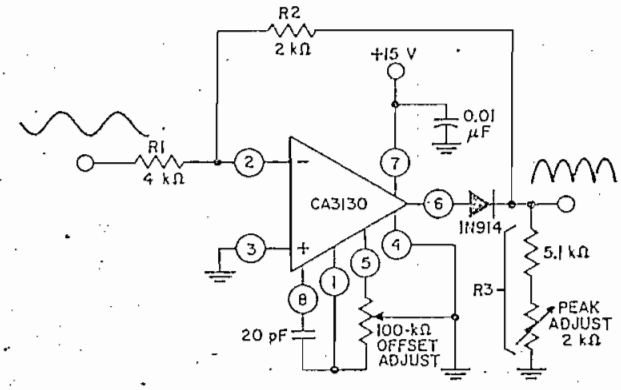
The absolute-value circuit using the CA3130 is shown in Fig. 18. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 18 is satisfied, the full-wave output is symmetrical.

Peak Detectors

Peak-detector circuits are easily implemented with the CA-3130, as illustrated in Fig. 19 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.

Error-Amplifier in Regulated Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to



$$\text{GAIN} = \frac{R2}{RI} = X = \frac{R3}{RI+R2+R3}$$

$$R3 = RI\left(\frac{X+X^2}{1-X}\right)$$

$$\text{FOR } X = 0.5: \frac{2\ k\Omega}{4\ k\Omega} = \frac{R2}{RI}$$

$$R3 = 4\ k\Omega\left(\frac{0.75}{0.5}\right) = 6\ k\Omega$$

20 V p-p INPUT: BW(-3dB) = 230 kHz, DC OUTPUT (AVG.) = 3.2 V
1 VOLT p-p INPUT: BW(-3dB) = 130 kHz, DC OUTPUT (AVG.) = 160 mV

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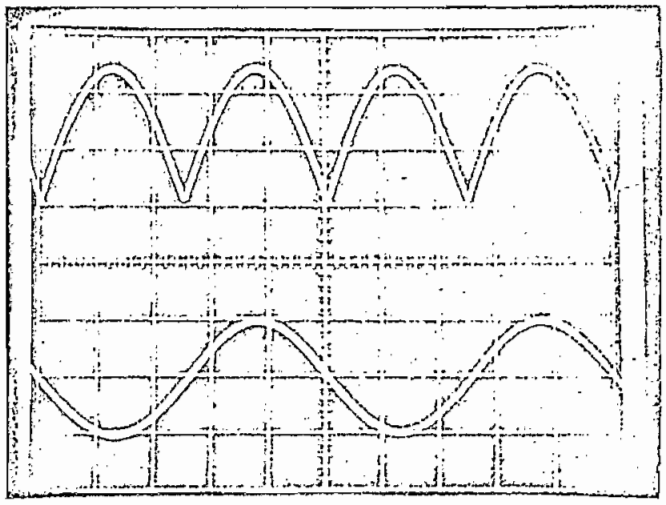

Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

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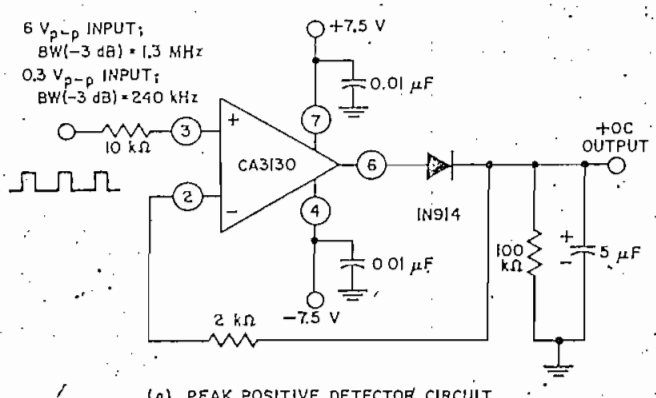
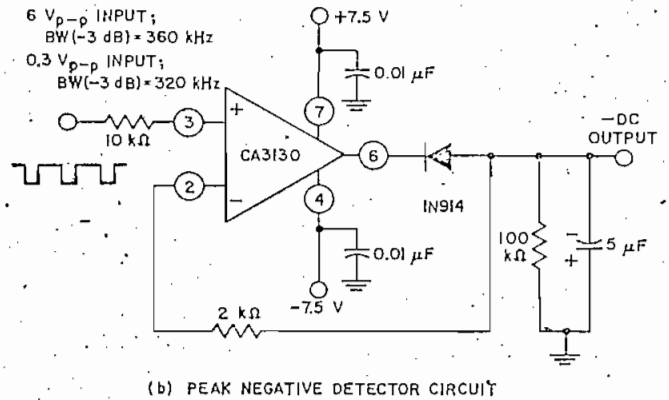
Fig. 18—Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.



(a) PEAK POSITIVE DETECTOR CIRCUIT



(b) PEAK NEGATIVE DETECTOR CIRCUIT

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Fig. 19—Peak-detector circuits.

approach zero. Fig. 20 shows the schematic diagram of a 40-mA power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Fig. 21 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 22. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

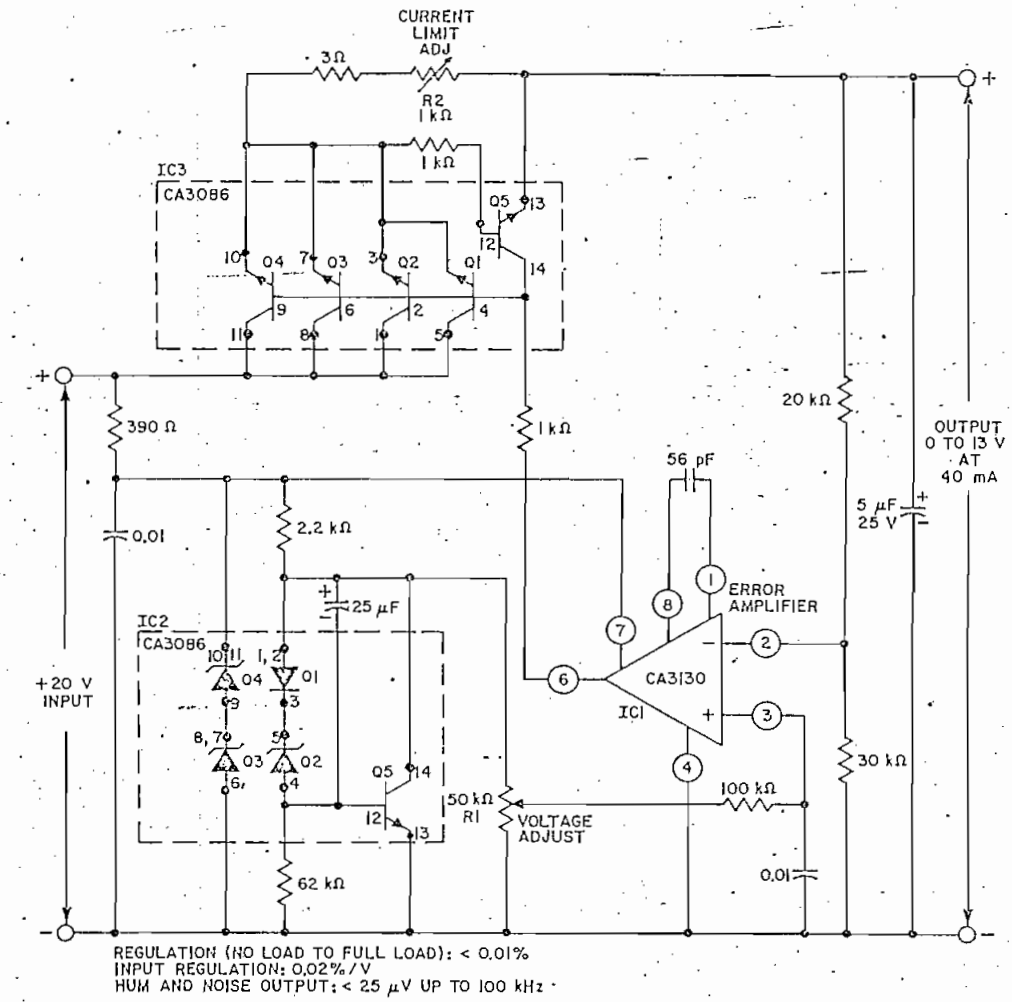


Fig. 20—Voltage regulator circuit (0 to 13 V at 40 mA).

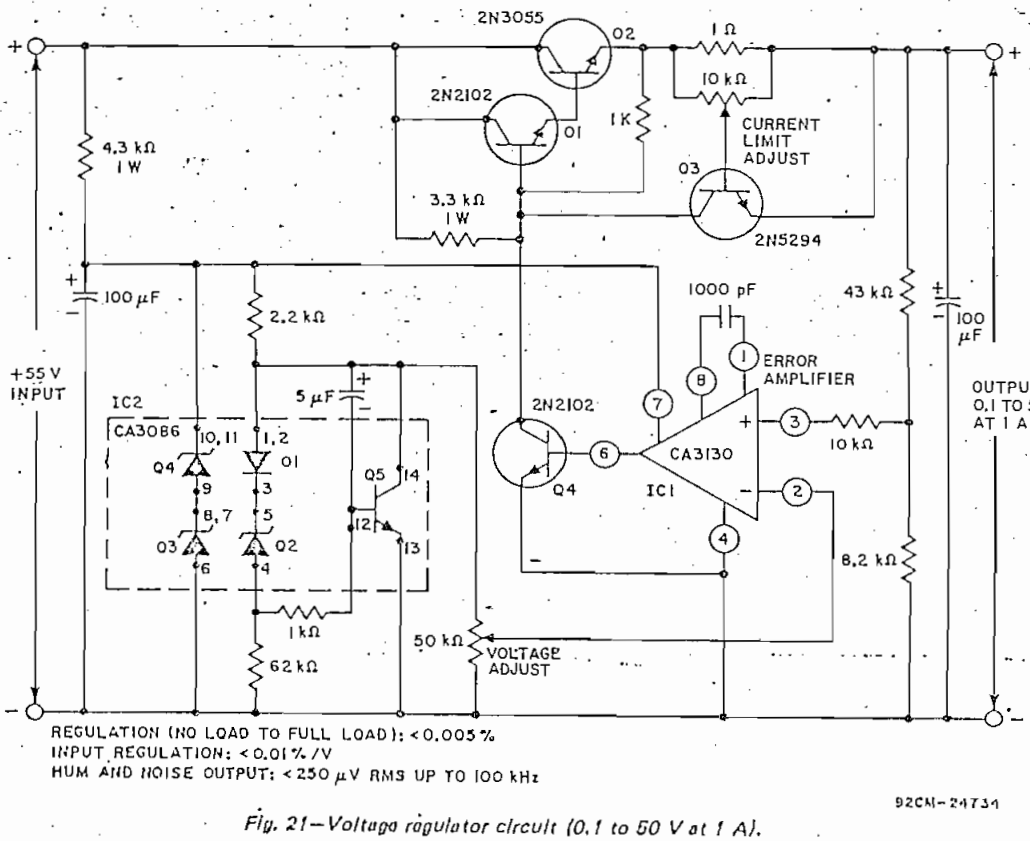


Fig. 21—Voltage regulator circuit (0.1 to 50 V at 1 A).

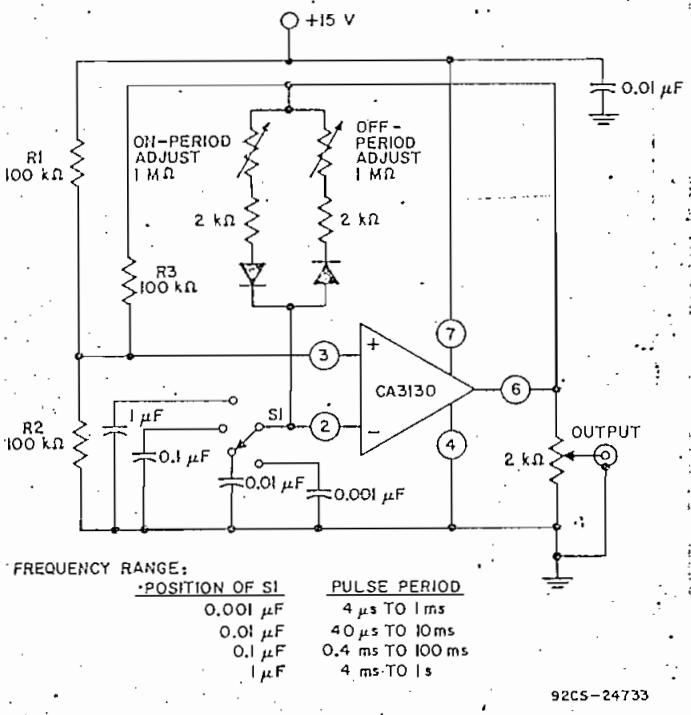


Fig. 22—Pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

Function Generator

Fig. 23 contains the schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

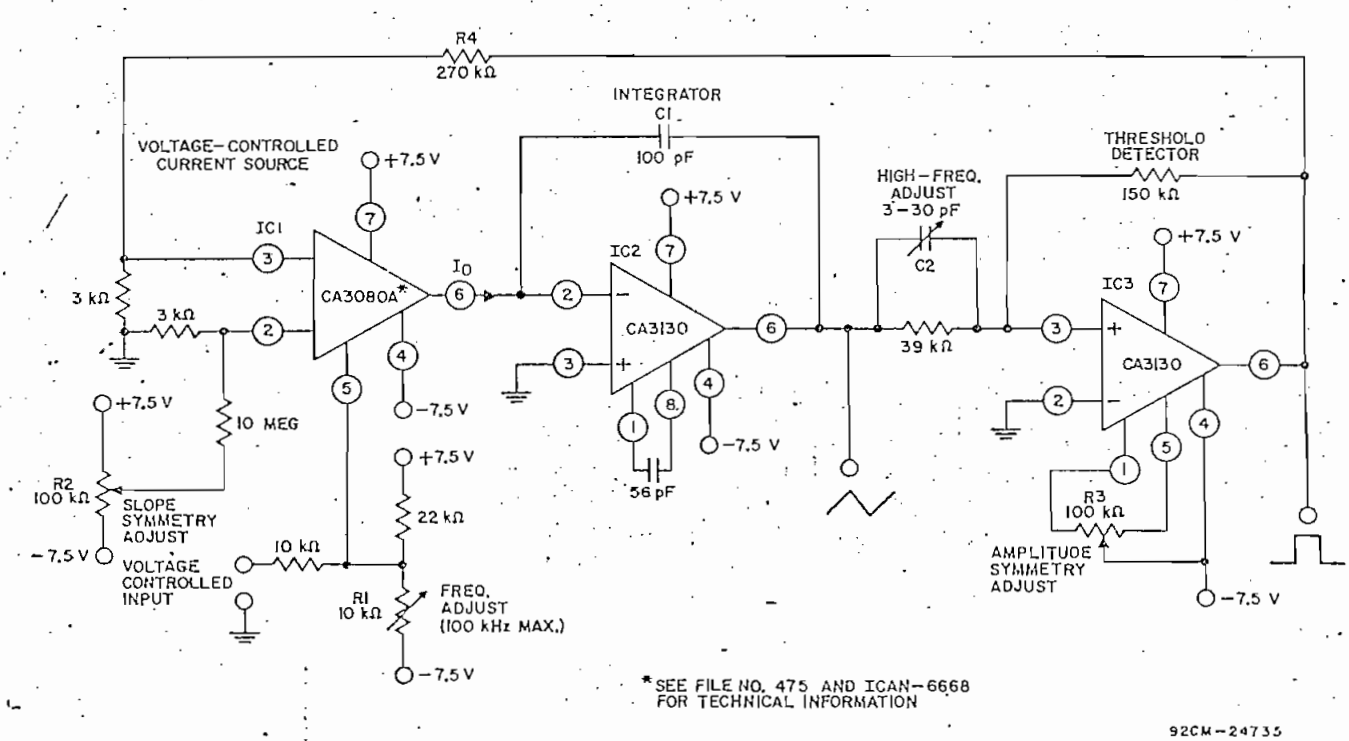


Fig. 23—Function generator (frequency can be varied 1,000,000/1 with a single control).

*See File No. 475 and ICAN-6668.

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 24, three COS/MOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15 V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5x.

The amplifier circuit in Fig. 24 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (–3 dB) is 50 kHz.

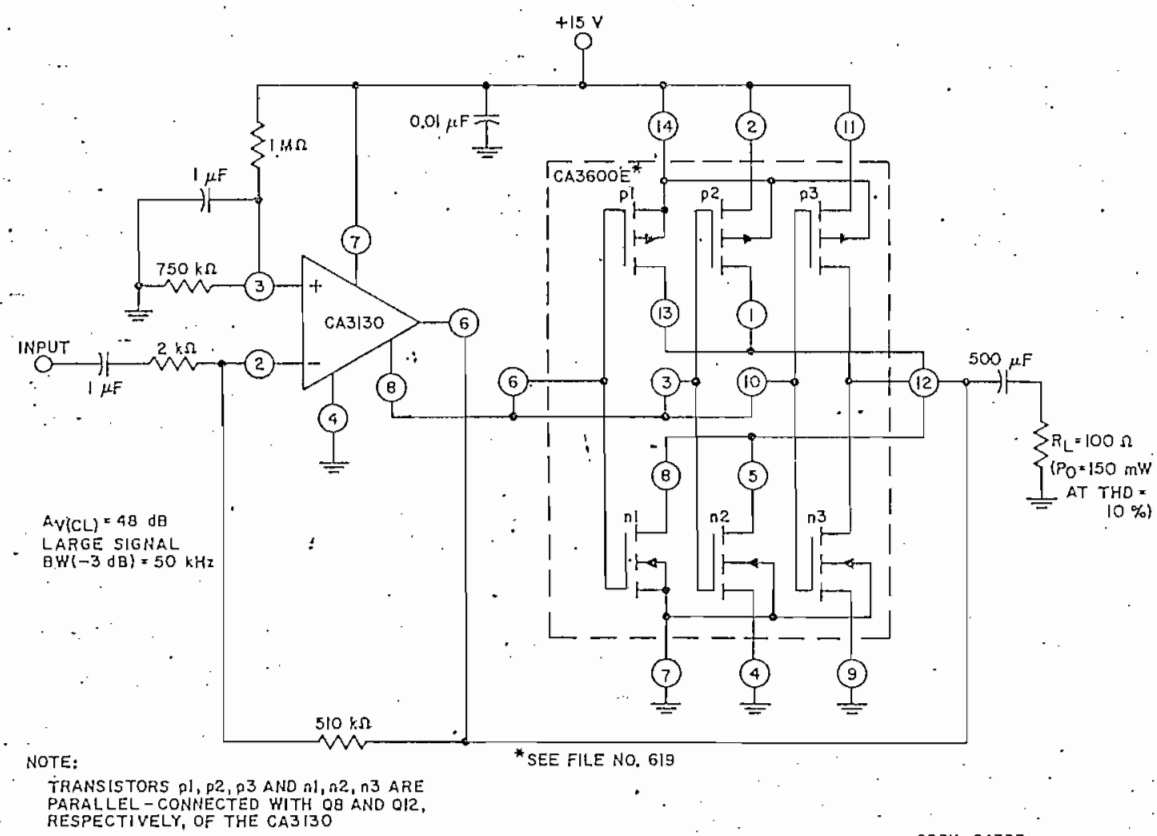
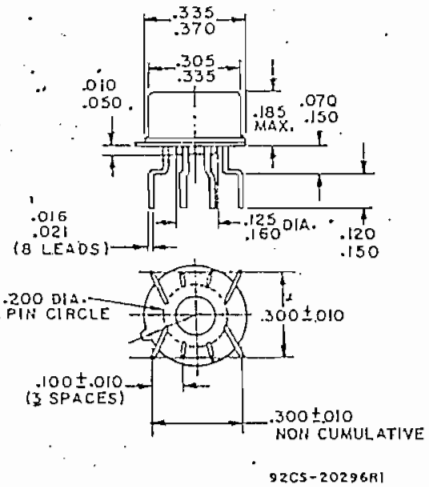


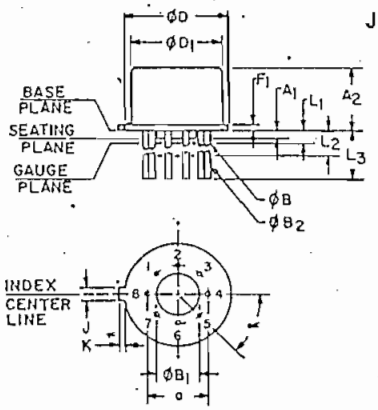
Fig. 24—COS/MOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.

DIMENSIONAL OUTLINES

8-Lead TO-5 with Dual-In-Line Formed Leads "DIL-CAN"



8-Lead TO-5
JEDEC MO-002-AL



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
e	0.200 TP		2	5.08 TP	
A_1	0.010	0.050		0.26	1.27
A_2	0.165	0.185		4.20	4.69
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0.125	0.160		3.18	4.06
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
J	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	45° TP			45° TP	
N	8		6	8	
N_1	3		5	3	

NOTES

1. Refer to JEDEC Publication No. 13 for Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radium of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

*See File No. 619 for technical information.

*When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

July 1971
Supersedes May 1971

MILITARY (A SUFFIX) -55 to +125°C
INDUSTRIAL (B SUFFIX) -20 to +85°C

Type	Package
DG181AA	TO-100
DG181BA	TO-100
DG182AA	TO-100
DG182BA	TO-100
DG184AP	16-Pin DIP
DG184BP	16-Pin DIP
DG185AP	16-Pin DIP
DG185BP	16-Pin DIP

DG181
DG182
DG184
DG185

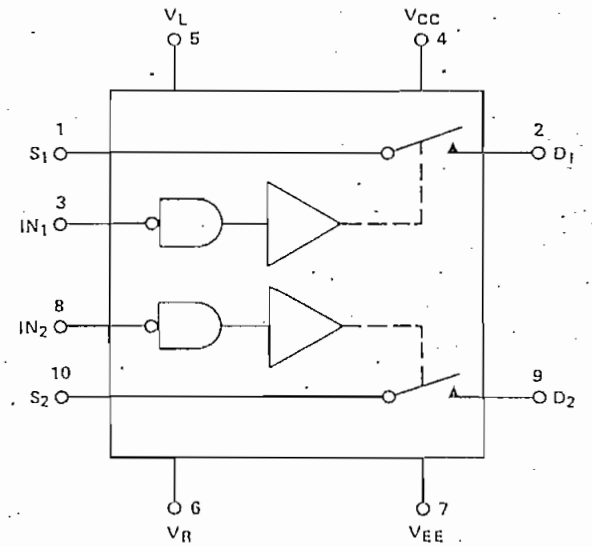
TWO CHANNEL HIGH-SPEED DRIVERS WITH SPST AND DPST JUNCTION FET SWITCHES

N-CHANNEL JUNCTION FETS AND MONOLITHIC DRIVERS FOR ANALOG OR DIGITAL SWITCHING APPLICATIONS

- Constant ON-Resistance with Signals to ±10 V and 100 MHz
- Cross-Talk and Open Switch Isolation, -50 dB at 10 MHz (100 Ohm Load)
- t_{on}, t_{off} < 150 ns, Break-Before-Make Action
- < 1 nA Leakage from Signal Channel in Both ON and OFF States
- Optional ±15 V Power Supplies
- TTL, DTL, RTL Direct Drive Compatibility

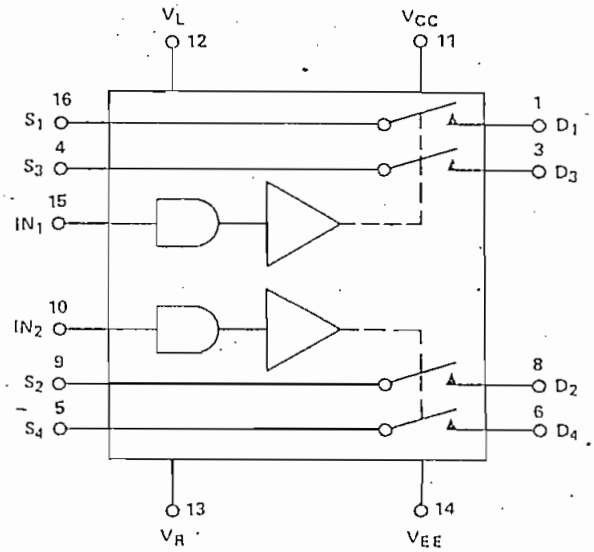
The DG181 series of analog switches features a unique circuit which eliminates the undesirable characteristics associated with other types of junction FET drive circuits. No design compromises are necessary to achieve all of the circuit performance features listed above. Applications include high-speed D/A converters, video camera switching, computer tape record/reproduce circuits, multiplexing, and commutation.

DG181, DG182



SWITCH STATES ARE FOR LOGIC "1" INPUT (V_{INH})

DG184, DG185



SWITCH STATES ARE FOR LOGIC "0" INPUT (V_{INL})

ABSOLUTE MAXIMUM RATINGS

$V_{CC} - V_{EE}$	36 V	$V_A - V_{EE}$	33 V
$V_{CC} - V_A$	33 V	$V_S - V_D$	±22 V
$V_L - V_{EE}$	36 V	$V_R - V_{EE}$	36 V
$V_L - V_{IN}$	8 V	$V_L - V_R$	8 V
$V_{IN} - V_R$	8 V	$V_R - V_{IN}$	2 V
Storage Temperature	-65°C to +150°C	Current (Any Terminal)	30 mA
Power Dissipation (Derate 10 mW/°C above 70°C)*	750 mW	Operating Temperature A Suffix	-55°C to +125°C
		Operating Temperature B Suffix	-20°C to +85°C

*Assumes device is mounted with all leads soldered or welded to PC board in ambient temperature above 70°C.

ELECTRICAL CHARACTERISTICS

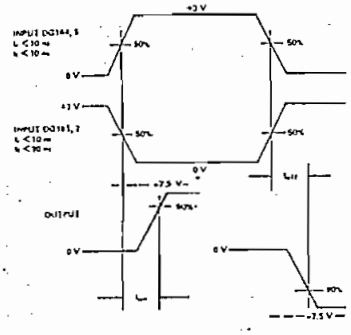
All DC parameters, t_{on} and t_{off}, are tested 100% at 25°C. Lots are sample tested to assure conformance with high and low temperature limits. NOTE: Automatic equipment test condition charts are available from factory or sales office as an aid to preparation of user specification control drawings.

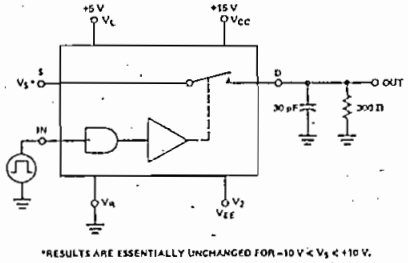
		Characteristic	Max Limits DG181A, DG184A -55°C	DG181A, DG184A 25°C	DG181A, DG184A 125°C	DG181B, DG184B -20°C	DG181B, DG184B 25°C	DG181B, DG184B 85°C	DG182A, DG185A -55°C	DG182A, DG185A 25°C	DG182A, DG185A 125°C	DG182B, DG185B -20°C	DG182B, DG185B 25°C	DG182B, DG185B 85°C	Unit	Test Conditions (Unless Otherwise Specified) V_{CC} = 15 V, V_{EE} = -15 V, V_L = 5 V, V_R = 0		
1	OUT	$r_{DS(ON)}$	30	30	60	50	50	75	75	75	150	100	100	150	Ω	V_S = ±$V_{A(MAX)}$, I_D = 1 mA		V_{INL} = 0.8 V V_{INH} = 2 V See drawings on page 1 for switch conditions when input is high or low.
2	OUT	$V_{A(MAX)}$		±7.5			±7.5			±10			±10		V	V_{CC} = 15 V, V_{EE} = -15 V		
3	OUT	$V_{A(MAX)}$		±10			±10			±10			±10		V	V_{CC} = 10 V, V_{EE} = -20 V		
4	OUT	$I_{S(OFF)}$*		1	100		5	100		1	100		5	100	nA	V_D = -10V, V_S = 10 V	V_{CC} = 10 V, V_{EE} = -20 V	
5	OUT	$I_{D(OFF)}$*		1	100		5	100		1	100		5	100	nA	V_S = -10 V, V_D = 10 V	V_{CC} = 10 V, V_{EE} = -20 V	
6	OUT	$I_{S(OFF)}$†		1	100		5	100		1	100		5	100	nA	V_D = -$V_{A(MAX)}$, V_S = $V_{A(MAX)}$		
7	OUT	$I_{D(OFF)}$†		1	100		5	100		1	100		5	100	nA	V_S = -$V_{A(MAX)}$, V_D = $V_{A(MAX)}$		
8	OUT	$I_{D(ON)} + I_{S(ON)}$*		-2	-200		-10	-200		-2	-200		-10	-200	nA	V_D = V_S = -$V_{A(MAX)}$		
9	IN	I_{INL}	-250	-250	-250	-250	-250	-250	-250	-250	-250	-250	-250	-250	μA	V_{IN} = 0		
10	IN	I_{INH}		10	20		10	20		10	20		10	20	μA	V_{IN} = 5 V		
11		t_{on}		150			180			150			150		ns	V_S = 7.5 V	R_L = 300Ω, C_L = 30 pF See Drawing	
12		t_{off}		130			150			130			150		ns	V_S = -7.5 V		
13		$C_{S(OFF)}$	9 Typical												pF	V_S = -5 V	f = 1 MHz	
14		$C_{D(OFF)}$	6 Typical												pF	V_D = -5 V	f = 1 MHz	
15		$C_{D(ON)} + C_{S(ON)}$	14 Typical												pF	V_D = V_S = 0	f = 1 MHz	
16		Crosstalk at 10 MHz	-50 Typical												dB	R_L = 100Ω, V_s = 3 V rms, f = 10 MHz		

*ON and OFF subscripts indicate conduction state of FET switch. L subscript indicates $V_{IN} = V_{INL}$. H subscript indicates $V_{IN} = V_{INH}$.
*Worst case leakage conditions.
†Tests insure that FET switch is OFF under worst case conditions.

CMJ-NG

SWITCHING TIME TEST CIRCUIT



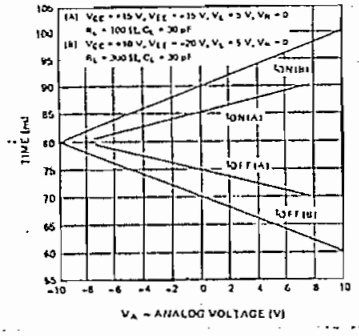


*RESULTS ARE ESSENTIALLY UNCHANGED FOR -10 V < V_S < +10 V.

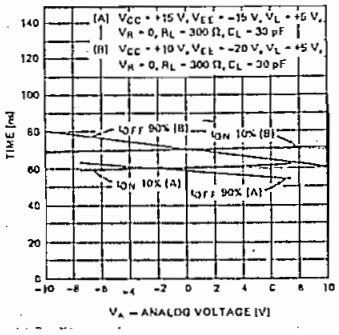
POWER SUPPLY CHARACTERISTICS (maximum limits)

	Characteristic	DG181A, B DG182A, B	DG184A, B DG185A, B	Unit	Test Condition
1	I_{CCL}	1.5	3	mA	V_{CC} = 15 V V_{EE} = -15 V V_L = 5 V V_R = 0 V_{INL} = 0 V_{INH} = 5 V (Total, not per channel)
2	I_{CCH}	1.5	3.1	mA	
3	I_{EEL}	-3	-5.5	mA	
4	I_{EEH}	-3	-4	mA	
5	I_{LL}, I_{LH}	4.5	4.5	mA	
6	I_{RL}, I_{RH}	-2	-2	mA	

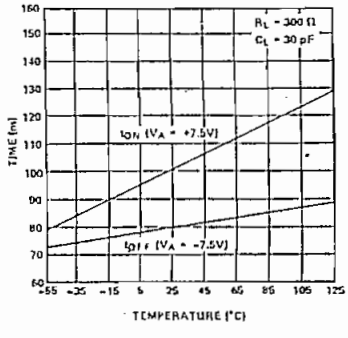
Switching Time vs Analog Voltage



Break Before Make Action

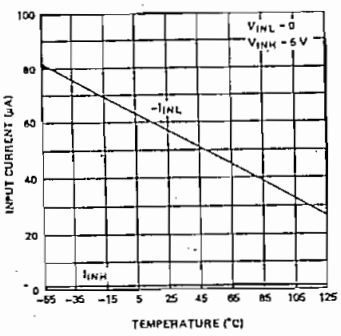


Switching Time vs Temperature

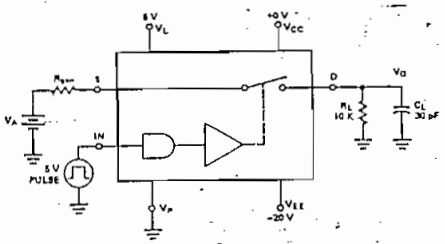


TYPICAL CHARACTERISTICS

Input Current vs Temperature

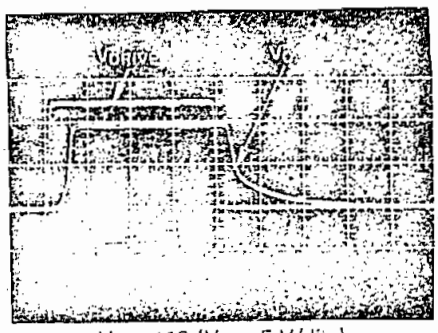


Typical delay, rise, fall, settling times, and switching transients in this circuit: (see photos at right)

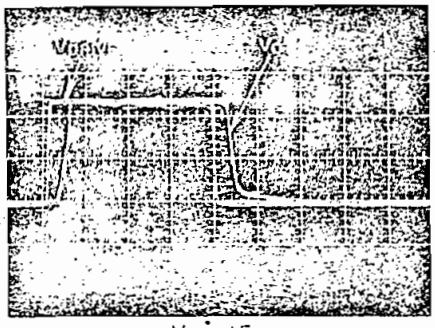


If R_{gen}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

All photos: horizontal scale = 200 ns/div., vertical scale = 2 V/div., unless otherwise noted.

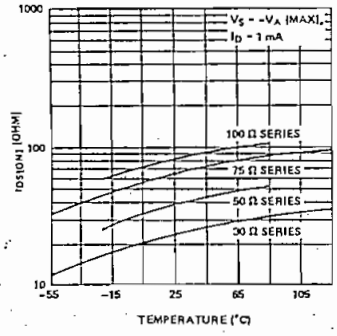


V_A = +10 (V_O = 5 V/div.)

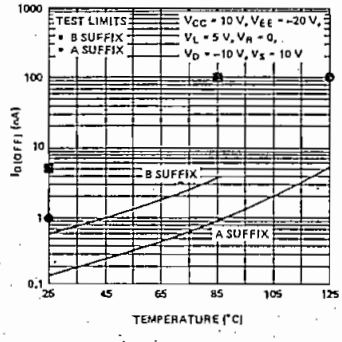


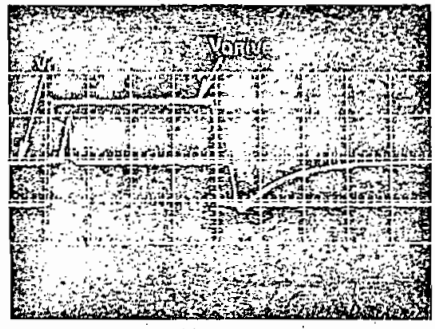
V_A = +5

$r_{DS(ON)}$ vs Temperature



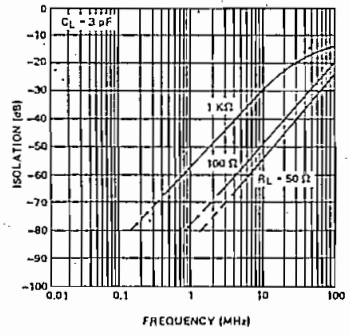
$I_{D(OFF)}$ vs Temperature

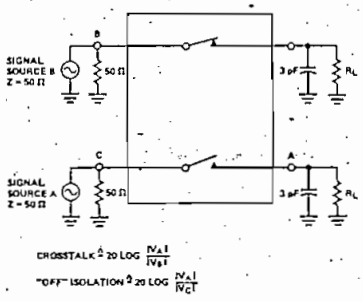


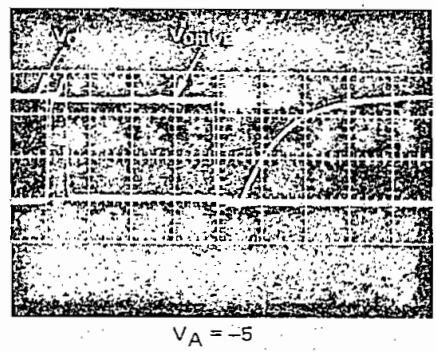


V_A = 0

Crosstalk and "OFF" Isolation vs Frequency

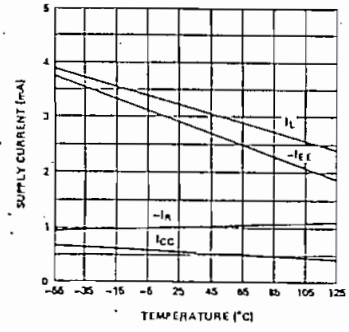




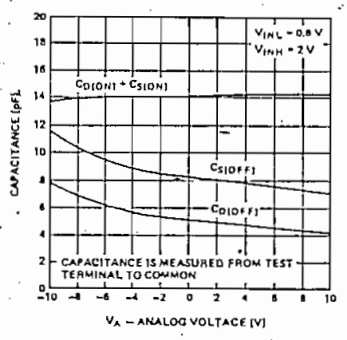


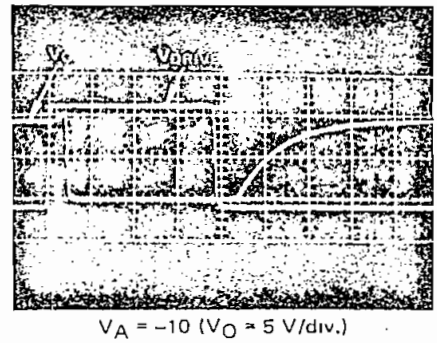
V_A = -5

Supply Currents vs Temperature



Switch Capacitance vs Analog Voltage





V_A = -10 (V_O = 5 V/div.)

APPLICATIONS

Input Interface - No external circuit elements are required to interface with TTL, DTL, or RTL logic.

Switching Transients and Settling Times - Switching transients are unavoidable unless some sort of neutralizing technique is used. Turn-on and turn-off transients occur because a step function control voltage applied to the FET gate terminal is coupled to the signal channel through C_{gd} and C_{sg} of the FET. Duration of the transient is largely under control of the external circuit . Settling time beyond the 150 ns switch actuation time is not affected by driver characteristics, but is purely a function of switch capacitance [$C_{D(ON)}$ + $C_{S(ON)}$], plus the external circuit R and C. Amplitude of the transient is a function of analog voltage levels and, to a lesser extent, the external circuit resistances. Total charge introduced into the load by the turn-off transient is approximately 60 picocoulombs. (See waveforms on page 3.)

High-Frequency Performance - High frequency or pulse waveform analog signals do not cause modulation of the switch ON resistance. There is no discernable change in ON resistance for analog signals of 7 V rms to 100 MHz. The single limitation to high-frequency performance is the value of switch OFF isolation, which decreases as frequency increases, and which may become of importance at operation beyond 10 MHz. (See characteristics curve on page 3.)

Switching Applications - Typical applications for the DG181 series are in high-speed D/A converters, video cameras, computer tape record/reproduce circuits, RF data processing, and low-Z multiplexing or switching circuits. Special versions of devices in the series are available with switch ON resistance as low as 2 ohms for most-significant-bit switching in R-2R D/AC ladder networks.

PRODUCT CONDITIONING

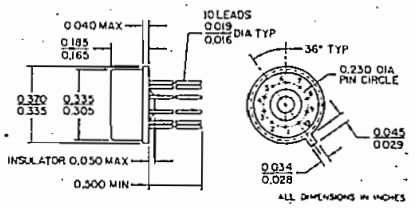
Military (A) Suffix
Units are processed according to MIL-STD-883, Method 5004, Class B, Notice 2 dated Nov. 20, 1969 (Burn-In on special order).

Industrial (B) Suffix
Units receive the following processing before final electrical test.

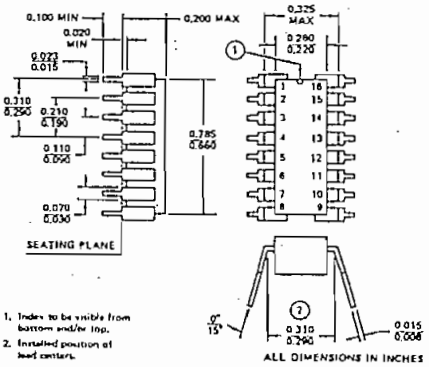
Temperature Cycle
-65 to +150° C, 5 Cycles

Hermeticity
Fluorocarbon Gross Leak, 100%
Helium Fine Leak, 2% AQL

MECHANICAL DATA



TO-100
DG181AA, DG182AA
DG181BA, DG182BA

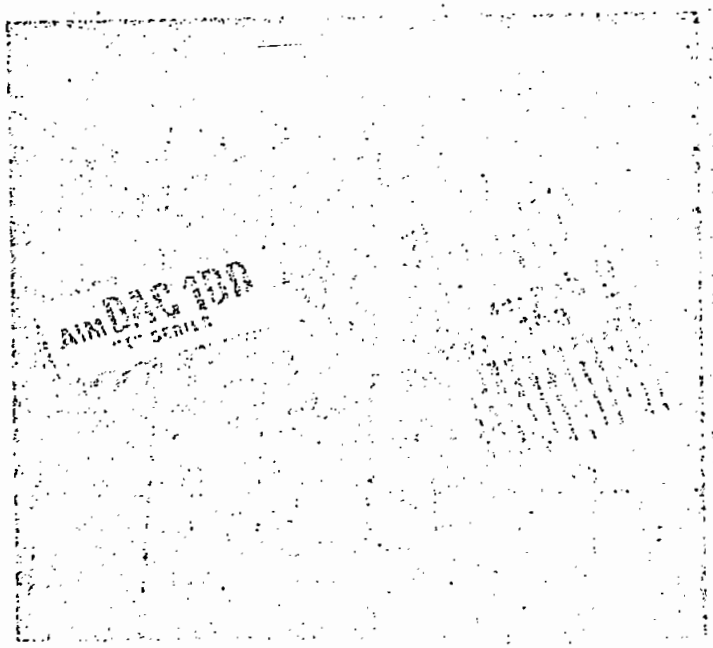


16-Pin Dual-In-Line Package
DG184AP, DG185AP
DG184BP, DG185BP

8 & 10 BIT I.C. DIGITAL-TO-ANALOG CONVERTER SERIES

FEATURES:

- COMPLETE ..... INCLUDES REFERENCE, CURRENT SOURCES LADDER, SWITCHES
- COMPACT ..... 16 PIN DIP OR 24 PIN FLATPACK
- COMPATIBLE ..... TTL, DTL LOGIC LEVELS
- LOW POWER ..... 80mW TYP AT ±6V
- WIDE SUPPLY RANGE ..... ±6V TO ±18V
- FAST SETTLING .... 225nS (8 BITS), 375nS (10 BITS)
- 8 & 10 BIT MODELS ..... WIDE CHOICE OF SPECIFICATIONS
- FLEXIBLE ..... HIGH SPEED 0-2mA OUTPUT
- RELIABLE ..... 100% POWER BURN-IN @ 125°C
- STABLE ..... TEMPCOS TO ±15ppM/°C MAX
- HIGH LINEARITY .. TO 0.05% MAX, –25°C TO +85°C
- WIDE OPERATING TEMP RANGE ...–55°/+125° AND 0°/+70°C
- LOW COST ..... FROM $9.95 @ 100 PCS.

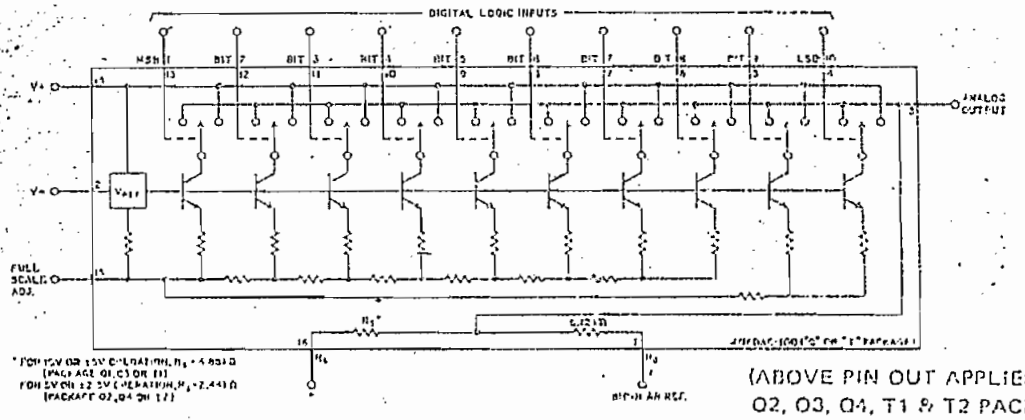


GENERAL DESCRIPTION

The AIMDAC 100 series are complete 10 bit resolution Digital-to-Analog converters constructed on two monolithic chips in a single 16 pin DIP or 24 pin flatpack. Featuring excellent linearity vs. temperature performance, the AIMDAC 100 includes a low tempco voltage reference, 10 current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output, and matched bipolar offset and feedback resistors are included for use with an external op amp for voltage output applications. Although all units have 10 bit resolution, a wide choice of linearity and tempco options are provided to allow optimization of price/performance ratio.

The small size, wide operating temperature range, low power consumption and high reliability construction make the AIMDAC100 ideal for aerospace applications, with MIL-M-38510 processing available. Low cost 0°/+70°C versions are available for all industrial requirements. Applications for the AIMDAC100 series include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power suppliers, analog meter movement drivers, waveform generators and in high speed Analog-to-Digital converters.

SIMPLIFIED SCHEMATIC AND PIN CONNECTION DIAGRAM (DUAL-IN-LINE PACKAGES)



(ABOVE PIN OUT APPLIES FOR 01, 02, 03, 04, T1 & T2 PACKAGES)

The premium performance of this product is achieved through an advanced processing technology. All Precision Monolithics products are guaranteed to meet or exceed published specifications.

ELECTRICAL CHARACTERISTICS:

These specifications apply for $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for Q1, Q2 and N1 devices; $0^\circ C \leq T_A \leq +70^\circ C$ for Q3, Q4, T1 and T2 devices, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		10	10	10	bits
Linearity	"A" option (±½ LSB – 10 bits)	–	–	0.05	% I_{FS}
	"B" option (±½ LSB –9 bits)	–	–	0.1	% I_{FS}
	"C" option (±½ LSB –8 bits)	–	–	0.2	% I_{FS}
	"D" option (±¾ LSB –8 bits)	–	–	0.3	% I_{FS}
Full Scale Tempco of I_{FS}	"A" option	–	–	15	ppm/°C
	"B" option	–	–	30	ppm/°C
	"C" option	–	–	60	ppm/°C
	"D" option	–	–	120	ppm/°C
	(For available linearity/tempco combinations, see Ordering Information)				
Settling Time	$T_A = 25^\circ C$, to 0.05%	–	–	375	ns
	$T_A = 25^\circ C$, to 0.1%	–	–	300	ns
	$T_A = 25^\circ C$, to 0.2%	–	–	225	ns
	$T_A = 25^\circ C$, to 0.4%	–	–	150	ns
	$T_A = 25^\circ C$, to 0.8%	–	–	100	ns
Full Scale Output Voltage	Connect FS Adjust to V–				
	10V Models (Q1, Q3, T1, N1)	10	–	10.1	V
	5V Models (Q2, Q4, T2, N1)	5	–	5.05	V
	(Limits guarantee adjustability to exact 10.0 (5.0)V with a 200Ω trimpot between FS Adjust and V–.)				
Zero Scale Output Voltage		–	–	0.006	% FS
Logic Inputs	Measured with respect to output pin				
High		2.1	–	–	V
Low		–	–	0.7	V
Logic Input Current, Each Input	V_{IN} = 0 to +6V	–	–	5	μA
Logic Input Resistance	V_{IN} = 0 to +6V	–	3	–	MΩ
Logic Input Capacitance		–	2	–	pF
Output Resistance		–	100	–	kΩ
Output Capacitance		–	13	–	pF
Applied Power Supplies:					
V+	Linearity within specification	+6	–	+18	V
V–	Linearity within specification	–6	–	–18	V
Power Supply Rejection	V_S = ±6V to ±18V	–	–	0.01	%per %
Power Consumption					
Q1, Q2, N1 models	V_S = ±6V	–	80	100	mW
	V_S = ±15V	–	200	250	mW
Q3, Q4 (T1), T2 models	V_S = ±15V	–	200	300	mW

AIMDAC100 APPLICATION NOTES

LOGIC CODING -- The AIMDAC100 uses complementary or inverted binary logic coding, i.e., an all "zeroes" input produces a full scale output, while an all "ones" input produces a zero scale output. The output may be easily modified to accommodate complementary offset binary, complementary one's complement and complementary two's complementary codes.

LOGIC COMPATIBILITY -- The input logic levels are directly compatible with DTL and TTL logic and may also be used with CMOS logic powered from a single +5 volt supply.

LOWER RESOLUTION APPLICATIONS -- The AIMDAC100 may be used in applications requiring less than 10 bits of resolution. All unused logic inputs *must* be tied to the high logic for proper operation. "Floating" logic inputs can cause improper operation.

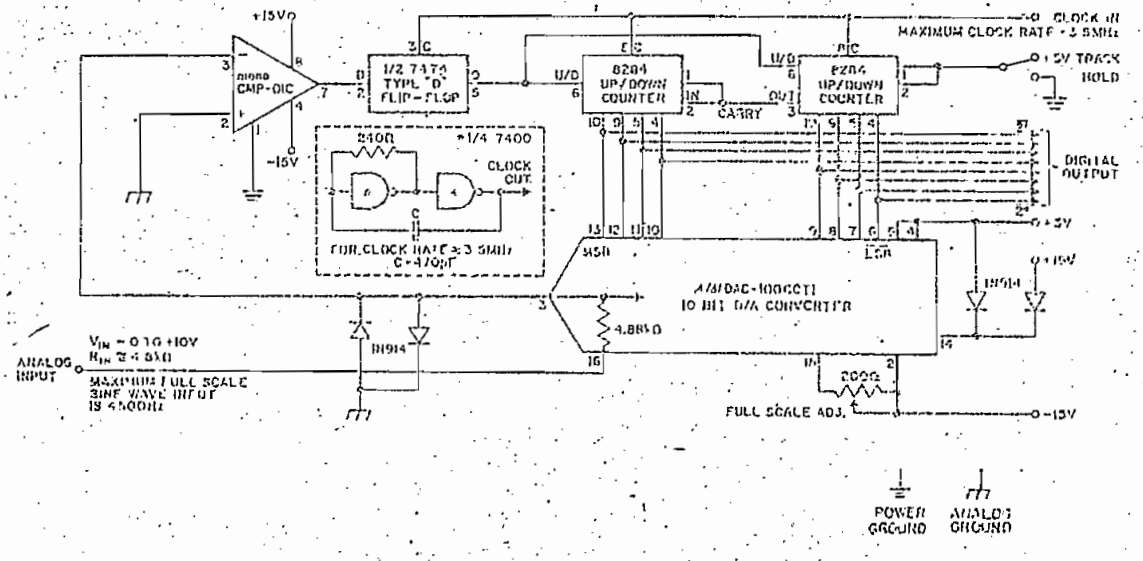
FULL SCALE OUTPUT ADJUSTMENT -- The output current of the AIMDAC100 may be reduced to produce an exact 10.000 (5.000) volt output by connecting a 200Ω adjustable resistance between the Full Scale Adjust pin and V--. Adjustment should be made with an input of all "zeroes."

BIPOLAR OPERATION -- The AIMDAC100 may be converted to bipolar operation by injecting a half-scale current into the output; this is accomplished by connecting the internal bipolar resistor to a +6.4 volt reference. Trimming of the zero output may be facilitated by placing a 500Ω adjustable resistance in series with the +6.4 volt reference. Trimming procedure is as follows: with inputs at 1 to all "ones", adjust Bipolar Offset pot to desired negative Full Scale Voltage; with inputs set to all "zeroes," adjust Full Scale pot to desired positive Full Scale Voltage. (Make certain correct end point voltages are used with one's and two's complement codings.)

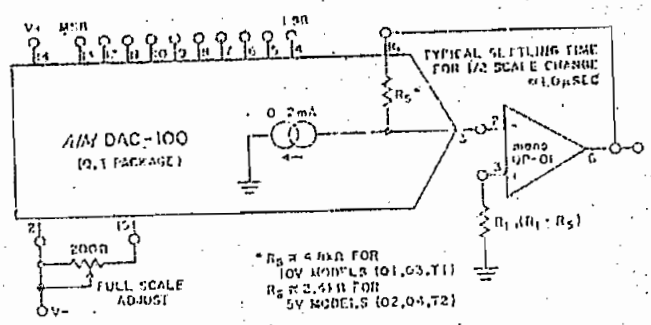
VOLTAGE AT OUTPUT PIN -- The AIMDAC100 is designed to be operated with the voltage at the output pin held very close to zero volts. Input logic threshold levels are directly affected by output pin voltage changes; voltage swings at the output may cause loss of linearity due to improper switching of bits. Large voltage swings may cause permanent damage and should be avoided. Proper operation can be obtained with output voltages held within ±0.7 volts; a pair of back-to-back silicon diodes tied from the output ground is a convenient way of clamping the output to this limit.

POWER SUPPLY SEQUENCING - IMPORTANT -- Occasional early AIMDAC100 devices may suffer temporary malfunction and possible permanent damage if voltage is present at the logic inputs before the V+ supply is available. A simple protection circuit may be implemented by using two silicon diodes to clamp the V+ terminal to the logic supply as shown in the diagram on page 7. AIMDAC100 devices with date codes of 7251 and later incorporate design changes which eliminate this effect and require no special precautions or protective circuitry.

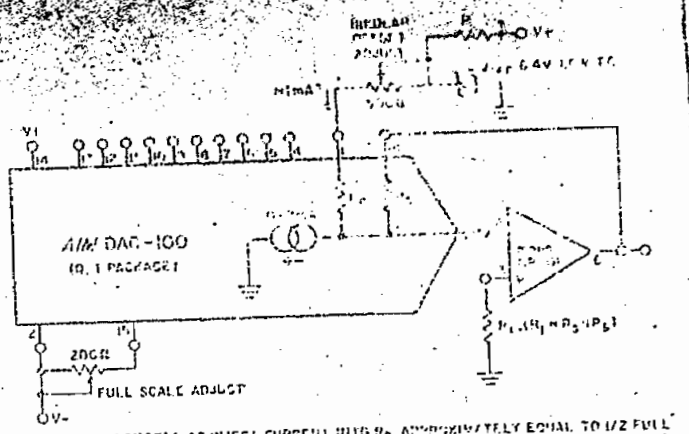
LOW COST 8 BIT TRACKING A/D CONVERTER



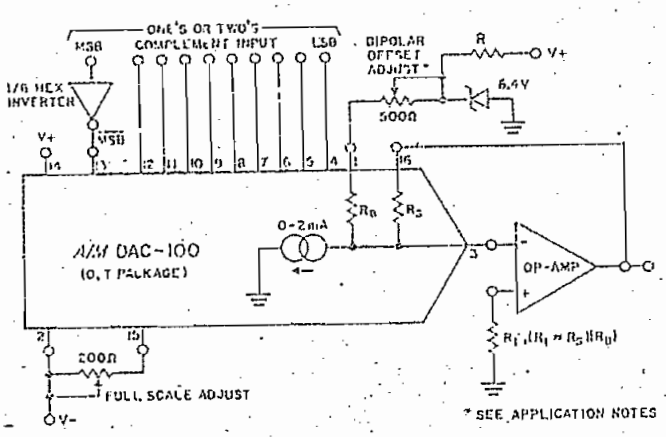
(FOR FULL DETAILS, REQUEST APPLICATION NOTE "A LOW COST, HIGH PERFORMANCE TRACKING A/D CONVERTER")



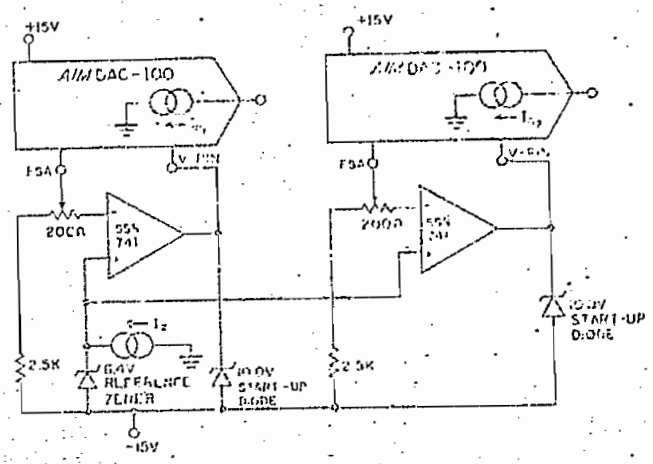
BASIC UNIPOLAR VOLTAGE OUTPUT 10 BIT D/A CONVERTER



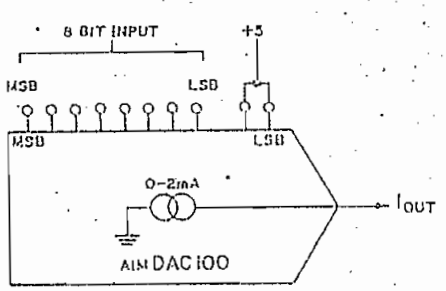
BIPOLAR VOLTAGE OUTPUT CIRCUIT



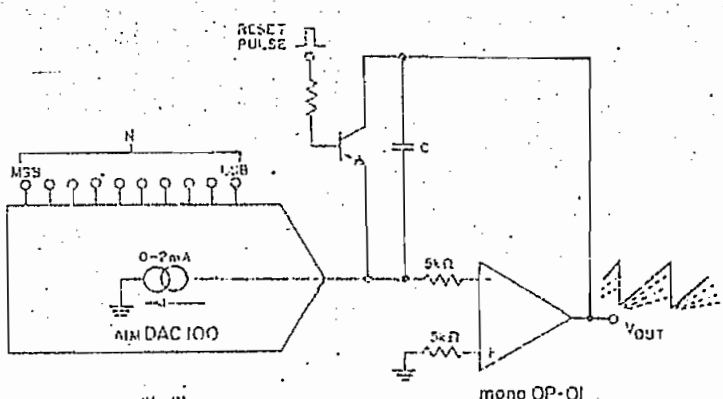
ACCOMODATING ONE'S OR TWO'S COMPLEMENT DIGITAL CODES



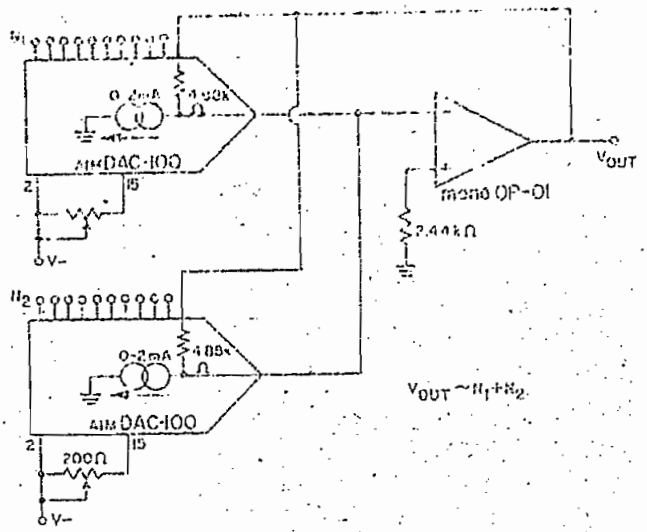
SLAVING AIM DAC-100 TO EXTERNAL REFERENCE



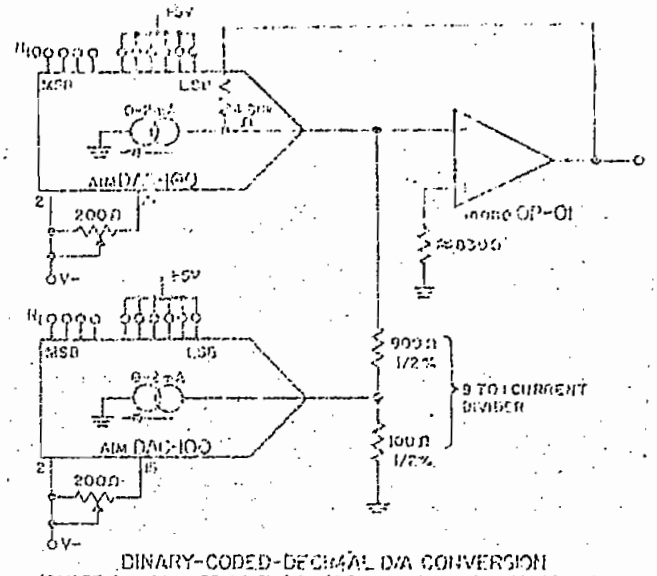
REDUCED RESOLUTION APPLICATIONS
(ALL UNUSED LOGIC INPUTS MUST BE TIED TO V_{LL})



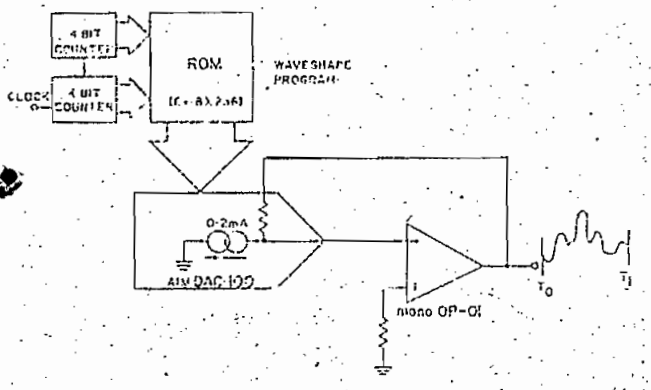
DIGITALLY PROGRAMMED RAMP GENERATOR



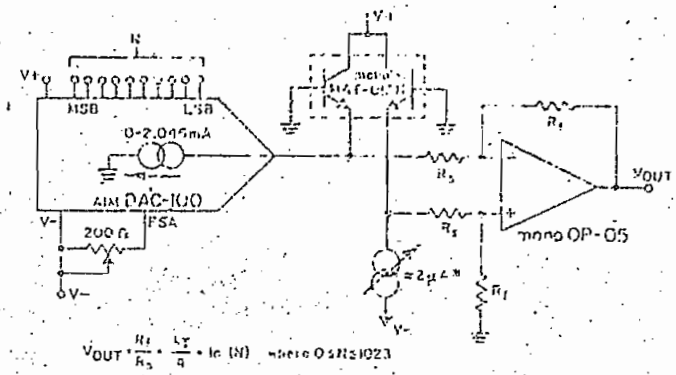
ANALOG SUM OF TWO DIGITAL NUMBERS
(USE 10VOLT FULL SCALE AIM DAC-100 MODELS FOR 0-10VOLT OUTPUT)



BINARY-CODED-DECIMAL D/A CONVERSION
(CAN BE EXPANDED TO 4 DIGITS BY ADDITION OF A THIRD DAC-100 AND 99 TO 1 CURRENT DIVIDER)



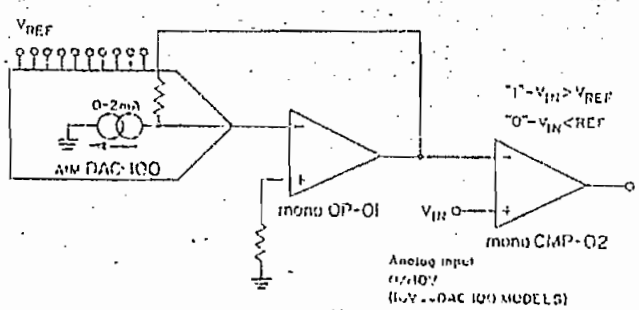
ARBITRARY PERIODIC WAVEFORM GENERATOR



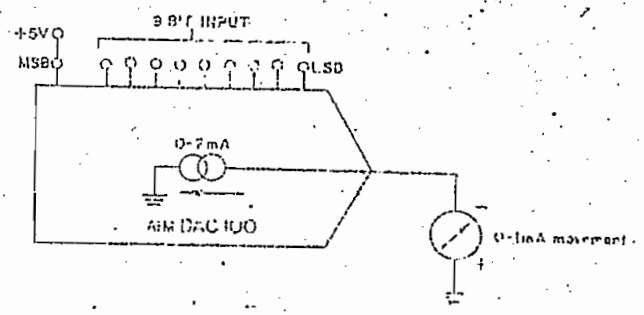
$V_{OUT} = \frac{R_f}{R_s} \cdot \frac{kT}{q} \cdot \ln(N)$ where $0 \le N \le 1023$

*ADJUST TO PROPER OUTPUT AT N=32

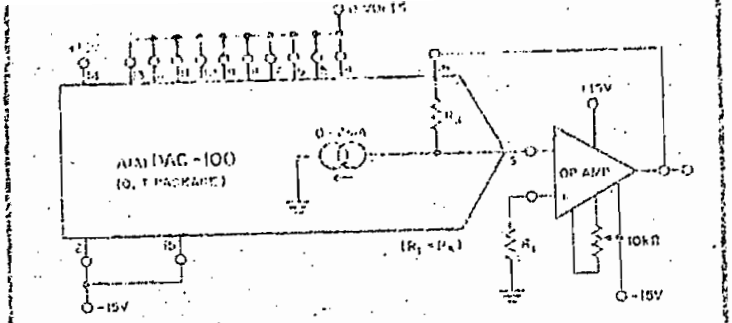
10 BIT DIGITAL-TO-LOGARITHMIC CONVERTER



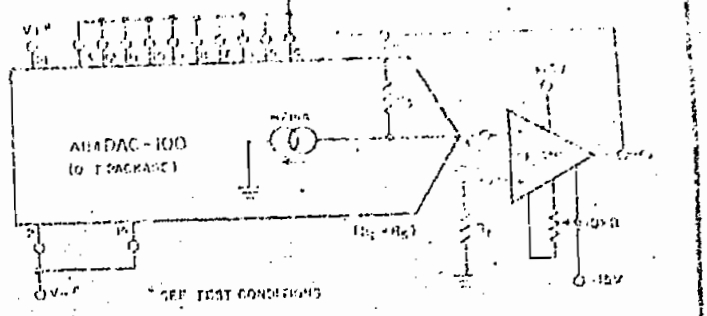
DIGITALLY PROGRAMMABLE LEVEL DETECTOR



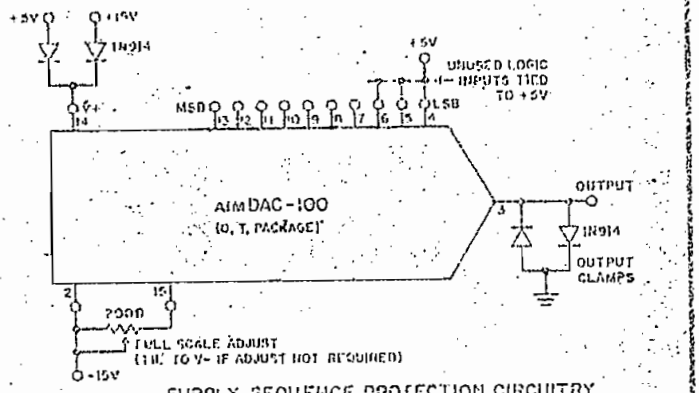
ANALOG DISPLAY OF DIGITAL NUMBER
(NOTE: 10 BIT RESOLUTION MAY BE USED WITH 0-1mA METER MOVEMENT)



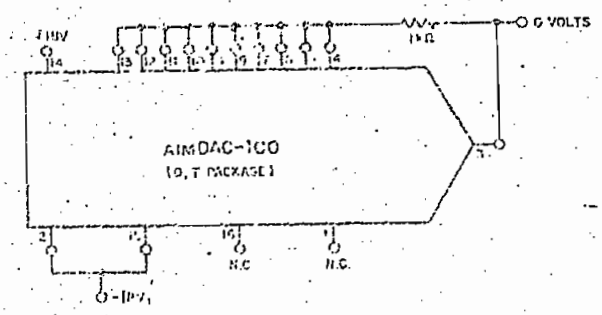
FULL SCALE OUTPUT VOLTAGE TEST CIRCUIT



POWER SUPPLY REJECTION TEST CIRCUIT

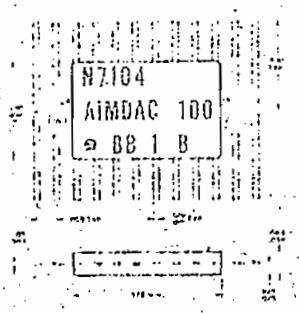


SUPPLY SEQUENCE PROTECTION CIRCUITRY
(IMPORTANT-SEE APPLICATION NOTES)

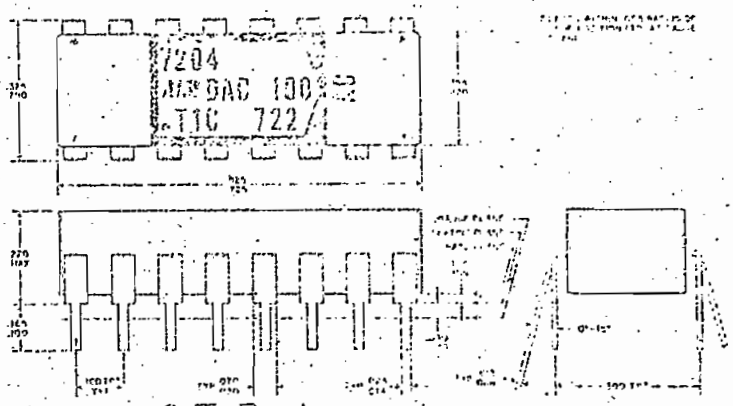


BURN-IN CIRCUIT

PACKAGE DIMENSIONS

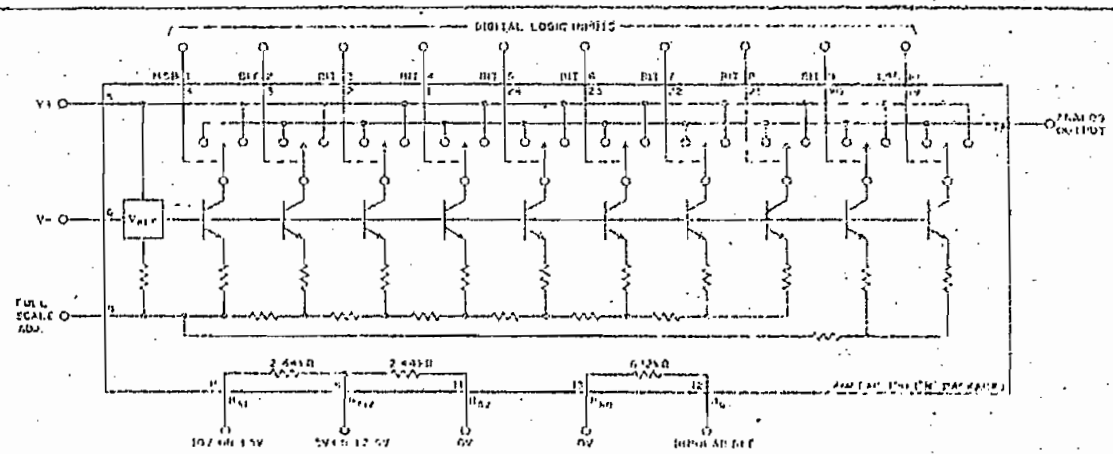


N Package



Q,T Packages

SIMPLIFIED SCHEMATIC AND PIN CONNECTION DIAGRAM — N1 TYPE 24 LEAD FLAT PACKAGES ONLY



NOTE: AIMDAC100 DEVICES CAPABLE OF DIRECTLY REPLACING μA722 DEVICES INCLUDING ASSOCIATED RESISTOR NETWORK ARE AVAILABLE; CONTACT FACTORY REGARDING AIMDAC100 "N2" SERIES FOR INFORMATION.

AMDAC100 DEFINITIONS

LSB–LEAST SIGNIFICANT BIT – The smallest incremental output change obtainable, which is ideally equal to the full scale output divided by $2^n - 1$, where n = number of bits.

MSB–MOST SIGNIFICANT BIT – The largest incremental output change obtainable by switching a single logic input, which is ideally equal to the ideal LSB multiplied by 2^{n-1} where n = number of bits.

LOGIC INPUT "0" – The (low) logic input voltage necessary to hold a bit on.

LOGIC INPUT "1" – The (high) logic input voltage necessary to hold a bit off.

LINEARITY – Maximum deviation of the output voltage from the straight line through zero scale and full scale at a given temperature, expressed as a percentage of $(V_{FS} - V_{ZS})$.

DIFFERENTIAL LINEARITY – Maximum deviation from the ideal LSB value of any step between successive states.

MONOTONICITY – Having each successive output state greater than or equal to the preceding one when the DAC is sequenced through all successive states from V_{ZS} to V_{FS}.

AVERAGE TEMPERATURE COEFFICIENT – Change in absolute full scale output in ppm between 25°C and either temperature extreme divided by the corresponding change in temperature.

ZERO SCALE OUTPUT VOLTAGE – The output voltage (V_{ZS}) produced by a zero scale input code (0000000).

RESOLUTION – The number of states (2^n) that the full scale output may be divided (resolved) into.

ACCURACY – The total deviation from the ideal output as a percentage of Full Scale Output. This deviation is due to the combination of errors from linearity, full scale tempco, zero offset and all other error sources. For the AMDAC100, worst case total accuracy may be closely approximated by adding the maximum linearity specification to the product of the Full Scale tempco times .0001% times the difference between maximum operating temperature and 25°C (Example: for AA grade, 0.05% + 15 × (85-25) × .0001% = 0.14%).

POWER SUPPLY REJECTION – The ratio of the percentage change in full scale output to the change in the supply voltage producing it.

POWER CONSUMPTION – The quiescent DC power required to operate the device.

SETTLING TIME – The elapsed time from the start of the input pulse until the output has settled to and remained within ± ½ LSB of its final value for a full scale excursion.

COMPLEMENTARY BINARY CODING – Logic code in which each lesser significant bit's weight is one-half the previous more significant bit's value. High logic input level turns the bit "off," low logic input level turns the bit "on."

For other related Precision Monolithics, Inc. components, see the following data sheets:

6 Bit I C D/A Converter monoDAC-01

8 & 10 Bit I C Sign/Magnitude DAC. monoDAC-02

8 & 10 Bit I C Two's Complement DAC monoDAC-04

Fast Precision Comparator monoCMP-01

Low Input Current Precision Comparator . . monoCMP-02

Fast Slewing/Fast Settling Op Amp monoOP-01

Low Noise, Low Drift Compensated Op Amp . monoOP-05

Dual Matched Op Amp monoOP-10

High Voltage Gas Discharge Display Digit Driver. monoDRV-01

Ultra Matched Dual Transistor monoMAT-01

Low Noise, Low Drift Op Amp SSS725

Improved Performance 741 Op Amp. SSS741

PRECISION MONOLITHICS INCORPORATED
1500 SPACE PARK DRIVE, SANTA CLARA, CALIFORNIA 95050
TEL. (408)246-9225 · TWX 910-339-0522 · CABLE MONO

A Western Digital Affiliate
LITHO IN U.S.A.

Am2502/2503/2504

Eight-Bit/Twelve-Bit Successive Approximation Registers

Advanced Micro Devices

Complex Digital Integrated Circuits

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel counter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

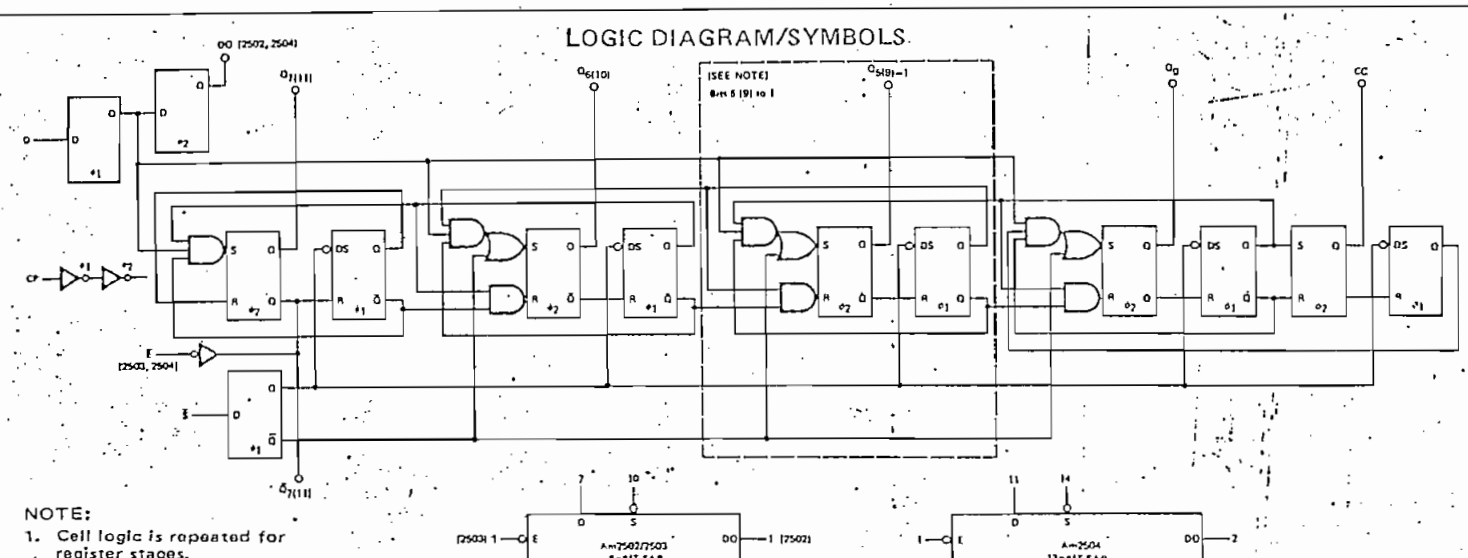
The Am2502, Am2503 and Am2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am2502 and Am2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am2503 and Am2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

LOGIC DIAGRAM/SYMBOLS



NOTE:
1. Cell logic is repeated for register stages.
   Q_5 to Q_1 Am2502/3
   Q_9 to Q_1 Am2504
2. Numbers in parentheses are for Am2504

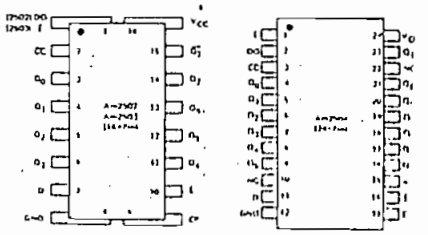
V_{CC} = Pin 16
GND = Pin 12
NC = Pins 10, 15, 22

ORDERING INFORMATION

Package Type	Temperature Range	Am2502 Order Number	Am2503 Order Number	Am2504 Order Number
Molded DIP	0°C to +75°C	AM2502PC	AM2503PC	AM2504PC
Hermetic DIP	0°C to +75°C	AM2502DC	AM2503DC	AM2504DC
Hermetic DIP	−55°C to +125°C	AM2502DM	AM2503DM	AM2504DM
Hermetic Flat Pak	−55°C to +125°C	AM2502FM	AM2503FM	AM2504FM
Dice	Note	AM2502XX	AM2503XX	AM2504XX

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top View



NOTE: PIN 1 is marked for orientation

age Temperature	
perature (Ambient) Under Bias	−55°C to +125°C
ply Voltage to Ground Potential Continuous	−0.5 V to +7 V
Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
Input Voltage	−0.5 V to +5.5 V
put Current, Into Outputs	30 mA
Input Current	−30 mA to +5.0 mA

ECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

2502XC Am2503XC Am2504XC $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0V \pm 5\%$
2502XM Am2503XM Am2504XM $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

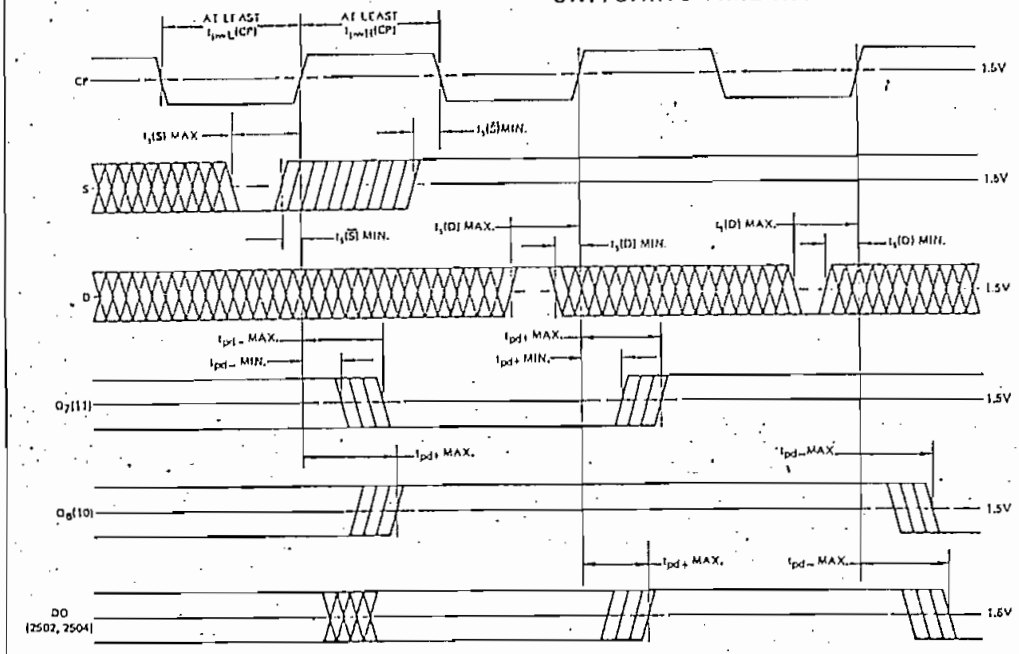
ameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.48mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 9.6mA V_{IN} = V_{IH} or V_{IL}				0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				6.0	40	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			−10	−25	−45	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am2502	XM		65	85	mA
				XC		65	95	
			Am2503	XM		60	80	mA
				XC		60	90	
			Am2504	XM		90	110	mA
				XC		90	124	

te 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

vitching Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$

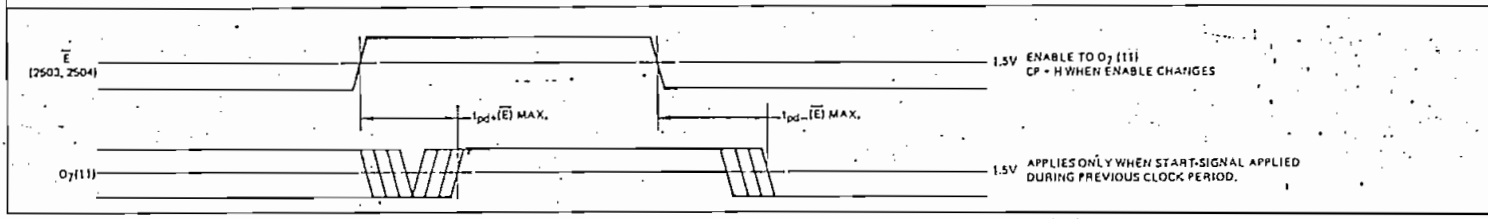
rameters	Description		Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay CP to Output HIGH		10	26	38	ns
t_{pd-}	Turn On Delay CP to Output LOW		10	18	28	ns
$t_s(D)$	Set-up Time Data Input		−10	4	8	ns
$t_s(S)$	Set-up Time Start Input		0	9	16	ns
$t_{pd+}(E)$	Turn Off Delay E to Q_7(11) HIGH	(Am2503/4)		13	19	ns
$t_{pd-}(E)$	Turn On Delay E to Q_7(11) LOW	C_P = H, $\overline{S}$ = L		16	24	ns
$t_{pwL}(CP)$	Minimum LOW Clock Pulse Width			28	46	ns
$t_{pwH}(CP)$	Minimum HIGH Clock Pulse Width			12	20	ns
f_{max}	Maximum Clock Frequency		15	25		MHz

SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2 L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP The clock input of the register.

$\overline{CC}$ The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D The serial data input of the register.

$\overline{E}$ The register enable. This input is used to expand the length of the register and when HIGH forces the $Q_7(11)$ register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

$Q_7(11)$ The true output of the MSB of the register.

$\overline{Q}_7(11)$ The complement output of the MSB of the register.

Q_i i = 7(11) to 0 The outputs of the register.

$\overline{S}$ The start input. If the start input is held LOW for at least a clock period the register will be reset to $Q_7(11)$ LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

DO The serial data output. (The D input delayed one bit).

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level).

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

$t_{pd-}(\overline{E})$ The propagation delay from the Enable signal HIGH-LOW transition to the $Q_7(11)$ output signal HIGH-LOW transition.

$t_{pd+}(\overline{E})$ The propagation delay from the Enable signal LOW-HIGH transition to $Q_7(11)$ output signal LOW-HIGH transition

$t_s(D)$ Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max. and t_s min. before the clock.

$t_s(\overline{S})$ Set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

$t_{pw}(CP)$ The minimum clock pulse width (LOW or HIGH) required for proper register operation.

Am2502/3 TRUTH TABLE

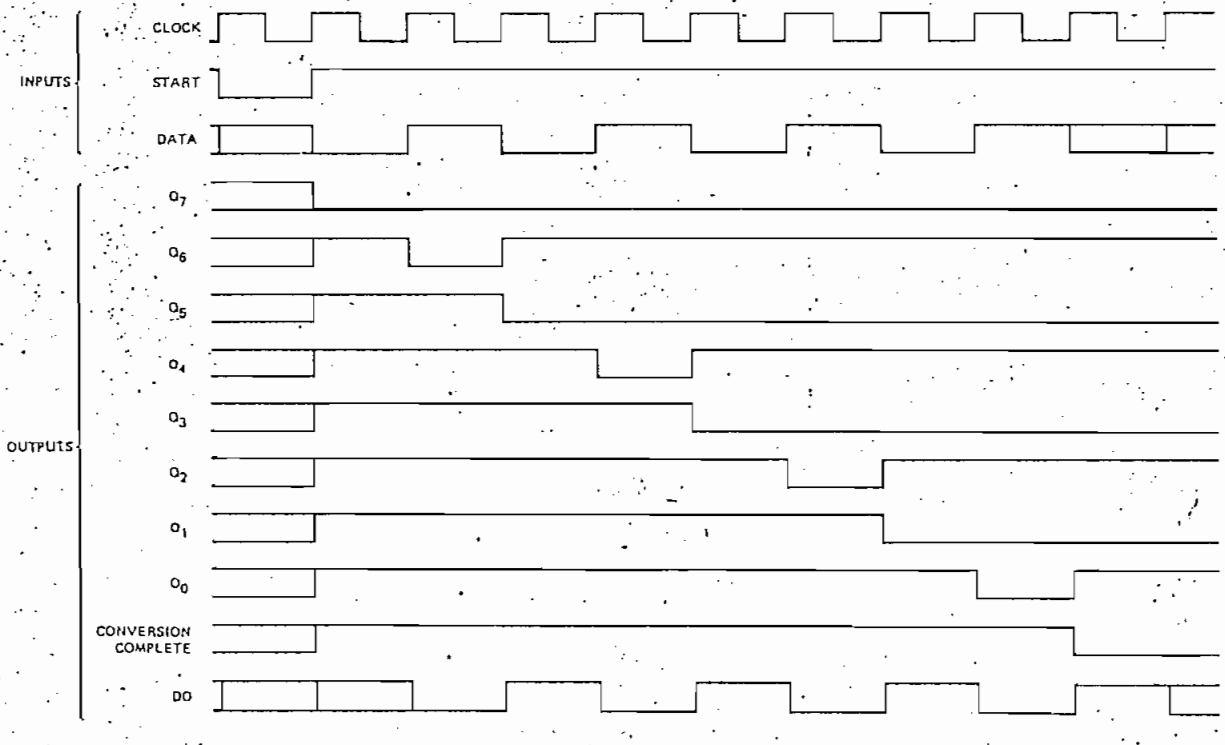
Time	Inputs			Outputs									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for Am2504 is extended to include 12 outputs.

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased −½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½ LSB and using the complement of the MSB Q_7 (11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

Am2502/3 TIMING CHART



Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Output Fanout HIGH	Output Fanout LOW
$\overline{E}$ (2503)	1	2	2	—	—
DO (2502)	1	—	—	12	6
$\overline{CC}$	2	—	—	12	6
Q_0	3	—	—	12	6
Q_1	4	—	—	12	6
Q_2	5	—	—	12	6
Q_3	6	—	—	12	6
D	7	2	2	—	—
GND	8	—	—	—	—
CP	9	1	1	—	—
$\overline{S}$	10	1	2	—	—
Q_4	11	—	—	12	6
Q_5	12	—	—	12	6
Q_6	13	—	—	12	6
$\overline{Q_7}$	14	—	—	12	6
Q_7	15	—	—	12	6
V_{CC}	16	—	—	—	—

MSI INTERFACING RULES

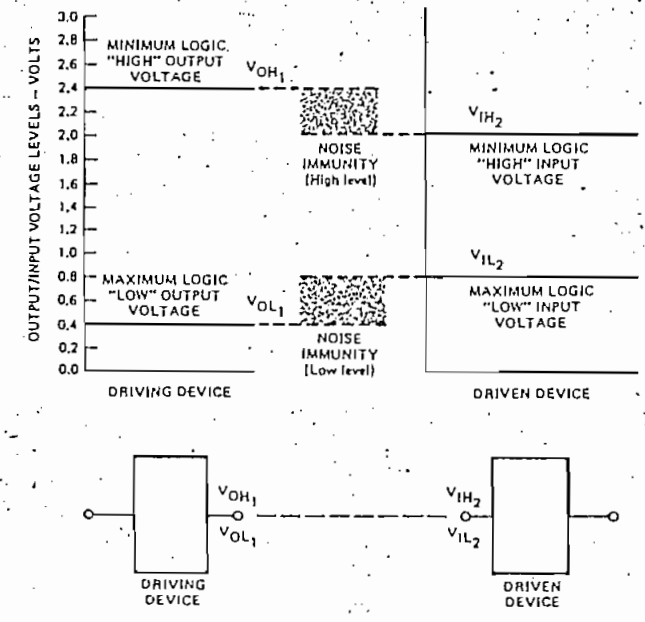
Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Output Fanout HIGH	Output Fanout LOW
$\overline{E}$	1	2	2	—	—
DO	2	—	—	12	6
$\overline{CC}$	3	—	—	12	6
Q_0	4	—	—	12	6
Q_1	5	—	—	12	6
Q_2	6	—	—	12	6
Q_3	7	—	—	12	6
Q_4	8	—	—	12	6
Q_5	9	—	—	12	6
NC	10	—	—	—	—
D	11	2	2	—	—
GND	12	—	—	—	—
CP	13	1	1	—	—
$\overline{S}$	14	1	2	—	—
NC	15	—	—	—	—
Q_6	16	—	—	12	6
Q_7	17	—	—	12	6
Q_8	18	—	—	12	6
Q_9	19	—	—	12	6
Q_{10}	20	—	—	12	6
$\overline{Q_{11}}$	21	—	—	12	6
NC	22	—	—	—	—
Q_{11}	23	—	—	12	6
V_{CC}	24	—	—	—	—

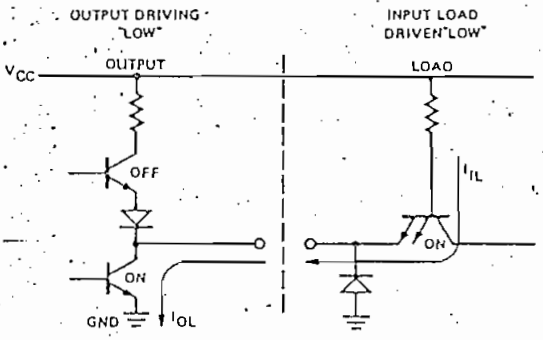
NC = No Connection

INPUT/OUTPUT INTERFACE CONDITIONS

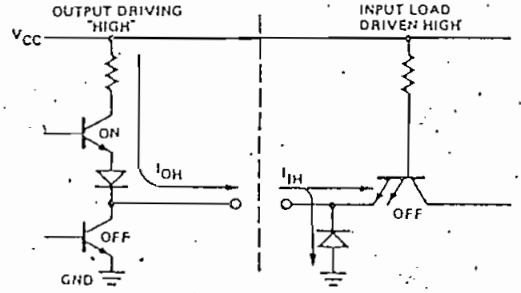
Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW

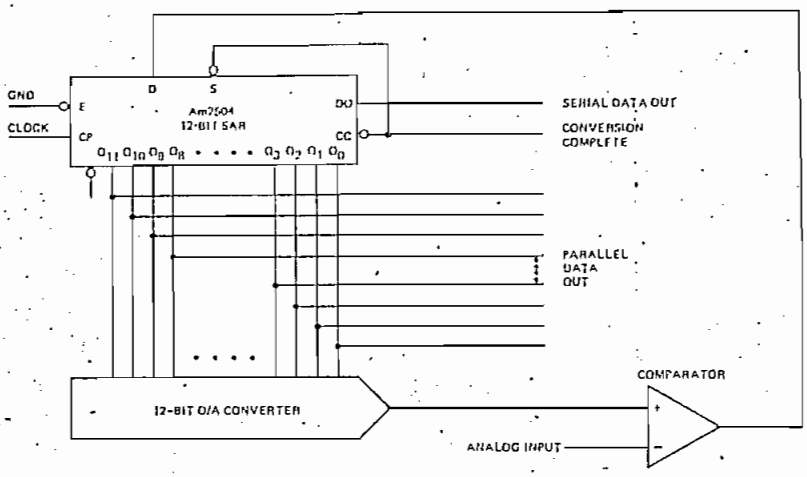


Current Interface Conditions — HIGH



Am2502/3/4 APPLICATION

Continuous Conversion Analog-to-Digital Converter



This shows how the Am2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second. A 10-bit continuous conversion can be performed by connecting Q_1 to Q_3 and using Q_1 as the conversion complete signal. The comparator can be the Am111 precision comparator, Am106 high-speed comparator, or Am686 very high-speed comparator.

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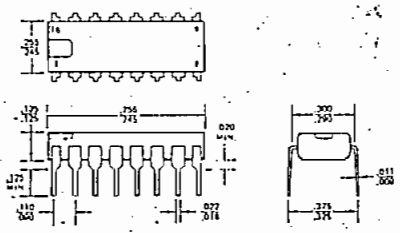
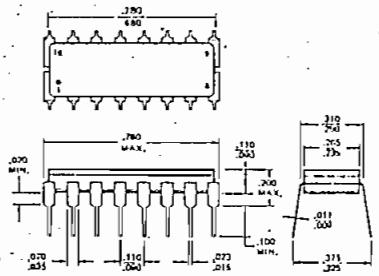
PHYSICAL DIMENSIONS

Am2502/3

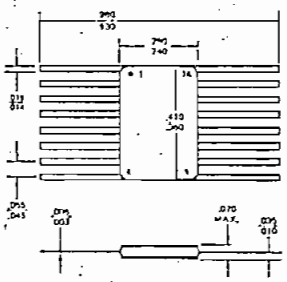
16-Pin Molded DIP



16-Pin Hermetic DIP

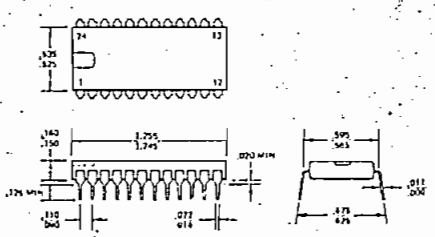


16-Pin Flat Pak

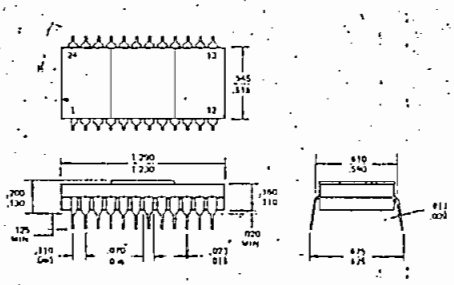


Am2504

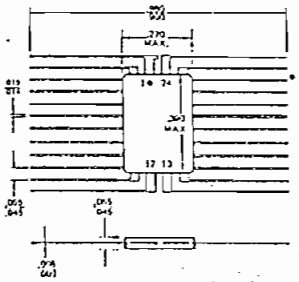
24-Pin Molded DIP



24-Pin Hermetic DIP

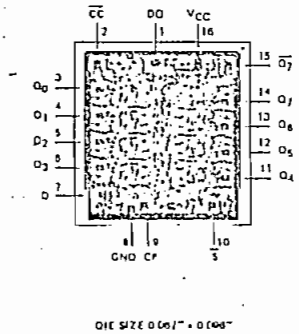


24-Pin Flat Pak

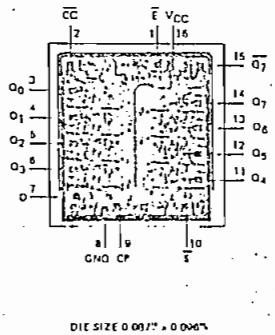


Metallization and Pad Layout

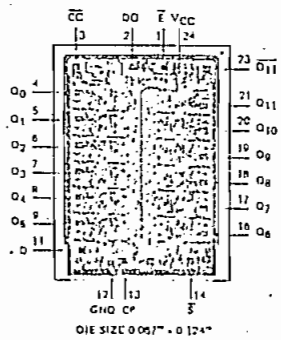
Am2502



Am2503



Am2504



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Voltage Comparators/Buffers

LM311 voltage comparator

general description

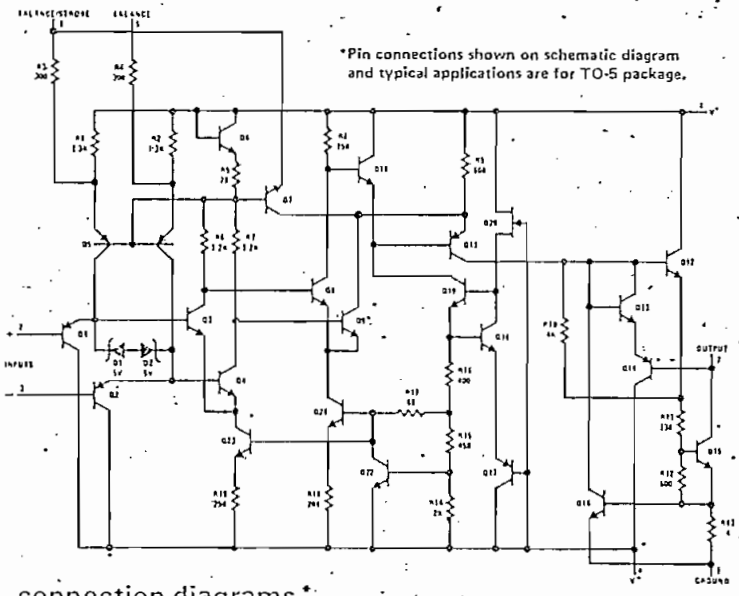
The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

features

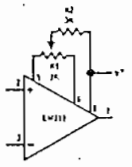
- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C.

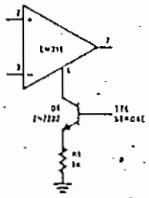
schematic diagram and auxiliary circuits



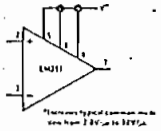
*Pin connections shown on schematic diagram and typical applications are for TO-5 package.



Offset Balancing



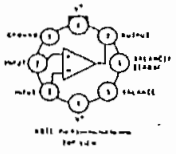
Strobing



Increasing Input Stage Current*

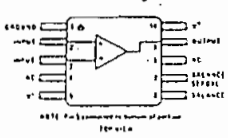
connection diagrams

Metal Can



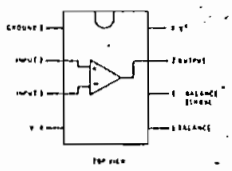
Order Number LM311H
See Package 11

Flat Package



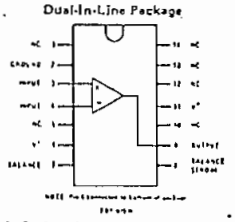
Order Number LM311F
See Package 3

Dual-In-Line Package



Order Number LM311N
See Package 20

Dual-In-Line Package



Order Number LM311D
See Package 1 or
Order Number LM311N-14
See Package 22

absolute maximum ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50K$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50K$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$, $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

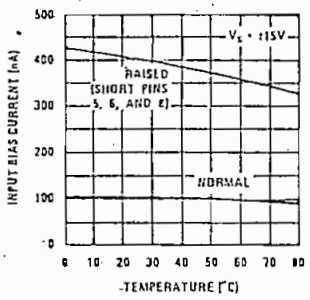
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C < T_A < 70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

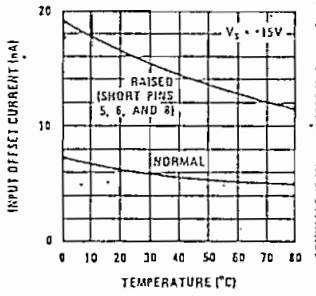
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

typical performance characteristics

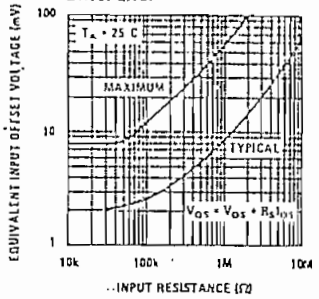
Input Bias Current



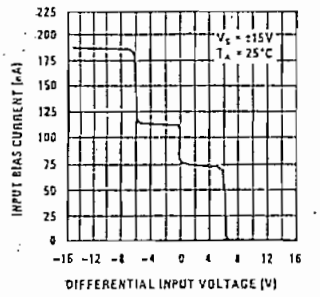
Input Offset Current



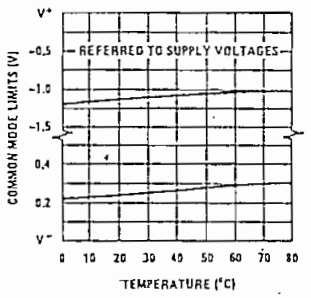
Offset Error



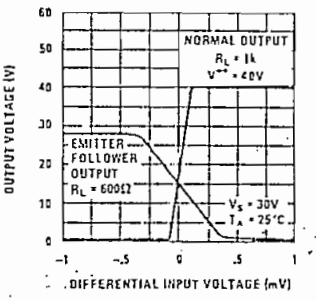
Input Characteristics



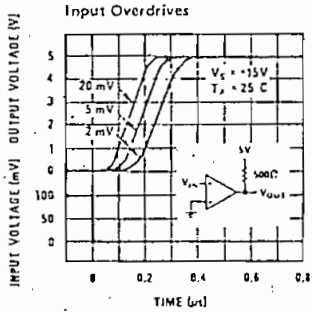
Common Mode Limits



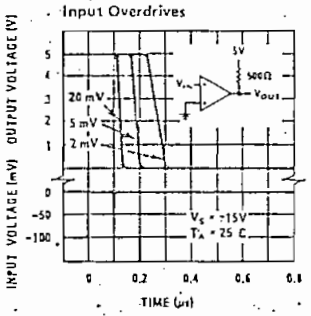
Transfer Function



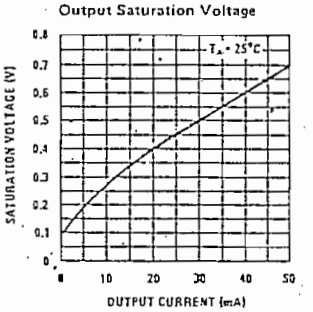
Response Time for Various Input Overdrives



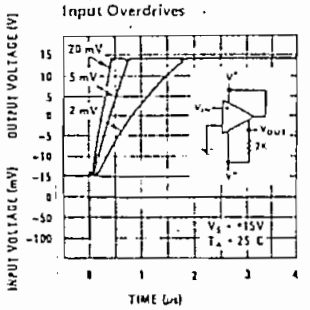
Response Time for Various Input Overdrives



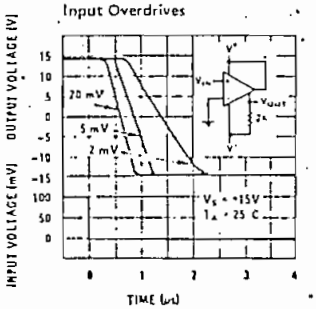
Output Saturation Voltage



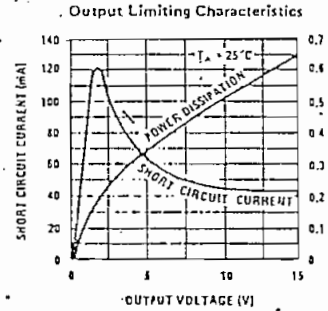
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

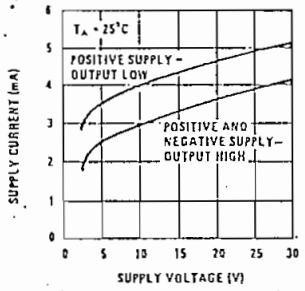


Output Limiting Characteristics

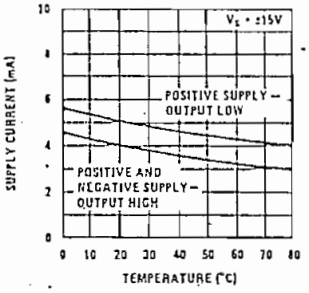


typical performance characteristics (con't)

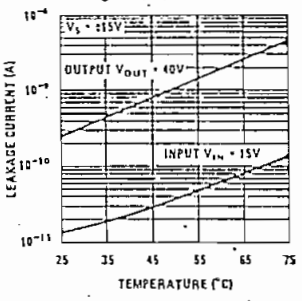
Supply Current



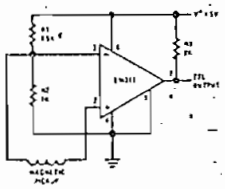
Supply Current



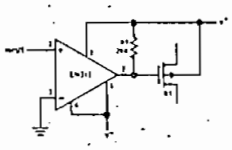
Leakage Currents



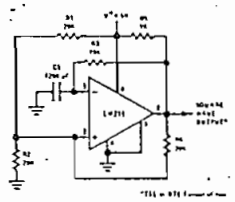
typical applications



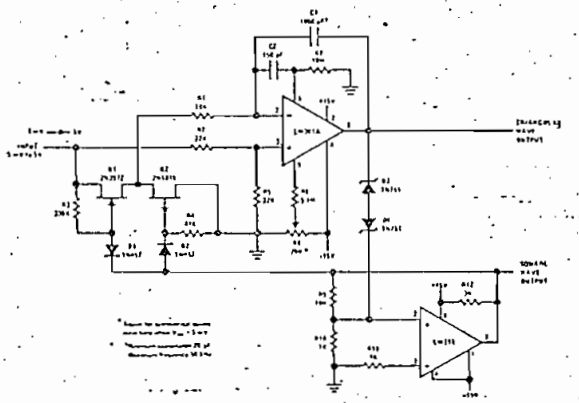
Detector for Magnetic Transducer



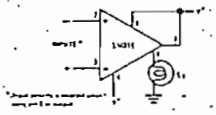
Zero Crossing Detector Driving MOS Switch



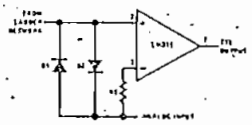
100 kHz Free Running Multivibrator



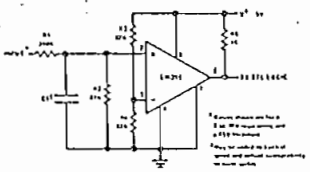
10 Hz to 10 kHz Voltage Controlled Oscillator



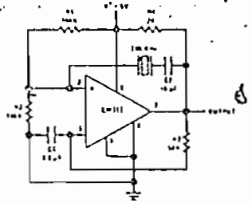
Driving Ground-Referred Load



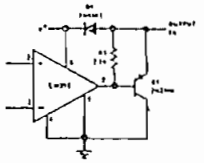
Using Clamp Diodes to Improve Response



TTL Interface with High Level Logic

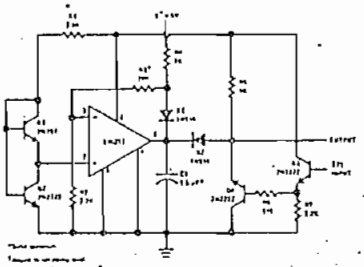


Crystal Oscillator

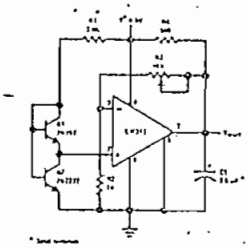


Comparator and Solenoid Driver

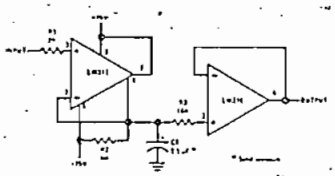
typical applications (con't)



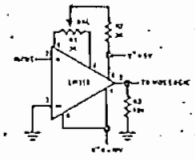
Precision Squarer



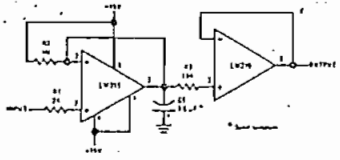
Low Voltage Adjustable Reference Supply



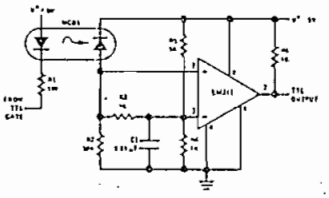
Positive Peak Detector



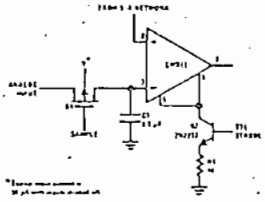
Zero Crossing Detector driving MOS logic



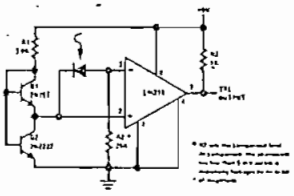
Negative Peak Dectector



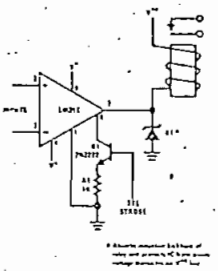
Digital Transmission Isolator



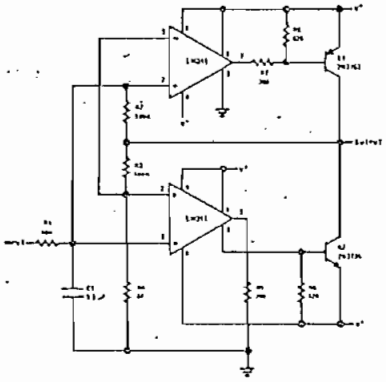
Strobing off Both Input* and Output Stages



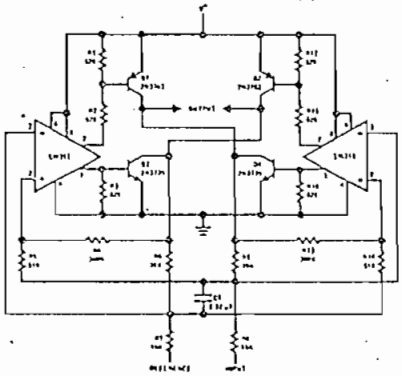
Precision Photodiode Comparator



Relay Driver with Strobe



Switching Power Amplifier



Switching Power Amplifier

SIGNETICS

512 AND 1024 BIT RECIRCULATING DYNAMIC SHIFT REGISTERS

2524
2525

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

FEATURES

- HIGH FREQUENCY OPERATION–5 MHz Typical Clock Rate
- SINGLE 512, SINGLE 1024
- TTL, DTL COMPATIBLE
- WRITE AND READ CONTROLS INCLUDED
- LOW POWER DISSIPATION–150μW/bit at 1 MHz
- LOW CLOCK CAPACITANCE–80pF for 512, 160pF for 1024 Bits
- +5, –5 POWER SUPPLIES
- STANDARD PACKAGE 8-LEAD DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

FAST ACCESS SWAPPING MEMORY SYSTEMS
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST BUFFER MEMORIES
CRT REFRESH MEMORIES
DELAY LINE MEMORY REPLACEMENT
DRUM MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold *silicon gate technology* allows high speed (5MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

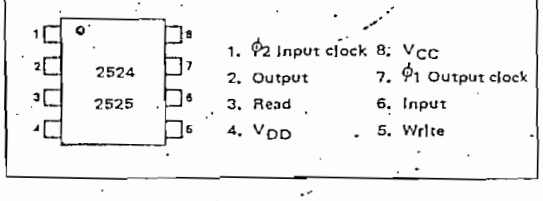
The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

SILICONE PACKAGING

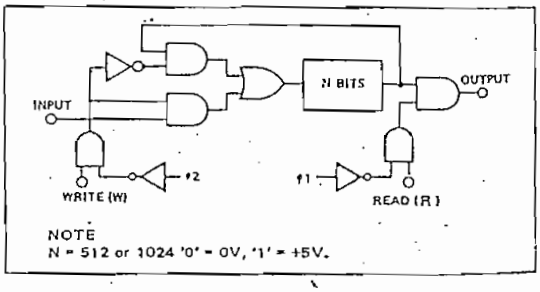
Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal-gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PIN CONFIGURATION (Top View)

V PACKAGE



BLOCK DIAGRAM



NOTE
N = 512 or 1024 '0' = 0V, '1' = +5V.

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read Mode Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2524V	512	8 pin DIP
2525V	1024	8 pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (2)	535mW@T_A>70°C
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to −20V

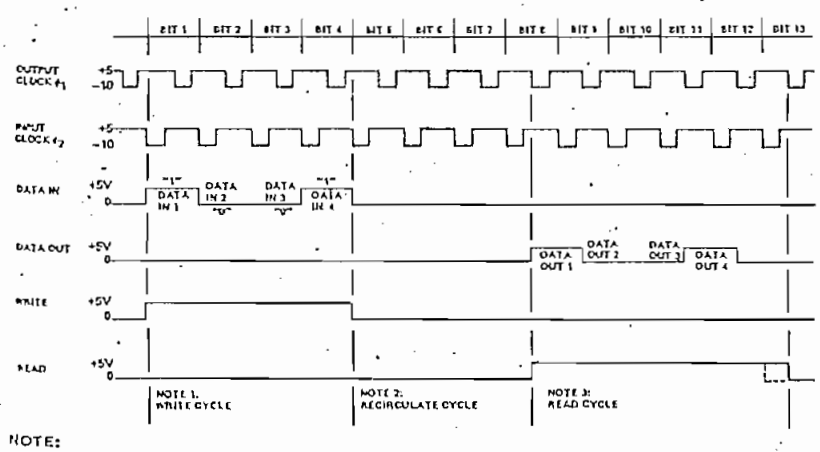
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rep. rate.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Parameters are valid over operating temperature range unless otherwise specified.
9. V_{CC} tolerance is ± 5%. Any variation is actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(9); V_{DD} = 5V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYPICAL	MAX	UNIT	CONDITION
I_{LI}	Input Load Current		10	500	nA	V_{IN} =-5.5V; T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	$V_{\phi1}$ = $V_{\phi2}$ = −12V; V_{DD} = −5 V_{OUT} =-5.5V; T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	V_{ILC} = -12V ; T_A = 25°C
I_{DD}	Power Supply Current: 2524		15	35	mA	Continuous Operation; ϕpW = 150nS; 1MHz
	2525		25	35	mA	V_{ILC} = −12V; T_A = 25°C V_{DD} = −5.5V
V_{IL}	Input "Low" Voltage	−5.0		1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	−12.0		−10.0	V	
V_{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

TIMING DIAGRAM



NOTE:
This is a simplified illustration of the timing of a 4 bit recirculating shift register showing the 3 basic modes of operation.

NOTE 1: (WRITE cycle)

The positive and negative going edge of the "Write" control is coincident with the negative going edge of the input clock (ϕ_2). The "Read" control may be either "1" or "0"

NOTE 2: (RECIRCULATE cycle)

Data recirculates if the "Write" control line is "0", "Read" may be either "1" or "0".

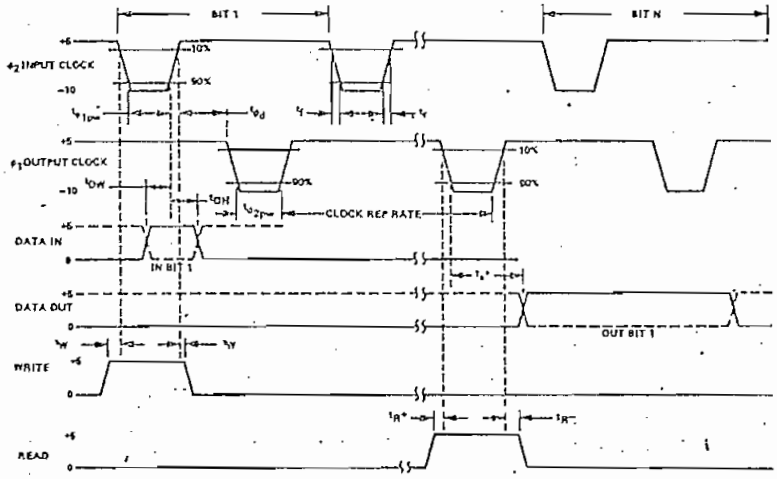
NOTE 3: (READ cycle)

The positive going edge of the "Read" control is coincident with the negative edge of the output clock (ϕ_1). The negative going edge of "Read" is coincident with the negative going edge of either clock pulse succeeding the last desired data output bit. "Write" may be either "1" or "0"

CONDITIONS OF TEST

Input rise and fall times: 10 sec Output load is 1 TTL gate

TIMING DIAGRAM



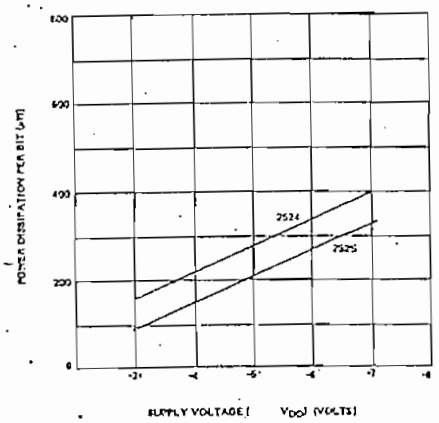
NOTE:
1. N = 512 for 2524 N= 1024 for 2525
2. Note that the Read Input is AND'ed with $\overline{\phi_1}$; therefore this function is not valid until ϕ_1 occurs.

AC CHARACTERISTICS $T_A = +25°C$ $V_{CC} = +5V(9)$; $V_{DD} = -5V \pm 5\%$; $V_{ILC} = -11V$

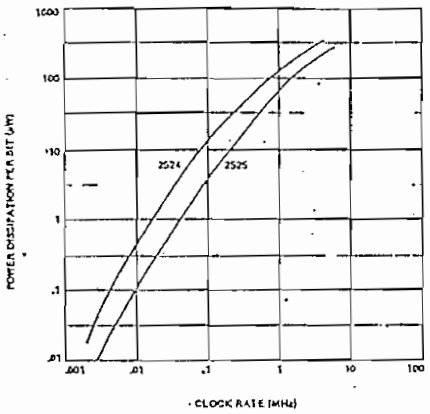
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	5	3	MHz	W = R = V_{CC}
$t_{\phi pw}$	Clock Pulse Width	135	85		ns	
$t_{\phi d}$	Clock Pulse Delay	10			ns	
t_r;t_f	Clock Pulse Transition	10		1000	ns	
t_{DW}	Data Write (Setup) Time	70			ns	
t_{DH}	Data to Clock Hold Time	20			ns	
t_{a+}	Clock to Data Out Delay			100	ns	
t_{R-}; t_{W-}	Clock to "Read" or "Write" Timing	0			ns	
t_{R-}; t_{W+}	Clock to "Read" or "Write" Timing	0			ns	
C_{in}	Input Capacitance			5	pF	1MHz; V_I=V_{CC};V_{AC}=25m V_{P-P}
C_{out}	Output Capacitance			5	pF	1MHz; V_0=V_{CC};V_{AC}=25m V_{P-P}
C_ϕ	Clock Capacitance 2524 2525			 80 160	 pF pF	1MHz; V=V_{CC}; V_{AC}=25m V_{P-P}
V_{OL}	Output "Low" Voltage		-1.0		V	R_L=3.0K; 1 TTL Load (I_L = 1.6mA) Note 10
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	R_L=3.0K; 1 TTL Load (I_L=100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	R_L = 5.6K; C_L = 10pF

CHARACTERISTIC CURVES

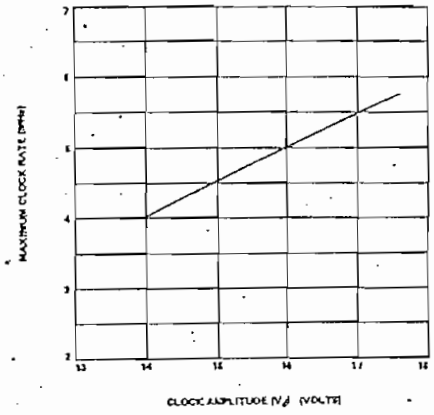
POWER DISSIPATION/BIT
VERSUS SUPPLY VOLTAGE



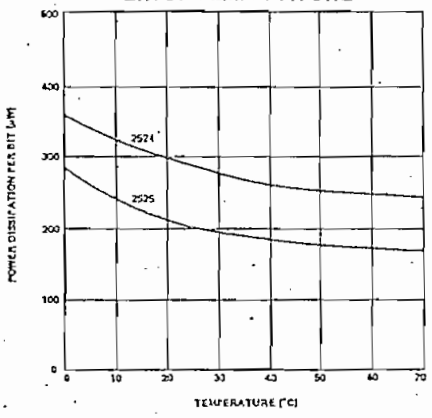
POWER DISSIPATION/BIT
VERSUS CLOCK RATE



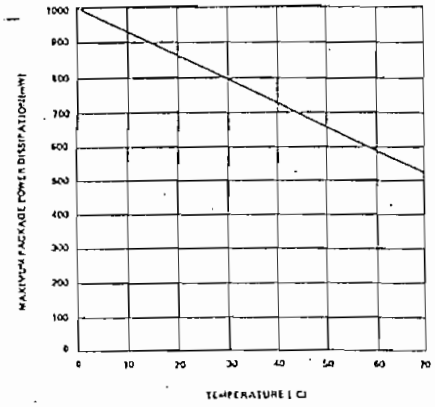
MAXIMUM CLOCK RATE
VERSUS CLOCK AMPLITUDE



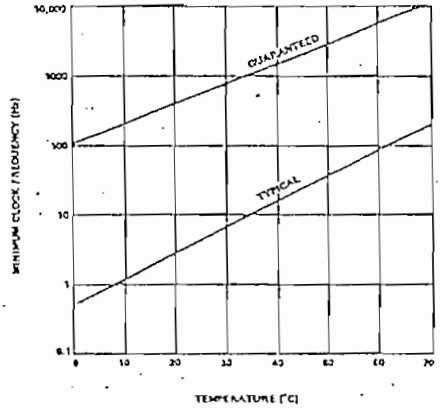
POWER DISSIPATION/BIT
VERSUS TEMPERATURE



MAXIMUM PACKAGE POWER
DISSIPATION VERSUS TEMPERATURE



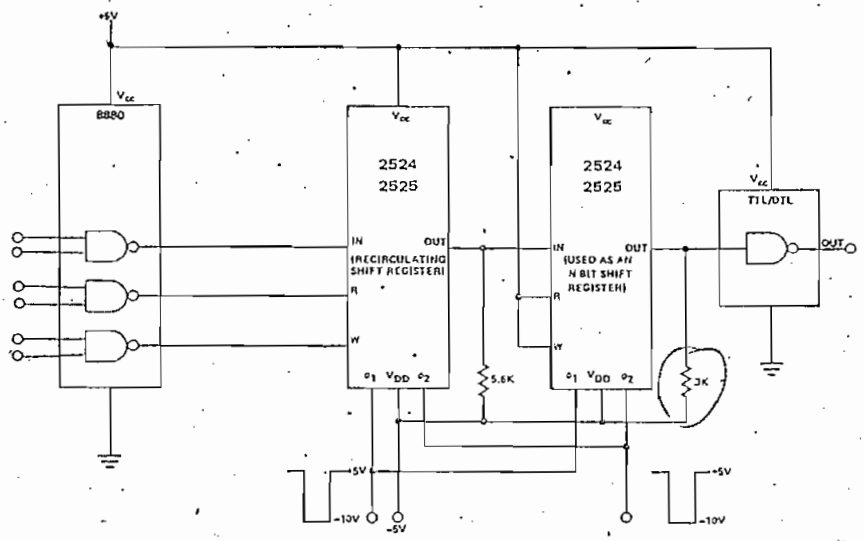
MINIMUM OPERATING CLOCK
FREQUENCY VERSUS TEMPERATURE



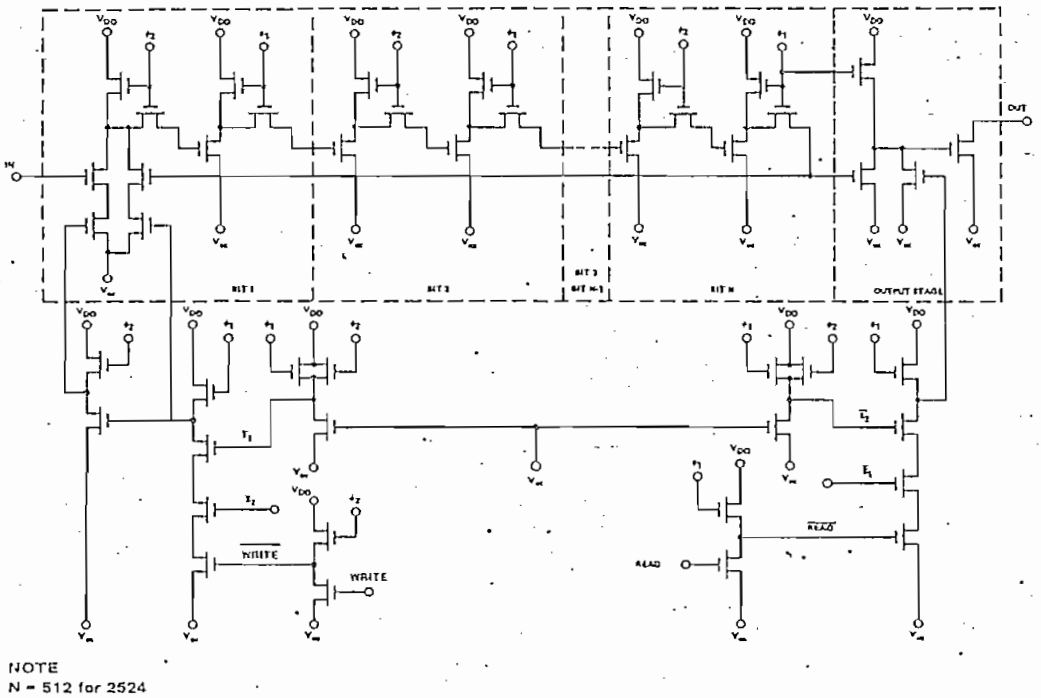
NOTE:
Conditions for typical curves: V_{CC} = +5V, V_{OD} = -5V, clock duty cycle = 35%, f_{CLK} = 3MHz, $V_{\phi p\text{-}p}$ = 16V, $\phi_{PW1} = \phi_{PW2}$ = 80ns, T_A = +25°C unless otherwise noted.

APPLICATIONS DATA

TTL/DTL/MOS INTERFACES



CIRCUIT SCHEMATIC



NOTE
N = 512 for 2524
N = 1024 for 2525

MOTOROLA
Semiconductors

MMH0026
MMH0026C

Specifications and Applications Information

DUAL MOS CLOCK DRIVER

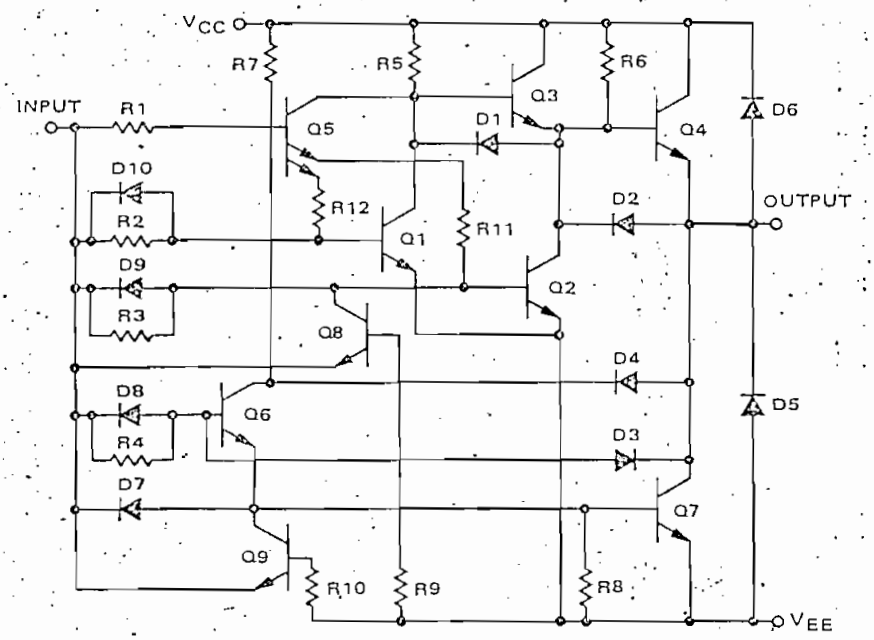
DUAL MOS
CLOCK DRIVER

MONOLITHIC
SILICON INTEGRATED CIRCUIT

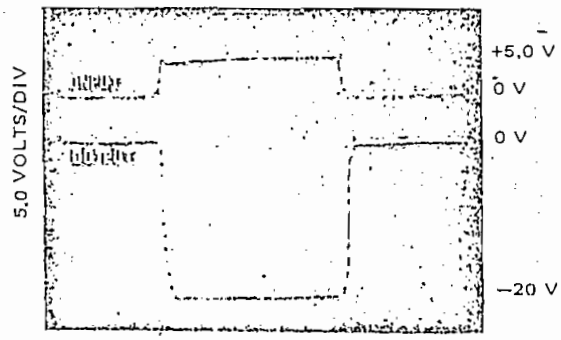
. . . designed for high-speed driving of highly capacitive loads in a MOS system.

- Fast Transition Times — 20 ns with 1000 pF Load
- High Output Swing — 20 Volts
- High Output Current Drive — ±1.5 Amperes
- High Repetition Rate — 5.0 to 10 MHz Depending on Load
- MTTL and MDTL Compatible Inputs
- Low Power Consumption when in MOS "0" State — 2.0 mW
- +5.0-Volt Operation for N-Channel MOS Compatibility

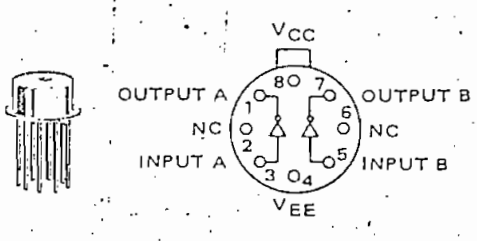
FIGURE 1 — CIRCUIT SCHEMATIC
(1/2 CIRCUIT SHOWN)



TYPICAL OPERATION
(R_S = 10 Ω, $C_L = C_{in}$ = 1000 pF, f = 1.0 MHz,
PW = 500 ns, V_{CC} = 0 V, V_{EE} = −20 V)

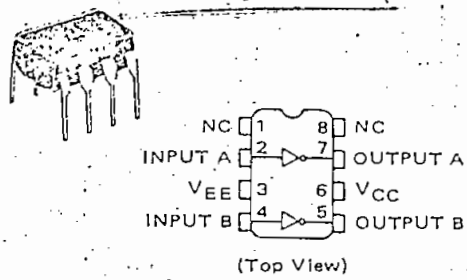


G SUFFIX
METAL PACKAGE
CASE 601-02
TO-99



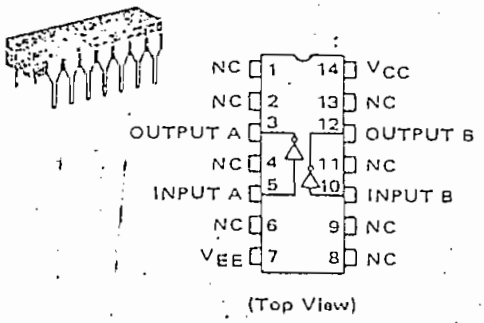
(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MMH0026C Only)



(Top View)

L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116



(Top View)

MDTL and MTTL are trademarks of Motorola Inc.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
Differential Supply Voltage	V_{CC}-V_{EE}	+22			Vdc
Input Current	I_{in}	+100			mA
Input Voltage	V_{in}	V_{EE} + 5.5			Vdc
Peak Output Current	I_{Opk}	±1.5			A
		G Pkg.	L Pkg.	Pl Pkg.	
Power Dissipation and Thermal Characteristics					
T_A = +25°C	P_D	680	1000	830	mW
Thermal Resistance, Junction to Air	θ_{JA}	220	150	150	°C/W
T_C = 25°C	P_D	2.1	3.0	1.8	W
Thermal Resistance, Junction to Case	θ_{JC}	70	50	70	°C/W
Junction Temperature	T_J	+175	+175	+150	°C
Operating Temperature Range	T_A				°C
MMH0026		−55 to +125	−55 to +125	—	
MMH0026C		0 to +85	0 to +85	0 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC}-V_{EE} = 10 V to 20 V, C_L = 1000 pF, T_A = −55 to +125°C for MMH0026 and 0 to +85°C for MMH0026C for min and max values; T_A = +25°C for all typical values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Logic "1" Level Input Voltage V_O = V_{EE} + 1.0 Vdc	V_{IH}	V_{EE} + 2.5	V_{EE} + 1.5	—	Vdc
Logic "1" Level Input Current V_{in}−V_{EE} = 2.5 Vdc, V_O = V_{EE} + 1.0 Vdc	I_{IH}	—	10	15	mA
Logic "0" Level Input Voltage V_O = V_{CC} −1.0 Vdc	V_{IL}	—	V_{EE} + 0.6	V_{EE} + 0.4	Vdc
Logic "0" Level Input Current V_{in}−V_{EE} = 0 Vdc, V_O = V_{CC} −1.0 Vdc	I_{IL}	—	−0.005	−10	μA
Logic "0" Level Output Voltage	V_{OH}				Vdc
V_{CC} = +5.0 Vdc, V_{EE} = −12 Vdc, V_{in} = −11.6 Vdc		4.0	4.3	—	
V_{in}−V_{EE} = 0.4 Vdc		V_{CC} −1.0	V_{CC} −0.7	—	
Logic "1" Level Output Voltage	V_{OL}				Vdc
V_{CC} = +5.0 Vdc, V_{EE} = −12 Vdc, V_{in} = −9.5 Vdc		—	−11.5	−11	
V_{in}−V_{EE} = 2.5 Vdc		—	V_{EE} + 0.5	V_{EE} + 1.0	
"On" Supply Current V_{CC}−V_{EE} = 20 Vdc, V_{in}−V_{EE} = 2.5 Vdc	I_{CCL}	—	30	40	mA
"Off" Supply Current V_{CC}−V_{EE} = 20 Vdc, V_{in}−V_{EE} = 0 V	I_{CCH}	—	10	100	μA

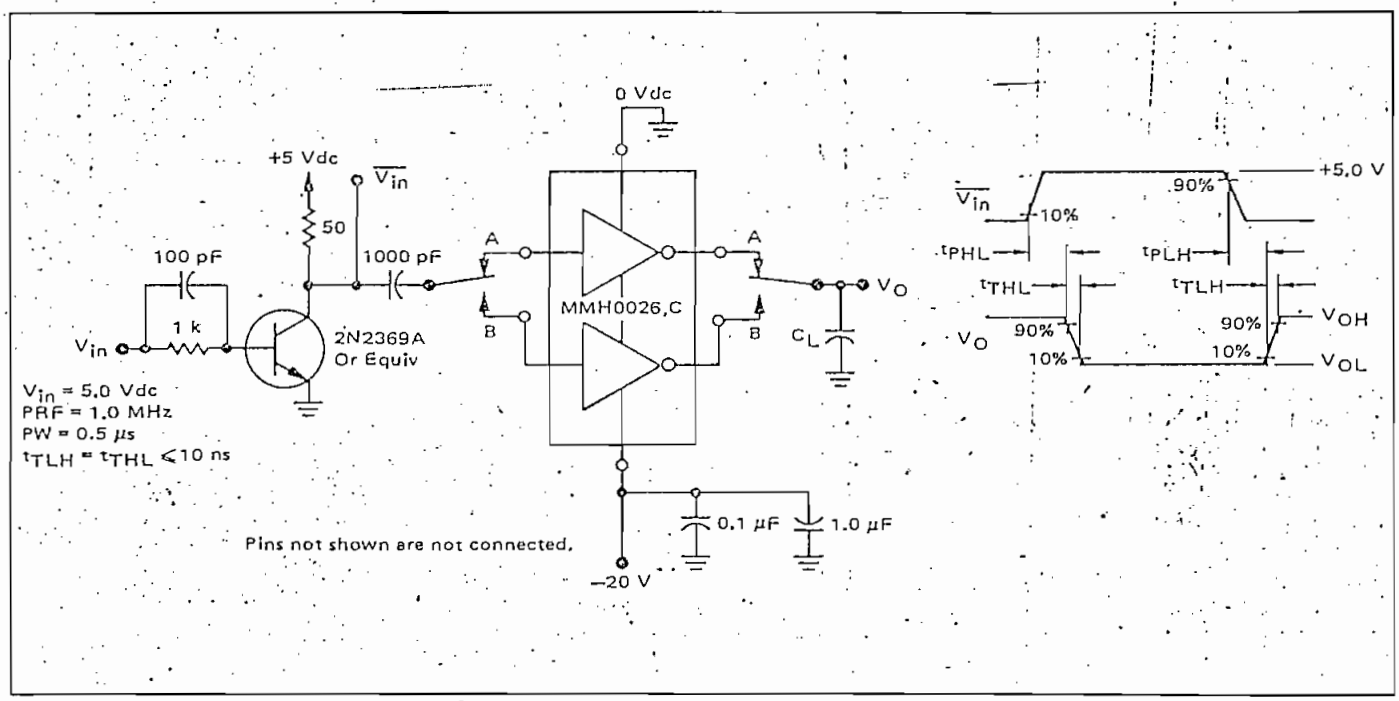
SWITCHING CHARACTERISTICS (See Figure 2.) (V_{CC}-V_{EE} = 10 V to 20 V, C_L = 1000 pF, T_A = −55 to +125°C for MMH0026 and 0 to +85°C for MMH0026C for min and max values; T_A = +25°C for all typical values unless otherwise noted.)

Propagation Time					
High to Low	t_{PHL}	5.0	7.5	12	ns
Low to High	t_{PLH}	5.0	12	15	
Transition Time (High to Low)	t_{THL}				ns
V_{CC}−V_{EE} = 17 Vdc, C_L = 250 pF		—	12	—	
V_{CC}−V_{EE} = 17 Vdc, C_L = 500 pF		—	15	18	
V_{CC}−V_{EE} = 20 Vdc, C_L = 1000 pF		—	20	35	
Transition Time (Low to High)	t_{TLH}				ns
V_{CC}−V_{EE} = 17 Vdc, C_L = 250 pF		—	10	—	
V_{CC}−V_{EE} = 17 Vdc, C_L = 500 pF		—	12	16	
V_{CC}−V_{EE} = 20 Vdc, C_L = 1000 pF		—	17	25	

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

TEST CIRCUIT

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL APPLICATIONS

FIGURE 3 – AC-COUPLED MOS CLOCK DRIVER

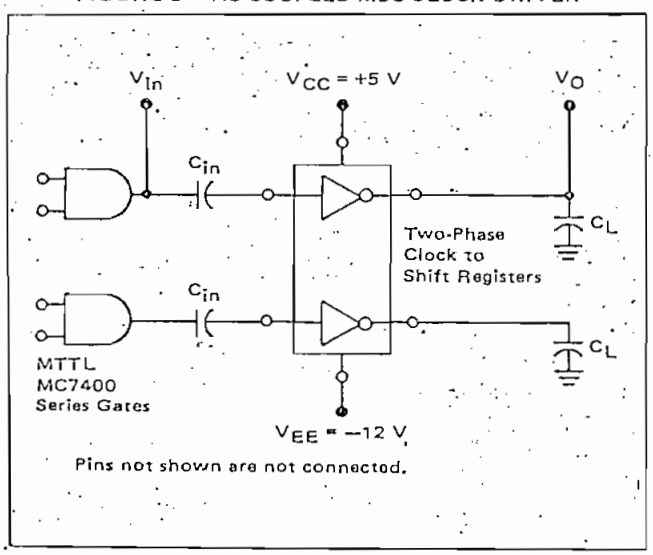
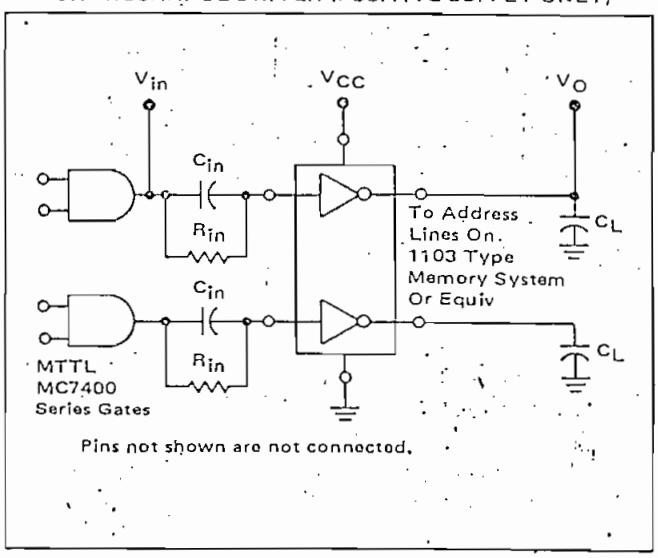


FIGURE 4 – DC-COUPLED RAM MEMORY ADDRESS OR PRECHARGE DRIVER (POSITIVE-SUPPLY ONLY)



TYPICAL CHARACTERISTICS

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 — INPUT CURRENT versus INPUT VOLTAGE

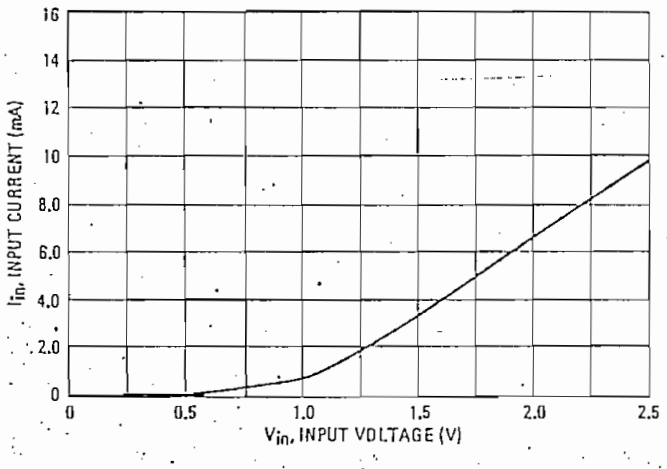


FIGURE 6 — SUPPLY CURRENT versus TEMPERATURE

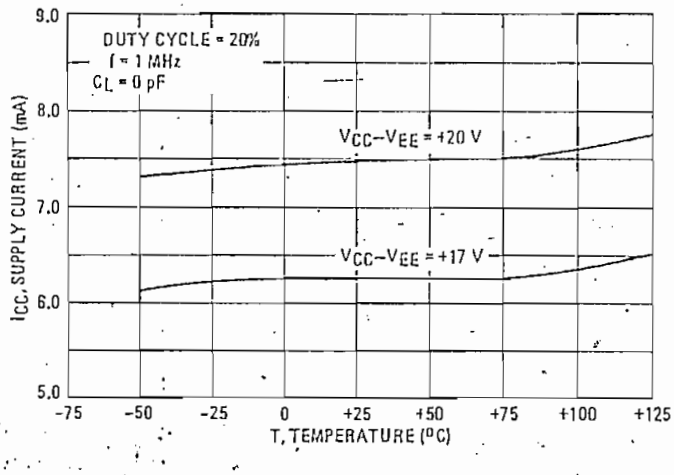


FIGURE 7 — OPTIMUM INPUT CAPACITANCE versus OUTPUT PULSE WIDTH

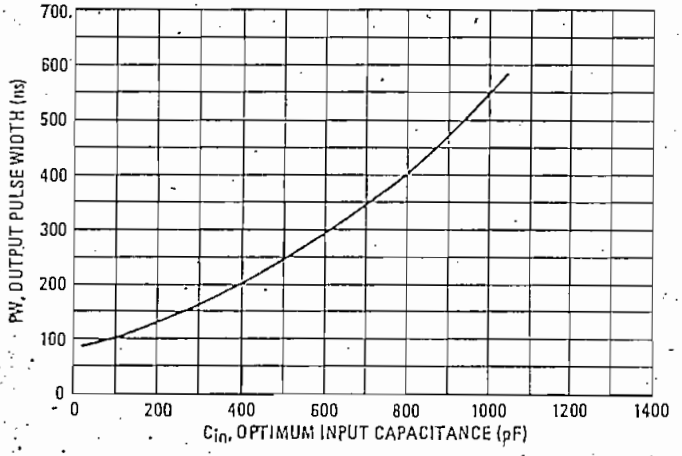


FIGURE 8 — TRANSITION TIMES versus LOAD CAPACITANCE

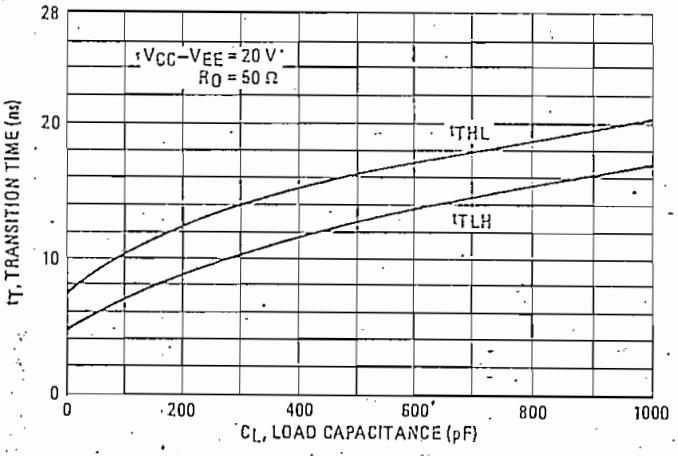


FIGURE 9 — PROPAGATION DELAY TIMES versus TEMPERATURE

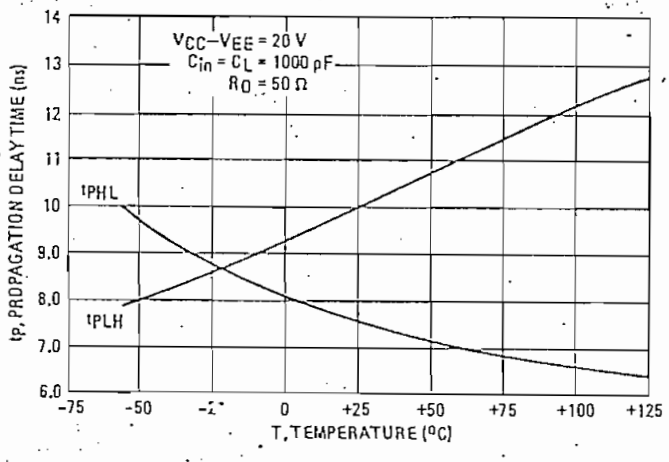
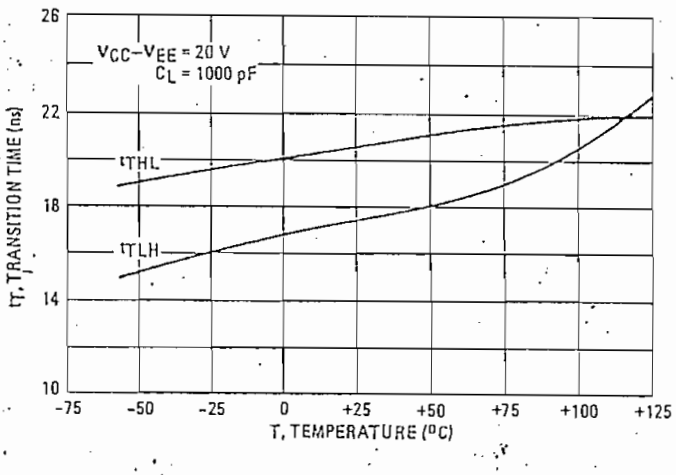


FIGURE 10 — TRANSITION TIMES versus TEMPERATURE



TYPICAL CHARACTISTICS (continued)

(V_{CC} = +20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 — TRANSITION TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

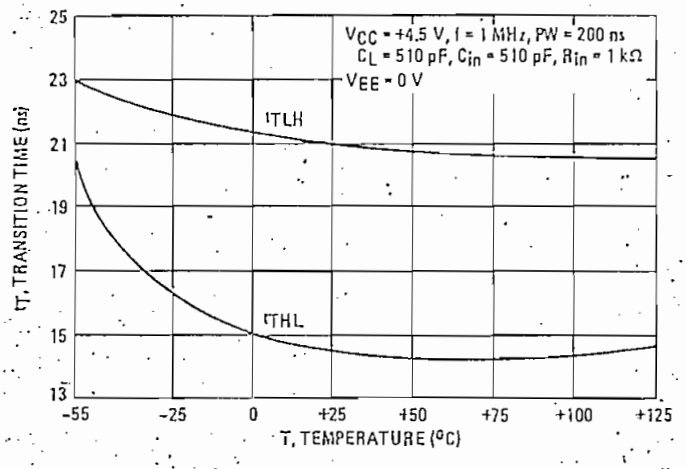


FIGURE 12 — PROPAGATION DELAY TIME versus TEMPERATURE FOR +5 VOLT DC COUPLED OPERATION (See Figure 4.)

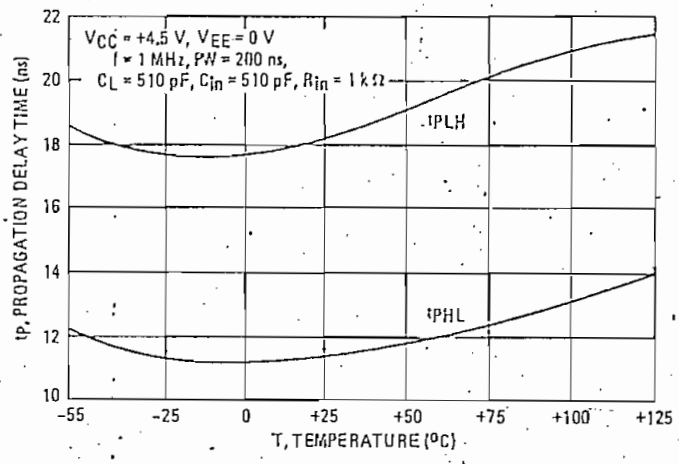


FIGURE 13 — DC-COUPLED SWITCHING RESPONSE versus R_{in} (See Figure 4.)

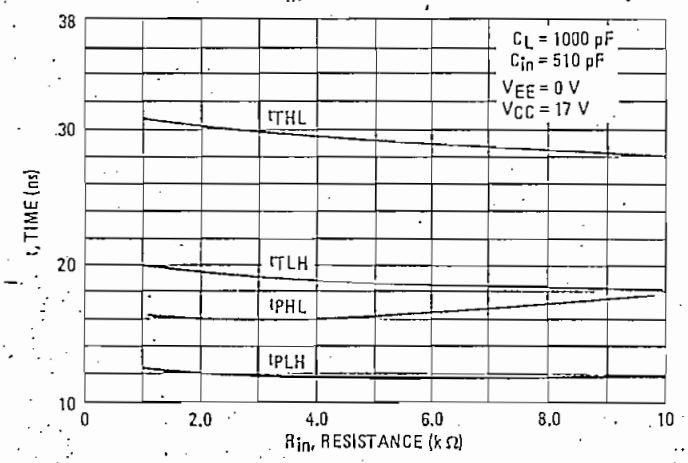


FIGURE 14 — DC-COUPLED SWITCHING versus C_{in} (See Figure 4.)

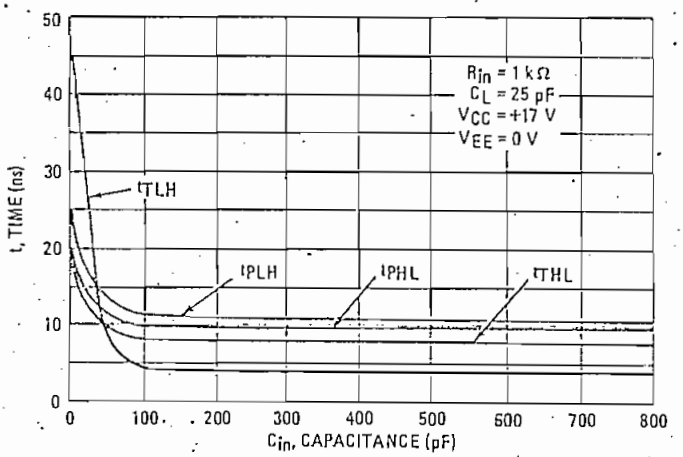


FIGURE 15 — MAXIMUM DC POWER DISSIPATION versus DUTY CYCLE (SINGLE DRIVER)

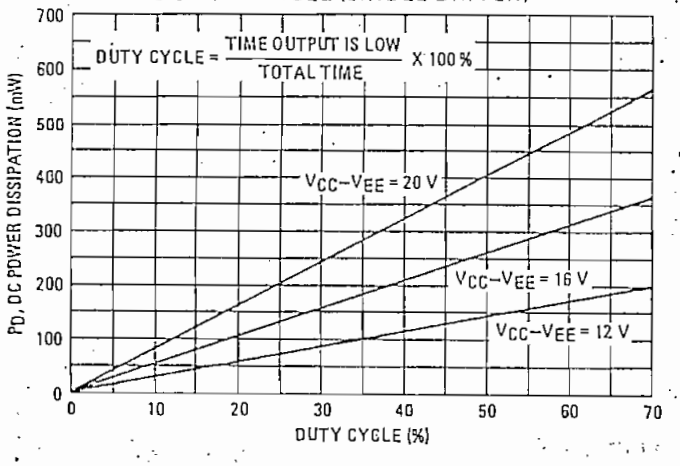
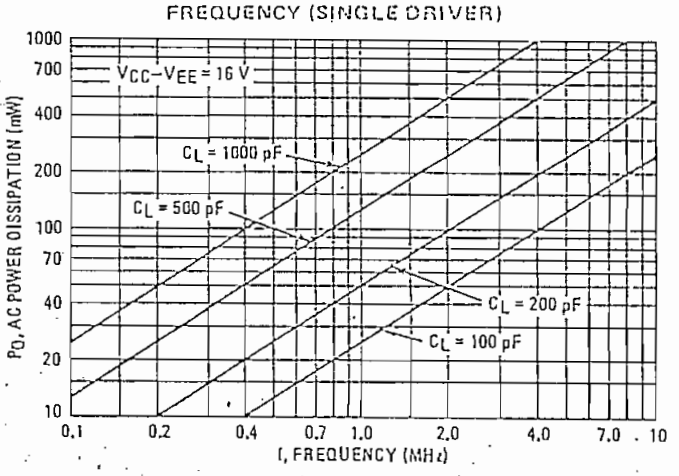


FIGURE 16 — AC POWER DISSIPATION versus FREQUENCY (SINGLE DRIVER)



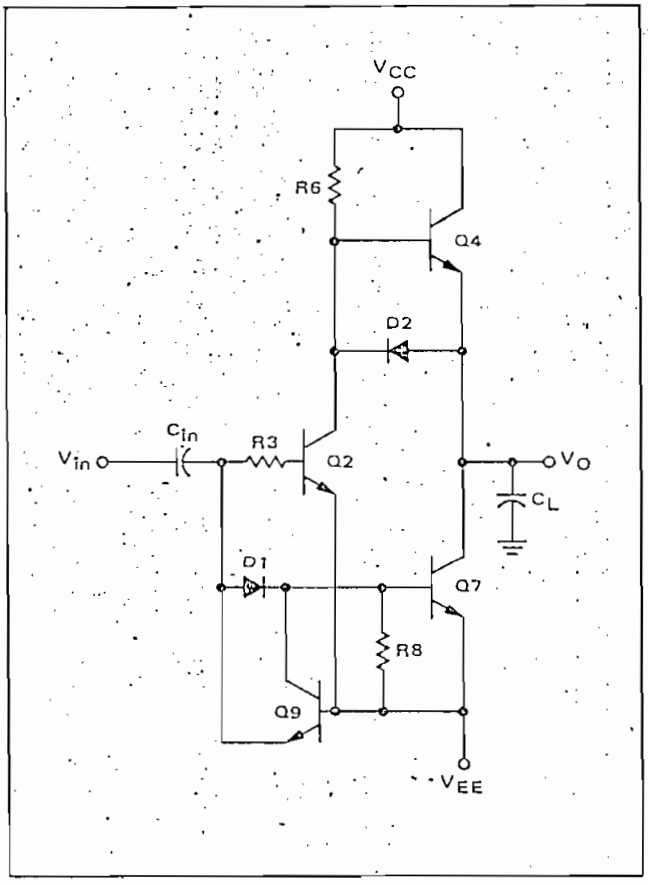
APPLICATIONS INFORMATION

OPERATION OF THE MMH0026

The simplified schematic diagram of MMH0026, shown in Figure 17, is useful in explaining the operation of the device. Figure 17 illustrates that as the input voltage level goes high, diode D1 provides an 0.7-volt "dead zone" thus ensuring that Q2 is turned "on" and Q4 is turned "off" before Q7 is turned "on". This prevents undesirable "current spiking" from the power supply, which would occur if Q7 and Q4 were allowed to be "on" simultaneously for an instant of time. Diode D2 prevents "zenering" of Q4 and provides an initial discharge path for the output capacitive load by way of Q2.

As the input voltage level goes low, the stored charge in Q2 is used advantageously to keep Q2 "on" and Q4 "off" until Q7 is "off". Again undesirable "current spiking" is prevented. Due to the external capacitor, the input side of C_{in} goes negative with respect to V_{EE} causing Q9 to conduct momentarily thus assuring rapid turn "off" of Q7.

FIGURE 17 — SIMPLIFIED SCHEMATIC DIAGRAM
(Ref.: Figure 1)



The complete circuit, Figure 1; basically creates Darlington devices of transistors Q7, Q4 and Q2 in the simplified circuit of Figure 17. Note in Figure 1 that when the input goes negative with respect to V_{EE}, diodes D7 through D10 turn "on" assuring faster turn "off" of transistors Q1, Q2, Q6 and Q7. Resistor R6 insures that the output will charge to within one V_{BE} voltage drop of the V_{CC} supply.

SYSTEM CONSIDERATIONS

Overshoot:

In most system applications the output waveform of the MMH0026 will "overshoot" to some degree. However, "overshoot" can be eliminated or reduced by placing a damping resistor in series with the output. The amount of resistance required is given by: $R_S = 2\sqrt{L/C_L}$ where L is the inductance of the line and C_L is the load capacitance. In most cases a series of damping resistor in the range of 10-to-50 ohms will be sufficient. The damping resistor also affects the transition times of the outputs. The speed reduction is given by the formula:

$t_{THL} \approx t_{TLH} = 2.2\ R_S\ C_L$ (R_S is the damping resistor).

Crosstalk:

The MMH0026 is sensitive to crosstalk when the output voltage level is high ($V_O \approx V_{CC}$). With the output in the high voltage level state, Q3 and Q4 are essentially turned "off". Therefore, negative-going crosstalk will pull the output down until Q4 turns "on" sufficiently to pull the output back towards V_{CC}. This problem can be minimized by placing a "bleeding" resistor from the output to ground. The "bleeding" resistor should be of sufficient size so that Q4 conducts only a few milliamperes. Thus, when noise is coupled, Q4 is already "on" and the line is quickly clamped by Q4. Also note that in Figure 1 D6 clamps the output one diode-voltage drop above V_{CC} for positive-going crosstalk.

Power Supply Decoupling:

The decoupling of V_{CC} and V_{EE} is essential in most systems. Sufficient capacitive decoupling is required to supply the peak surge currents during switching. At least a 0.1-μF to 1.0-μF low inductive capacitor should be placed as close to each driver package as the layout will permit.

Input Driving:

For those applications requiring split power supplies ($V_{EE} < GND$), ac coupling, as illustrated in Figure 3, should be employed. Selection of the input capacitor size is determined by the desired output pulse width. Maximum performance is attained when the voltage at

the input of the MMH0026 discharges to just above the device's threshold voltage (about 1.5 V). Figure 7 shows optimum values for C_{in} versus the desired output pulse width. The value for C_{in} may be roughly predicted by:

$$C_{in} = (2 \times 10^{-3})\ (PW_O). \qquad (1)$$

For an output pulse width of 500 ns, the optimum value for C_{in} is:

$$C_{in} = (2 \times 10^{-3})\ (500 \times 10^{-9}) = 1000\ pF.$$

If single supply operation is required (V_{EE} = GND), then dc coupling as illustrated in Figure 4 can be employed. For maximum switching performance, a speed-up capacitor should be employed with dc coupling. Figures 13 and 14 show typical switching characteristics for various values of input resistance and capacitance.

POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\ (\theta_{JC} + \theta_{CA}) \qquad (2)$$

or

$$T_J = T_A + P_D\ (\theta_{JA}) \qquad (3)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
θ_{JC} = thermal resistance, junction to case
θ_{CA} = thermal resistance, case to ambient
θ_{JA} = thermal resistance, junction to ambient.

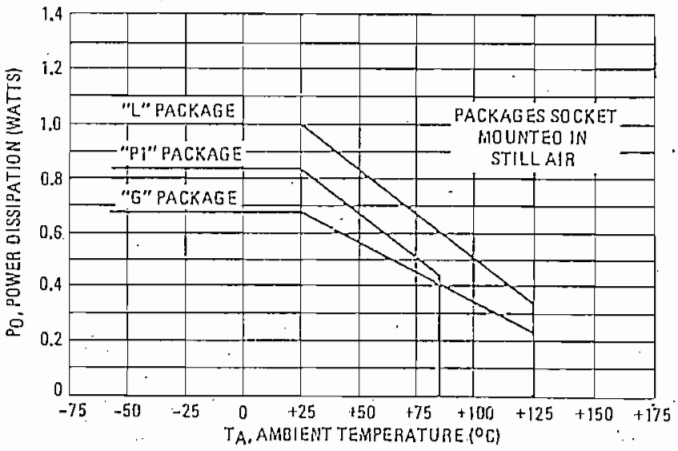
Power Dissipation for the MMH0026 MOS Clock Driver:

The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. This power dissipation, when substituted into equation (3), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for three integrated circuit packages in the maximum ratings section of this data sheet.

TABLE 1 — THERMAL CHARACTERISTICS OF "G", "L" AND "P1" PACKAGES

PACKAGE TYPE (Mounted in Socket)	θ_{JA} (°C/W) Still Air		θ_{JC} (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"G" (Metal Package)	220	175	70	40
"L" (Ceramic Package)	150	100	50	27
"P1" (Plastic Package)	150	100	70	40

FIGURE 18 — MAXIMUM POWER DISSIPATION versus AMBIENT TEMPERATURE (As related to package)



With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (2) or (3) and the maximum thermal resistance values given in Table 1 or alternately, by using the curves plotted in Figure 18. If, however, the power dissipation determined by a given system produces a calculated junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the θ_{CA} term can be reduced. Lowering the θ_{CA} term can be accomplished by increasing the surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

APPLICATIONS INFORMATION (continued)

The following examples illustrate the thermal considerations necessary to increase the power capability of the MMH0026.

Assume that the ceramic package is to be used at a maximum ambient temperature (T_A) of +70°C. From Table 1: θ_{JA}(max) = 150°C/watt, and from the maximum rating section of the data sheet: T_J(max) = +175°C. Substituting the above values into equation (3) yields a maximum allowable power dissipation of 0.7 watts. Note that this same value may be read from Figure 18. Also note that this power dissipation value is for the device mounted in a socket.

Next, the maximum power consumed for a given system application must be determined. The power dissipation of the MOS clock driver is conveniently divided into dc and ac components. The dc power dissipation is given by:

$$P_{dc} = (V_{CC} - V_{EE}) \times (I_{CCL}) \times (\text{Duty Cycle}) \qquad (4)$$

$$\text{where } I_{CCL} = 40\text{ mA } (\frac{V_{CC} - V_{EE}}{20\text{ V}}).$$

Note that Figure 15 is a plot of equation (4) for three values of (V_{CC}–V_{EE}). For this example, suppose that the MOS clock driver is to be operated with V_{CC} = +16 V and V_{EE} = GND and with a 50% duty cycle. From equation (4) or Figure 15, the dc power dissipation (per driver) may be found to be 256 mW. If both drivers within the package are used in an identical way, the total dc power is 512 mW. Since the maximum total allowable power dissipation is 700 mW, the maximum ac power that can be dissipated for this example becomes:

$$P_{ac} = 0.7 - 0.512 = 188\text{ mW}$$

The ac power for each driver is given by:

$$P_{ac} = (V_{CC} - V_{EE})^2 \times f \times C_L \qquad (5)$$

where f = frequency of operation

C_L = load capacitance (including all strays and wiring).

Figure 16 gives the maximum ac power dissipation versus switching frequency for various capacitive loads with V_{CC} = 16 V and V_{EE} = GND. Under the above conditions, and with the aid of Figure 16, the safe operating area beneath Curve A of Figure 19 can be generated.

Since both drivers have a maximum ac power dissipation of 188 mW, the maximum ac power per driver becomes 94 mW. A horizontal line intersecting all the capacitance load lines at the 94 mW level of Figure 16 will yield the maximum frequency of operation for each of the capacitive loads at the specified power level. By using the previous formulas and constants, a new safe operating area can be generated for any output voltage swing and duty cycle desired.

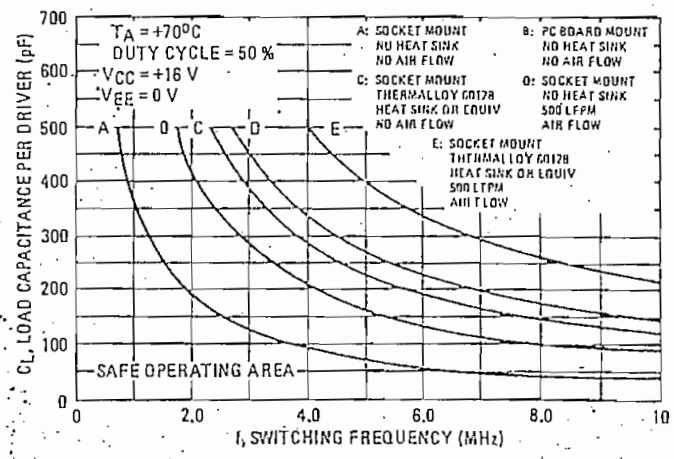
Note from Figure 19, that with highly capacitive loads, the maximum switching frequency is very low. The switching frequency can be increased by varying the following factors:

(a) decrease T_A
(b) decrease the duty cycle
(c) lower package thermal resistance θ_{JA}.

In most cases conditions (a) and (b) are fixed due to system requirements. This leaves only the thermal resistance θ_{JA} that can be varied.

Note from equation (2) that the thermal resistance is comprised of two parts. One is the junction-to-case thermal resistance (θ_{JC}) and the other is the case-to-ambient thermal resistance (θ_{CA}). Since the factor θ_{JC} is a function of the die size and type of bonding employed, it cannot be varied. However, the θ_{CA} term can be changed as previously discussed, see Page 7.

FIGURE 19 – LOAD CAPACITANCE versus FREQUENCY FOR "L" PACKAGE ONLY
(Both drivers used in identical way)



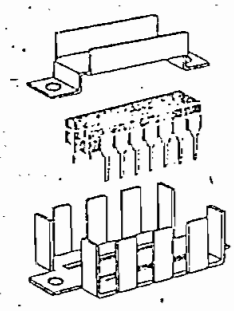
Heat Sink Considerations:

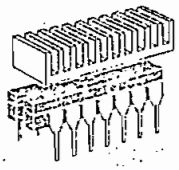
Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 20. In the previous example, with the ceramic package, no heat sink and in a still air environment, θ_{JA}(max) was 150°C/W.

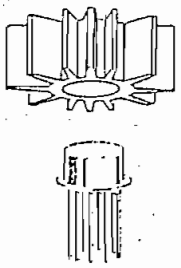
For the following example the Thermalloy 60128 type heat sink, or equivalent, is chosen. With this heat sink, the θ_{CA} for natural convection from Figure 21 is 44°C/W. From Table 1 θ_{JC}(max) = 50°C/W for the ceramic

APPLICATIONS INFORMATION (continued)

FIGURE 20 — THERMALLOY* HEAT SINKS


6007A


6012B


2230-5

*Manufactured by Thermalloy Co. of Texas.

package. Therefore, the new θ_{JA}(max) with the 6012B heat sink added becomes:

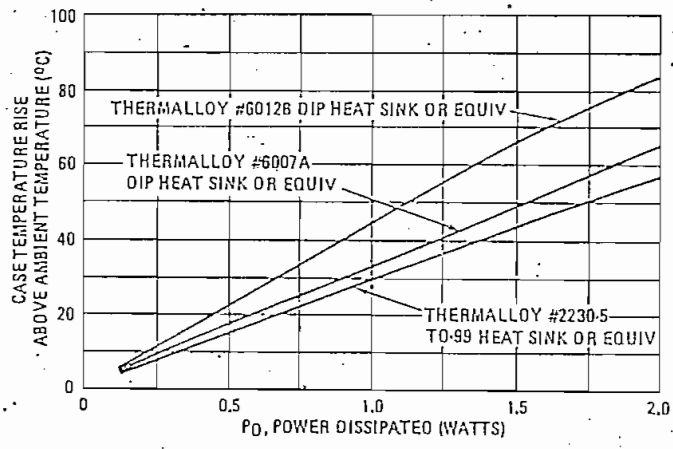
$$\theta_{JA}(max) = 50^{\circ}C/W + 44^{\circ}C/W = 94^{\circ}C/W.$$

Thus the addition of the heat sink has reduced θ_{JA}(max) from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (3) at T_A = +70°C is:

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{94^{\circ}C/W} = 1.11 \text{ watts.}$$

This gives approximately a 58% increase in maximum power dissipation. The safe operating area under Curve C of Figure 19 can now be generated as before with the aid of Figure 16 and equation (5).

FIGURE 21 — CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 22, forced air can be employed to reduce the θ_{JA} term. Note, however, that this curve is expressed in terms of typical θ_{JA} rather than maximum θ_{JA}. Maximum θ_{JA} can be determined in the following manner:

From Table 1 the following information is known:

(a) θ_{JA}(typ) = 100°C/W
(b) θ_{JC}(typ) = 27°C/W

Since:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (6)$$

Then:

$$\theta_{CA} = \theta_{JA} - \theta_{JC} \quad (7)$$

Therefore, in still air

$$\theta_{CA}(typ) = 100^{\circ}C/W - 27^{\circ}C/W = 73^{\circ}C/W$$

From Curve 1 of Figure 22 at 500 LFPM and equation (7),

$$\theta_{CA}(typ) = 53^{\circ}C/W - 27^{\circ}C/W = 26^{\circ}C/W.$$

Thus θ_{CA}(typ) has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical θ_{CA} by a ratio of 1:2.8. Since the typical value of θ_{CA} was reduced by a ratio of 1:2.8, θ_{CA}(max) of 100°C/W should also decrease by a ratio of 1:2.8.

This yields an θ_{CA}(max) at 500 LFPM of 36°C/W.

Therefore, from equation (6):

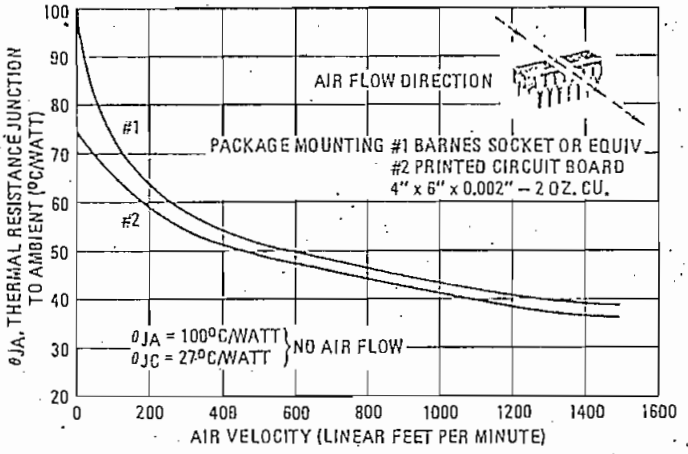
$$\theta_{JA}(max) = 50^{\circ}C/W + 36^{\circ}C/W = 86^{\circ}C/W.$$

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (3):

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{+86^{\circ}C/W} = 1.2 \text{ watts.}$$

APPLICATIONS INFORMATION (continued)

FIGURE 22 – TYPICAL THERMAL RESISTANCE (θ_{JA}) OF "L" PACKAGE versus AIR VELOCITY



As with the previous examples, the dc power at 50% duty cycle is subtracted from the maximum allowable device dissipation (P_D) to obtain a maximum P_{ac}. The safe operating area under Curve D of Figure 19 can now be generated from Figure 16 and equation (5).

Heat Sink and Forced Air Combined:

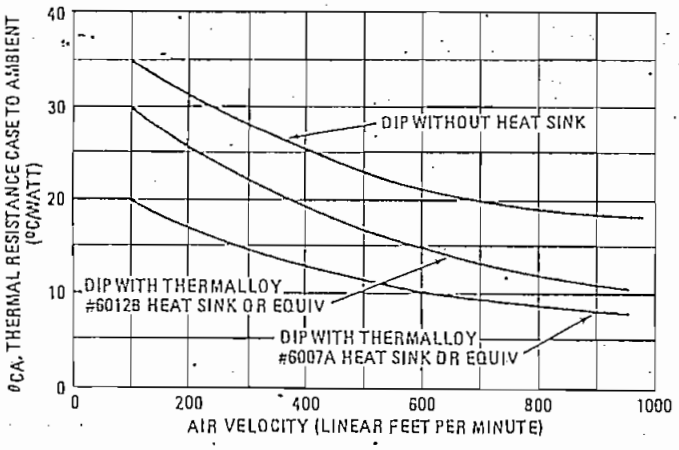
Some heat sink manufacturers provide data and curves of θ_{CA} for still air and forced air such as illustrated in Figure 23. For example the 6012B heat sink has an θ_{CA} = 17°C/W at 500 LFPM as noted in Figure 23. From equation (6):

$$\text{Max } \theta_{JA} = 50^{\circ}C/W + 17^{\circ}C/W = 67^{\circ}C/W$$

From equation (3) at T_A = +70°C

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{67^{\circ}C/W} = 1.57 \text{ watts.}$$

FIGURE 23 – THERMAL RESISTANCE θ_{CA} versus AIR VELOCITY



As before this yields a safe operating area under Curve E in Figure 19.

Note from Table 1 and Figure 22 that if the 14-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical θ_{JA} is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine a safe operating area for this condition.

Given data from Table 1:

$$\text{typical } \theta_{JA} = 100^{\circ}C/W$$
$$\text{typical } \theta_{JC} = 27^{\circ}C/W$$

From Curve 2 of Figure 22, θ_{JA}(typ) is 75°C/W for a PC mount and no air flow. Then the typical θ_{CA} is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of θ_{CA} for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical θ_{CA} by a ratio of 1:1.5 below the typical value of θ_{CA} in a socket mount. Therefore, the maximum value of socket mount θ_{CA} of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum θ_{CA} becomes:

$$\theta_{CA} = \frac{100^{\circ}C/W}{1.5} = 66^{\circ}C/W \text{ for PC board mount}$$

Therefore the maximum θ_{JA} for a PC mount is from equation (6).

$$\theta_{JA} = 50^{\circ}C/W + 66^{\circ}C/W = 116^{\circ}C/W.$$

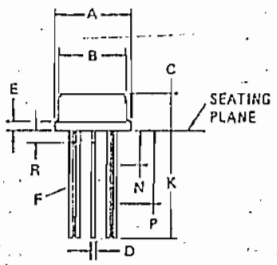
With maximum θ_{JA} known, the maximum power dissipation can be found and the safe operating area determined as before. See Curve B in Figure 19.

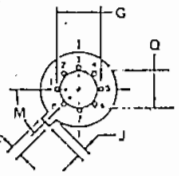
CONCLUSION

In most cases, heat sink manufacturer's publish only θ_{CA} socket mount data. Although θ_{CA} data for PC mounting is generally not available, this should present no problem. Note in Figure 22 that an air flow greater than 250 LFPM yields a socket mount θ_{JA} approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of θ_{CA} on the type environment and measurement techniques employed. For example, θ_{CA} would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

OUTLINE DIMENSIONS

G SUFFIX
CASE 601-02
TO-99
METAL PACKAGE



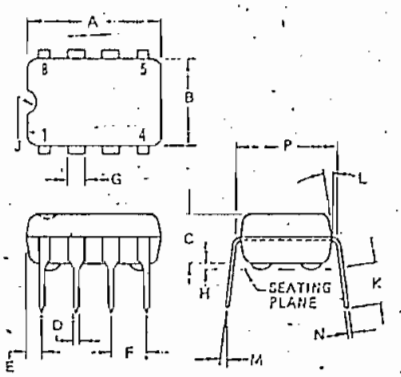


Weight≈0.920 gram

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.510	9.390	0.335	0.370
B	7.750	8.500	0.305	0.335
C	4.200	4.690	0.165	0.185
D	4.070	0.533	0.016	0.021
E	–	1.020	–	0.040
F	0.406	0.482	0.016	0.019
G	5.080 TP		0.200 TP	
H	0.712	0.864	0.028	0.034
J	0.737	1.140	0.029	0.045
K	12.700	–	0.500	–
M	45° TYP		45° TYP	
N	–	1.270	–	0.050
P	6.350	12.700	0.250	0.500
Q	3.560	4.060	0.140	0.160
R	0.254	1.010	0.010	0.040

All JEDEC dimensions and notes apply

P1 SUFFIX
CASE 626
PLASTIC PACKAGE

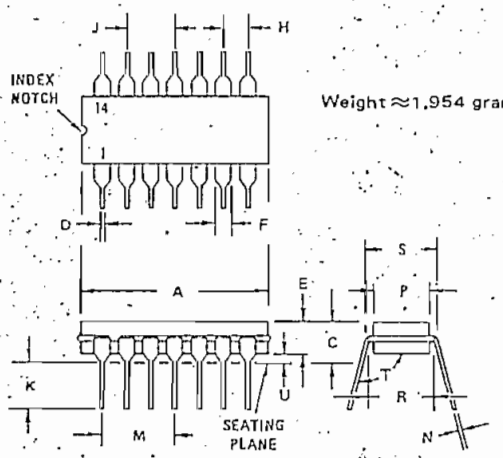


Weight≈0.446 gram

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.39	9.90	.370	.390
B	6.09	6.35	.240	.250
C	3.43	3.94	.135	.155
D	.381	.483	.015	.019
E	–	1.14	–	.045
F	2.54 TP		0.100 TP	
G	.762	1.52	.030	.060
H	.508 NOM		.020 NOM	
J	.762	1.078	.030	.040R
K	2.92	3.43	.115	.135
L	7° TYP		7° TYP	
M	0°	10°	0°	10°
N	.203	.279	.008	.011
P	7.37	7.87	.290	.310

NOTES:
1. DIMENSION "P" IS TO LEAD CENTERLINE WHEN FORMED PARALLEL.
2. FOUR (4) INSULATING STANDOFFS ARE PROVIDED.

L SUFFIX
CASE 632-02
TO-116
CERAMIC PACKAGE



Weight≈1.954 grams

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	17.400	19.000	0.660	0.780
C	–	5.080		0.200
D	0.381	0.584	0.015	0.023
F	0.770	1.770	0.030	0.070
H	2.290	2.790	0.090	0.110
J	4.830	5.330	0.190	0.210
K	2.540	–	0.100	–
M	7.370	7.870	0.290	0.310
N	0.203	0.381	0.008	0.015
P	5.590	7.110	0.220	0.280
R	7.370	7.870	0.290	0.310
S	–	8.260	–	0.325
T			90°	105°
U	0.508	0.762	0.020	0.030

NOTE:
1. "R" – Installed Position of Lead Centers.
2. "S" – Overall Installed Width.

All JEDEC TO-116 dimensions and notes apply.

MOTOROLA
Semiconductors

MC1508L-8
MC1408L-8
MC1408L-7
MC1408L-6

Specifications and Applications Information

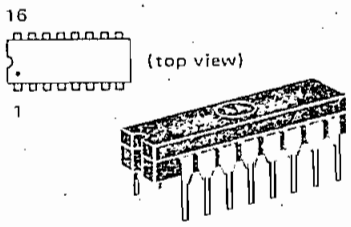
EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

- Relative Accuracy: ±0.19% Error maximum (MC1508L-8, MC1408L-8)
- Seven and Six-Bit Accuracy Available (MC1408L-7, MC1408L-6)
- Fast Settling Time — 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing — +0.5 V to -5.0 V
- High-Speed Multiplying Input Slew Rate 4.0 mA/μs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V



L SUFFIX
CERAMIC PACKAGE
CASE 620

FIGURE 1 — D-to-A TRANSFER CHARACTERISTICS

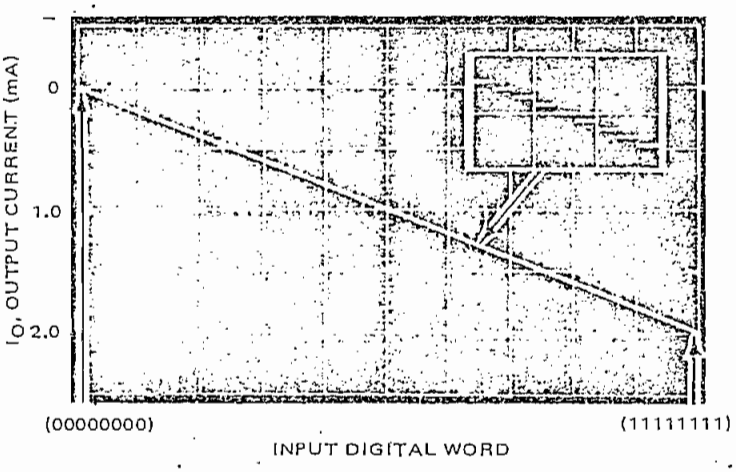
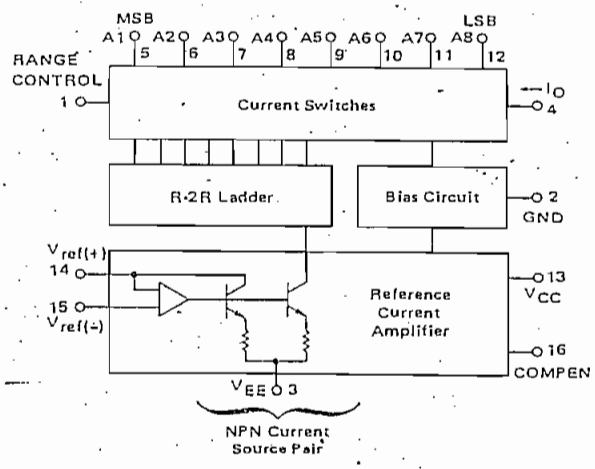


FIGURE 2 — BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

MTTL is a trademark of Motorola Inc.

DS 9238

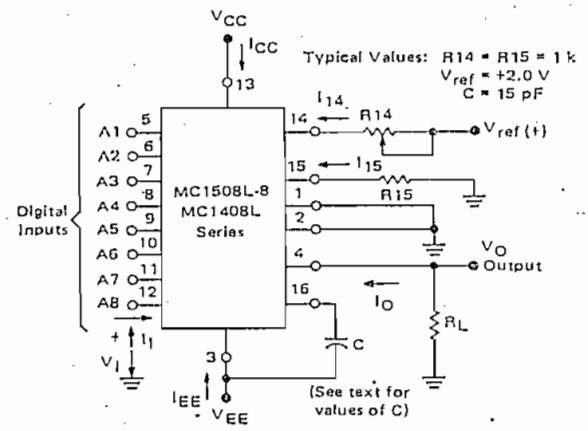
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	+5.5,0	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14},V_{15}	V_{CC},V_{EE}	Vdc
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range MC1508L8 MC1408L Series	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{Vref}{R14}$ = 2.0 mA, MC1508L-8: T_A = -55°C to +125°C. MC1408L Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) MC1508L8, MC1408L8 MC1408L7, See Note 1 MC1408L6, See Note 1	4	E_r	 — — —	 — — —	 ±0.19 ±0.39 ±0.78	%
Settling Time to within 1/2 LSB [includes t_{PLH}] (T_A=+25°C) See Note 2	5	t_S	—	300	—	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH},t_{PHL}	—	30	100	ns
Output Full Scale Current Drift		TCI_O	—	±20	—	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2.0 —	 — —	 — 0.8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3	 I_{IH} I_{IL}	 — —	 0 -0.4	 0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	—	-1.0	-3.0	μA
Output Current Range V_{EE} = -5.0 V V_{EE} = -6.0 to -15 V	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R14 = 1000 Ω	3	I_O	 1.9	 1.99	 2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	—	0	4.0	μA
Output Voltage Compliance ($E_r \leq 0.19\%$ at T_A = +25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 — —	 — —	 -0.6,+0.5 -5.0,+0.5	Vdc
Reference Current Slew Rate	6	SR I_{ref}	—	4.0	—	mA/μs
Output Current Power Supply Sensitivity		PSRR(—)	—	0.5	2.7	μA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	— —	+13.5 -7.5	+22 -13	mA
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR} V_{EER}	+4.5 -4.5	+5.0 -15	+5.5 -16.5	Vdc
Power Dissipation All bits low V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc	3	P_D	 — — — —	 105 190 90 160	 170 305 — —	mW

Note 1. All current switches are tested to guarantee at least 50% of rated output current.
Note 2. All bits switched.

FIGURE 3 — NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 4 — RELATIVE ACCURACY TEST CIRCUIT

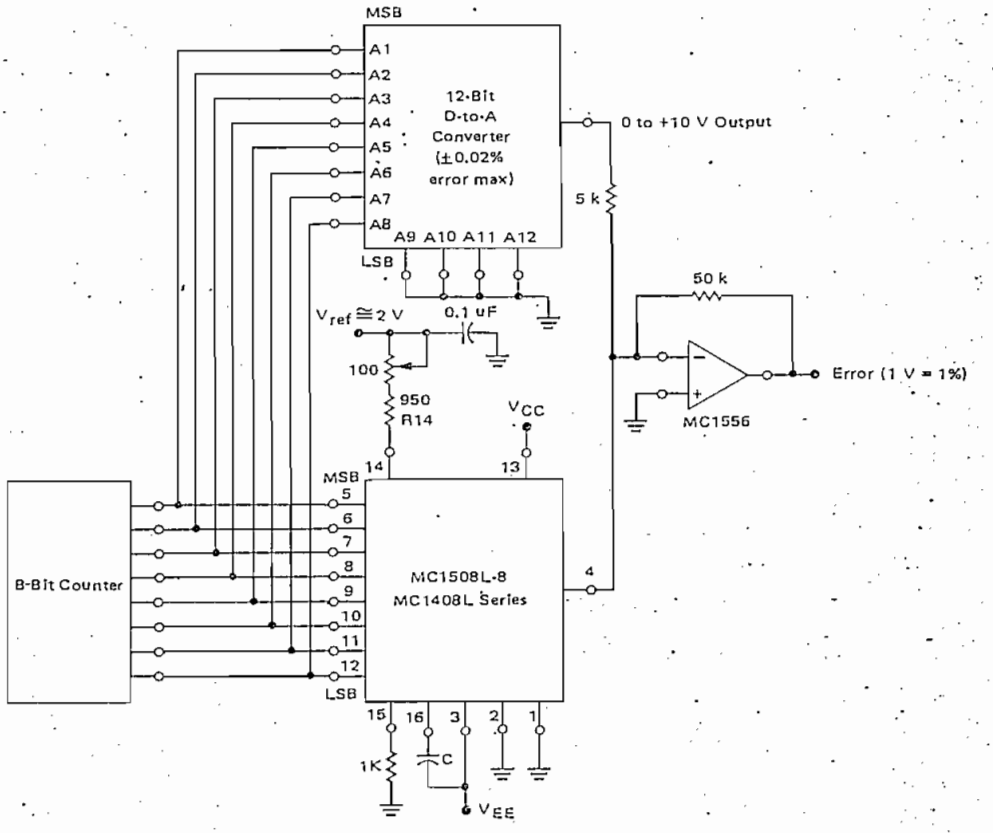
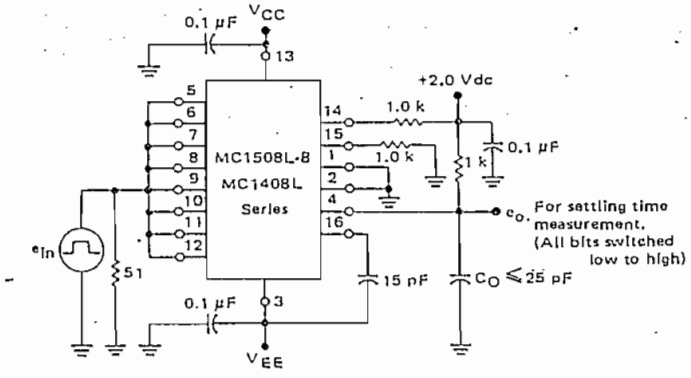
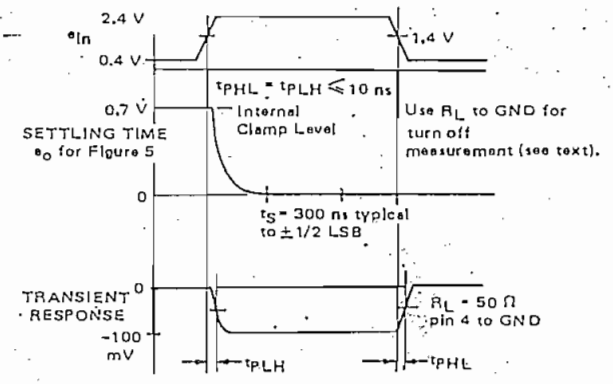


FIGURE 5 — TRANSIENT RESPONSE and SETTLING TIME





TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT

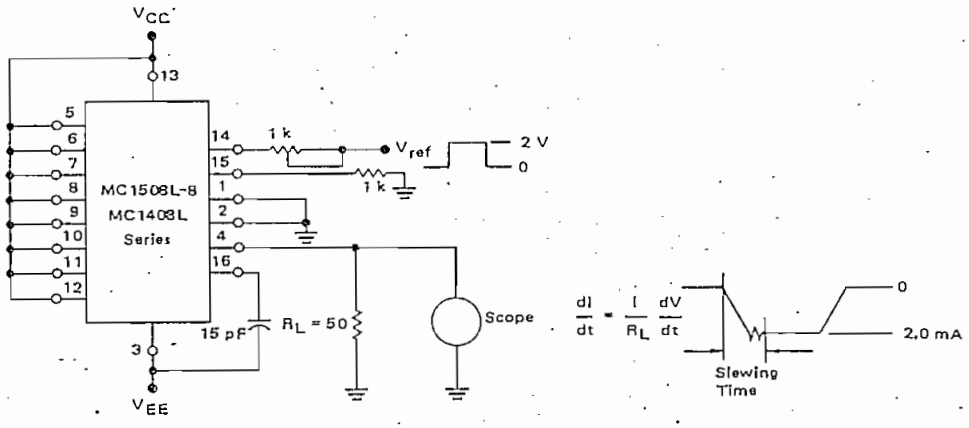


FIGURE 7 – POSITIVE V_{ref}

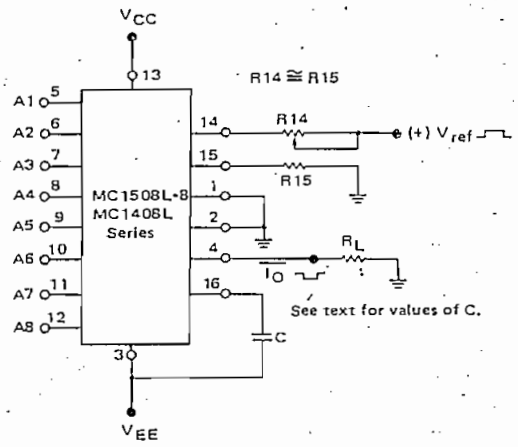
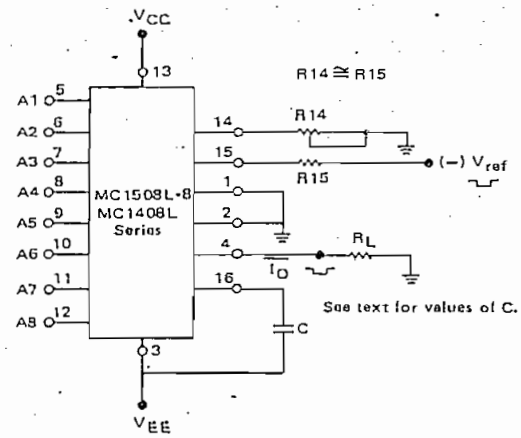
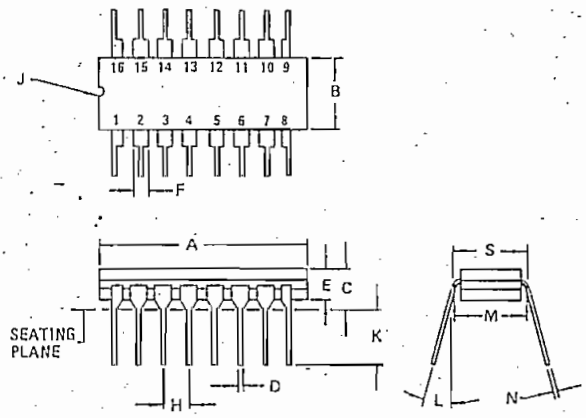


FIGURE 8 – NEGATIVE V_{ref}



OUTLINE DIMENSIONS



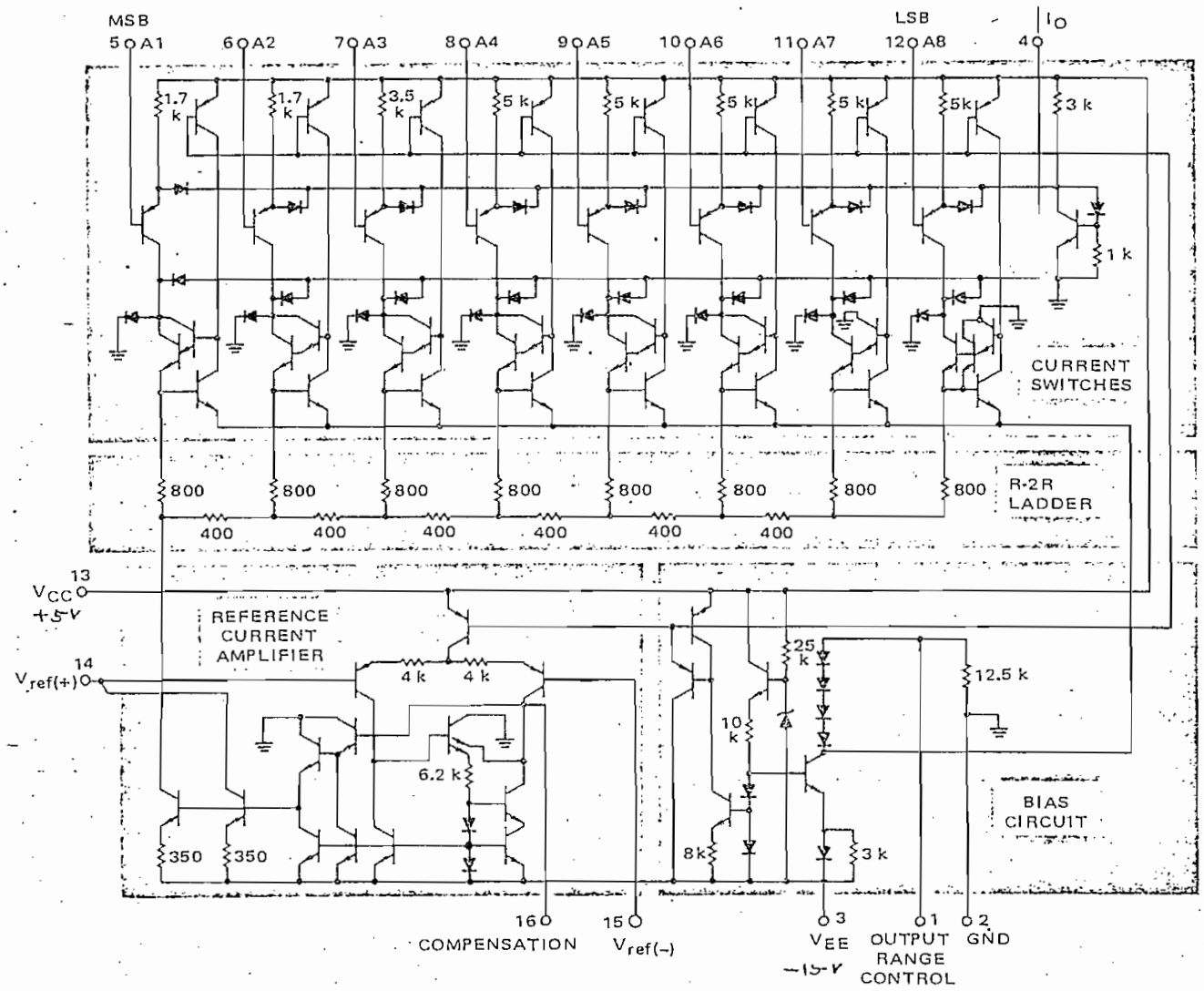
NOTES:
1. DIM. "M" IS MEASURED AT CENTER OF LEADS WHEN FORMED PARALLEL.
2. "J" INDEX:
   NOTCH IN LEAD, INK DOT, OR NOTCH IN CERAMIC.

Weight ≈ 1.197 grams

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.790	19.810	0.740	0.780
B	6.100	6.990	0.240	0.275
C	4.320	5.080	0.170	0.200
D	0.381	0.508	0.015	0.020
E	3.430	4.190	0.135	0.165
F	1.400	1.650	0.055	0.065
H	2.54 TP		0.100 TP	
J	0.381	0.889	0.015	0.035
K	2.930	3.430	0.115	0.135
L	0°	15°	0°	15°
M	7.620 TP		0.300 TP	
N	0.203	0.305	0.008	0.012
S	–	8.260	–	0.325

CASE 620
CERAMIC PACKAGE

FIGURE 9 — MC1508L-8/MC1408L SERIES EQUIVALENT CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1508L-8 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of −0.6 to +0.5 volts at +25°C, due to the current switching methods employed in the MC1508L-8. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded; so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1508L-8 may be extended to −5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than −10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between −5.0 V and −10 V is desired, a voltage of between 0 and −5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −6.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1508L-8 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1508L-8 has a very low full scale current drift with temperature.

The MC1508L-8/MC1408L Series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1508L-8 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1508L-8 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1508L-8.

Multiplying Accuracy

The MC1508L-8 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the 1.6 μA contributes an error of 0.1 LSB. This is well within eight-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1508L-8 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

GENERAL INFORMATION (Continued)

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leq 500$ ohms and $C_O \leq 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC-1508L-8. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 — LOGIC INPUT CURRENT versus INPUT VOLTAGE

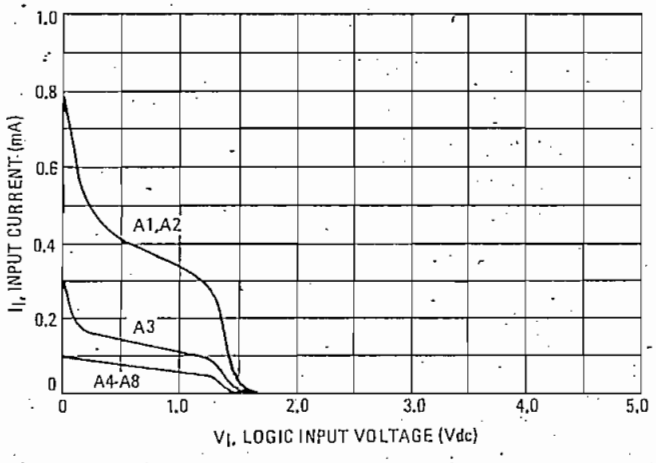


FIGURE 11 — TRANSFER CHARACTERISTIC versus TEMPERATURE
(A5 thru A8 thresholds lie within range for A1 thru A4)

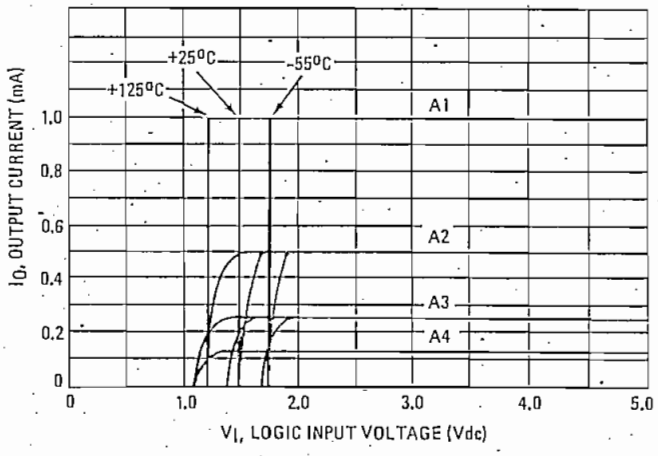


FIGURE 12 — OUTPUT CURRENT versus OUTPUT VOLTAGE
(See text for pin 1 restrictions)

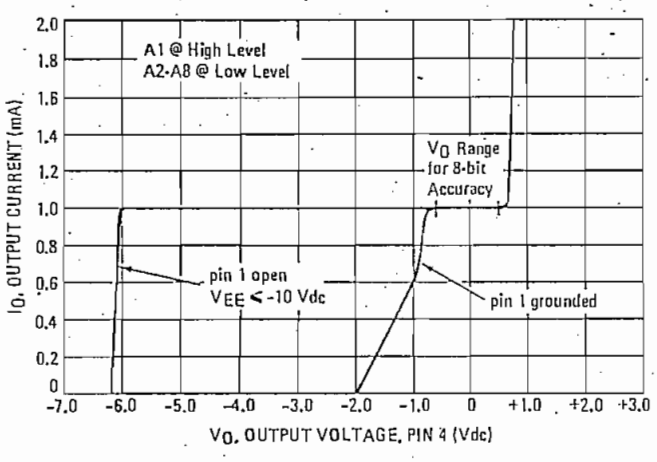
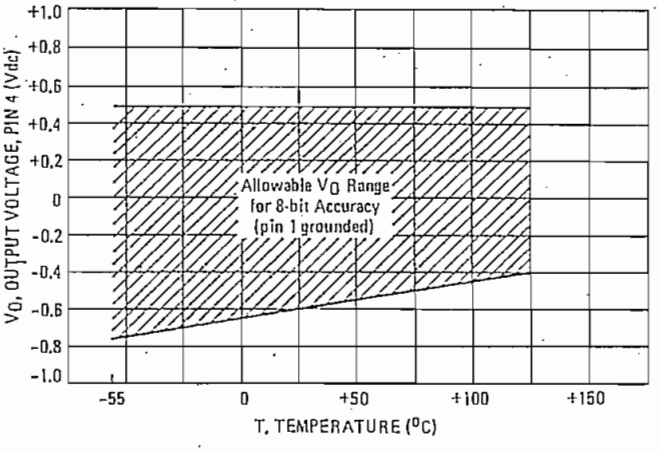


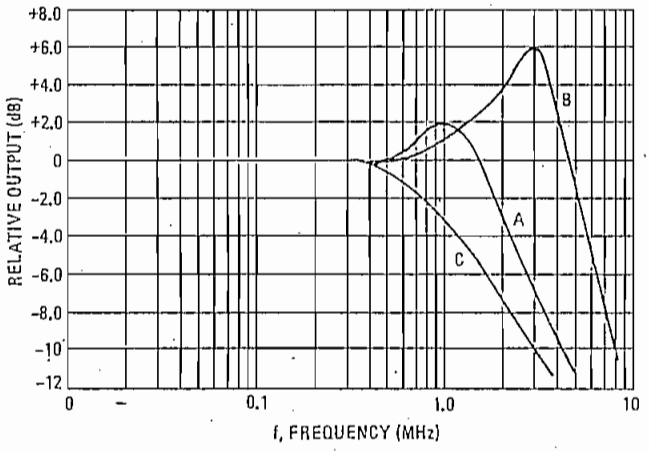
FIGURE 13 — MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE
(Negative range with pin 1 open is -5.0 Vdc over full temperature range)



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted.)

FIGURE 14 — REFERENCE INPUT FREQUENCY RESPONSE



Unless otherwise specified:

R14 = R15 = 1.0 kΩ
C = 15 pF, pin 16 to V_{EE}
R_L = 50 Ω, pin 4 to GND

Curve A: Large Signal Bandwidth
Method of Figure 7
V_{ref} = 2.0 V(p-p) offset 1.0 V above GND

Curve B: Small Signal Bandwidth
Method of Figure 7 R_L = 250 Ω
V_{ref} = 50 mV(p-p) offset 200 mV above GND

Curve C: Large and Small Signal Bandwidth
Method of Figure 25 (no op-ampl, R_L = 50 Ω)
R_S = 50 Ω
V_{ref} = 2.0 V
V_S = 100 mV(p-p) centered at 0 V

FIGURE 15 — TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

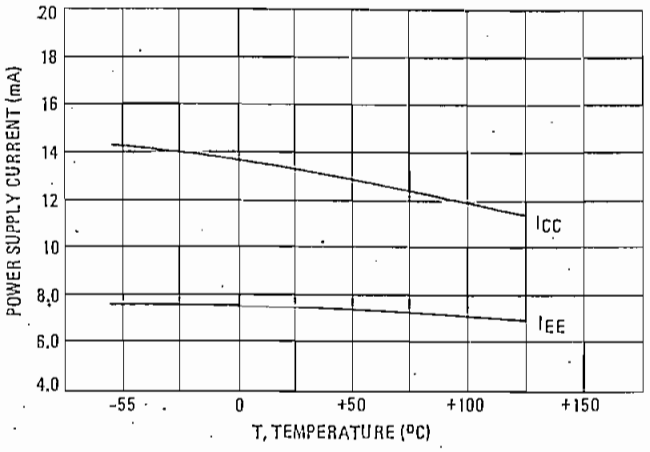
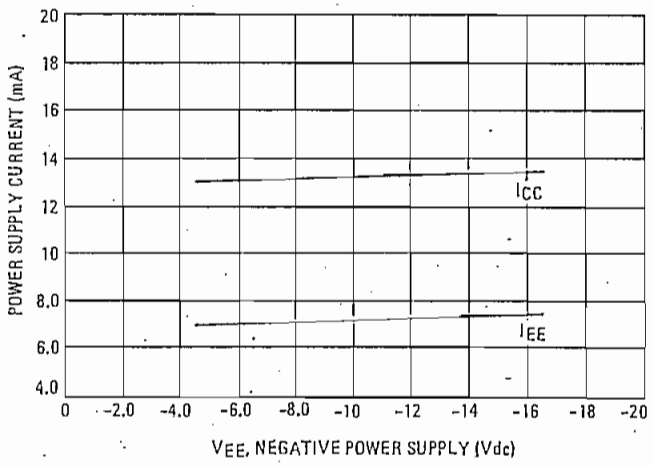
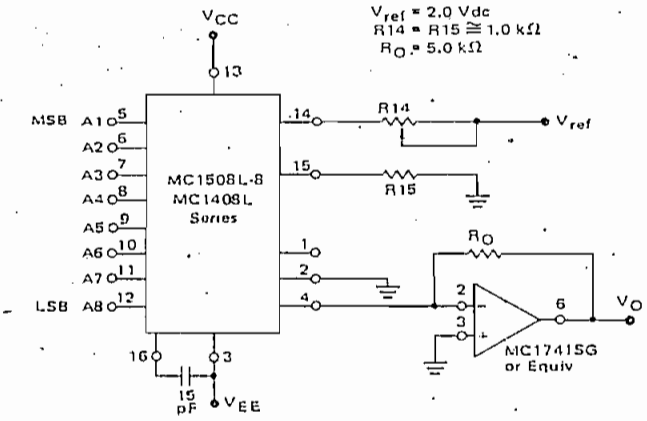


FIGURE 16 — TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 — OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

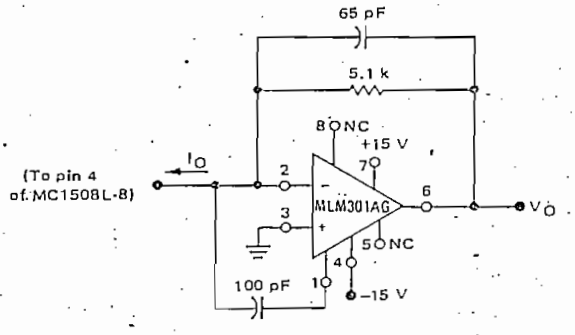
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1508L-8 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

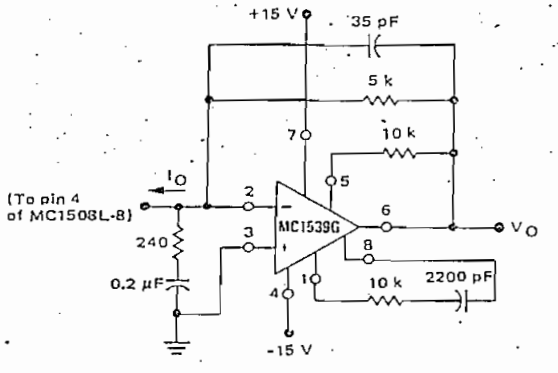
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 18



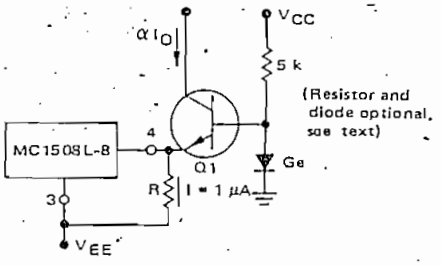
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 — EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1508L-8 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

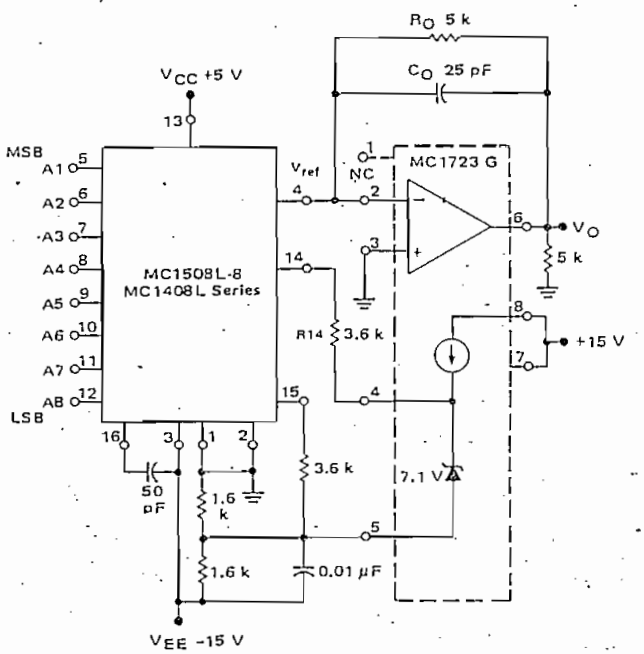
Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the −5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from −2.0 to −8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ±0.05 volt; or 0 to 5.1 volts in 20 mV increments, ±10 mV.

FIGURE 21 — COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



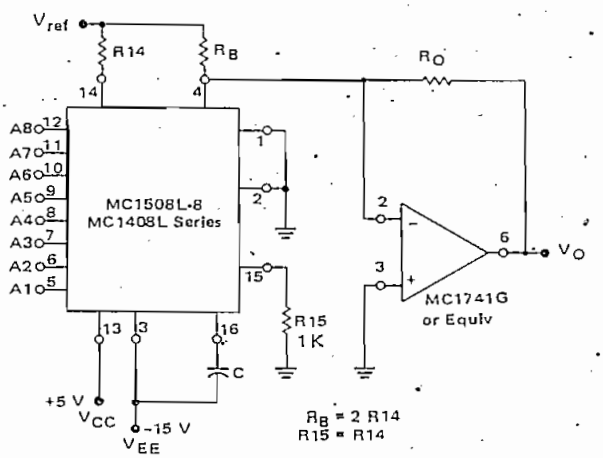
$$V_O = V_{ref} = \frac{R_O}{R14}\{A\}$$

Settling time for a 10-volt step ≅ 1.0 μs

Bipolar or Negative Output Voltage

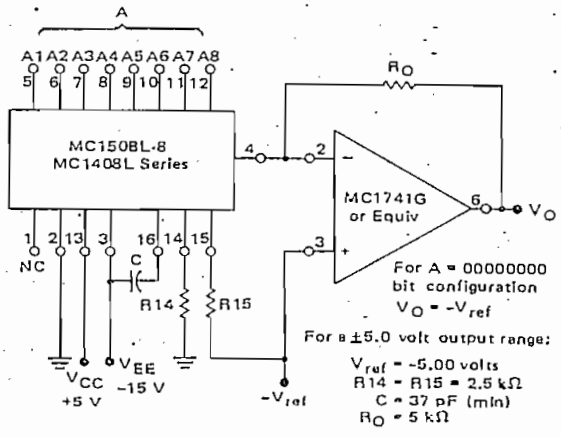
The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range.

FIGURE 22 — BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]-\frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 — BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



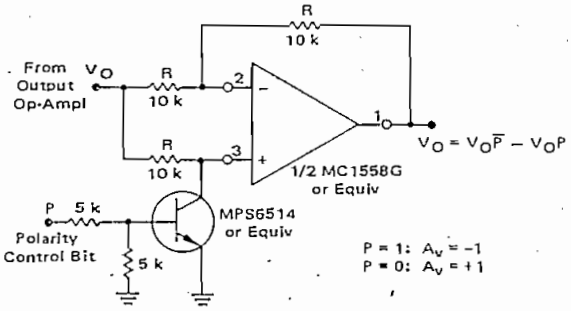
Decrease R_O to 2.5 kΩ for a 0 to -5.0 volt output range. This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information.

APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and −1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 — POLARITY SWITCHING CIRCUIT
(8-Bit Magnitude Plus Sign D-to-A Converter)



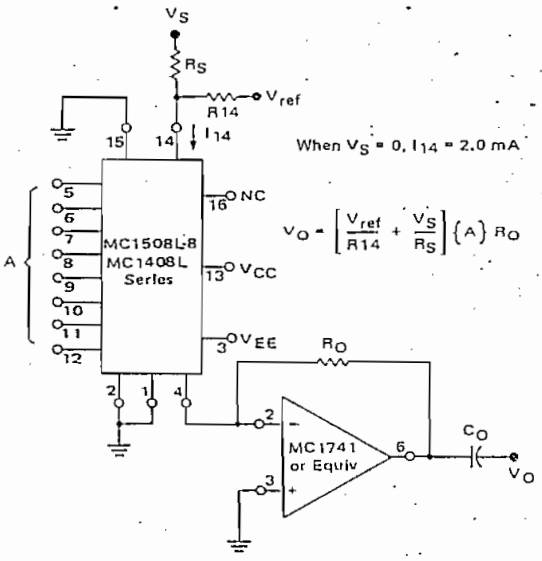
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1508L-8 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ±1.0 mA variation in relation to I_{14}. I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 — PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1508L-8 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref}.

FIGURE 26 — PANEL METER READOUT CIRCUIT

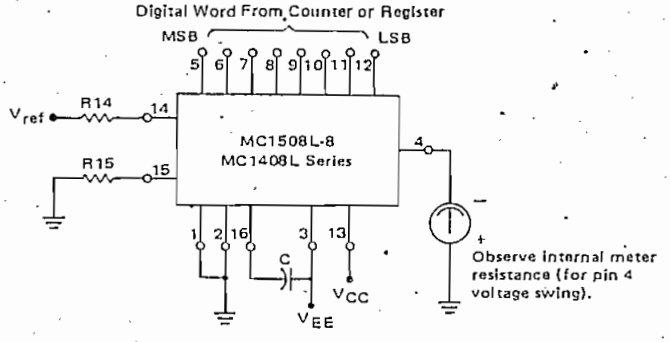
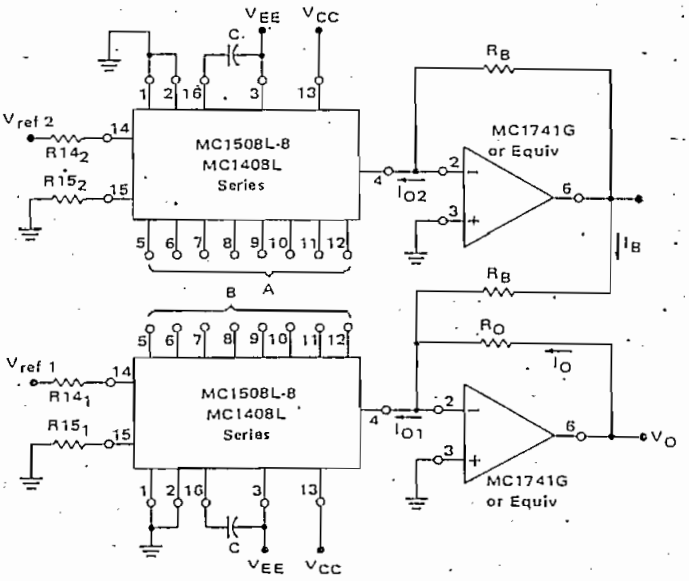


FIGURE 27 — DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$$I_O = I_{O1} - I_{O2} = \frac{V_{ref\,1}}{R14_1}\{A\} - \frac{V_{ref\,2}}{R14_2}\{B\}$$

$I_{O2} = -I_B$

$I_B + I_O = I_{O1}$

Digital Subtraction:

Let $\frac{V_{ref\,1}}{R14_1} = \frac{V_{ref\,2}}{R14_2}$

Programmable Amplifier:

Connect Digital Inputs so A = B

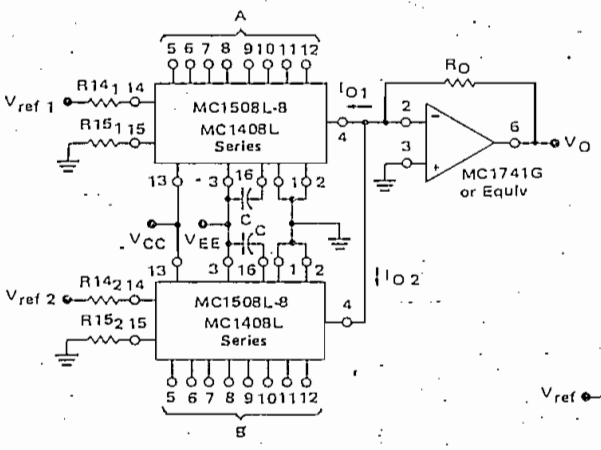
$$V_O = \frac{V_{ref\,1}}{R14_1} R_O[\{A\} - \{B\}]$$

$$V_O = \{A\}\left[\frac{V_{ref\,1}}{R14_1} - \frac{V_{ref\,2}}{R14_2}\right]$$

This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R14_1$ and $R14_2$ or $R15_1$ and $R15_2$. V_O will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R14_1$ and $R14_2$ to a positive reference higher than the most positive input, and drive $R15_1$ and $R15_2$. This yields high input impedance, bipolar differential and common-mode range.

FIGURE 28 — DIGITAL SUMMING and CHARACTER GENERATION



$$V_O = (I_{O1} + I_{O2})\, R_O$$

$$V_O = \left[\frac{V_{ref\,1}}{R14_1}\{A\} + \frac{V_{ref\,2}}{R14_2}\{B\}\right] R_O$$

In a character generation system one MC1508L-8 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

FIGURE 29 — POSITIVE PEAK DETECTING SAMPLE and HOLD
(Features indefinite hold time and optional digital output.)

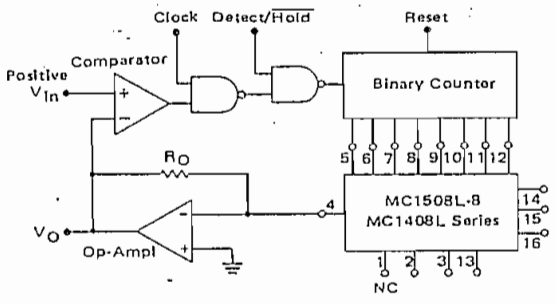


FIGURE 30 — NEGATIVE PEAK DETECTING SAMPLE AND HOLD

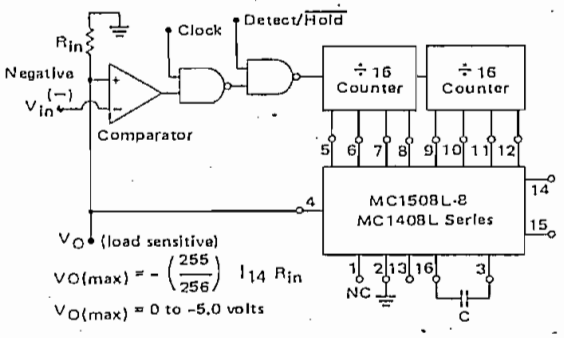
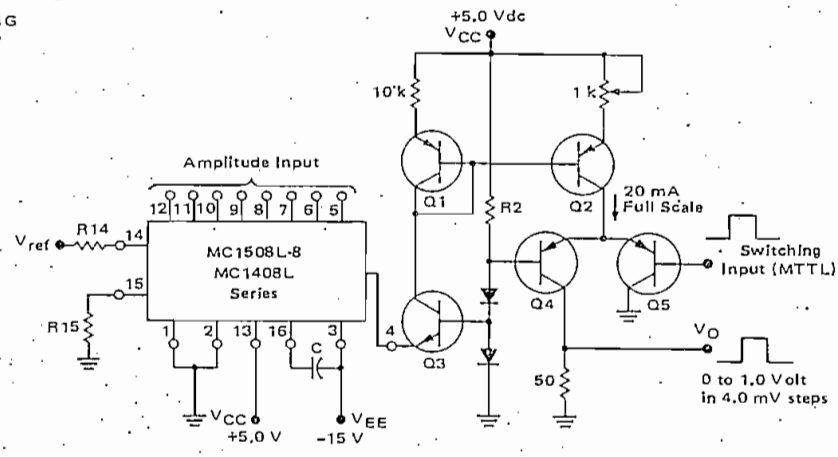
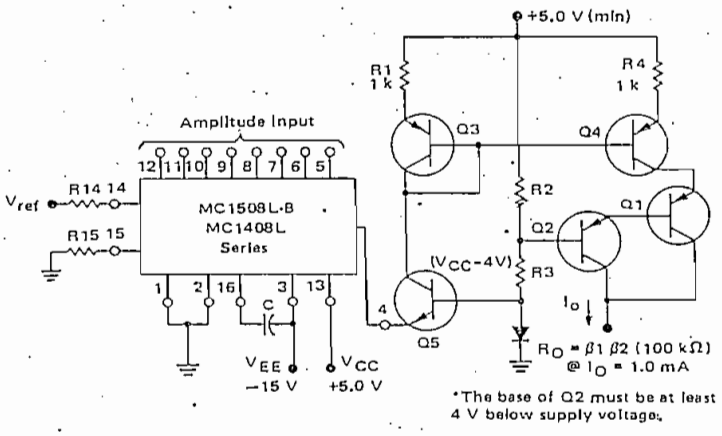


FIGURE 31 — PROGRAMMABLE PULSE GENERATION



Fast rise and fall times require the use of high-speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

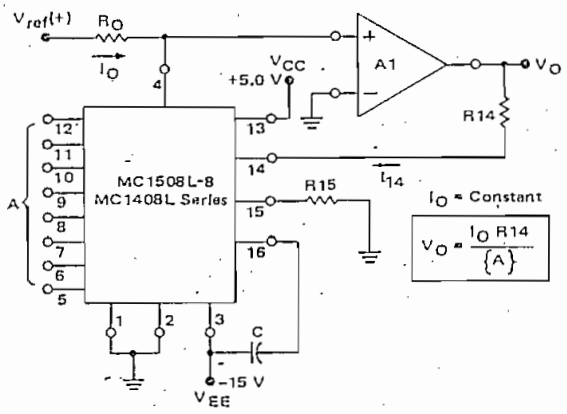
FIGURE 32 — PROGRAMMABLE CONSTANT CURRENT SOURCE



Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

APPLICATIONS INFORMATION (continued)

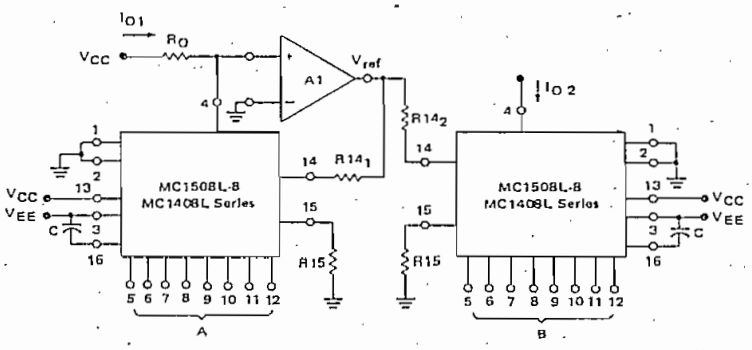
FIGURE 33 — ANALOG DIVISION BY DIGITAL WORD



This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, I_O can be set at 16 μA so that I_{14} will have a maximum value of 3.984 mA for a digital bit input configuration of 00000001.

Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

FIGURE 34 — ANALOG QUOTIENT OF TWO DIGITAL WORDS



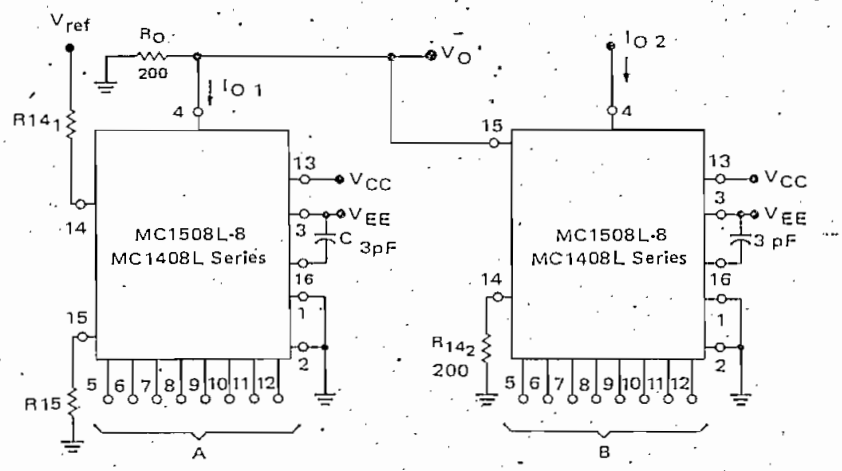
$$V_{ref} = \frac{I_{O1} R14_1}{\{A\}}$$

$$I_{O2} = \frac{V_{ref}}{R14_2} \{B\}$$

If $R14_1 = R14_2$

$$I_{O2} = I_{O1} \left\{\frac{B}{A}\right\}$$

FIGURE 35 — ANALOG PRODUCT OF TWO DIGITAL WORDS
(High-Speed Operation)



$$V_O = -I_{O1} R_O = \frac{V_{ref}}{R14_1} \{A\} R_O$$

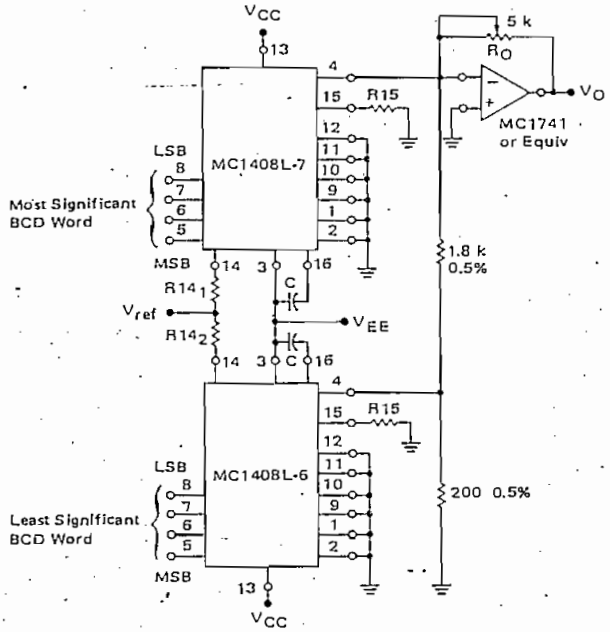
$$I_{O2} = \frac{\{B\} |V_O|}{R14_2} = \frac{\{B\}}{R14_2} \left[R_O \left(\frac{V_{ref}}{R14_1} \right) \{A\} \right]$$

Since $R_O = R14_2$ and $K = \frac{V_{ref}}{R14_1}$

$$I_{O2} = K \{A\} \{B\}$$, K can be an analog variable.

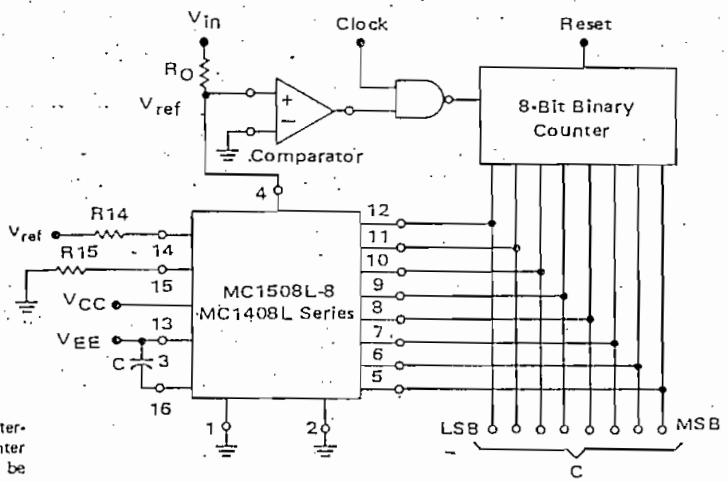
APPLICATIONS INFORMATION (continued)

FIGURE 36 — TWO-DIGIT BCD CONVERSION



Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L-6 may be used for the least significant word.

FIGURE 37 — DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION



$$C = \frac{V_{in}/R_O}{V_{ref}/R14}$$

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

CHAPTER 8

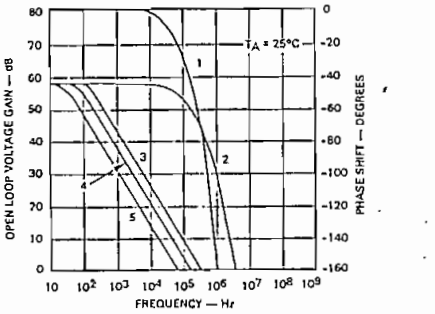
µA723 Precision Voltage Regulator Applications

EQUENCY COMPENSATION

stability of any power supply configuration can be assured .wo steps. First, consider the dc and ac performance of n the internal gain stage of the µA723 and all other active ges used. Then, provide the necessary compensation using ndard operational amplifier techniques.

723 Open Loop Voltage Gain and Phase Shift as a nction of Frequency

ure 8-1 shows the open loop frequency response of the 723 voltage gain stage. The increase in the rate of phase ft seen in *Figure 8-1* is due to the Beta fall off of the output ge at higher frequencies. This increasing phase shift rate uires that the µA723 be compensated whether or not the vice is used with external components.



. 8-1 µA723 Open Loop Voltage Gain and Phase Shift as a Function of Frequency

commended frequency compensation for the unity gain is ner a 5000 pF capacitor from the compensation terminal the V– terminal or a 20 pF Miller compensation capacitor nnected from the frequency compensation terminal to the erting input. To allow proper operation when using the ller compensation, the inverting input must be isolated m the remaining circuitry by some impedance. This is il- trated in *Figure 8-8a*.

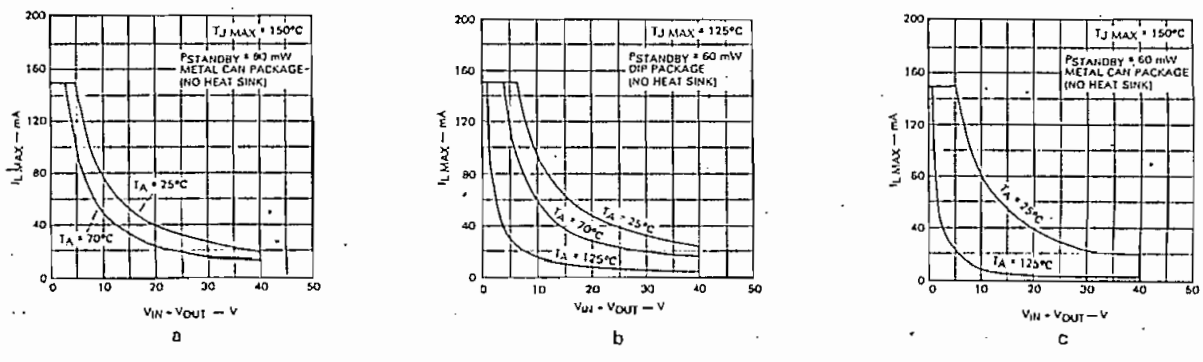
For output voltages greater than V_{REF}, the closed loop gain will be greater than unity. If higher closed loop gains are used, the compensation capacitor can be reduced in direct proportion to the increase in gain.

When using an external series pass device, the 3 dB bandwidth of this device must also be considered, particularly since the majority of these devices have a much lower bandwidth than the µA723. For instance, if a 2N3055 is selected as the series pass device to be used in a unity gain configuration power supply, this device has a minimum f_T of 800 kHz and a maximum Beta of 70. This introduces a 3 dB point in the overall loop gain at approximately 11 kHz, which means that heavier frequency compensation of the regulator is required to assure stability. Since the first break point of 11 kHz is due to the external power device, the regulator should have less than unity gain at the second break point. The second break point is the first break point of the µA723 gain stage, which occurs at approximately 80 kHz as shown in *Figure 8-1*. Adequate compensation is provided by a 0.02 µF capacitor from the compensation terminal to common — or by a 40 pF Miller capacitor from the compensation terminal to the inverting input. As before, for any increase from unity gain, there can be a proportional reduction in the compensation capacitor. However, the value of the Miller capacitor may not be reduced in direct proportion to the standard compensation reduction; this is to allow for gain variations in the µA723 and for parasitic capacitances. Extra capacitance may be required at both the input and the output of any power supply due to the inductive effects of long lines. Adding output capacitance provides the additional benefit of reducing the output impedance occurring at higher frequencies.

THERMAL CONSIDERATIONS

µA723 Load Current Capabilities

Figure 8-2 provides a quick reference to the allowable power dissipation of the µA723 in terms of the input/output differential voltage and load current. *Figure 8-2a* is for the µA723C in the TO-100 package (10-lead metal can); *Figure 8-2b* is for the µA723/µA723C in the TO-116 package (14-lead, hermetic dual in-line); and *Figure 8-2c* refers to the MIL temperature range µA723 in the metal can package.



. 8-2 µA723 Load Current Capabilities for Maximum Load Current as a Function of Input/Output Voltage Differential

μA723 Maximum Power Dissipation in Free Air

The previous curves are based on the free-air dissipation ratings shown in *Figure 8-3* below. The thermal derating factor is 6.8 mW/°C for the TO-100 metal can and 8 mW/°C for the TO-116 hermetic DIP. When it is necessary to heat sink the TO-100 package, a thermal resistance of 50°C/W, junction-to-case may be used.

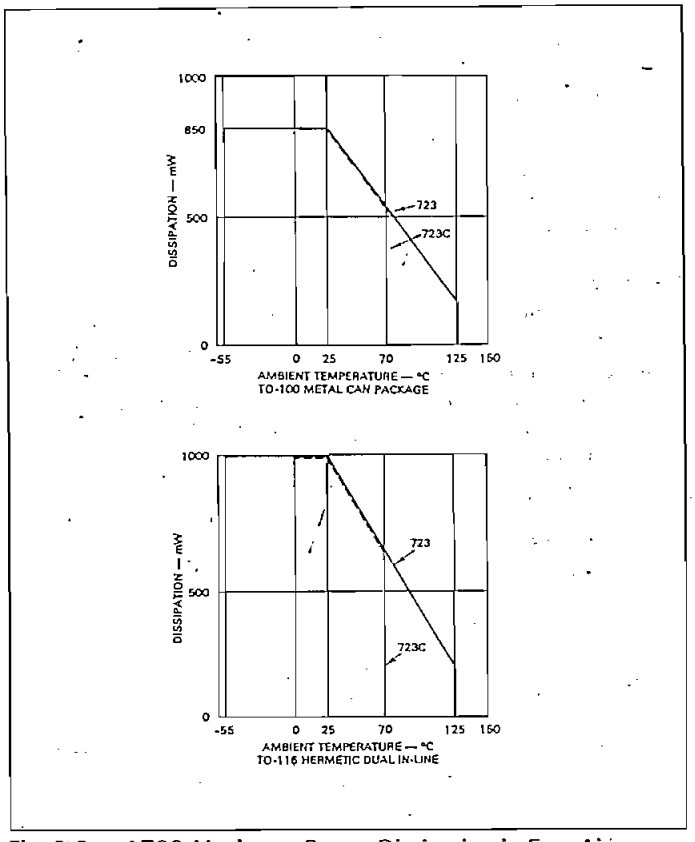


Fig. 8-3 μA723 Maximum Power Dissipation in Free Air

The relationship between power dissipation P_D, maximum ambient temperature T_A, and thermal resistance from case-to-ambient Θ_{CA}, is then:

$$P_D = \left(\frac{150°C - T_A}{50°C/W - \theta_{CA}}\right) W, \text{ or } \theta_{CA} = \left(\frac{150°C - T_A}{P_D}\right) - 50°C/W$$

These equations may be used to calculate the maximum allowable power dissipation, P_D, or the maximum allowable heat sink resistance, Θ_{CA}, from a given set of conditions:

FUNCTIONAL TEST CIRCUIT

Simplified Tester Schematic

A simplified functional test circuit for the μA723 is given in *Figure 8-4*. The output voltage is set for a nominal +5.0 V. The basic test steps are as follows.

1. Load Regulation at 50 mA, Close S1

   Measure output voltage change with S2 open and closed, (a load current change of 50 mA).

2. Line Regulation, Open S2

   Measure output voltage change resulting from a change in input voltage V_{IN}.

3. Short Circuit Current, Open S1 and S2

   Measure output current when the output is shorted to ground.

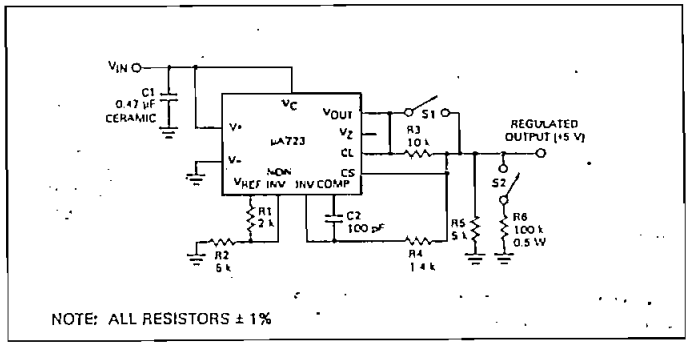


Fig. 8-4 Simplified Tester Schematic

TYPICAL APPLICATIONS

Introduction

The required output voltage for the following μA723 applications can be calculated from the equation accompanying each circuit. In all cases the resulting resistor values are assumed to include any potentiometer resistance used. In addition, *Table 8-1* is included at the end of the section and affords a quick reference for many standard output voltage requirements. The previous section on frequency compensation gives guidance to the suitable values of compensating capacitors used in the various appications. Specific transistor types are not included in this section. However, Appendix C includes a discussion of the selection of power devices and a list of preferred types.

In the following applications, the μA723 is represented in a number of ways. In those circuits where the regulator operation is very basic, the symbol of *Figure 8-5* is used. Lead functions can be identified by referring to *Figure 7-1*.

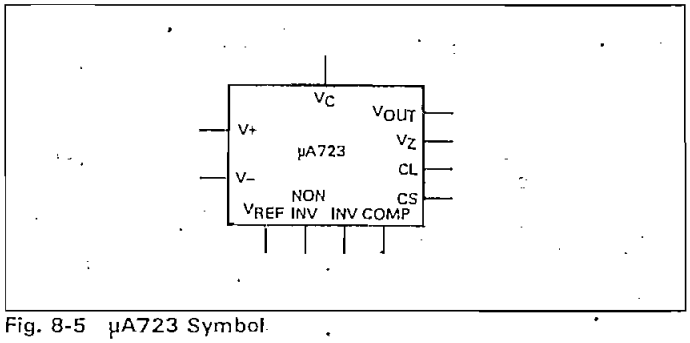


Fig. 8-5 μA723 Symbol

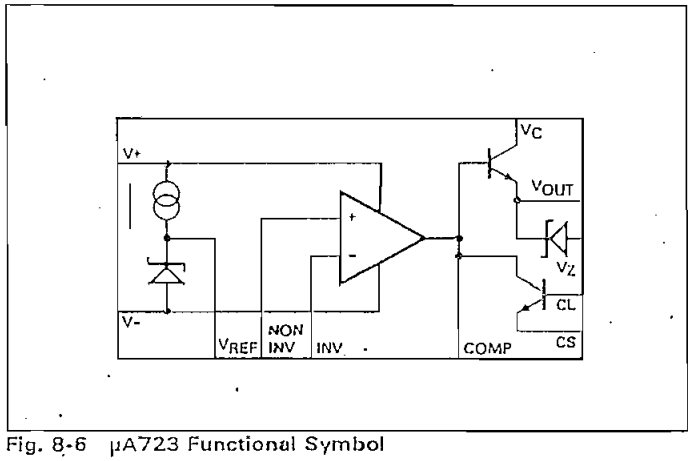


Fig. 8-6 μA723 Functional Symbol

In those applications where the circuit operation is clarified by the use of a functional schematic of the µA723, *Figure 8-6* is used. This block bears a close resemblance to the simplified schematic of *Figure 7-1*. In some cases the individual components of this block may be rearranged in order to simplify a particular schematic. The reference voltage is represented by a single Zener diode, nominal voltage 7.15 V supplied from a constant current source. The output Zener diode, V_{OUT} to V_Z, is shown only in the required applications.

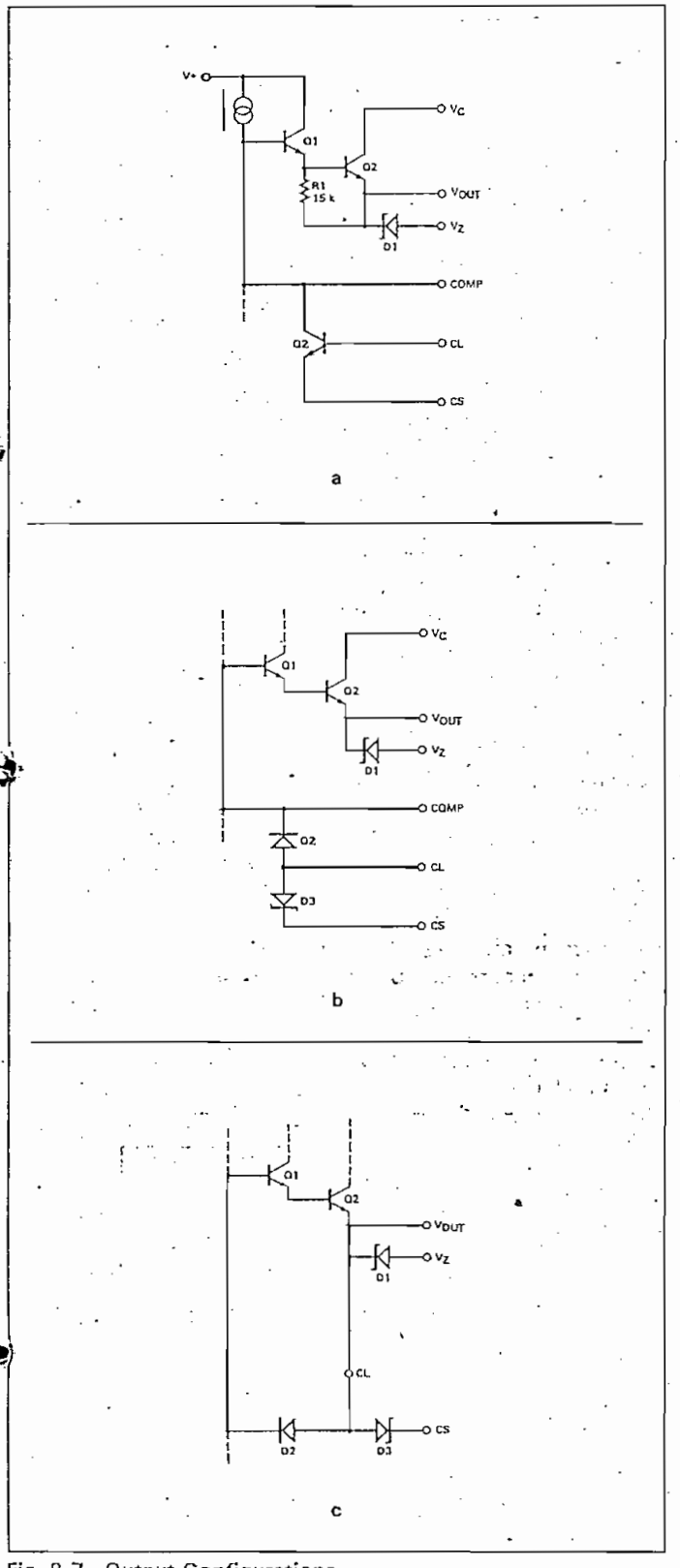


Fig. 8-7 Output Configurations

Output Configurations

Many of the applications use internal Zener diodes for level shifting or for the generation of stabilized voltages. An explanation of where these diodes exist in the µA723 circuit may help to avoid any problems arising from improper biasing.

The µA723 output stage schematic is reproduced in *Figure 8-7a*. The V_Z terminal provides direct access to a 6.2 V Zener diode whose cathode is internally connected to V_{OUT}. Provided the internal current limit transistor is not required for output short circuit protection, its base emitter junction provides another 6.2 V Zener diode (See *Figure 8-7b*). Note, however, that the anode of this diode, terminal CL, is connected internally by the collector base junction diode to the base of the output drive transistor. When using the CL – CS Zener diode, the collector base diode must always be reverse biased. Maximum permissible CL – CS Zener current is 5 mA. Correct biasing is assured in *Figure 8-7c* by interconnecting the V_{OUT} and CL terminals to provide both positive and negative 6.2 V Zener diodes referenced to the V_{OUT} terminal.

Positive Regulators, 150 mA Maximum

Figure 8-8a shows the basic low voltage configuration suitable for output voltages ranging from 2 to 7 V. The reference voltage, V_{REF}, is first divided down by R1, R2 and, if desired, potentiometer P1. Then it is applied to the non-inverting input of the error amplifier. C_{REF} may be added if ripple rejection greater than that specified for the µA723 (74 dB) is required. The presence of C_{REF} also reduces the regulated output noise voltage considerably.

Capacitor C1 provides frequency compensation. C1 is isolated from the low impedance output by R3 which also balances the error amplifier source impedances to give minimum temperature drift. To minimize component count at the expense of temperature drift, R3 may be omitted. In this case, C1 cannot be used for frequency compensation. Instead, C2 may be used from the compensation terminal to ground as shown in *Figure 8-8b*. To minimize power dissipation, the V+ and V_C terminals may be supplied separately, with V+ requiring a minimum of 9.5 V, while the V_C supply may be as low as 3 V above the regulated output voltage. The schematics shown in *Figure 8-8a* and *8-8b* have output voltages given by

$$V_O = \left(\frac{R2}{R1 + R2}\right) V_{REF} \text{ where } (R1 + R2) > 1.5\ k\Omega$$

Output voltages from 7 to 37 V are obtainable with *Figure 8-8c* in which

$$V_O = \left(\frac{R1 + R2}{R2}\right) V_{REF}$$

If the reference bypass capacitor is required in this circuit, it should be connected from the non-inverting input to ground using R3 to increase the reference source impedance and improve the effectiveness of the reference capacitance. A 150 mA output current is available with R_{SC} set to zero. When short circuit current limiting is desired, R_{SC} may be used to limit the maximum output current to

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$$

where V_{SENSE} (the sense voltage, or the voltage between terminals CL and CS) is given in *Figure 8-8a*. The resulting output current limit has a temperature coefficient of –0.3%/°C.

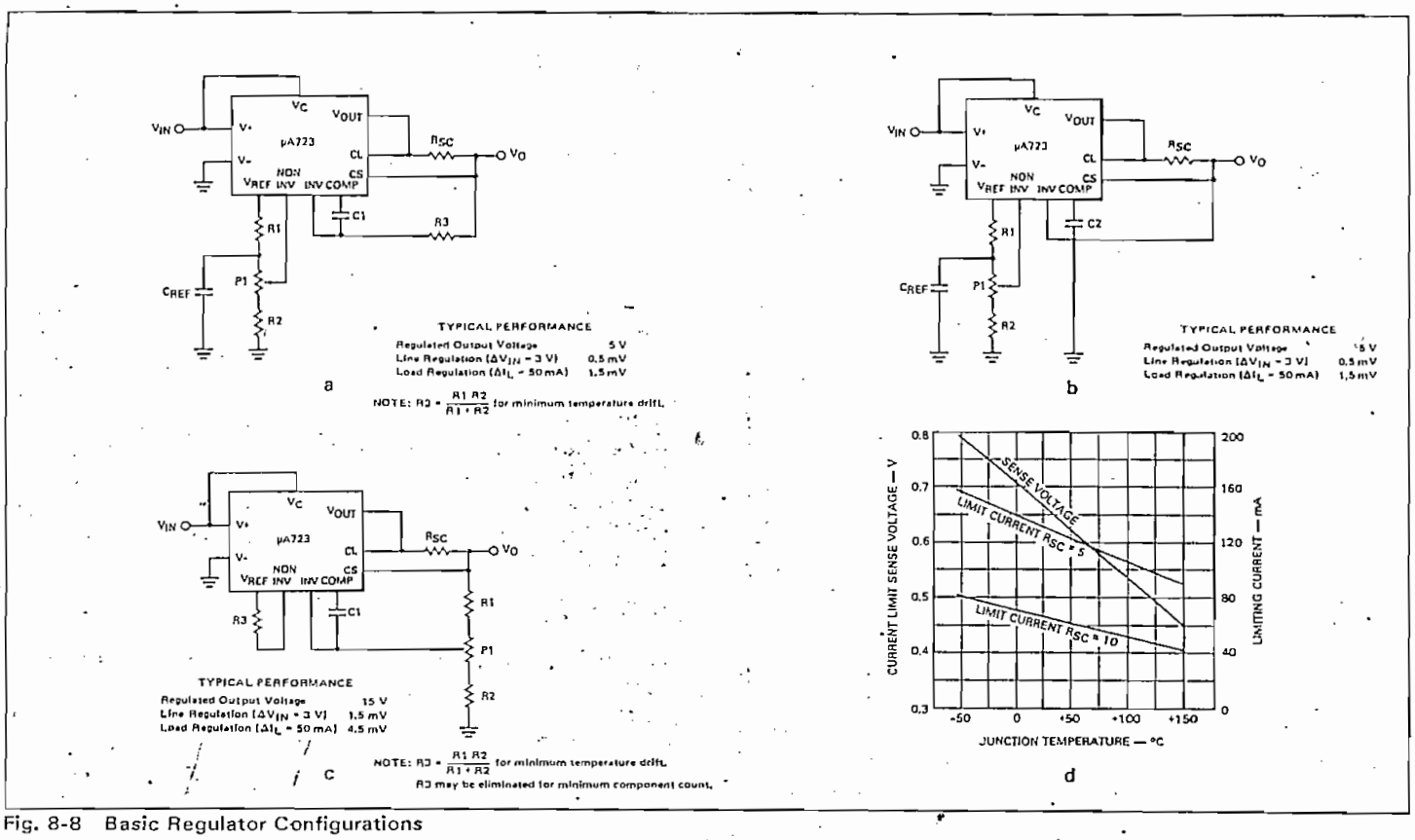


Fig. 8-8 Basic Regulator Configurations

Positive Regulators, High Output Current

In *Figure 8-9a,* an npn transistor, Q1, boosts the available output current beyond the capability of the μA723. Q1 can consist of several transistors cascaded to satisfy very high current requirements. In this circuit, one V_{BE} voltage must be added to the 3 V minimum input/output differential requirement for each transistor added. Depending on the type of transistor used for Q1, R3 should be added giving I_{CBO} compensation, and alleviating the safe area limitation of the output device. With R_{SC} set to zero the maximum output current capability is (Q1 Beta) x (150 mA). R_{SC} may be used to limit the short circuit current to any desired value up to this maximum in the same manner as outlined previously in *Figure 8-8.*

An alternate circuit is shown in *Figure 8-9b.* Using an external pnp transistor, maximum output current is again (Q1 Beta) x (150 mA). One V_{BE} should be added to the minimum input/output differential voltage requirement for each additional transistor. The circuits in *Figure 8-9* may supply outputs in the range of 2 to 37 V by selecting the appropriate feedback network. *Figure 8-9a* is shown for output voltages from 7 to 37 V, whereas *Figure 8-9b* is shown for output voltages from 2 to 7 V.

If it is required to vary the output continuously over a 10 to 1 range, it is necessary first to attenuate V_O so that V_{INV} never exceeds V_{REF} even when V_O is at its maximum value, then provide a potentiometer adjustment from V_{REF} to the non-inverting input. This is illustrated in *Figure 8-9c*, where V_O is attenuated by a ratio of 5.2:1.

Maximum permissible V_O is then 35 V (giving a V_{INV} of 6.8 V), which requires 38.6 V < V_{IN} < 40 V. Minimum V_O is determined by the minimum value for V_{INV}. The specified minimum V_{INV} is 2 V; however, it will be found that typically V_{INV} may be reduced to approximately 0.72 V before the circuit no longer regulates. This corresponds to a V_O of 3.7 V.

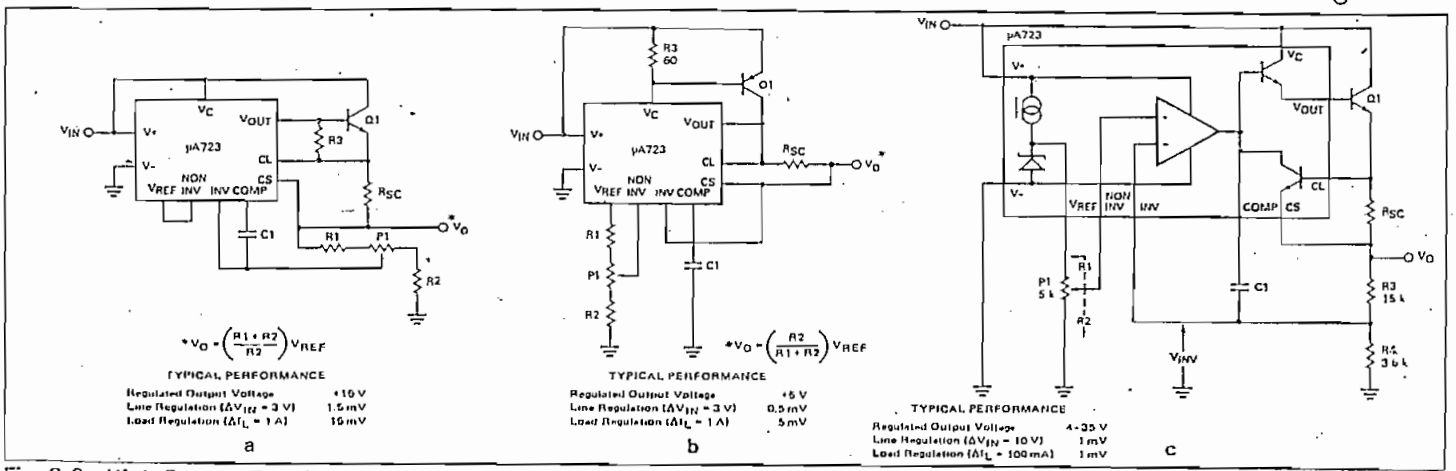


Fig. 8-9 High Current Regulators

Other 10 to 1 voltage ranges may be obtained by varying the attenuation ratio, (R3 + R4)/R4, from 5.2 to, say, 1.4. Then V_O range will be 1 V to 10 V (13.6 V < V_{IN} < 39 V).

Figure 8-9c,

$$V_O = V_{REF}\left(\frac{R2}{R4}\right)\left(\frac{R3+R4}{R1+R2}\right)$$

or, with the values of R3 and R4 as shown,

$$V_O = 5.2\ V_{REF}\left(\frac{R2}{R1+R2}\right)$$

Positive Shunt Regulator

The µA723 may be used in a shunt regulating mode by adding an external transistor, Q1. Special attention should be paid to ensure that the series limiting resistor, R4, is capable of handling the high power dissipation inherent in this mode of operation. *Figure 8-10a* is used with the 14-lead DIP version of the µA723. When the 10-lead metal can is used, however, it is necessary to add a 6.2 V Zener diode externally, as in *Figure 8-10b.*

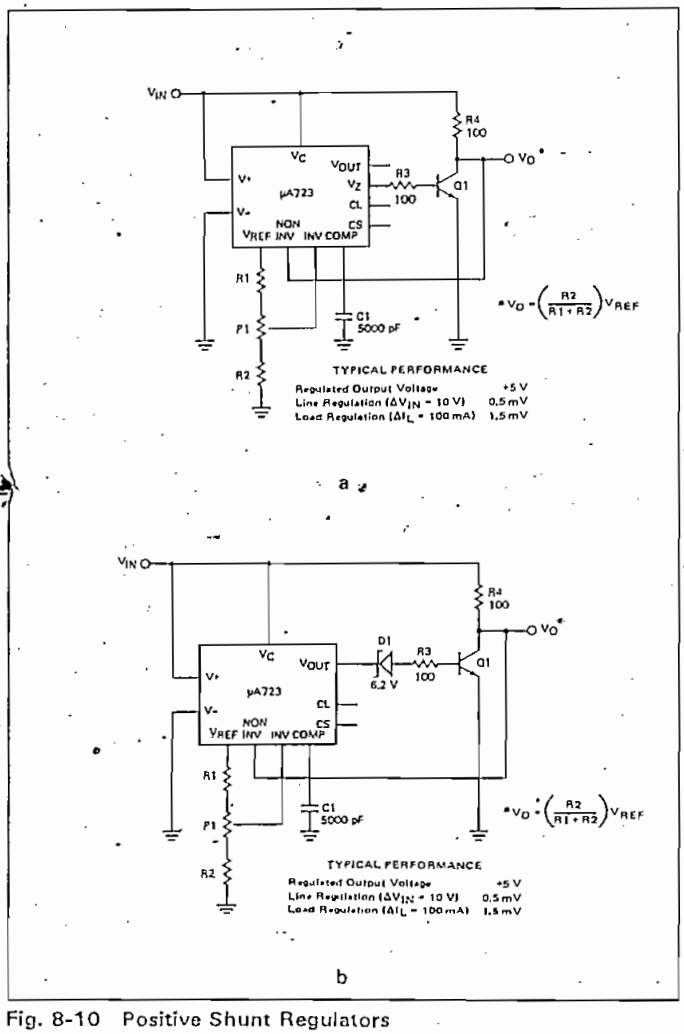


Fig. 8-10 Positive Shunt Regulators

Positive Regulators, High Line Rejection

As shown in *Figure 8-11a* and *8-11b,* the circuits each use the internal current limit transistor to preregulate the V+ supply, thereby increasing the line rejection to more than 100 dB. The CS – CL terminals provide a 6.2 V Zener diode referenced to the output voltage, which is then used to supply V+. In these applications R3 must be chosen so that the current into the CS terminal is limited to 5 mA maximum.

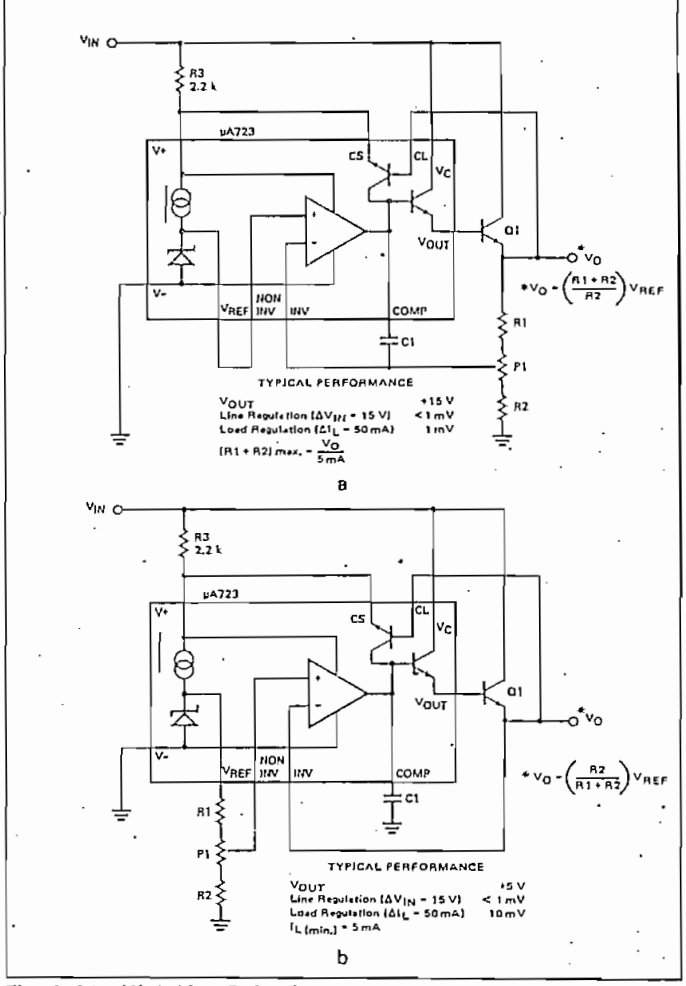


Fig. 8-11 High Line Rejection

Positive Regulators, High Input Voltage

Input voltages greater than 40 V may be applied when the µA723 is connected as shown in *Figure 8-12a.* The regulated output voltage must remain less than 38 V to protect the regulator. R3 may be replaced with a FET current source in those cases where the variation of input voltage imposes excessive power dissipation in the internal series pass device. Q2 provides short circuit protection, if required (the internal current limit transistor cannot be used in this application). The maximum input voltage is determined by the breakdown characteristics of Q1. When using the µA723 DIP version, D1 may be omitted and the V_Z terminal grounded; in this case V_{REF} must be resistively divided by two before being applied to the inverting input.

Note that in this type of application where the µA723 output stage is used as an additional inverting amplifier rather than the usual emitter follower, V_{REF} must be connected to the inverting input of the error amplifier to maintain correct phase relationships around the regulating loop, i.e., negative feedback from the output.

When using a pnp series pass device, high input voltages may be tolerated by using a Zener diode to reduce the voltage appearing across the µA723, as in *Figure 8-12b.* For example, if D1 is a 20 V Zener diode, input voltages to 60 V are permissible. D1 must be selected such that no more than 40 V is applied to the µA723 V+ and V_C terminals under maximum input voltage conditions. Similarly, the regulated output voltage must not exceed 37 V to maintain the specified input-to-output differential.

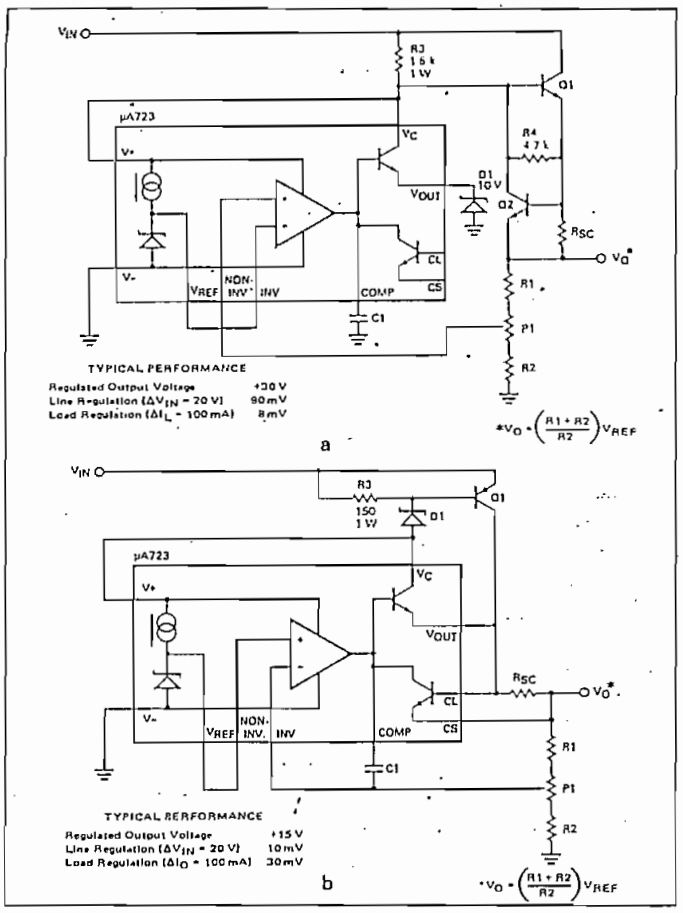


Fig. 8-12 High Input Voltage

Positive Regulator, Floating

The µA723 may be used to directly regulate hundreds of volts using the configuration shown in *Figure 8-13,* in which a floating power source is provided for the regulator by D1. The series pass transistor becomes the only limiting factor in determining the maximum voltage and current which may be controlled. The V_{REF} terminal supplies all the current drawn by the sensing resistors and the total current must not exceed 5 mA. R5 must be selected to provide sufficient current to bias D1 and to supply the µA723 standby current at the minimum input voltage condition. D2, D3 and D4 are for protection purposes; fast switching diodes should be used.

If Q1 is a high f_T device, it may be necessary to add C2 to reduce the output noise level. If V_{IN} is switched on and off, causing a very high dV_{IN}/dt to appear at the µA723 terminals, C3 may be added to ensure correct biasing throughout the circuit. In normal use when on/off switching takes place before the usual rectifier/filter supply for V_{IN}, C3 is not necessary.

It will be noted from *Figure 8-13* that

$$V_O = V_{REF}\left[\left(\frac{R2}{R1}\right) - \left(\frac{R3}{R1}\right)\left(\frac{R1+R2}{R3+R4}\right)\right]$$

If R3 and R4 are made equal,

$$V_O = \frac{V_{REF}}{2}\left(\frac{R2-R1}{R1}\right)$$

The normal minimum regulated output voltage limitation of 2 V for the µA723 does not apply to this circuit, output voltages down to zero volts being readily obtainable.

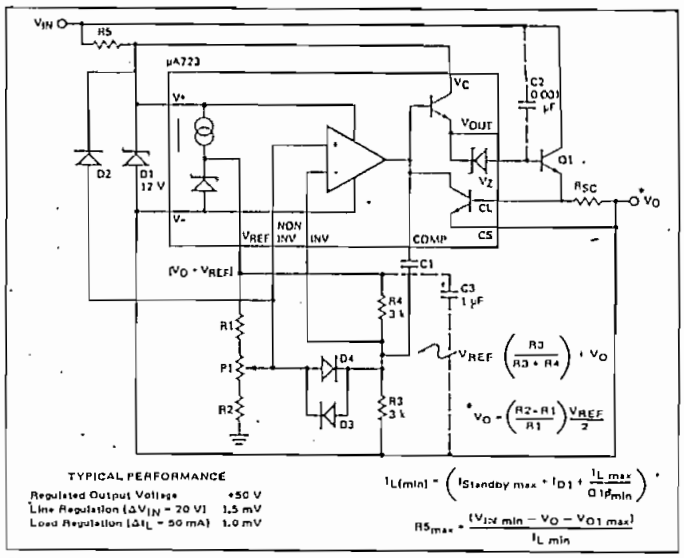


Fig. 8-13 Floating Positive Regulator

Assuming the regulator is operating correctly, then the INV input will equal the NON-INV input, i.e.,

$$(V_O + V_{REF})\left(\frac{R2}{R1+R2}\right) = (V_{REF})\left(\frac{R3}{R3+R4}\right) + V_O$$

$$V_O\left(\frac{R2}{R1+R2} - 1\right) = V_{REF}\left[\left(\frac{R3}{R3+R4}\right) - \left(\frac{R2}{R1+R2}\right)\right]$$

$$V_O = V_{REF}\left[\left(\frac{R2}{R1}\right) - \left(\frac{R3}{R1}\right)\left(\frac{R1+R2}{R3+R4}\right)\right]$$

Positive Regulators, Low Input/Output Differential

Either of the two circuits shown will allow an input-to-output voltage difference close to the saturation point of the series pass device. As in all applications, the $V_{IN(2)}$ of *Figure 8-14b*

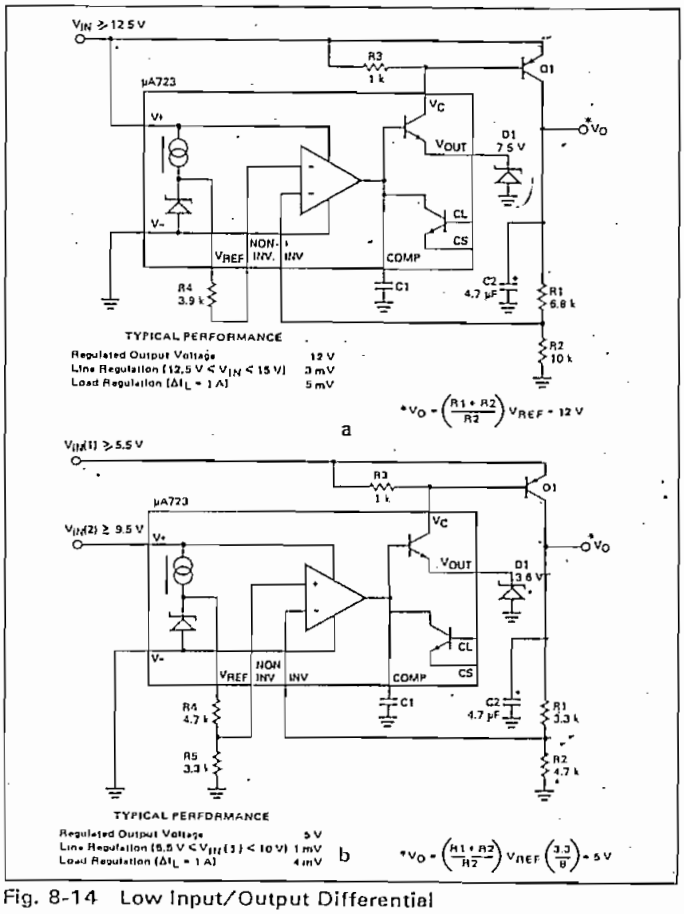


Fig. 8-14 Low Input/Output Differential

must be 9.5 V minimum. The 7.5 V Zener diode may be eliminated (See *Figure 8-14a*) when using the dual in-line package by grounding the V_Z terminal and reducing the V_{REF} to 3 V by a 4.7 kΩ/3.3 kΩ voltage divider to the non-inverting input of the μA723.

Positive Regulators, Marginal Input Voltage

The two circuits shown in *Figure 8-15* offer some relief from the 9.5 V minimum V+ voltage when regulating lower voltages. In those cases where the average voltage applied to the input is greater than the required minimum — but the negative ripple peaks are lower — a diode/capacitor peak detector will provide the solution *(Figure 8-15a). Figure 8-15b* shows one method of using a voltage doubler to assure that using a minimum of external components, the proper bias voltage is applied to the V+ terminal.

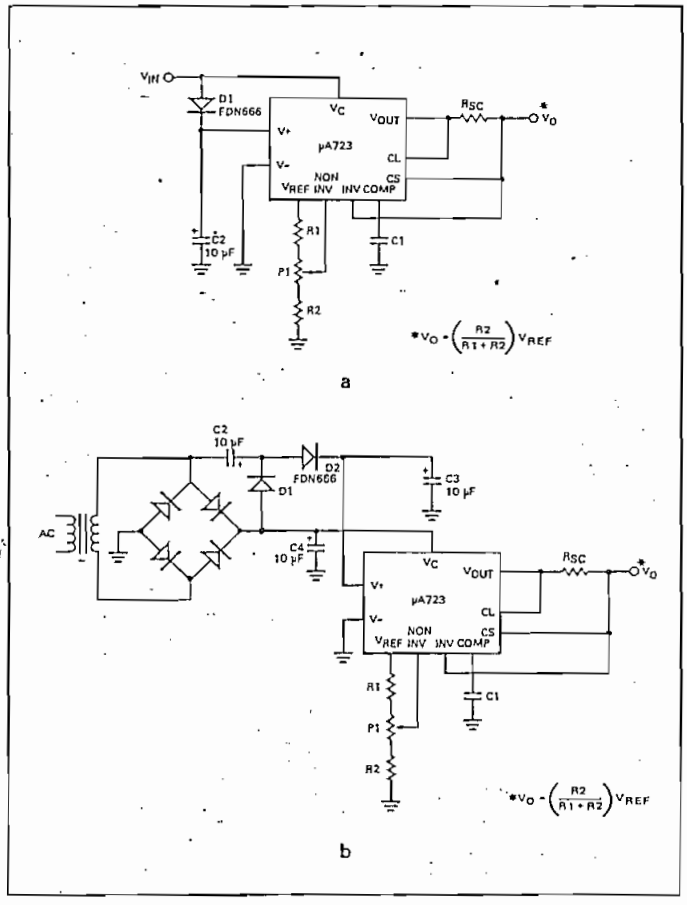


Fig. 8-15 Marginal Input Voltage

Negative Regulators, Medium/High Output Current

This configuration *(Figure 8-16a)* will regulate any negative voltage between –9.5 V and –40 V. Since the uA723 is operated between ground and the regulated output, the maximum unregulated input voltage is determined by the voltage breakdown and power dissipation capabilities of the pnp series pass device, Q1. Base current for Q1 is supplied through resistor R5 such that the minimum input-to-output differential is controlled both by the base current required by Q1 and the value of R5.

A Darlington connection may be used for Q1 to reduce the base current requirement *(Figure 8-16b)* and to increase the output current capability. Either the complementary Darlington as shown, or a standard pnp pair may be used.

For output voltages in the range –2 V to –9.5 V, the output voltage alone is insufficient to bias the μA723 in *Figure 8-16a.* This condition is satisfied in *Figure 8-16c* by an external, regulated or unregulated, positive voltage applied to the V+ and V_C terminals. The maximum limit of 40 V between the V+ and V– terminals must be observed. Maximum values for $-V_{IN(2)}$ and the input-to-output differential are determined as for *Figure 8-16a.*

In all cases, *a* through *c*, if the V_Z terminal is unavailable, then the V_{OUT} terminal may be used with a series 6.2 V Zener diode.

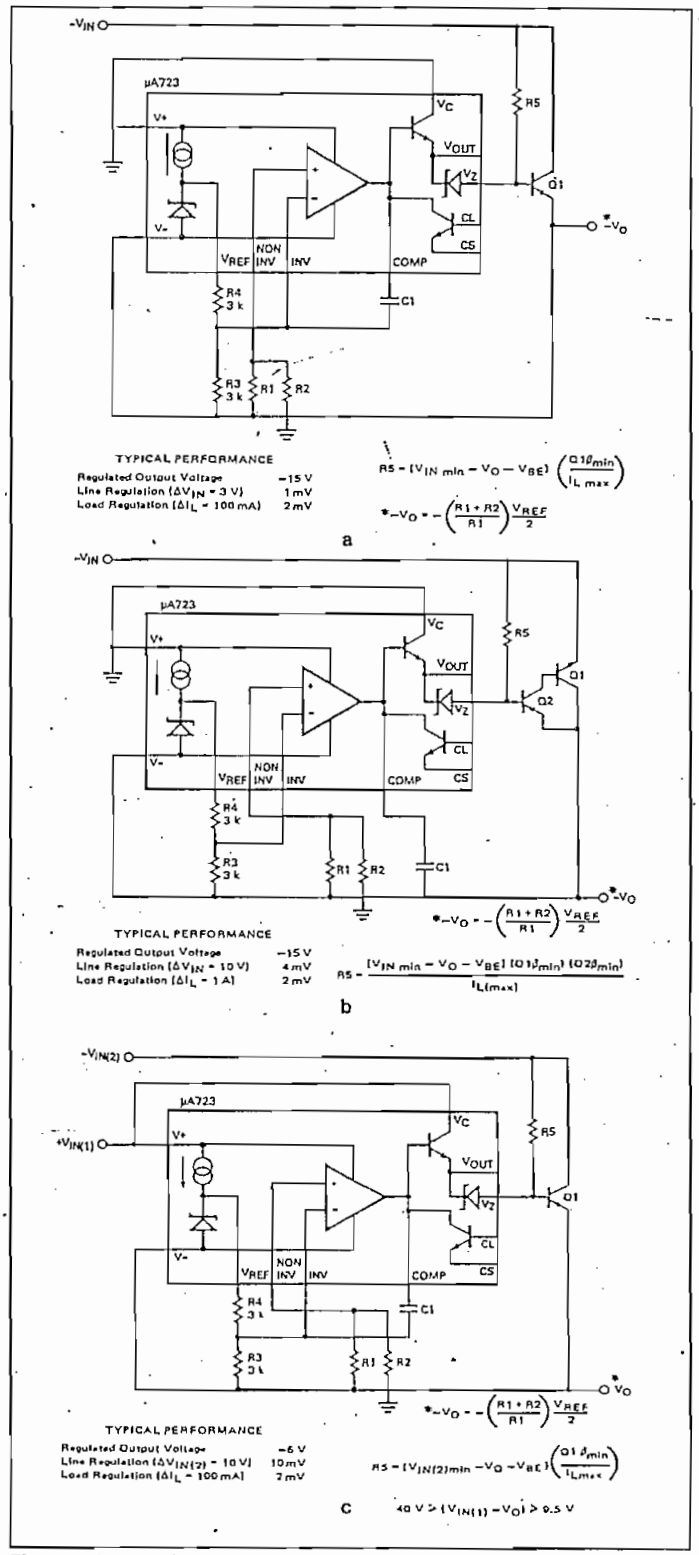


Fig. 8-16 Medium/High Output Current

Negative Shunt Regulator

For low to medium output currents the series pass transistor of the previous circuits may be omitted. However, special attention must be paid to the dissipation of D1 and R5, and the internal dissipation of the µA723. Maximum permissible current shunted to ground via the V_{OUT} terminal is 150 mA.

Figure 8-17 as shown in suitable for output voltages in the range –9.5 V to –40 V. By removing the V+ and V_C terminals from ground and supplying them with a low value positive voltage as in *Figure 8-16c*, output voltages from –2 V to –9.5 V are obtainable. Total voltage from V– to V+ of 9.5 V minimum and 40 V maximum must be observed. If the maximum current from the V_{OUT} terminal is less than 20 mA in a particular application, then D1 may be omitted and the output connected to V_Z instead of V_{OUT}.

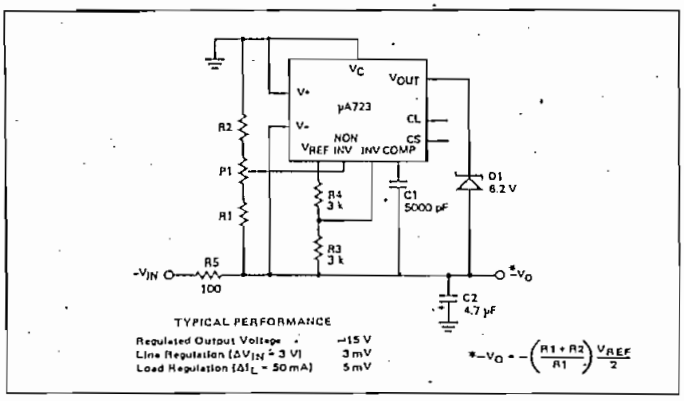


Fig. 8-17 Negative Shunt

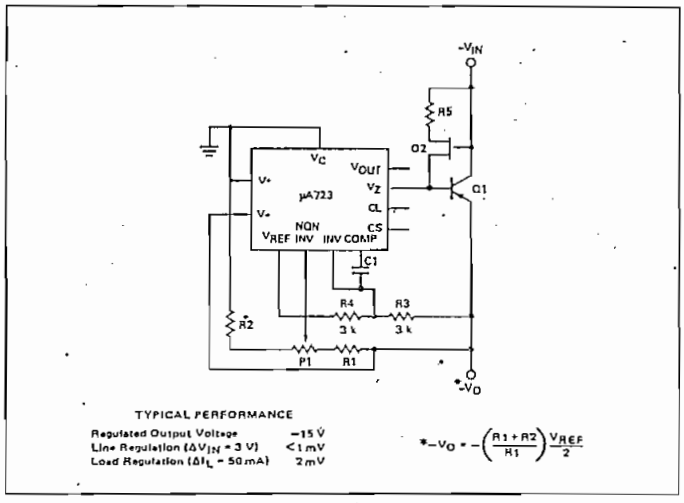


Fig. 8-18 Negative High Line Rejection

Negative Regulator, High Line Rejection

In the negative regulators with a series pass device, the only variation seen by the control circuitry under varying input conditions is the current variation caused by the fixed resistance across the series transistor's collector-base junction.

By replacing the resistor with a FET current source in *Figure 8-18*, the line rejection is greatly improved, typically exceeding 100 dB. Output voltage range is –9.5 V to –40 V, extendable down to –2 V by the addition of a positive supply as in *Figure 8-16c*. R5 and Q2 must be selected to provide sufficient base current for Q1 under worst case conditions. A good choice for Q2 would be a 2N5484 with R5 equal to zero, since its I_{DSS} (zero gate voltage drain current) of 1 to 5 mA will provide sufficient base current for Q1 in most applications.

Negative Regulator, Floating

When the desired output voltage exceeds the 40 V maximum which may be applied across the device, then a Zener diode should be used to limit the voltage, as shown *(Figure 8-19)*. The actual Zener voltage selected may be between 9.5 V and 40 V with little change in performance. This circuit is the complement of *8-13*. R6 must be selected to provide sufficient current to bias D1 and to supply the µA723 standby current under minimum input voltage conditon. Select R5 according to the requirements outlined in *Figure 8-16b*.

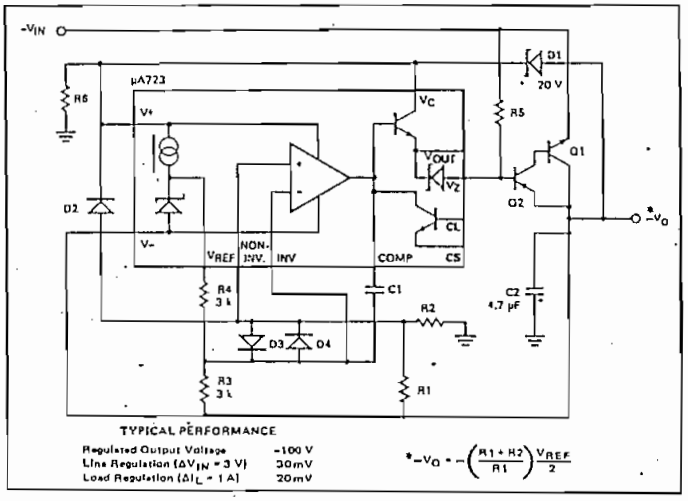


Fig. 8-19 Negative Floating

Current Regulators

In *Figure 8-20a* the regulator will force a voltage to appear across R_P which is equal to the voltage existing across R2. The resulting current is summed with the regulator's standby current, I_{SB}, and the current through R2, to provide a regulated current, I_L, into the load, R_L. Due to this summation, line regulation decreases for output currents below 10 mA.

The input voltage must be greater than I_L $R_{L(max)}$ +9.5 V to ensure sufficient voltage across the µA723. *Figure 8-20a* is shown sourcing current from a positive voltage $+V_{IN}$. V_{IN} can, of course, be grounded while returning R_L to a negative voltage. Similarly, the output terminal may be grounded or taken to a negative voltage when the V_{IN} terminal will provide a regulated current sink of magnitude I_L. In no case may the voltage from V– to V+ exceed 40 V.

$$I_L = \left(\frac{R2}{R1+R2}\right)\left(\frac{V_{REF}}{R_P}\right) + I_{SB} + I_{R2} = \left(\frac{V_{REF}}{R1+R2}\right)\left(1+\frac{R2}{R_P}\right) + I_{SB}$$

for output currents in excess of 10 mA, this approximates to:

$$I_L = \left(\frac{R2}{R1+R2}\right)\left(\frac{V_{REF}}{R_P}\right) + I_{SB} \simeq \left(\frac{3000}{R_{P(\Omega)}}\right) + I_{SB} \text{ mA}$$

with the values of R1 and R2 shown.

If a voltage compliance greater than 40 V is required, or if the regulation of *Figure 8-20a* is insufficient, the configuration in *Figure 8-20b* may be used. It is a precision floating current source capable of 0.05% regulation. In this circuit a floating 20 V supply (typically a half wave rectified output from a separate transformer winding of the main supply) is used to power the µA723, such that standby and reference currents do not add to the programmed output current.

$$I_L = \left(\frac{R2}{R1+R2}\right)\left(\frac{V_{REF}}{R_P}\right).$$

If P1 is adjusted so that V_{R2} = 3.0 V, as indicated in the schematic, then

$$I_L = \frac{3000}{R_{P(\Omega)}} \text{ mA}.$$

Both output current and voltage compliance are limited by the capabilities of the series pass device Q1. Diodes D2 through D4 are protection diodes which should be included whenever V_{IN} exceeds 40 V.

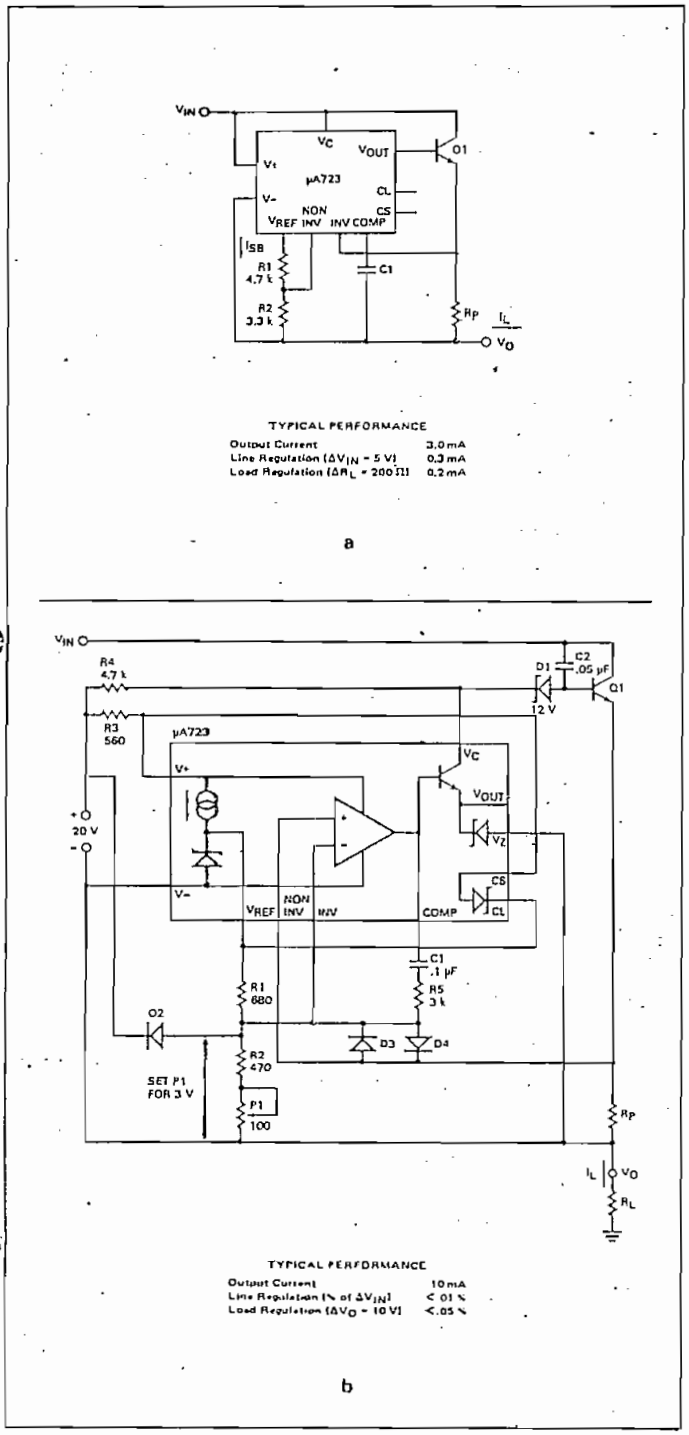


Fig. 8-20 Current Regulators

Precision Voltage Regulator

Figure 8-21 uses the same principle as the previous circuit to give a voltage output capable of 0.005% load regulation. Output voltage range is from zero volts up to the series pass device limit. Output current is also limited only by the series pass device; short circuit protection is available in this configuration by selecting R_{SC} as previously described. Protection diodes D2, D3, and D4 should be added whenever V_{IN} exceeds 40 V.

$$V_O = \left(\frac{R2-R1}{R1}\right)\frac{V_{REF}}{2}$$

With the component values shown, this gives an output voltage range of zero to 100 V.

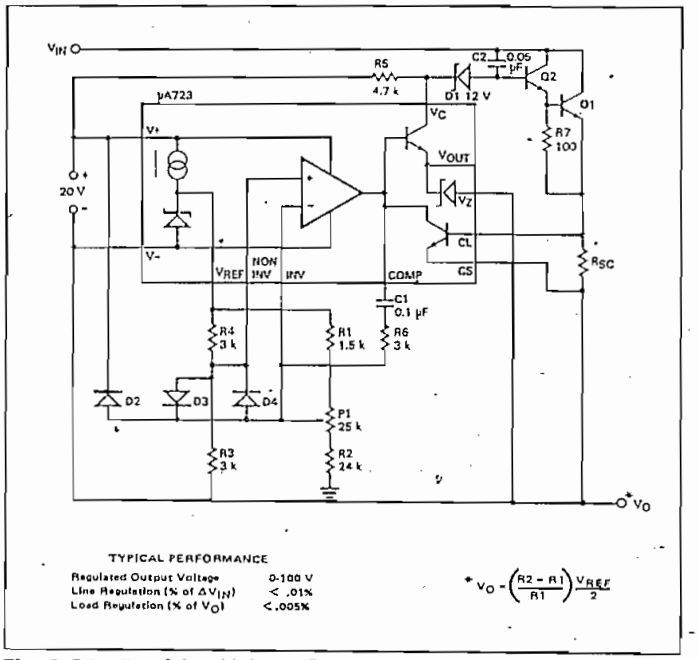


Fig. 8-21 Precision Voltage Regulator

Foldback Current Limiting

Foldback current limiting is a superior alternative to standard current limiting techniques particularly where intolerable output device power dissipation is a problem. Typically, this is a consequence of device/heat sink limitations under short circuit conditions.

In the following discussions it is assumed that a regulated output voltage is available up to a maximum output current I_M. The output current then folds back with decreasing load resistance to a value of I_{SC} (with a short-circuit load). The "knee" of the current limiting characteristic will be similar to that shown in Chapter 7 *(Figure 7-8d* and *h)* for normal current limiting. The regulation degrades considerably as I_M is approached, and in a practical regulator the useful output current may be limited to approximately 80% of I_M.

A minimum parts/cost method for providing the positive feedback required for foldback action is shown in *Figures 8-22a* and *b*. This technique introduces positive feedback by increased current flow through R1 and R2 under short circuit conditions. This forward biases the sensing transistor's base-emitter junction. The final percentage of foldback depends on the relative contributions of the voltage drop across R2, and R_{SC} to the base current of the sensing transistor. In the active region where the voltage buildup of R2 and R_{SC} provides base current to the sensing transistor, recovery of the

full output capability will take place whenever a short circuit is removed from the output. As soon as there is no voltage buildup across R_{SC} providing a portion of the base current, 100% positive feedback has been realized and a reset is required to restore normal operation once the short is removed.

In *Figures 8-22a* and *b,* the input to the current limit transistor is $(V_{RSC} + V_{R2})$, leading to

$$I_{SC} = \frac{V_{SENSE}}{R_{SC}}\left(\frac{R1 + R2}{R1}\right) - \frac{V_{IN}}{R_{SC}}\left(\frac{R2}{R1}\right) \text{ and}$$

$$I_M = I_{SC} + \frac{V_O}{R_{SC}}\left(\frac{R2}{R1}\right)$$

Design equations to give a desired I_M with approximately zero I_{SC} are

$$R1\ (k\Omega) = V_{IN} - V_{SENSE}\ (V)$$
$$R2\ (k\Omega) = V_{SENSE}\ (V)\ (\text{i.e. } R2 = 620\ \Omega)$$

$$\text{and } R_{SC} = \frac{V_O}{I_M}\left(\frac{R2}{R1}\right), \text{ or } R_{SC} = \frac{V_O}{I_M}\left(\frac{V_{SENSE}}{V_{IN} - V_{SENSE}}\right)$$

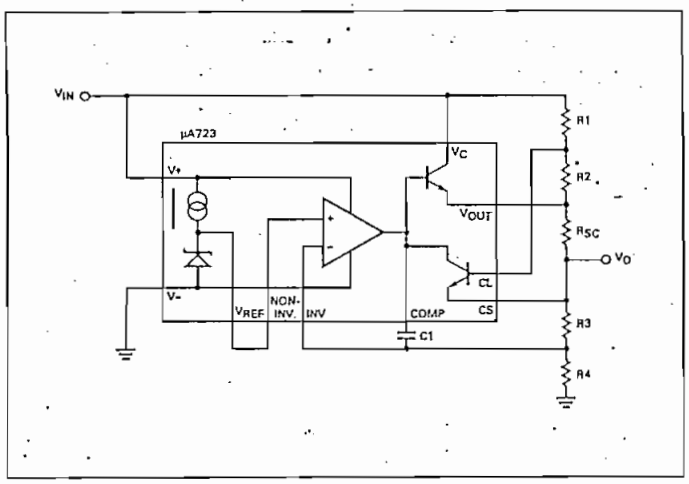


Fig. 8-22a Foldback Current Limiting Positive Regulator

In *Figure 8-22b* it is recommended to use a Darlington configuration for the bypass transistors, Q1 and Q2. This enables R5 to be a relatively high value, typically >50 K, which requires Q3 to sink a low current under short circuit conditions.

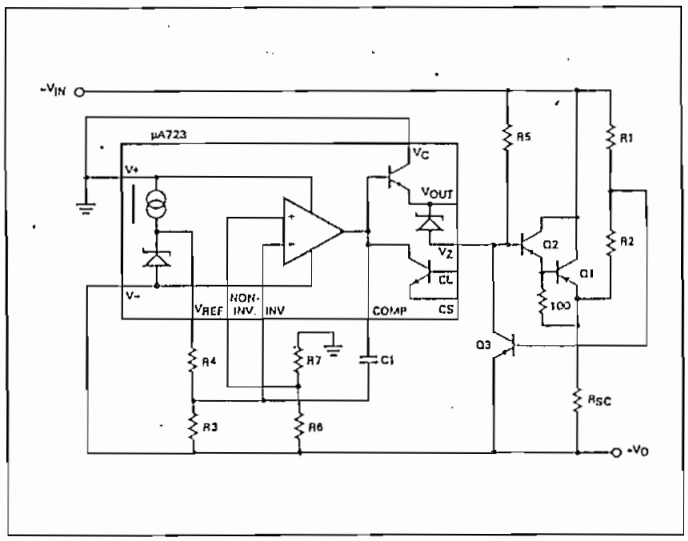


Fig. 8-22b Foldback Current Limiting Negative Regulator

As R5 is reduced the current through it increases drastically when $-V_O$ goes to zero volts, and Q3 base current increases to a point where the foldback circuit is no longer operative.

From the start of base emitter conduction of the sense transistor to the full shut off of the power supply's series pass devices requires a 2 μA base current. This represents a 10 mV increase in base emitter voltage over the base emitter zero current threshold.

The latch condition, or 100% positive feedback, is generated by any change in the input voltage which increases the voltage drop across R2 past the 10 mV window with a short circuit applied, and can only be removed by breaking the positive feedback path by some manual reset to allow the series pass devices to once more be driven in a normal fashion.

The addition of an external transistor Q1 in *Figure 8-22c* provides the same foldback limiting as *Figure 8-22a* but allows the extension of the active recovery region by several times that of the basic approach.

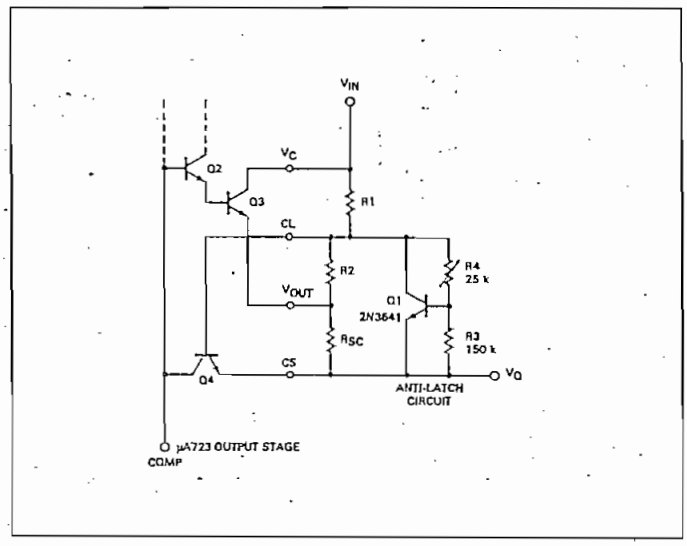


Fig. 8-22c Foldback Current Limiting (Modified)

Latch problems are due to saturation of the current sensing transistor. Because the additional circuitry shown operates as an antisaturation circuit, it bypasses base current above a value set by the voltage divider R3, R4 and the base emitter threshold of Q1. This additional transistor acts as a V_{BE} voltage regulator and, assuming a good thermal link, temperature tracks the threshold changes of the current sensing transistor, tending to keep the foldback current drive at a constant level.

Foldback resistors R1 and R2 are calculated using the equation of *Figure 8-22a*. The 2N3641 used for Q1 was selected for both high base emitter diode conductivity and reasonable Beta at 2 μA collector current.

Final adjustment under short circuit conditions occurs when R4 in *Figure 8-22c* is set just above the point of minimum output current under short circuit load and high ac line operation.

An alternate method of providing foldback current limiting is illustrated in *Figures 8-22d* and *8-22e*. Here, the base of the current limit transistor is fed from a potential divider from V_{OUT} to ground. The input to this transistor now equals $(V_{RSC} - V_{R3})$, which leads to:

$$I_{SC} = \frac{V_{SENSE}}{R_{SC}}\left(\frac{R3 + R4}{R4}\right) \text{ and } I_M = I_{SC} + \frac{V_O}{R_{SC}}\left(\frac{R3}{R4}\right)$$

To determine the resistor values required to give a short circuit current I_{SC} and a maximum output current of I_M, first determine the ratio of R3 to (R3 + R4):

$$\frac{R3}{(R3+R4)} = \alpha = \left(\frac{I_M}{I_{SC}} - 1\right) \quad \frac{V_{SENSE}}{V_O}$$

Now set R4 (kΩ) equal to V_O (V), then

$$R3 = \left(\frac{\alpha}{1-\alpha}\right) R4 \text{ and } R_{SC} = \frac{V_{SENSE}}{I_{SC}} \quad \left(\frac{1}{1-\alpha}\right)$$

Obviously, α must lie between zero (R3→short circuit) and unity (when R4→short circuit). This controls the range of the ratio I_M/I_{SC} such that its upper limit is approximately 1.5 x V_O. For a 5 V regulator, for instance, maximum value for I_M/I_{SC} is about 7.5; for a 12 V regulator it is about 18. This indicates that there is a restriction on obtaining very low short circuit currents with the figures of *8-22d* and *8-22e*. By contrast, note that *Figures 8-22a* and *b* are designed to give approximately zero short circuit current.

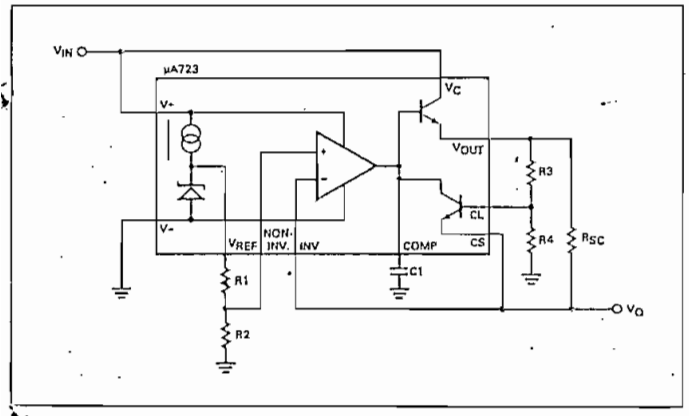


Fig. 8-22d Foldback Current Limiting Positive Regulator (Alternate Method)

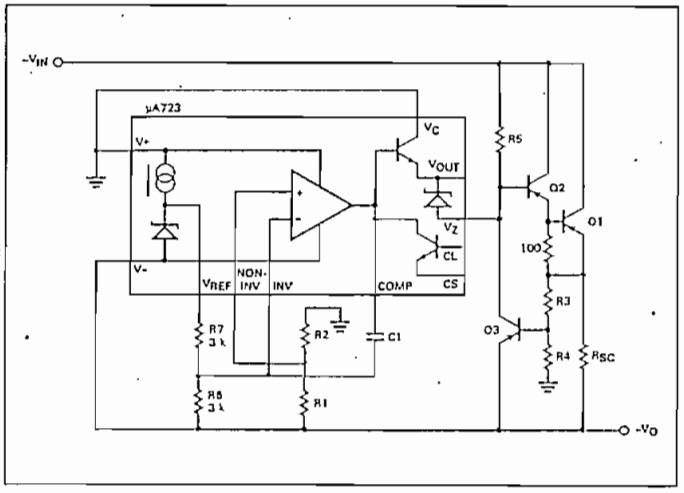


Fig. 8-22e Foldback Current Limiting Negative Regulator (Alternate Method)

Another approach to low power dissipation under short circuit condition is shown in *Figure 8-22f*. This circuit does not follow the decreasing current, decreasing voltage load line which occurs with the standard foldback technique. Instead, under a short circuit, the output voltage decreases in a normal current limiting fashion, i.e., at a constant high output current until the output voltage is below that necessary to keep the FET pinched off. As soon as the output voltage reaches the pinch off voltage, a low impedance path is established around the drivers and the output device, which turns off the compound followers.

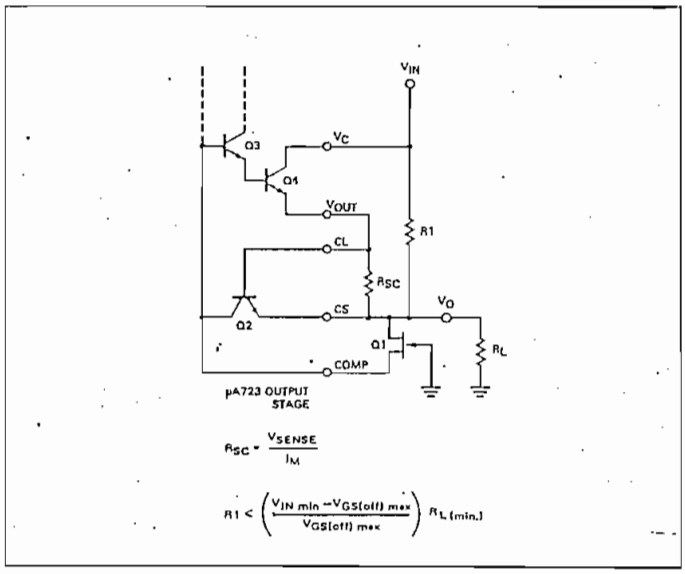


Fig. 8-22f Foldback Current Limiting (FET)

A voltage across the normal load resistor exceeding the pinch off voltage of the FET whenever the short is removed, provides recovery. Bypass resistor R1 supplies this voltage.

The FET should be selected with a maximum pinch off voltage approximately two-thirds the value of V_O. Its minimum pinch off voltage should not be so low as to demand excessive safe area requirements in the μA723 output stage.

Short Circuit Sensing, Low Loss

In high current power supplies, the 0.5 V necessary to sense the current limit point leads to a considerable power loss. In *Figure 8-23* a higher overall power supply efficiency is achieved by requiring a much lower sense voltage. The current limit point is determined by the portion of the μA777s output swing applied as positive feedback, which in turn is determined by the ratio between R1 and R2. In the example shown, the ratio is 1000-to-1. The voltage swing at the output is approximately 13 V, so the sense voltage threshold is 13 mV. When this threshold is exceeded by a voltage developed across R_{SC}, the current sense resistor, the μA777 is driven from its reset state (output high) to its active state (output low), this, in turn, shuts off the power supply by pulling the compensation terminal toward ground. The reset button restores normal operation.

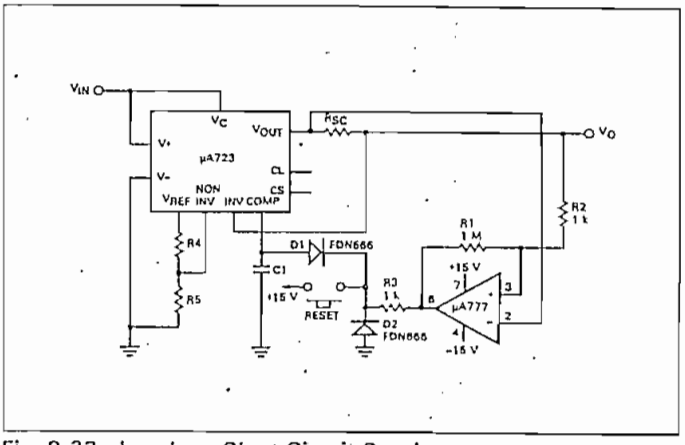


Fig. 8-23 Low Loss Short Circuit Sensing

Short Circuit Sensing, Temperature Stabilized

This circuit modification takes advantage of the internal temperature tracking which occurs in an integrated circuit. Since the current limit transistor and the internal series pass devices are at the same temperature and were fabricated at the same time, their base emitter temperature coefficients will be approximately the same. In *Figure 8-24* the current limit transistor is connected in a manner such that the temperature coefficients cancel. This is accomplished with a bridge circuit via resistors R4 and R5 which reduce the voltage drop (and therefore the temperature coefficient) to a 1 diode drop level. This voltage, appearing across R4, is balanced by an equal and opposite voltage developed across R3 by a FET current source. The current limit transistor is connected across these two voltages, plus the voltage across R_{SC} due to the output current. At room temperature the current source is adjusted by P2 such that there is zero voltage between points A and B. Therefore, at room temperature, the current limit transistor is activated when the µA723 sense voltage is developed across R_{SC}, the voltages across R3 and R4 cancelling each other.

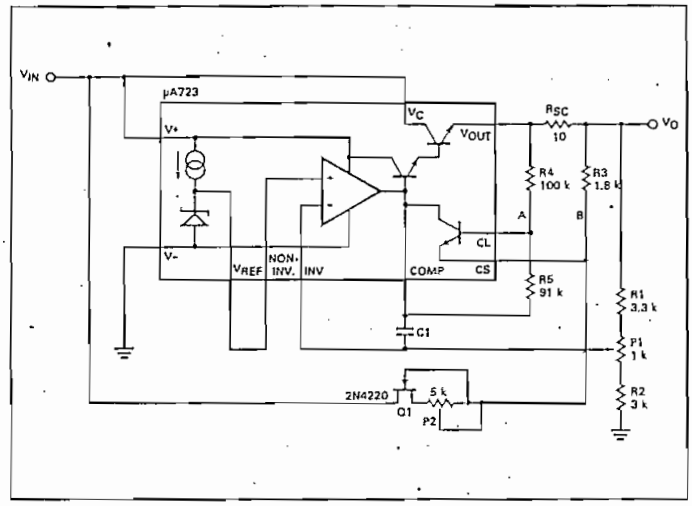


Fig. 8-24 Temperature Stabilized Short Circuit Sensing

The threshold of the current limit transistor will tend to track the voltage across R4 with temperature. Therefore, providing the current source remains constant with temperature, current limit set by R_{SC} also remains constant with temperature.

Figure 8-24 is shown for an output voltage of 15 V from a 25 V unregulated input. A higher breakdown FET will be required for use with higher input voltages.

Remote Shutdown

A µA723 regulator may be turned off by pulling down the compensation terminal, thereby shunting the drive current for the output stage to ground. The simplest method of achieving this in a positive regulator is shown in *Figure 8-25a*. When the current limiting function is required, an external transistor may be substituted (Q1 in *Figure 8-25b).* The logic input may be from any positive voltage source, e.g., TTL or CMOS, capable of driving greater than 100 uA into the CL terminal or Q1 base. Typically, R3 may be 3.0 kΩ from a 5 V TTL system, or 10 kΩ from a 10 V CMOS system.

To protect the output stage from excessive reverse base emitter voltage transients during the shutdown, D1 should be included when the output voltage V_O is greater than 10 V. R4 reduces the peak current that flows when Q1 saturates.

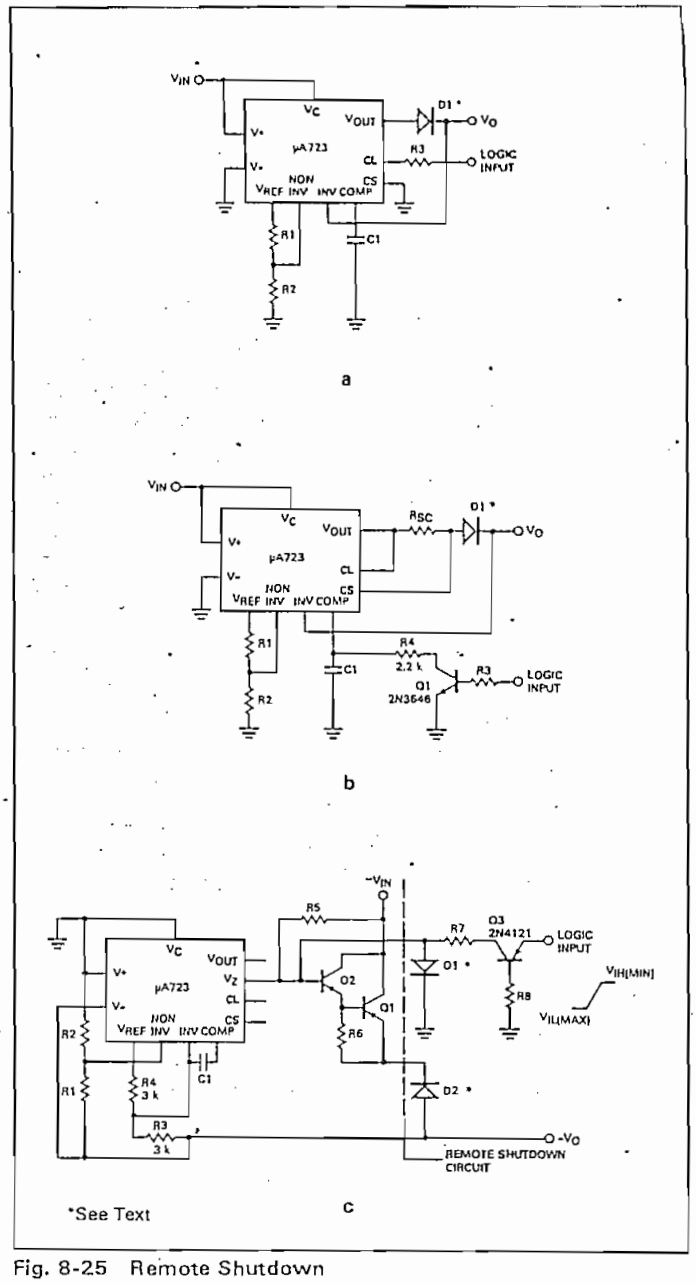


Fig. 8-25 Remote Shutdown

Remote shutdown, when applied to a negative regulator, requires the additional circuitry to the right of the dashed line in *Figure 8-25c*. In operation, a logic Low input, $V_{IL(max)}$, will hold Q3 off, disabling the shutdown circuit. A logic High input, $V_{IH(min)}$, from a TTL or CMOS gate turns Q3 on with the base drive limited by R8. Resistor R5 is calculated in the normal worst case manner for the series pass devices selected.

$$R5 = \frac{(V_{IN(min)} - V_O - 2V_{BE^*})}{Q2I_{B(max)}}$$

*(This term becomes $3V_{BE}$ is D2 is included.)

When Q3 is turned on, D1 is forward biased at a current limited by R7. The ratio of R5 and R7 is calculated such that the output of the supply is always at ground when the logic input is High.

$$\frac{R7}{R5} = \frac{V_{IH(min)}}{V_{IN(max)}},$$

The formula shown guarantees that the junction of R5 and R7 is always positive during shutdown — R8 = 10 R7, to give a forced β of 10 for Q3, fully saturating that device. Diode D2

protects the output devices from reverse base emitter transient voltages, and should be included when the output voltage is greater than the combined base emitter breakdown voltages of the series pass devices.

Overvoltage Crowbar Protection

Figure 8-26 shows a µA723 used as a latched comparator and SCR driver. It also provides the temperature compensated reference necessary for accurate overvoltage sensing. In normal operation, P1 is adjusted so that the voltage at point A is more negative than the reference voltage, V_{REF} (typically 7.15 V). Therefore, the voltage across R2 will bias the comparator (the µA723 error amplifier) such that its output, V_{OUT} is driven toward V–, and the internal 6.2 V Zener diode is cut off. Hence no gate current is able to flow into the SCR D2, which remains in an OFF state. Diode D1 blocks the positive feedback path in this condition, therefore, no current flows through R4.

By "crowbar" action, the comparator changes its state as soon as the voltage across R2 reverses polarity, that is, as soon as the voltage at point A becomes more positive than V_{REF}. Potentiometer P1 is set so that this occurs at the desired overvoltage trip point, typically (V_O + 10%). When the comparator switches, V_{OUT} is pulled up toward V+, and the SCR is fired with gate current limited by R5. When V_{OUT} exceeds V_{REF} the positive feedback loop R4/D1 latches the comparator into its switched state.

The action of firing the SCR places a low impedance across the unregulated supply to ground, and this blows fuse F1. From the initial overvoltage to the SCR clamping takes approximately 1 µs; if required the switching action may be made slower by a capacitor from the µA723 COMP terminal to the inverting input.

Over/Under Voltage Monitoring

There are many systems where it is important that, when the regulated supply lines deviate from their nominal values, an alarm is indicated and some action, such as system shutdown or system changeover, is initiated. Such a fault detection system requires overvoltage and undervoltage monitors for both positive and negative power supplies. The µA723 may be used very effectively in this application and provides a TTL-compatible output signal.

Figure 8-27a gives an indication of an undervoltage on a positive supply line. The internal reference voltage of the µA723, V_{REF}, is used to generate a threshold voltage of 2.0 V across R4. The voltage to be monitored, V_M, is divided down by R_M and R1. The voltage across R1 is compared to the threshold voltage across R4 by the µA723 error amplifier. When V_M is at its nominal value, the output of the µA723 is in its high state, which is set at approximately 3.3 V by clamping the COMP terminal to the junction of R2 and R3 on the V_{REF} voltage divider. Current drain from V_{OUT} through R6 is nominally 15 mA.

If the monitored supply, V_M, should fall by a predetermined amount, the error amplifier changes state, and the output voltage V_O assumes its low state. R6 is able to drive one TTL load (1.6 mA at 0.4 V_{max} V_O). Positive switching action is assured by the hysteresis applied through R5. R_M is adjusted so that the voltage across R1 equals the threshold voltage (2.0 V) when V_M is at the desired undervoltage trip level.

This circuit will give an overvoltage indication on a positive supply line by interchanging the amplifier inputs as shown by the dashed lines.

Figure 8-27b performs the same functions for a negative supply line. The monitored supply voltage, $-V_M$, is referenced to V_{REF} in this circuit, to provide the level shifting from any negative input to the +2.0 V threshold voltage.

Response times for these monitor circuits are typically less than 1 µs.

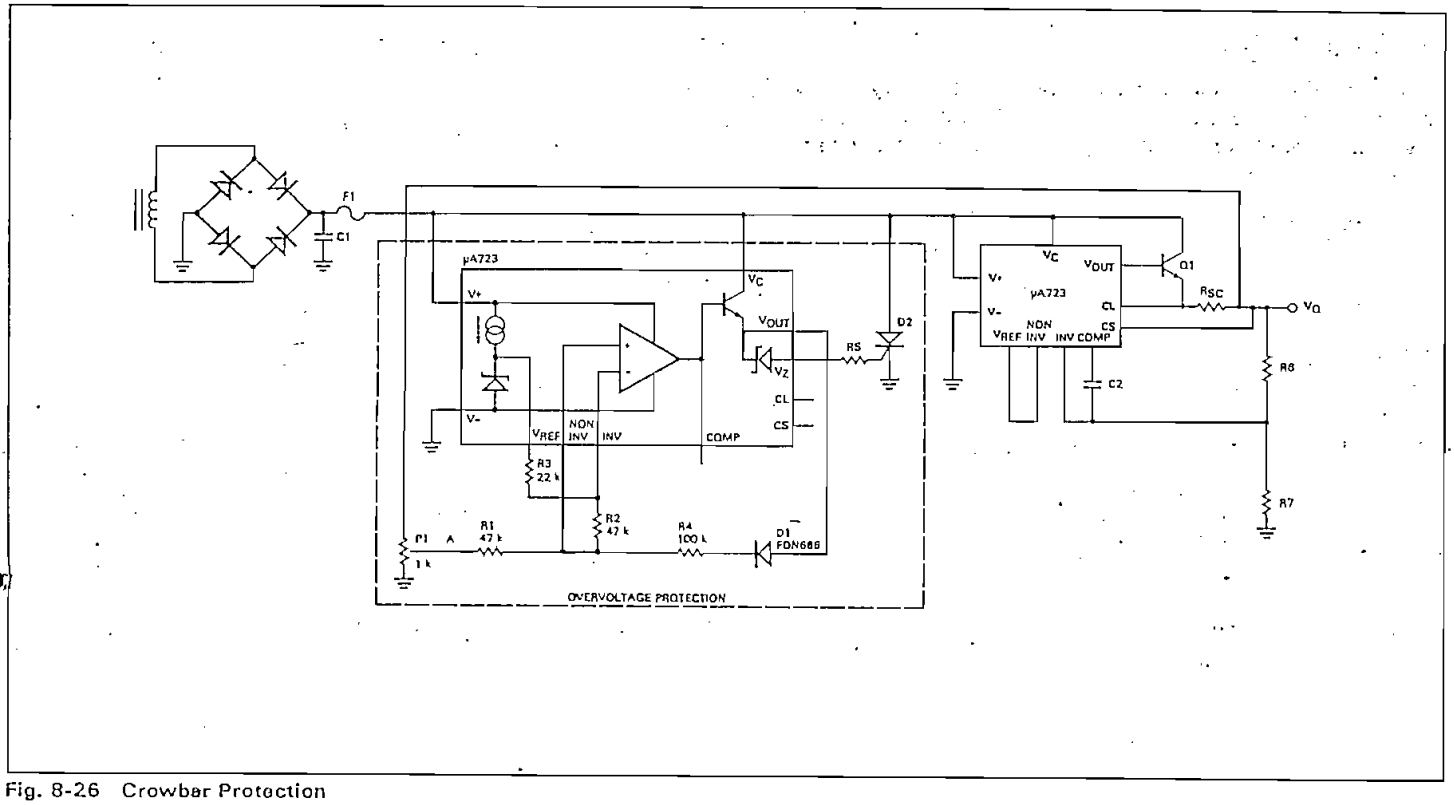


Fig. 8-26 Crowbar Protection

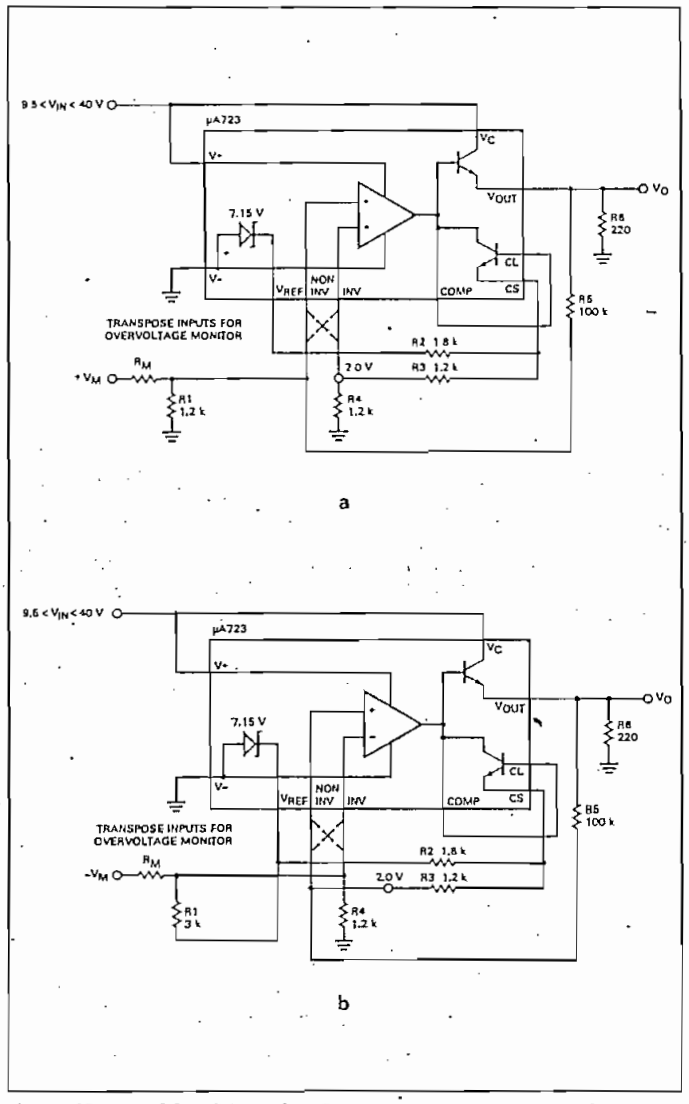


Fig. 8-27 Positive/Negative Supply Undervoltage Monitors

Switching Regulators

Figure 8-28a is a *positive* switching regulator; *Figure 8-28b* is a *negative* output version. The principles of operation of switching regulators and design equations are given in Appendix A.

Referring to *Figure 8-28a* and *Figure 8-28b,*

$$V_O = \left(\frac{R2}{R1+R2}\right) V_{REF}, \quad \text{and} \quad -V_O = -\left(\frac{R1+R2}{R1}\right)\frac{V_{REF}}{2}$$

Other gain setting configurations may be used, such as those used in the linear regulators to extend the output voltage range. R6 *(Figure 8-28a)* limits the base drive to Q2 to approximately 10 mA by using the internal current limit transistor in the μA723.

The efficiency of these circuits is typically 75% at 1 A output current, and 73% at 2 A output current. If the V_Z terminal is not available *(Figure 8-28b),* a 6.2 V Zener diode can be used in series with V_{OUT}. As in the linear negative voltage regulators, the minimum output voltage using this configuration is –9.5 V. Voltages between –2 V and –9.5 V are obtained by supplying a positive voltage to the V+ and V_C terminals such that the range of voltage applied between the V– and V+ terminals is between 9.5 V and 40 V. Values for R4, L1 and C1 are calculated from design information given in Appendix A.

One method of providing short circuit protection for the positive switching regulator is shown in *Figure 8-28c,* a modification of *Figure 8-28a.* The internal current limiting transistor is used to sense the voltage across R_{SC} in the same manner as linear regulators. For output voltages above 5 V, D2 and D3 should be added to protect the error amplifier input stage from excessive voltages during output short circuit conditions.

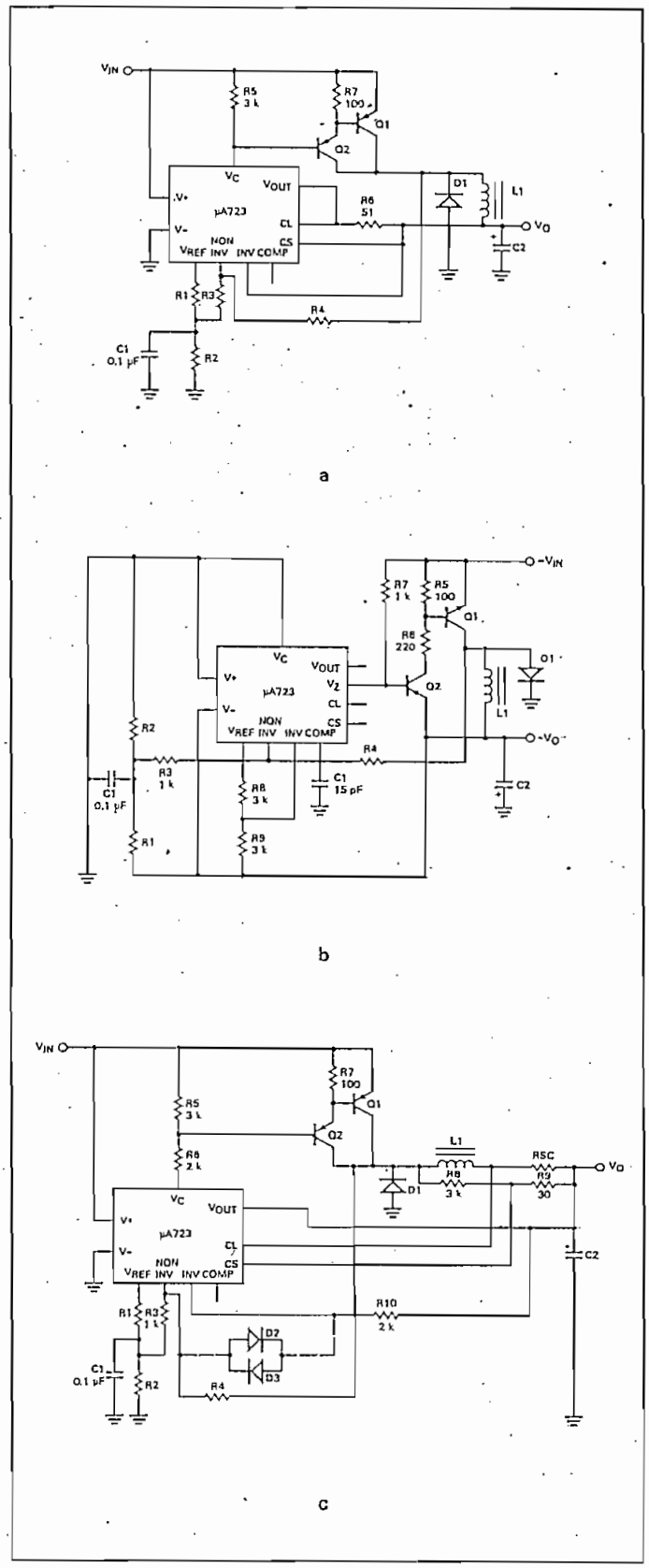


Fig. 8-28 Switching Regulators

The voltage necessary to turn on the current limiting transistor is the sum of V_{SENSE} (the V_{BE} of the current limiting transistor) and the voltage across R9. Then, as shown in the formula below,

$$V_{RSC} = V_{SENSE} + (V_{IN} - V_O)\left(\frac{R9}{R8 + R9}\right), \text{ and}$$

$$I_{LIMIT} = \left(\frac{V_{SENSE}}{R_{SC}}\right) + \frac{(V_{IN} - V_O)}{R_{SC}}\left(\frac{R9}{R8 + R9}\right)$$

R8 and R9 are included to supply positive feedback and, hence, maintain switching action even under short circuit conditions. This prevents over-dissipation if the regulator were allowed to go into a linear mode. Typically, R8 may be 3 kΩ and R9 30Ω so that to a first approximation, current limit is derived as follows:

$$I_{LIMIT} = \left(\frac{V_{SENSE}}{R_{SC}}\right) + \frac{(V_{IN} - V_O)}{100\ R_{SC}}$$

OUTPUT VOLTAGE	APPLICABLE CIRCUITS	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10%			OUTPUT VOLTAGE	APPLICABLE CIRCUITS	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10%		
	(Note 1)	R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
3.0	8-8 a,b (8-9a)8-9b	4.12	3.01	1.8	0.5	1.2	100	8-13	3.57	102	2.2	10	91
3.6	8-10	3.57	3.65	1.5	0.5	1.5	250	8-21	3.57	255	2.2	10	240
5.0	8-11b (8-12)	2.15	4.99	.75	0.5	2.2	−6 (Note 2)		3.57	2.43	1.2	0.5	.75
6.0	8-15 8-28a	1.15	6.04	0.5	0.5	2.7	−9	8-16	3.48	5.36	1.2	0.5	2.0
9.0	8-8c	1.87	7.15	.75	1.0	2.7	−12	8-17 8-18	3.57	8.45	1.2	0.5	3.3
12	8-9a(8-9b) (8-10)	4.87	7.15	2.0	1.0	3.0	−15	8-28b	3.65	11.5	1.2	0.5	4.3
15	8-11a 8-12 (8-28a)	7.87	7.15	3.3	1.0	3.0	−28		3.57	24.3	1.2	0.5	10
28		21.0	7.15	5.6	1.0	2.0	−45		3.57	41.2	2.2	10	33
45	8-13	3.57	48.7	2.2	10	39	−100	8-19	3.57	97.6	2.2	10	91
75	8-21	3.57	78.7	2.2	10	68	−250		3.57	249	2.2	10	240

NOTES:
1. Circuits in parenthesis may be used if R1/R2 divider is placed on opposite side of error amplifier.
2. V^+ must be connected to a +3.5 V or greater supply.

Table 8-1 Resistor Values for Standard Output Voltages