7

Changing Wafer Size and the Move to 300mm

7 Changing Wafer Size and the Move to 300mm

As discussed in Chapter 1, the industry's ability to increase productivity by 25-30 percent per year is the combined result of wafer size transitions, shrinking device geometries, equipment productivity improvements, and incremental yield improvements. Wafer size transitions historically account for 4 percent of the 25-30 percent productivity gain.

Companies make wafer size transitions because of the overall cost benefits resulting from the larger number of dice per wafer, thereby using the same number of process steps to produce more dice. Based on historical trends, peak demand for 200mm wafers will be reached around 2003, as shown in Figure 7-1. In addition, this SEMATECH study[1] indicates that each wafer size remains in production for approximately 24 years – allowing companies sufficient time to recoup investments in the technology.

This lifecycle perspective can be used as a guide as the industry makes transitions to larger wafers. By the year 2000, the first processing on 300mm (12 inch) wafers is anticipated. 300mm wafers will accommodate roughly twice as many dice per wafer as 200mm wafers. Driving forces for all wafer size transitions include the factors of ever-increasing die size and increasing numbers of integrated functions per chip. Less obvious, yet no less important factors such as increasing global competition, 200mm installed base and market conditions are influencing the rapidity with which 300mm silicon wafers will become manufacturing-worthy and cost effective. Today, while manufacturers in the silicon world are making 150 to 200mm transitions and evaluating 300mm processing, many GaAs manufacturers are undergoing or considering transitions to 150mm processing from 100mm. The relative wafer sizes are shown in Figure 7-2.

Upgrading to a New Wafer Size

Wafer size increases can also be viewed in terms of percentage increase in wafer area, as shown in Figure 7-3. Interestingly, the move from 100mm (4 inch) wafers to 150mm (6 inch) wafers increased the silicon area by 125 percent — the same relative gain that will be realized when semiconductor companies make the transition from today's 200mm (8 inch) wafers to 300mm (12 inch). Beyond 300mm, the same gain requires a jump to 450mm wafers. Trends indicate that wafer size transitions industry-wide have typically enabled a 4 percent per year productivity improvement, and the transition to 300mm should provide between 2 and 4 percent per year lower IC cost/cm^2.[1]

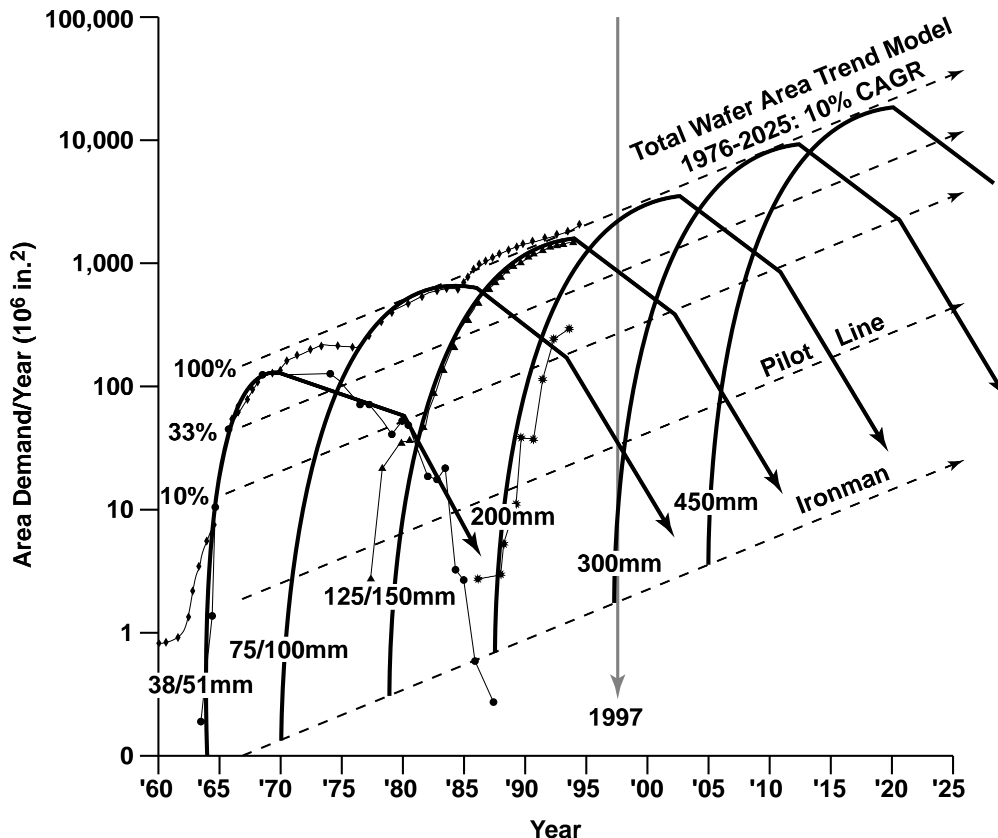


Figure 7-1. Lifecycles of Different Wafer Sizes

Figure 7-4 illustrates the number of dice per wafer based on wafer size and die size, while Figure 7-5 can be used for more precise calculation of the maximum number of dice per wafer. Unfortunately, due to equipment productivity and price increases for larger wafer processing tools, the cost savings resulting from wafer size transitions may not scale with these die per wafer calculations. For instance, 200mm wafers offer nearly twice the area of 150mm wafers (1.78X), but many early adopters of 200mm technology argue that this transition did not result in twice as many chips produced for the same manufacturing costs. In fact, if the cost of owning and operating 200mm equipment is twice as high as the 150mm equipment, then the manufacturing cost (per square centimeter of silicon) is the same. In this case, the cost savings only results from the need for less than twice as many pieces of equipment to process the larger wafers. For these reasons, the question of whether or not a fab can cost-effectively make wafer size transitions depends greatly on the utilization and efficiency of the wafer processing equipment.

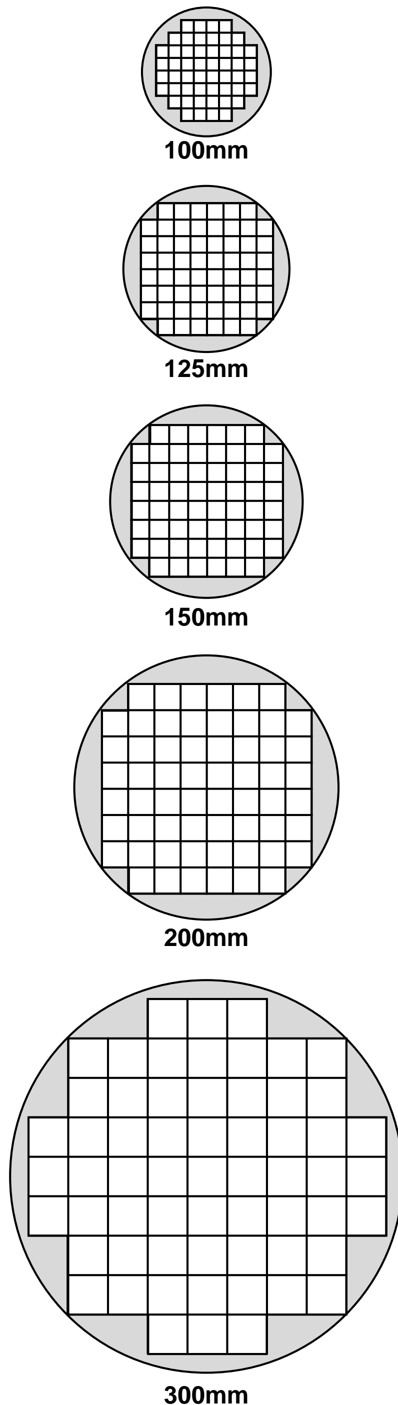


Figure 7-2. Relative Difference in Wafer Sizes

Evaluating the Cost Benefits of 150 to 200mm Transitions

In making wafer size transitions, generally speaking, only a percentage of tools can be used to process subsequent wafer sizes. Interestingly enough, many fabs and equipment manufacturers anticipated making small modification to equipment when making transitions from 100mm to 125mm or 125mm to 150mm wafer processing. In reality, only 40-50 percent of the systems were transferable; equipment needed to be redesigned, and usually new equipment sets were needed. When making transitions from 150mm to 200mm wafer processing, only a handful of systems can be used on both sizes. It is anticipated that none of the 200mm processing systems will be used to process upcoming 300mm wafers.

As users might expect, transitions in wafer size require complete evaluations of cost factor differences for each different process tool in the fab. A simplified cost-of-ownership (COO) study of 150mm versus 200mm wet benches performed by Intel[2] revealed that the top four contributors to COO are significantly different for 200mm and 150mm wet cleaning equipment (Figure 7-6). Deionized (DI) water costs, capital costs, consumable costs and facilities costs dominated 200mm benches while capital, facilities, monitor wafer, and DI water costs dominated for 150mm systems. Most significantly, DI water, in going from 150 to 200mm wafer processing, jumps from being the fourth highest cost factor to the first. This difference is primarily due to the tripling of flow rates needed to achieve equivalent rinsing of the 200mm batch. Interestingly, while the test wafer cost rose from $35 to $135, its impact on COO lessened because the monitoring frequency stayed constant between the two wafer sizes.

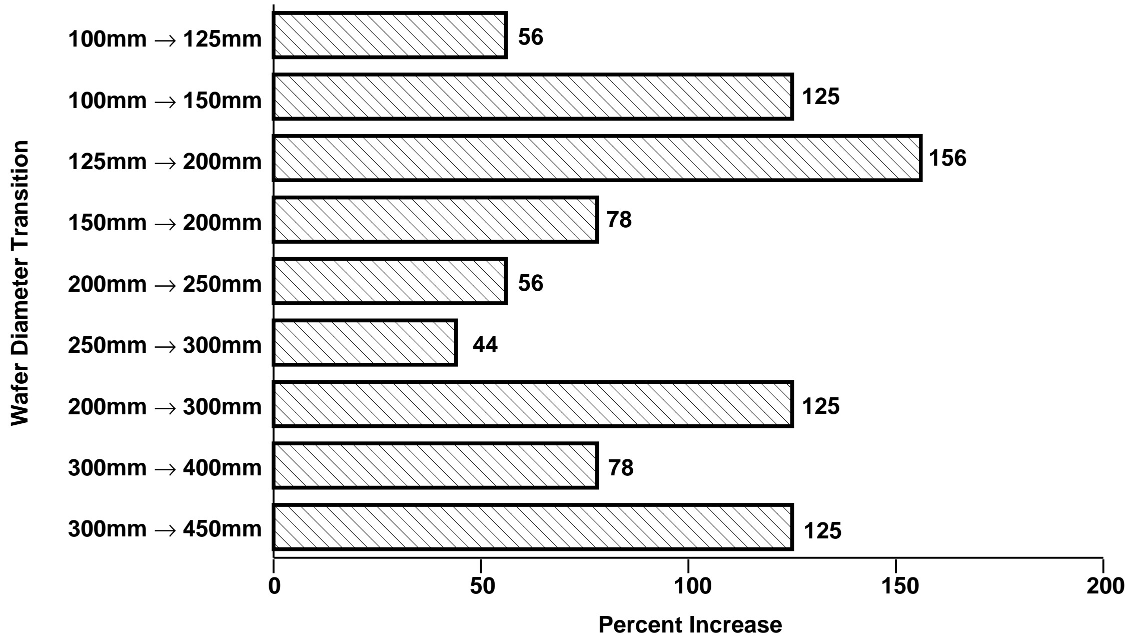


Figure 7-3. Wafer Area Increases (Percent)

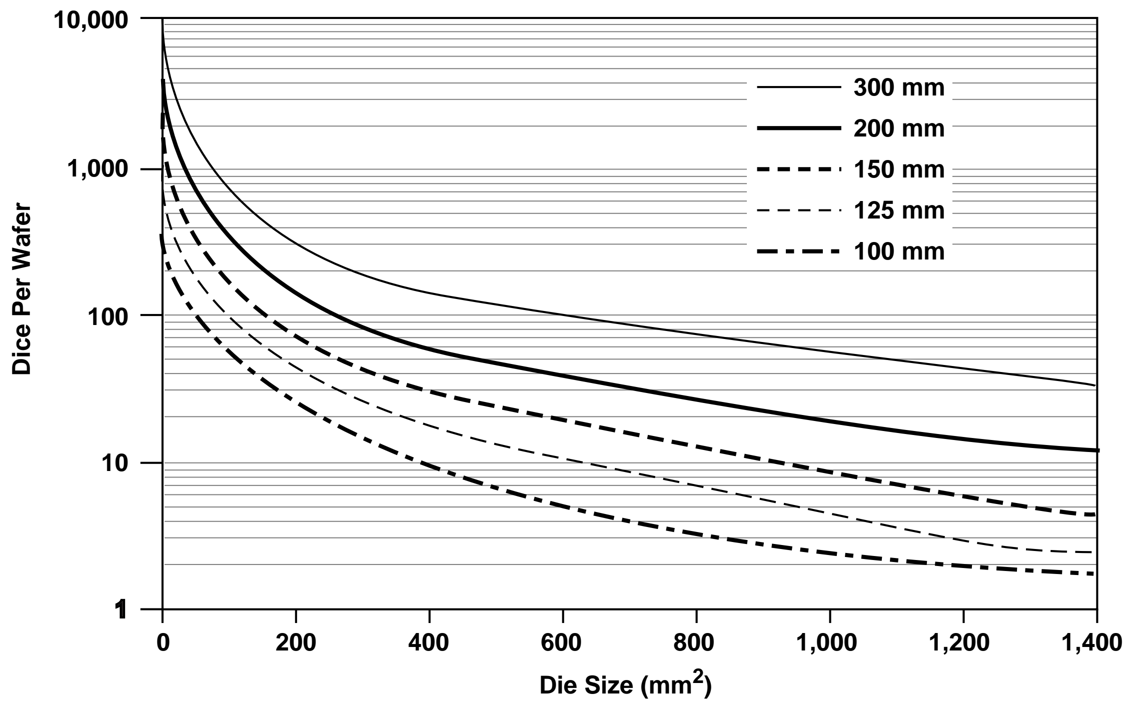


Figure 7-4. Dice Per Wafer Based on Die Size and Wafer Size

DIE SIZE** √AREA		DIE AREA		CANDIDATE NUMBER OF WHOLE DICE					
mils	mm	mil² x1,000	mm²	3-INCH	100mm	125mm	150mm	200mm	300mm
300	7.6	90.0	58.1	52	96	156	240	448	1,060
310	7.9	96.1	62.0	44	88	148	224	424	1,012
320	8.1	102.4	66.1	44	80	140	208	392	936
330	8.4	108.9	70.3	40	76	120	192	376	880
340	8.6	115.6	74.6	32	76	120	188	340	820
350	8.9	122.5	79.0	32	68	112	164	332	780
360	9.1	129.6	83.6	32	60	112	156	308	732
370	9.4	136.9	88.3	32	52	96	148	292	688
380	9.7	144.4	93.2	32	52	96	148	268	656
390	9.9	152.1	98.1	24	52	88	140	256	616
400	10.2	160.0	103.2	24	52	80	120	248	600
410	10.4	168.1	108.5	24	52	80	120	240	556
420	10.7	176.4	113.8	24	44	76	112	216	540
430	10.9	184.9	119.3	24	44	76	112	208	508
440	11.2	193.6	124.9	16	40	68	104	208	492
450	11.4	202.5	130.6	16	32	68	96	188	460
460	11.7	211.6	136.5	16	32	60	96	188	440
470	11.9	220.9	142.5	16	32	52	88	180	432
480	12.2	230.4	148.6	16	32	52	88	164	392
490	12.4	240.1	154.9	12	32	52	80	156	392
500	12.7	250.0	161.3	12	32	52	76	148	376
510	13.0	260.1	167.8	12	32	52	76	148	356
520	13.2	270.4	174.5	12	24	52	76	148	340
530	13.5	280.9	181.2	12	24	44	68	132	332
540	13.7	291.6	188.1	12	24	44	68	120	316
550	14.0	302.5	195.2	12	24	40	68	120	308
560	14.2	313.6	202.3	12	24	40	60	120	292
570	14.5	324.9	209.6	12	24	32	52	112	284
580	14.7	336.4	217.0	12	24	32	52	112	268
590	15.0	348.1	224.6	12	16	32	52	112	256
600	15.2	360.0	232.3	12	16	32	52	104	256
610	15.5	372.1	240.1	12	16	32	52	96	248
620	15.7	384.4	248.0	4	16	32	52	96	240
630	16.0	396.9	256.1	4	16	32	52	88	224
640	16.3	409.6	264.3	4	16	32	44	88	216
650	16.5	422.5	272.6	4	16	24	44	88	208
660	16.8	435.6	281.0	4	12	24	44	80	208
670	17.0	448.9	289.6	4	12	24	40	80	200
680	17.3	462.4	298.3	4	12	24	40	76	188
690	17.5	476.1	307.2	4	12	24	32	76	188
700	17.8	490.0	316.1	4	12	24	32	76	180
710	18.0	504.1	325.2	4	12	24	32	68	180
720	18.3	518.4	334.5	4	12	24	32	68	164
730	18.5	532.9	343.8	4	12	24	32	68	164
740	18.8	547.6	353.3	4	12	16	32	68	156
750	19.0	562.5	362.9	4	12	16	32	60	156
760	19.3	577.6	372.6	4	12	16	32	60	148
770	19.6	592.9	382.5	4	12	16	32	52	148
780	19.8	608.4	392.5	4	12	16	32	52	148
790	20.1	624.1	402.6	4	12	16	24	52	148
800	20.3	640.0	412.9	4	12	16	24	52	132
810	20.6	656.1	423.3	4	12	16	24	52	132
820	20.8	672.4	433.8	4	12	16	24	52	120
830	21.1	688.9	444.5	4	4	12	24	52	120
840	21.3	705.6	455.2	4	4	12	24	52	120
850	21.6	722.5	466.1	4	4	12	24	52	120
860	21.8	739.6	477.2	4	4	12	24	44	112
870	22.1	756.9	488.3	4	4	12	24	44	112
880	22.4	774.4	499.6	4	4	12	24	44	112
890	22.6	792.1	511.0	4	4	12	24	44	112
900	22.9	810.0	522.6	4	4	12	16	40	112
910	23.1	828.1	534.3	4	4	12	16	40	104
920	23.4	846.4	546.1	4	4	12	16	40	96
930	23.6	864.9	558.0	4	4	12	16	32	96
940	23.9	883.6	570.1	4	4	12	16	32	96
950	24.1	902.5	582.3	4	4	12	16	32	88
960	24.4	921.6	594.6	4	4	12	16	32	88
970	24.6	940.9	607.0	4	4	12	16	32	88
980	24.9	960.4	619.6	—	4	12	16	32	88
990	25.1	980.1	632.3	—	4	12	16	32	80
1,000	25.4	1,000.0	645.2	—	4	12	12	32	80

* Corner of die at center of full radius wafer.
3mm band around edge of wafer not used.
** Size after die separation, 3 mil saw kerf.

Source: ICE

22673

*Figure 7-5. Die Size Versus Die Count**

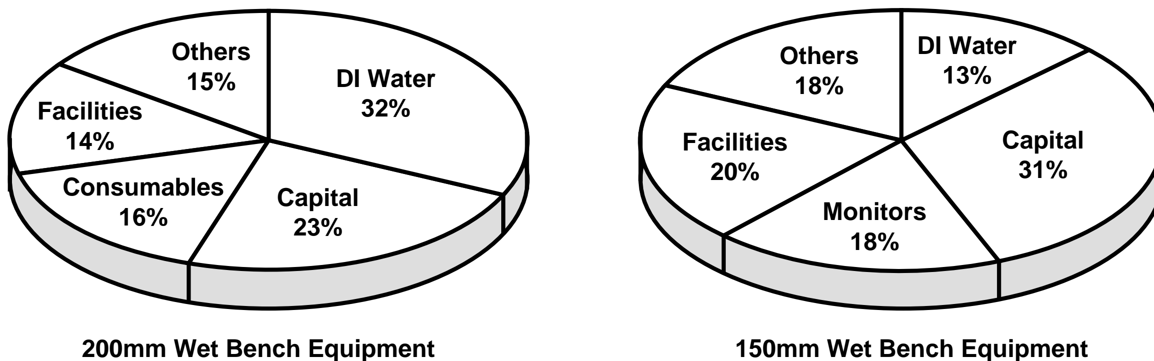


Figure 7-6. Components of Operating Costs of 200mm and 150mm Wet Benches

Studies like this and others can be used to target key areas for cost reduction in 200mm fabs. In this example, the authors cited possible reductions in bath volume through cassette or cassette-less processing (which would bring DI water and consumables costs down), or the use of hot DI water or sonic energy rinses to reduce rinse times. Operating costs can be reduced by optimizing the system for higher throughput and utilization. For instance, an increase of 10 wafers per hour throughput or 5 percent utilization would reduce the 200mm COO by 13 to 15 cents. Initial cost of the wet bench would have to be reduced by $500,000 to have an equivalent impact.[2] Many of the current 200mm wafer cleaning systems feature reduced use of DI water and chemicals, smaller tool footprint, increased system availability, and higher throughputs.

In summary, the factor affecting cost savings the most in wafer size transitions is the relative cost-effectiveness of the equipment used to process the two wafer sizes. Users making the transition must weigh the added cost of next-generation equipment and possibly lower throughput and productivity (especially with single-wafer systems) versus the long-term benefits of more dice per wafer, assuming that the same or better yields can be realized on the larger wafers. Understanding such differences, it comes as no surprise to learn that the transition from 150mm to 200mm processing occurred the slowest of any transition, requiring 5 years to reach 100 million square inches of production instead of 3 years in the case of 150, 125 and 100mm wafers.[3] 200mm processing tools first became available in the late 1980s, and approximately a decade later about a third of all wafers shipped are 200mm.

The Promise of 300mm Wafers

As of early 1997, seven IC manufacturers were planning 300mm pilot line operations for 1998, and anticipating production ramp-up in 1999. These firms include:

- Hitachi
- IBM
- Intel
- Motorola
- NEC
- Samsung
- Texas Instruments

Beyond these early indications, TI has announced its intention to install a 300mm line at its plant in Avezzano, Italy; Sony plans to build a line in Nagasaki Prefecture, Japan; and Intel, Mitsubishi, Toshiba and Siemens also intend to build pilot line 300mm fabs in the 1998-1999 time frame. SEMI estimates that low and medium volume fabs will emerge by the year 2000 and high volume 300mm fabs (starting 20,000 wafer per month) will soon follow (see Figure 7-7). The first devices produced on these wafers will probably be high-margin advanced logic chips (DSPs, ASICs, FPGAs, PLDs) and microprocessors, probably 0.18µm generation devices, while memory manufacturers are expected to trail in 300mm adoption due to low margins experienced over the last year and a half.

Semiconductor manufacturers have unquestionably stated that 300mm development will not be performed solely by the IC manufacturers, as they were in previous generations with Intel enabling the transition to 150mm and IBM managing the transition to 200mm. In the case of 300mm, the technical challenges are so involved that they require an unprecedented level of industry-wide cooperation.

Many sources estimate the industry's overall cost of making the transition to 300mm wafers at between $15 and $20 billion. This includes development of the tools and techniques for making the wafers, development costs of all the wafer processing and handling tools, all computer integrated manufacturing (CIM) software, factory automation tools, and cleanroom technology. Development costs for 300 or 400mm equipment are estimated by Applied Materials to be at least 1.4 to 1.7X the cost of developing new 200mm systems. Possibly $50 to $100 million or more in development costs for each process technology step will be needed. Samsung estimates that a 20,000 wafer per month 300mm line will cost approximately $2.4 billion, and will require a 12,000m^2 cleanroom (130,000ft^2), while a 30,000 wafer per month fab will cost approximately $3.6 billion, requiring 18,000m^2 (200,000ft2) of cleanroom space.

Early studies by SEMATECH estimated that 300mm tool costs would increase by 50 percent over 200mm, tool throughput would be reduced by 40 percent. Starting wafer cost would be decreased by 30 percent per unit as estimated by VLSI Research (Figure 7-8).

Fab Size (Wafers per Month)	1998	1999	2000	2001	2002
High Volume (20,000)	—	—	5	4	2
Medium Volume (10,000)	—	1	4	—	1
Low Volume (2,000)	2	5	—	—	—
Pilot Line (500-1,000)	9	5	—	—	—

Source: SEMI 22665

Figure 7-7. Planned 300mm Wafer Fabs

Today industry experts are much more confident that these costs can be brought down with TI's Robert Doering estimating a 20-40 percent increase in tool cost, 3-14 percent more dice per wafer (based on lower edge loss for larger chips), and an overall reduction in cost per chip of 27-39 percent, as shown in Figure 7-9.[4] In addition, TI estimates that labor cost, materials use and emissions should be comparable between the two wafer sizes and that higher yields may be possible. As of 1Q '97, prime 300mm were as high as $1,500 but are expected to drop to $650-$800 each in volume.

A 300mm test wafer is shown in Figure 7-10. One industry participant estimated that possibly over 40,000 test wafers will be required to validate equipment in 1997 alone. Bringing down the starting wafer cost is absolutely critical. Intel has stated that the 300mm cost per wafer cannot exceed 200mm cost per wafer. To meet this, higher throughputs on all tools is required and the utilization of chemicals and materials must be increased (dramatically in some cases), including that of ultrapure DI water.

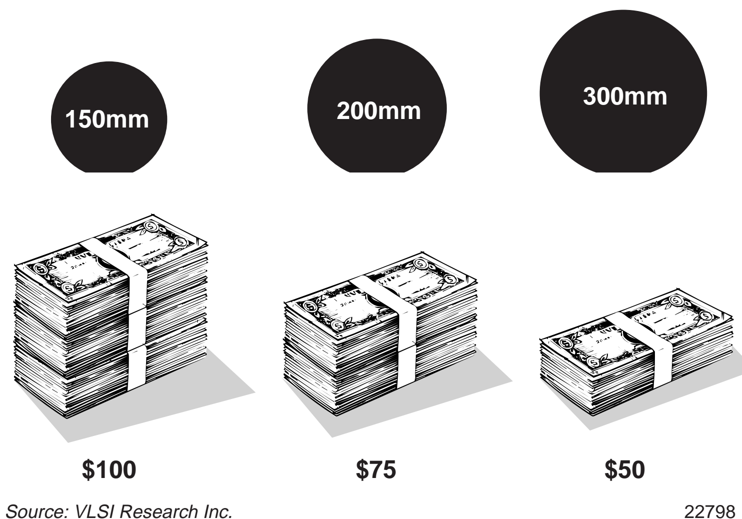


Figure 7-8. Cost/Unit of Silicon

Cost Per Square cm	25 - 30% Less
Usable Portion of Wafer	3 - 14% More
Cost Per Chip	27 - 39% Less
Labor	About Equal
Tool Capital Cost	20 - 40% More
Materials Use	About Equal
Emissions	About Equal
Process/Probe Yield	Slightly Better

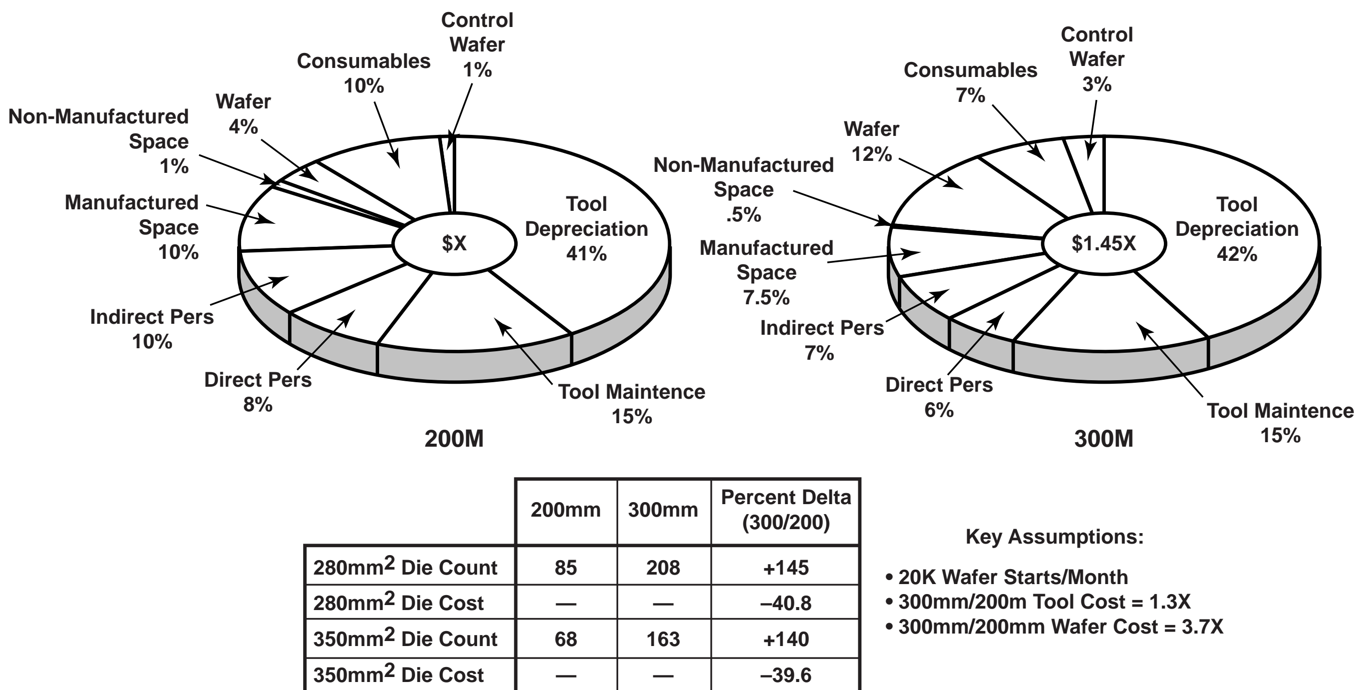
Source: Texas Instruments 22623

Figure 7-9. 300mm Versus 200mm at Maturity

Source: MRS Technology 22622

Figure 7-10. A 300mm Test Wafer

Although the issues raised by the prospect of conversion to 330mm are multifaceted, the motivation is clearly economic rather than technical. At the 2nd annual global 300mm symposium[6] held in June of 1997, Motorola's Manufacturing Technology Development presented a comparison of 256M DRAM die cost on 200mm and 300mm wafers showing a 40 percent lower die cost assuming comparable sized fabs (Figure 7-11). Even with downsizing the 300mm fab to equalize die output, they predict a die cost savings of between 25-30 percent.



	200mm	300mm	Percent Delta (300/200)
280mm2 Die Count	85	208	+145
280mm2 Die Cost	—	—	–40.8
350mm2 Die Count	68	163	+140
350mm2 Die Cost	—	—	–39.6

Source: Motorola MTD 22772

Figure 7-11. 256M DRAM Die Cost Analysis

300mm Development

The development of 300mm processing capability is primarily taking place in Austin, Texas, and Yokohama, Japan.

In early 1996, a cooperative venture was formed between 10 Japanese firms to assess and improve 300mm wafer quality, and to evaluate 300mm wafer processing equipment. Companies involved in the venture include NEC, Toshiba, Hitachi, Fujitsu, Mitsubishi, Matsushita, Oki, Sanyo, Sharp, and Sony. Wafer standards are being developed by a working group including representatives from the EIAJ, JEIDA, SIRIJ, Japan Society of Newer Metals, and SEAJ. The group is testing 10-15 wafer processing systems at its lab in Yokohama, and is expected to have received 60 systems by the end of 1997, including a 248nm stepper from Canon. The SELETE organization is expected to spend roughly $350 million between 1996 and 2000, and between SELETE, the Japan Working Group for 300mm Technology and the Association of Super-advanced Electronics Technologies, approximate funding is $550million (60 billion yen) over five years.

Meanwhile, a parallel effort was organized among U.S., European, Korean, and Taiwanese firms, the International 300mm Initiative (I3001). Participants include Intel, Motorola, Lucent Technologies, Texas Instruments, IBM, AMD, Siemens, SGS-Thomson, Philips, Samsung, Hyundai, LG Semicon, and TSMC. Both groups target late 1997 or early 1998 for first 300mm wafer use, and first production on 0.25µm or 0.18µm generation of devices (256M and 1G DRAMs, respectively).

I3001 anticipates having 70-80 wafer processing tools tested and qualified by the end of 1998. Initially funded at $26 million ($2 million from each of its 13 members), I3001's 18-month program goals include:

- providing inputs to international standards activities,
- developing consensus on performance metrics and demonstration methods,
- demonstrating 300mm equipment/materials for 0.25µm processing,
- defining a program by mid-1998 for demonstrating and qualifying 0.18µm equipment, which will be performed through 2000.

Over 30 pieces of equipment will begin demonstration in SEMATECH's lab in Austin in 1997. These tools are manufactured from a number of different vendors worldwide including ADE, Applied Materials, JEOL, Kokusai, Leica, Lumonics, Mattson, Schmitt Measurement, SCP, SEZ, Tencor, TEL and Verteq.

Equipment Developments

Some of the equipment-level developments in 300mm processing include the following:

- AET Thermal shipped an RTA system to MEMC
- Applied shipped its first 300mm RTP system to Hyundai
- Empak announced its first front-opening pod
- Equipe Technologies developed a vacuum cluster tool platform
- Horiba developed an interferometer-based wafer flatness tester
- Kokusai Electric has prototyped a 300mm diffusion furnace

- Nanometrics installed a thin film metrology tool at SELETE's lab
- PRI Automation developed a tool that loads wafer carriers to and from a load port, first integrated on Eaton's and STEAG's tools
- SubMicron Systems is developing a 300mm automated wet station
- Tokyo Seimitsu and Kulicke & Soffa are developing a 300mm dicing machine

Standards

Standardization of many tool-specific issues should reduce 300mm capital equipment cost significantly. As summarized in The Production Cost Savings Forum Report[5], lack of standardization in the industry on non-competitive parts of the wafer processing systems typically leads to capital cost increases of up to 2X the base system cost. For this reason, such standards are being developed for 300mm processing with many of the issues are summarized in Figure 7-12.

Sputtering challenges include step coverage of barrier metals and the ability to fill higher aspect ratio holes uniformly. Bringing down the cost of high energy ion implanters will increase the likelihood that its brought into the fab, while low current challenges for shallower source and drain junctions remain a challenge. The industry has identified exposure tools and defect detection tools as being two of the most significant challenges for 300mm processing. Stepper performance (depth of field, overlay and resolution) of 248nm tools is the primary concern, followed by reliability of the system and excimer laser, stage speed and accuracy, and vibration control. Efficient in-situ monitoring and cleaning processes are needed for CVD multi-chamber systems in addition to the accommodation of new materials in both CVD and etch. Small batch (also called mini-batch) systems are being considered for wafer cleaning and furnace processes.

Beyond the processing equipment, factory automation in a 300mm fab is critical. In particular, a lack of standards for automated production and handling systems exists. The industry must also standardize the way that process tools and handlers interface with the carrier. Currently both open and closed carriers are being considered.

Most believe that the transitional lot size of 24 wafers would not be manageable beyond 200mm processing. Thirteen wafer lots and smaller are being considered. Ergonomic issues become critical at 300mm and larger wafer sizes. For instance, 150mm wafers are 0.675mm thick and weigh about 30 grams, while 200mm wafers have a thickness of 0.725mm and weigh 50-60 grams. The proposed new 300mm wafer will be approximately 0.800mm thick, weighing about 140 grams. The automation needed to move batches of 300mm wafers will be costly. This is an issue that many Japanese and other IC manufacturers realized early in 200mm processing, and many U.S. manufacturers are beginning to understand as they implement automation to improve the efficiency of today's 200mm fabs. Even so, 200mm processing equipment has no standard equipment interface and there are multiple differences in loading height, depth and direction by equipment manufacturer and equipment type.

	Type		Comment	
	Batch	Single Wafer	Device Manufacturer	Equipment Manufacturer
Sputterer	—	7 Device Manufacturers	• Less particles/higher coverage and better filling • Sputtering in finer, higher aspect ratio holes • Less contamination, residues • Establishment of chamber monitoring technologies (stage temperature uniformity, RGA, particles etc.) • Across the surface erosion cathode • Improve existing technologies for larger diameter • Step coverage, especially bottom coverage (barrier metal, etc.)	—
Implanter	3 Device Manufacturers	6 Device Manufacturers	• Equipment stability, maintenance free equipment • Higher speed, charge up, footprint, lower weight • Lower prices for high energy implanter • Control over contamination, and damage • Batch type for high dose; single wafer for medium dose • Contamination reduction • Medium dose: improve the beam current uniformity across the wafer • High dose: better throughput • Single wafer high current implanter equipment (without a drop in throughput) • Introduction of high energy implanter, smaller equipment footprint	—
Lithography	—	7 Device Manufacturers 2 Suppliers	• Excimer lithography capability (control over the atmosphere) • Faster pattern defect inspection and automation (wafers) • Optical system function (0.18-0.25µm) • Efficient in-line setup between CV/DV and stepper • Safer, longer lifetime, and finer geometry excimer process • Measures for reducing construction cost and running cost • Localized hollowing by equipment module • Mask transfer/loading method (less clean environment) standardization of mask I/O among stocker, transfer system, and lithography system • Vibration specification • Lack of basic performance (resolution, depth of field, dimensional tolerance, overlay accuracy) • Larger field size, improvement in resolution alignment, resist development (excimer, etc.)	• Resolution, overlay accuracy, exposure field size (balance against throughput) • Capability for new resist material
CVD	3 Device Manufacturers	7 Device Manufacturers 3 Suppliers	• Fewer particles/higher coverage, better planarization • Wider applications (smaller geometries, new materials) • Improved dust control and safety • In situ monitoring and cleaning • Hardware specification for making native oxide free polysilicon and SiN deposition possible using multi-chamber system • Single wafer LPCVD (high throughput needed)	• Keep up with advanced process with high density plasma • Higher reliability, particle free transfer mechanism • Multi-chamber, continuous processing

Source: SEMI

22674/22675

Figure 7-12. 300mm Tool Development Issues

	Type		Comment	
	Batch	Single Wafer	Device Manufacturer	Equipment Manufacturer
Dry Etch	—	7 Device Manufacturers 2 Suppliers	• Elimination of particles/no residues/anisotropic etching/low damage • EDP reliability • Wider applications (finer geometries, new material) • Better control over dust and safety • In situ monitoring and cleaning • Process technology for 0.2µm • Uniformity and throughput improvement with better profile selectivity will be required for 12" diameter • Improve existing technology for larger diameter • Finer geometry processing (contact) and selectivity (Al) are needed, although no problem with single wafer • Stable performance and self cleaning technology	• Ensuring performance uniformity • Improvement in plasma uniformity (to keep up with larger chamber)
Wet Etch	5 Device Manufacturers	7 Device Manufacturers 1 Suppliers	• Less particles/control over suface cleanliness/ control over atmosphere • Particle • Single wafer and in-line process, simpler, dry process • Combination of dry etch and light etch • Use multiple chemicals for resist stripping depending on the process • Small, low capacity wet etcher for various applications • Combined use of single wafer treatment equipment and small batch treatment equipment • Problems of micro-roughness and native oxide treatment • Less chemicals should be used for single wafer treatment	• Lot size (throughput) definition for compound process
Diffusion	6 Device Manufacturers 1 Suppliers		• Non-contact wafer temperature measurement method • Speed of temperature ramp up and ramp down (prevent wafer warp) • Wider use of RTP, low temperature treatment • Improved uniformity • 8" diameter: entire process is batch type for 64M, cluster for critical steps with 256M (single wafer or 25 wafer batch treatment necessary) • 12" diameter: same as 8" for critical steps, mini batch treatment for other steps • Maintain the throughput • Need to develop high speed anneal • Small batch treatment • Lower equipment cost and establishment of low temperature process for single wafer diffusion	• Structure of end station tie-in • Wafer cooling • Matching between beam scanning system and electron flood gun • Better transfer system reliability

Source: SEMI

22676/22677

Figure 7-12. 300mm Tool Development Issues (continued)

Beyond equipment concerns, Figure 7-13 shows the targeted production schedule for 300mm starting wafers from five major suppliers, and looking out further the supply escalates beyond the year 2001 (Figure 7-14) according to the Japan Society of New Metals. As shown in Figure 7-15, exports of silicon from Japan has increased significantly in recent years as semiconductor manufacturing in other regions has continued to increase. One of the major challenges for silicon suppliers is managing 300mm demand together with balancing demand for wafers of the various other sizes. Some of the challenges for 400mm have already been anticipated (Figure 7-16).

	Monthly Prototype Production Targets				
Company	July 96	Dec. 96	July 97	Dec. 97	July 98
SEH	1,000 →	5,000 →			20,000
Sumitomo	500 →	1,000 →		5,000	10,000
Mitsubishi	500 →	1,000 →			2,000
Komatsu	—	—	1,000 →		5,000
Toshiba	—	—	—	—	1,000
Total	2,000	7,000	8,000	13,000	38,000

Source: Nikkei Sangyo Shimbun, Nihon Keizai 22625

Figure 7-13. Japan 300mm Wafer Supplier Plans

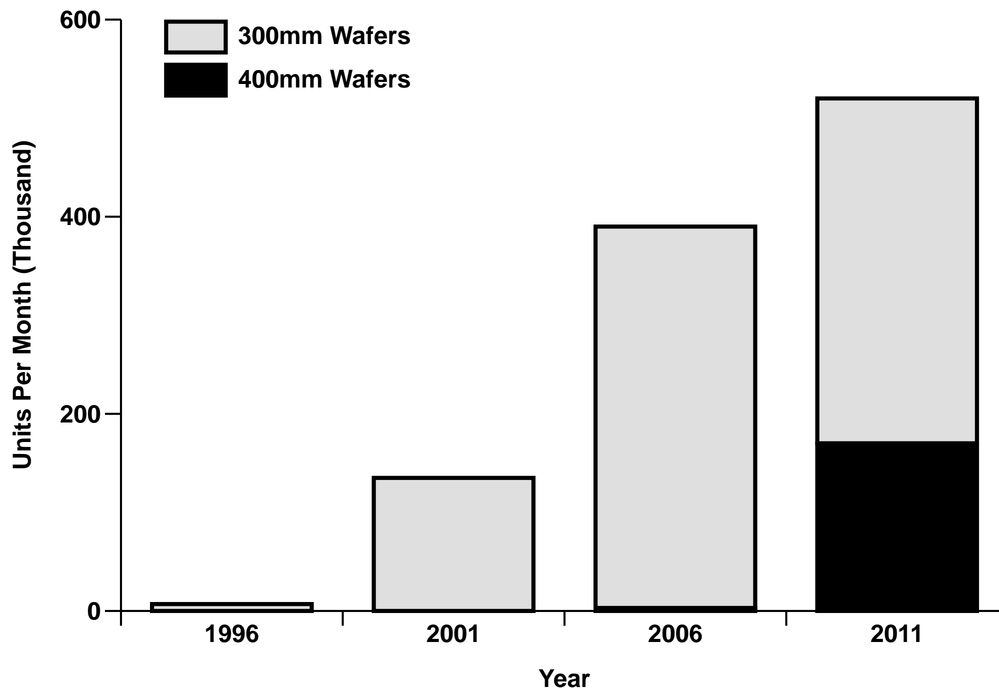


Figure 7-14. Large Diameter Wafer Forecast

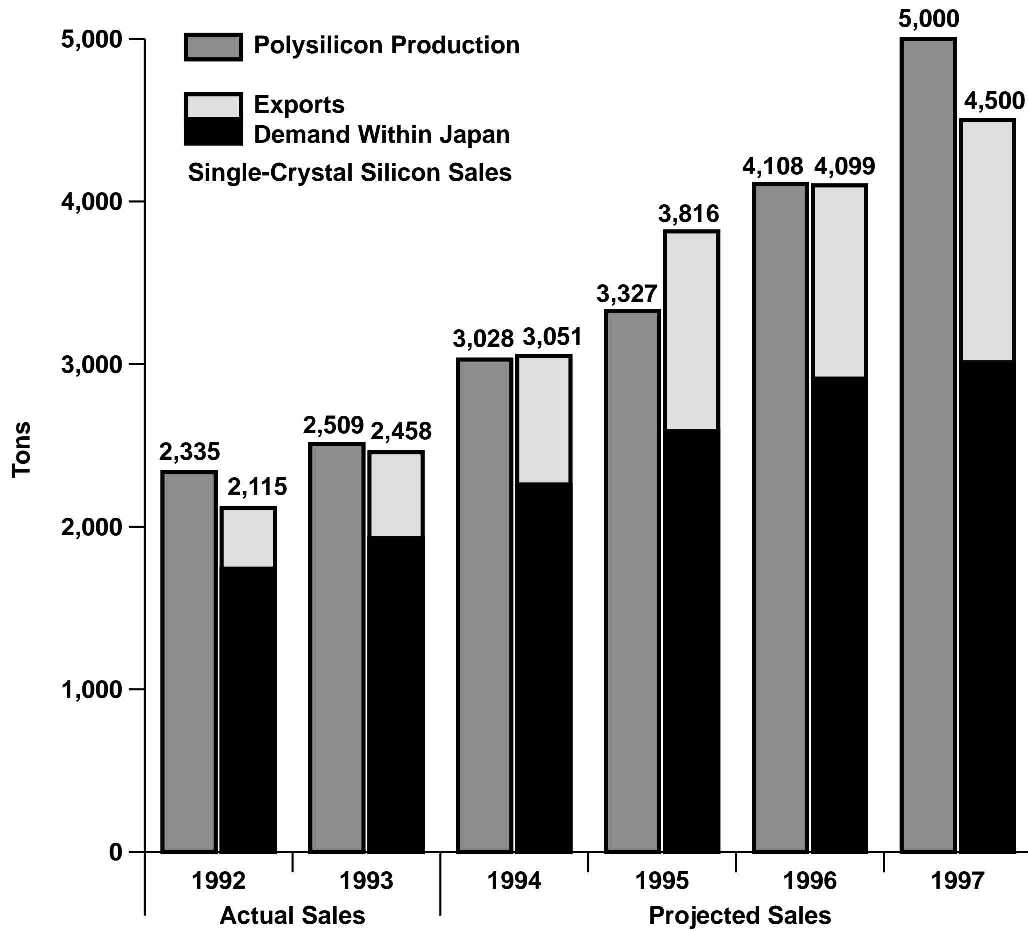


Figure 7-15. Projected and Actual Sales Figures For Ultrahigh Purity Silicon

Outlook for 300mm Wafer Processing

Perhaps the biggest question in 300mm development pertains to the issue of cost – How will the semiconductor manufacturing and equipment and materials suppliers, with a combined market size of approximately \$170 billion, build a \$15-20 billion infrastructure for 300mm processing in a few years while meeting on-going requirements for device and process development for 0.25μm, 0.18μm, and future generations of devices? Possibly many semiconductor manufacturers will find that through alternative device design techniques, smaller die size will be possible, thereby delaying 300mm adoption out to the 0.15μm or 0.13μm generation.

The second pressing question is to what the extent will the two consortiums, I3001 and SELETE, cooperate? Information from SEMI indicates that standards will be jointly developed but the tool projects are clearly separate efforts. Time will tell to what extent 300mm processing information will be shared.

Department	Goal	1996	1997	1998	1999	2000
Crystal Growth	Growth of a 400kg. 400mm diameter dislocation-free silicon ingot	Equipment design and simulation	Equipment fabrication and basic experiments	Equipment revision and crystal growth	Integration with other processes	—
Wafer Fabrication	Develop crystal cutting, polishing, etching, and wet cleaning processes capable of making wafers with flatness of 0.13µm or better, surface metal contamination of 10^8 atoms/cm^2, and controlled particle size of 0.04µm or better	Equipment design	Equipment fabrication and experiments	Equipment revision and experiments	Integration with inspection/ evaluation techniques	Integration with other processes
Epitaxial Growth	Grow epi films with thickness and resistivity variations of 1 percent or better, and transistions region width of 0.5µm or less	Equipment design	Equipment fabrication and experiments	Equipment revision and experiments	Equipment revision and final experiments	Integration with other processes

Source: Super Silicon Crystal Research Institute 22628

Figure 7-16. Roadmap for 400mm Wafers

Outside of the largest semiconductor manufacturers, companies will carefully observe the advantages and disadvantages associated with the 300mm transition. No one in the industry can foresee how many companies will ultimately use these larger wafers. This, of course, should come as no surprise, as to date, a number of manufacturers have never needed to progress beyond 150, 125, or even 100mm wafer processing. In any case, wafer size transitions, especially the move to 300mm, will not become a reality until it can be made more cost-effective.

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