

Chapter 1

From Zero to One

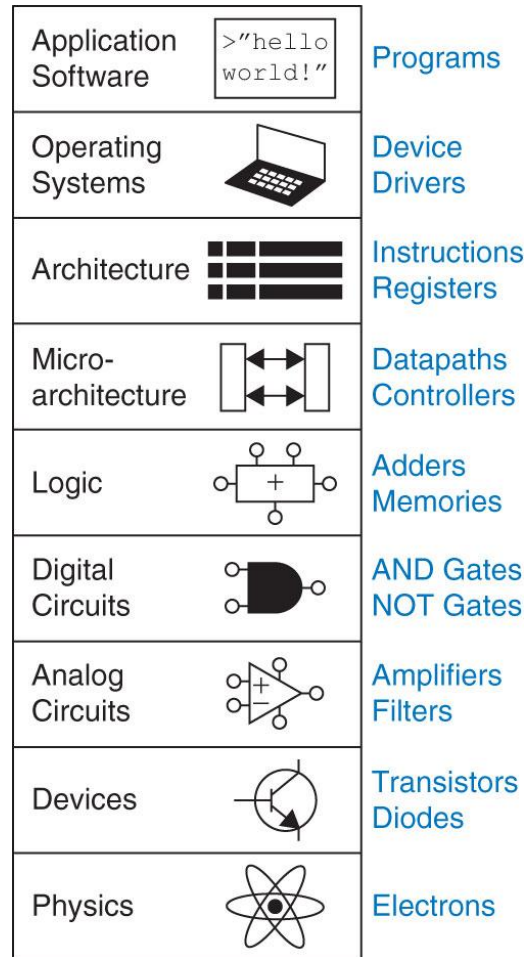


Figure 1.1 Levels of abstraction for an electronic computing system

(Image by Euroarms Italia. www.euroarms.net · 2006.)

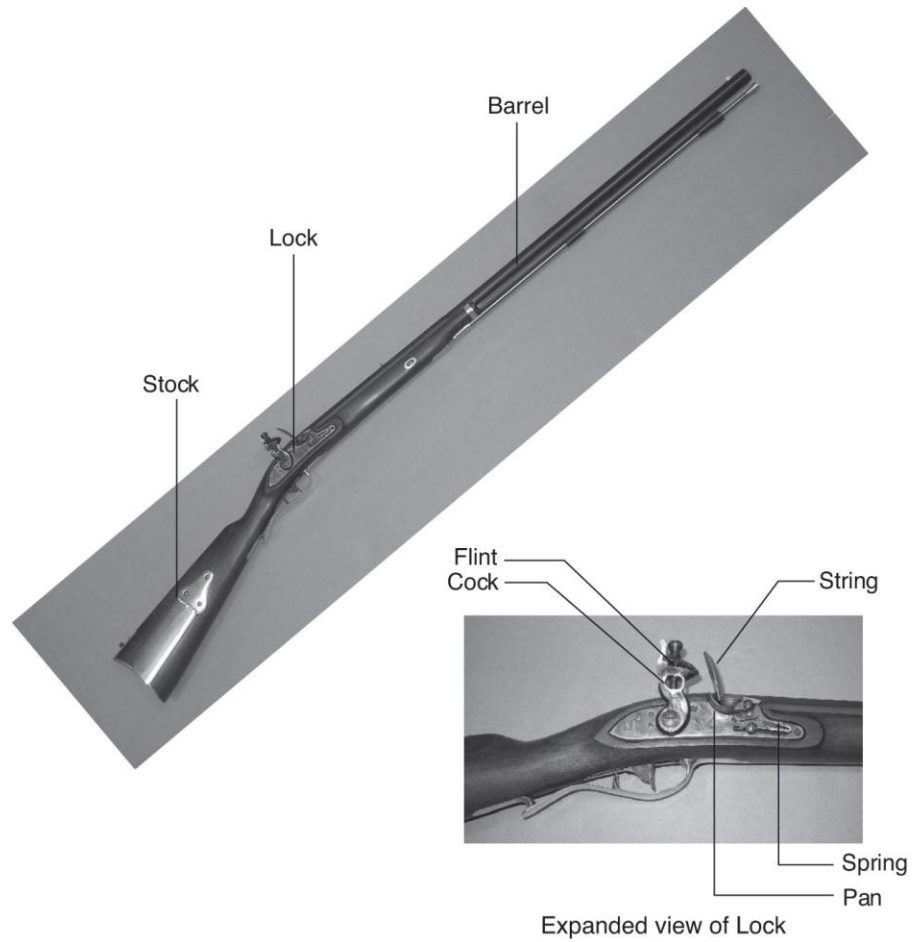


Figure 1.2 Flintlock rifle with a close-up view of the lock

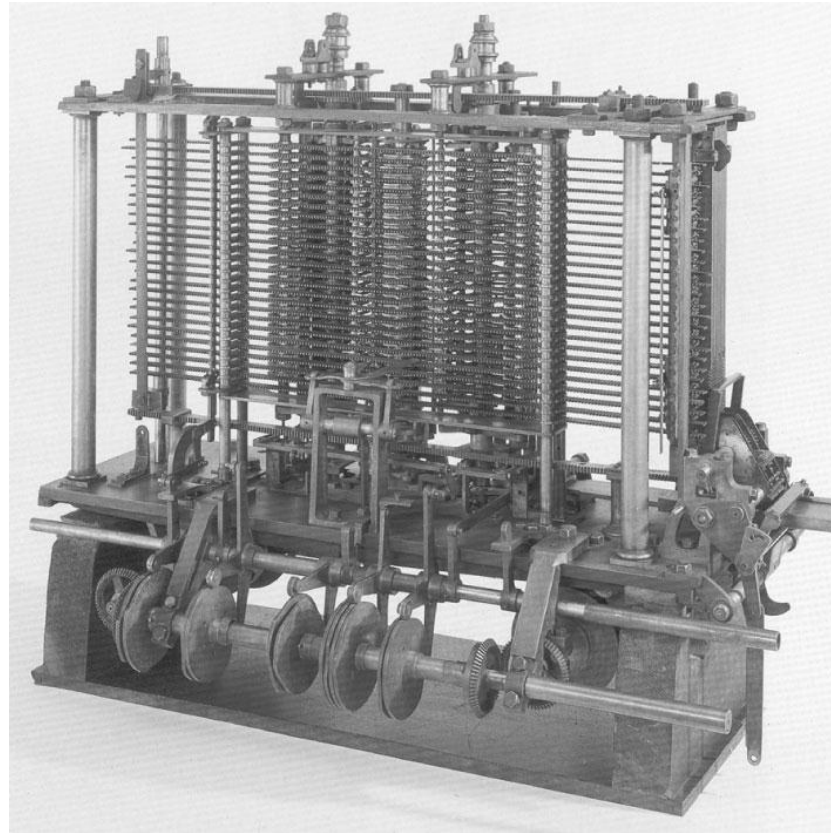


Figure 1.3 Babbage's Analytical Engine, under construction at the time of his death in 1871
(image courtesy of Science Museum/Science and Society Picture Library)

1's column
10's column
100's column
1000's column

$$9742_{10} = 9 \times 10^3 + 7 \times 10^2 + 4 \times 10^1 + 2 \times 10^0$$

nine seven four two
thousands hundreds tens ones

Figure 1.4 Representation of a decimal number

1's column
2's column
4's column
8's column
16's column

$$10110_2 = 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 22_{10}$$

one sixteen no eight one four one two no one

Figure 1.5 Conversion of a binary number to decimal

1's column
16's column
256's column

$$2ED_{16} = 2 \times 16^2 + E \times 16^1 + D \times 16^0 = 749_{10}$$

two
two hundred
fifty six's

fourteen
sixteens

thirteen
ones

Figure 1.6 Conversion of a hexadecimal number to decimal

101100
└─┘ └─┘
most least
significant significant
bit bit
(a)

DEAFDAD8
└─┘ └─┘
most least
significant significant
byte byte
(b)

Figure 1.7 Least and most significant bits and bytes

$$\begin{array}{r} 11 \\ 4277 \\ + 5499 \\ \hline 9776 \end{array}$$

(a)

← carries →

$$\begin{array}{r} 11 \\ 1011 \\ + 0011 \\ \hline 1110 \end{array}$$

(b)

Figure 1.8 Addition examples showing carries: (a) decimal (b) binary

$$\begin{array}{r} 111 \\ 0111 \\ + 0101 \\ \hline 1100 \end{array}$$

Figure 1.9 Binary addition example

$$\begin{array}{r} 11\ 1 \\ 1101 \\ + 0101 \\ \hline 10010 \end{array}$$

Figure 1.10 Binary addition example with overflow

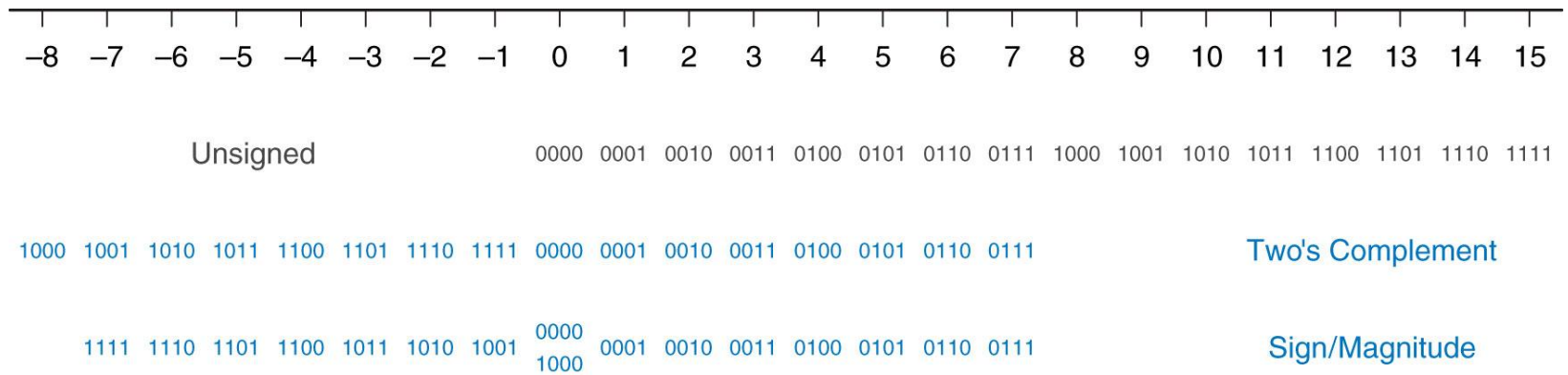
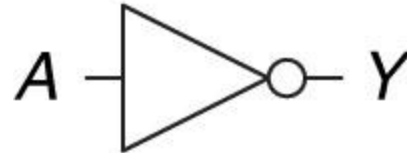


Figure 1.11 Number line and 4-bit binary encodings

NOT

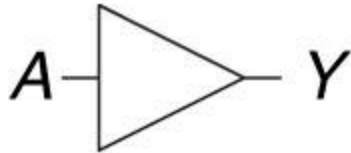


$$Y = \bar{A}$$

A	Y
0	1
1	0

Figure 1.12 NOT gate

BUF

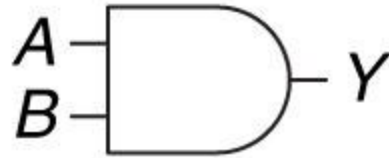


$$Y = A$$

A	Y
0	0
1	1

Figure 1.13 Buffer

AND

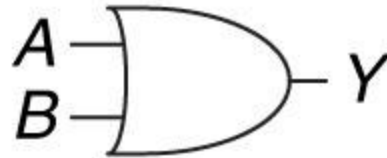


$$Y = AB$$

<i>A</i>	<i>B</i>	<i>Y</i>
0	0	0
0	1	0
1	0	0
1	1	1

Figure 1.14 AND gate

OR

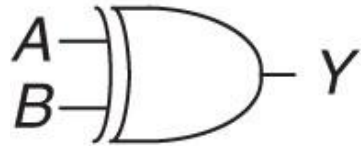


$$Y = A + B$$

<i>A</i>	<i>B</i>	<i>Y</i>
0	0	0
0	1	1
1	0	1
1	1	1

Figure 1.15 OR gate

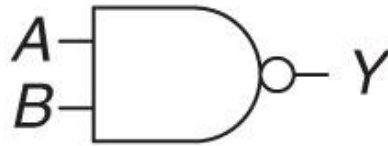
XOR



$$Y = A \oplus B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

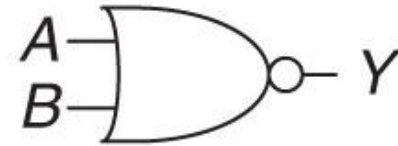
NAND



$$Y = \overline{AB}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR

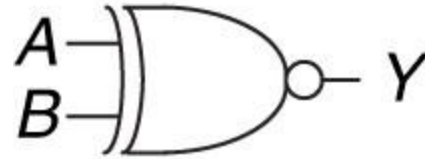


$$Y = \overline{A+B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Figure 1.16 More two-input logic gates

XNOR



$$Y = \overline{A \oplus B}$$

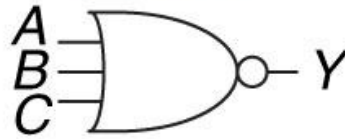
A	B	Y
0	0	
0	1	
1	0	
1	1	

Figure 1.17 XNOR gate

<i>A</i>	<i>B</i>	<i>Y</i>
0	0	1
0	1	0
1	0	0
1	1	1

Figure 1.18 XNOR truth table

NOR3



$$Y = \overline{A + B + C}$$

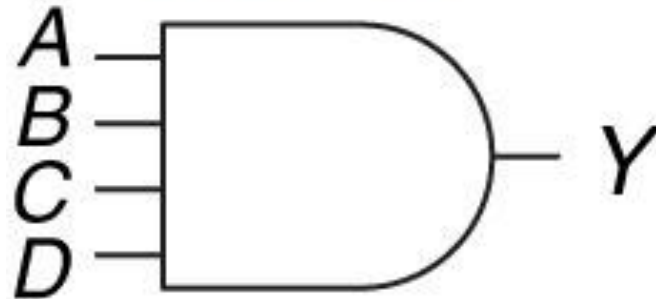
A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Figure 1.19 Three-input NOR gate

<i>A</i>	<i>B</i>	<i>C</i>	<i>Y</i>
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 1.20 Three-input NOR truth table

AND4



$$Y = ABCD$$

Figure 1.21 Four-input AND gate

<i>A</i>	<i>C</i>	<i>B</i>	<i>D</i>	<i>Y</i>
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Figure 1.22 Four-input AND truth table

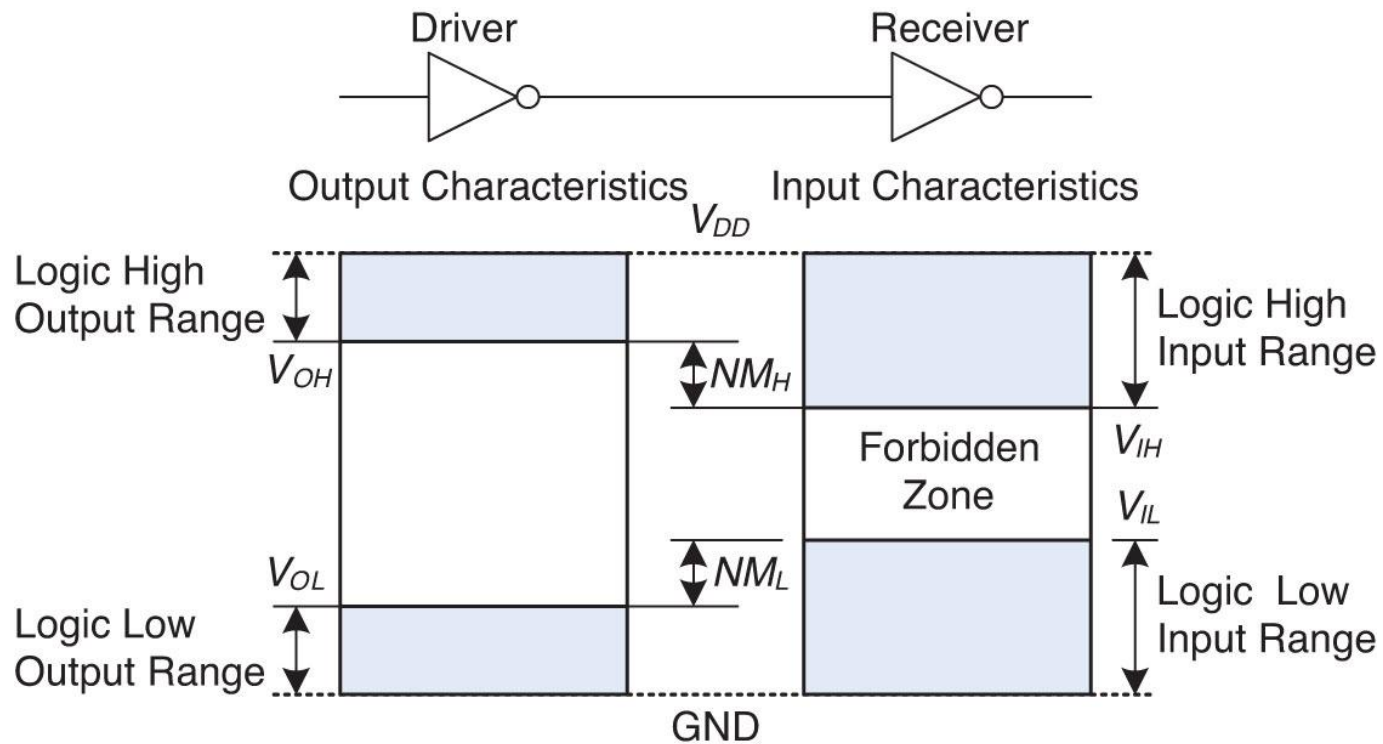


Figure 1.23 Logic levels and noise margins

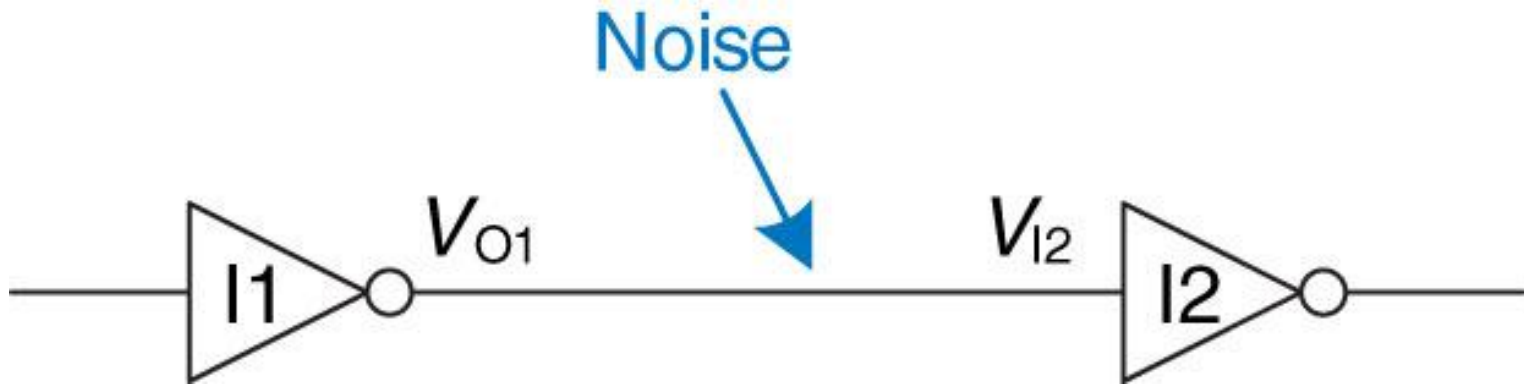


Figure 1.24 Inverter circuit

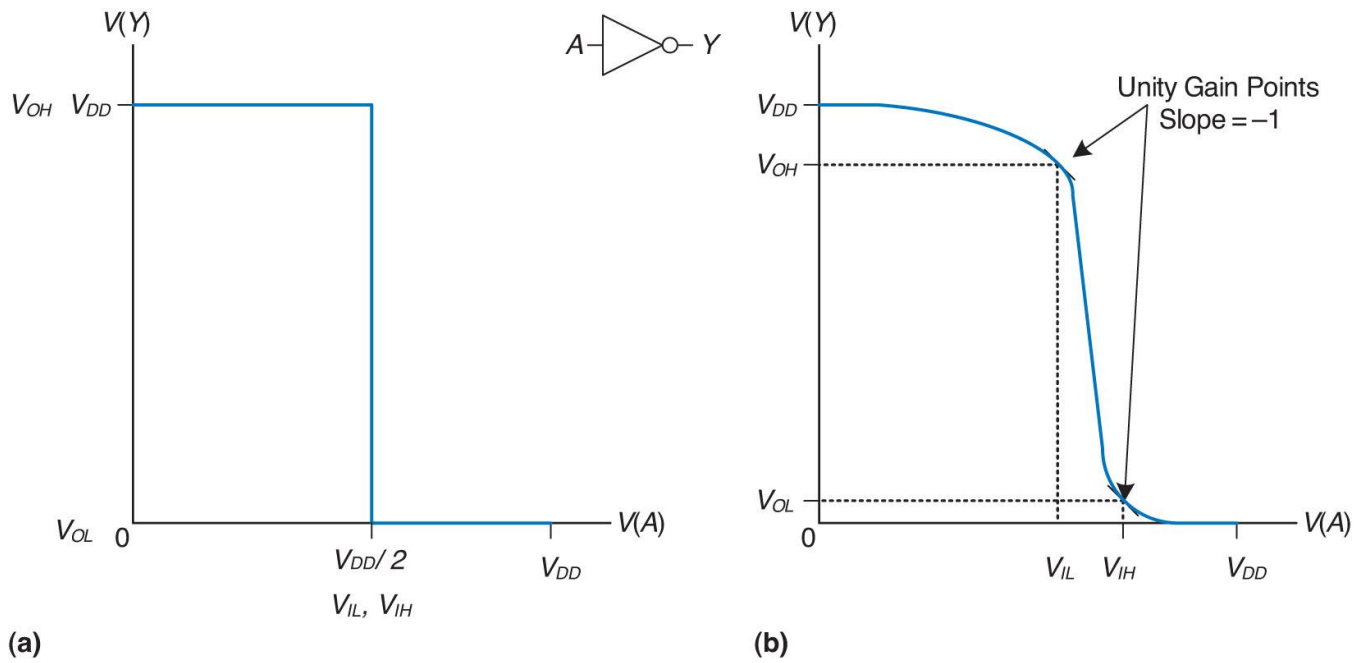


Figure 1.25 DC transfer characteristics and logic levels

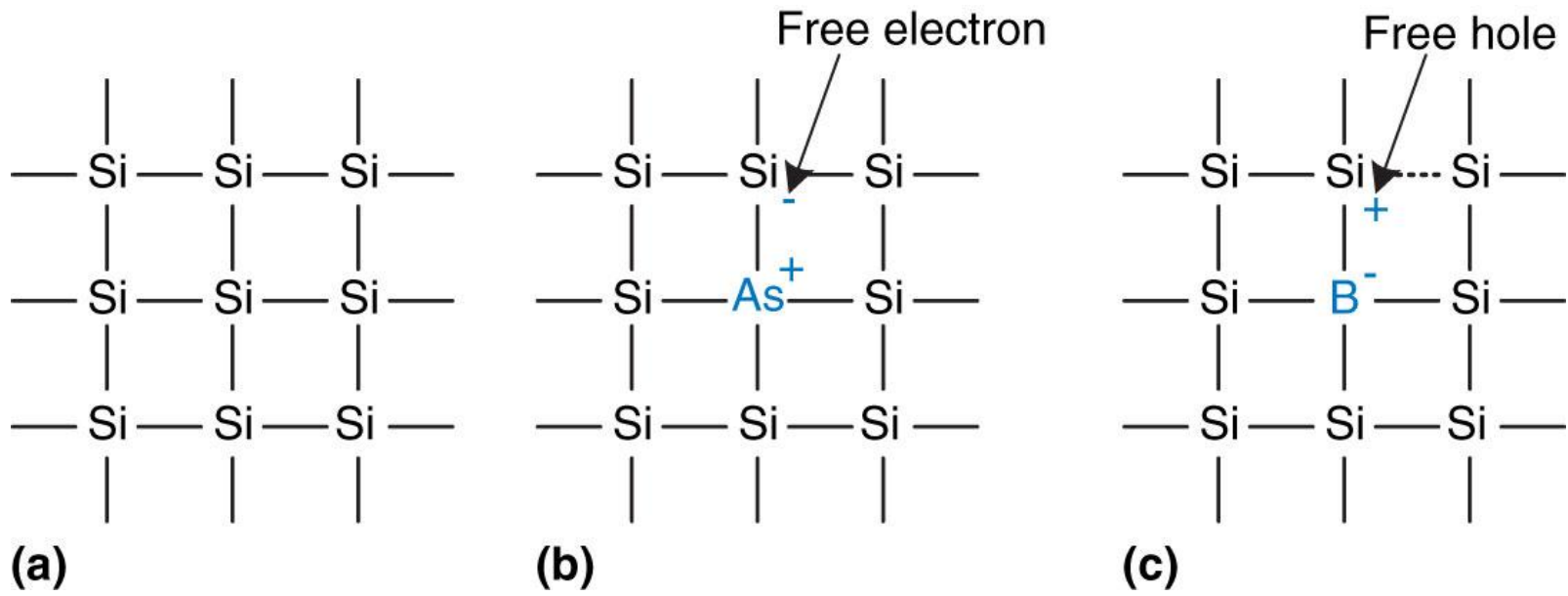


Figure 1.26 Silicon lattice and dopant atoms

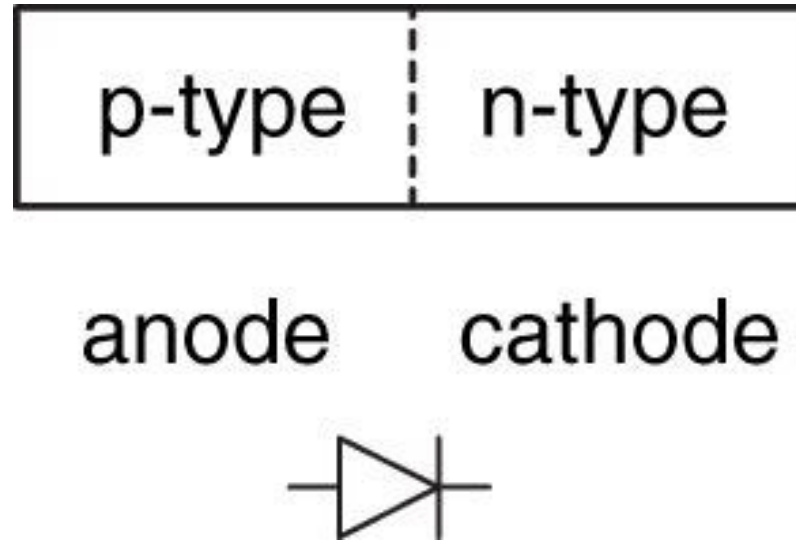


Figure 1.27 The p-n junction diode structure and symbol

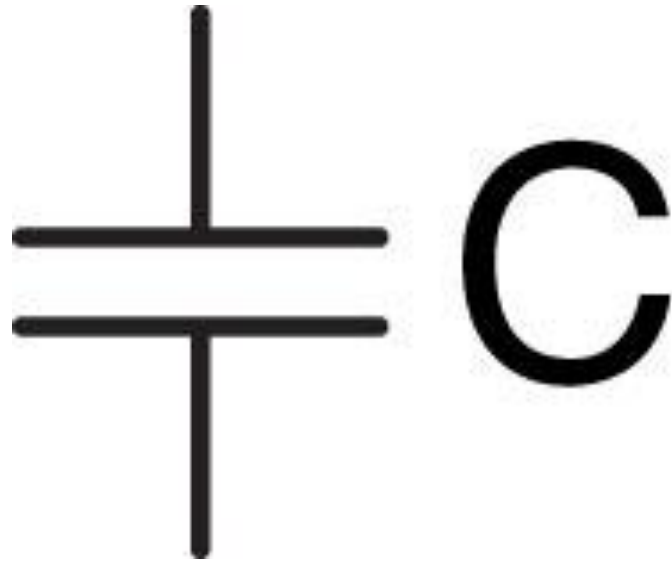
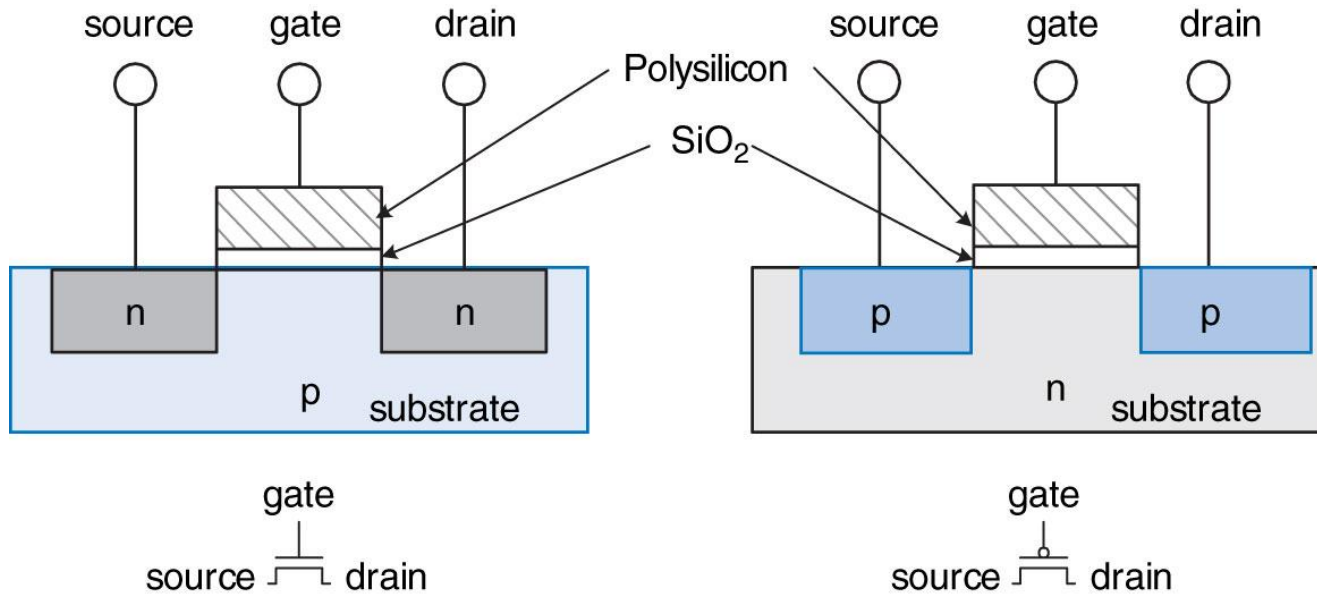


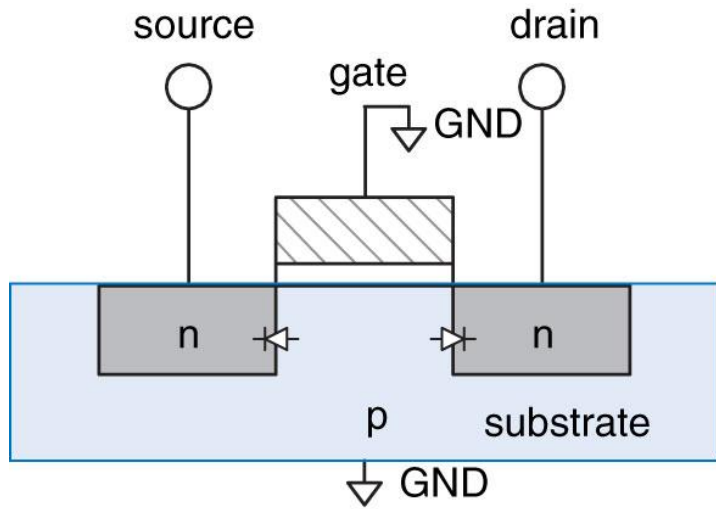
Figure 1.28 Capacitor symbol



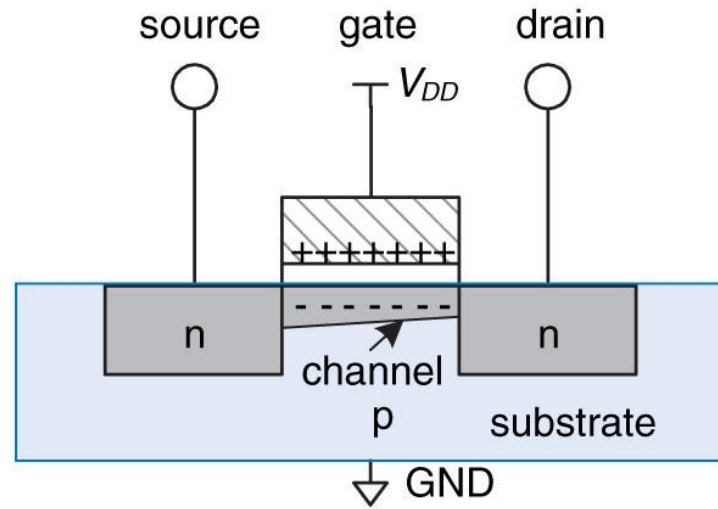
(a) nMOS

(b) pMOS

Figure 1.29 nMOS and pMOS transistors



(a)



(b)

Figure 1.30 nMOS transistor operation

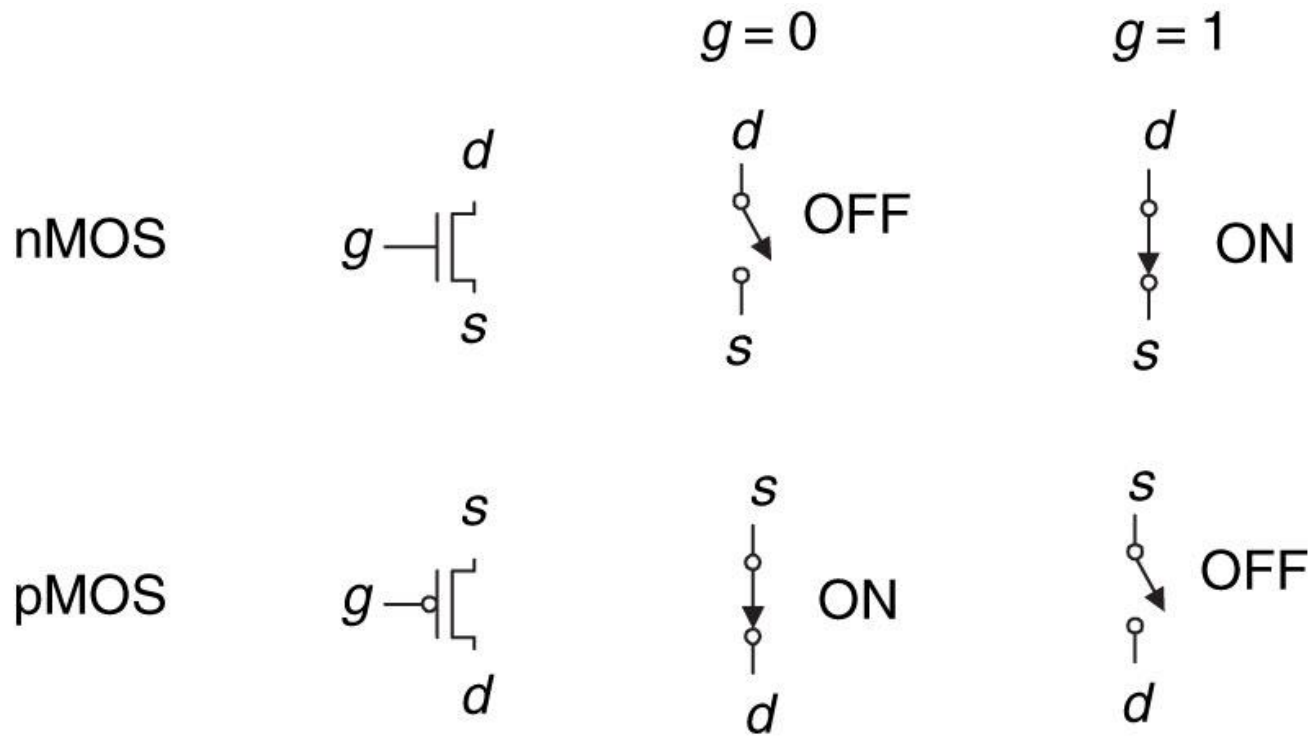


Figure 1.31 Switch models of MOSFETs

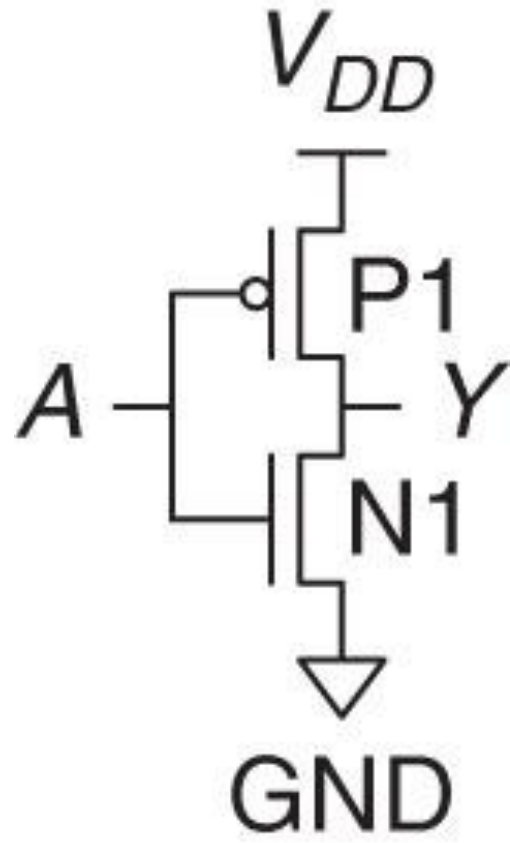


Figure 1.32 NOT gate schematic

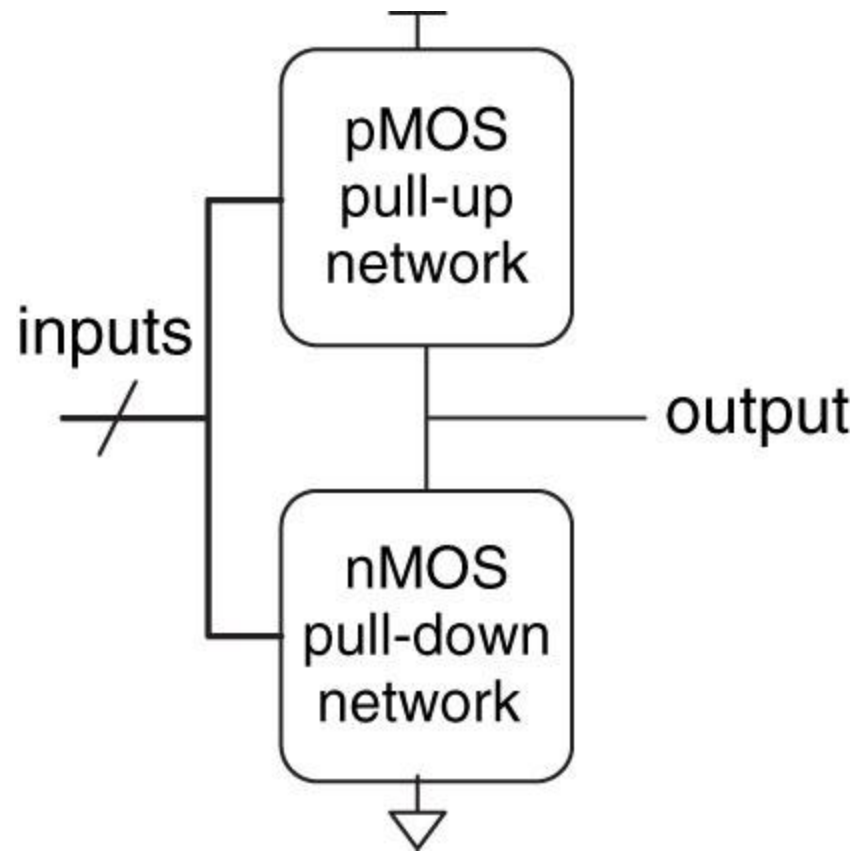


Figure 1.34 General form of an inverting logic gate

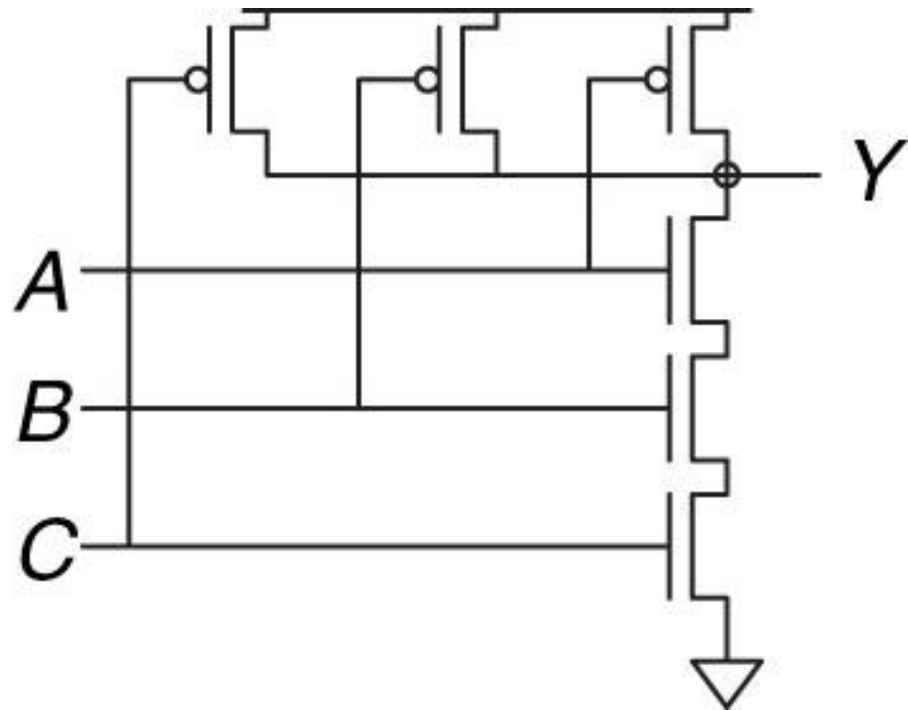


Figure 1.35 Three-input NAND gate schematic

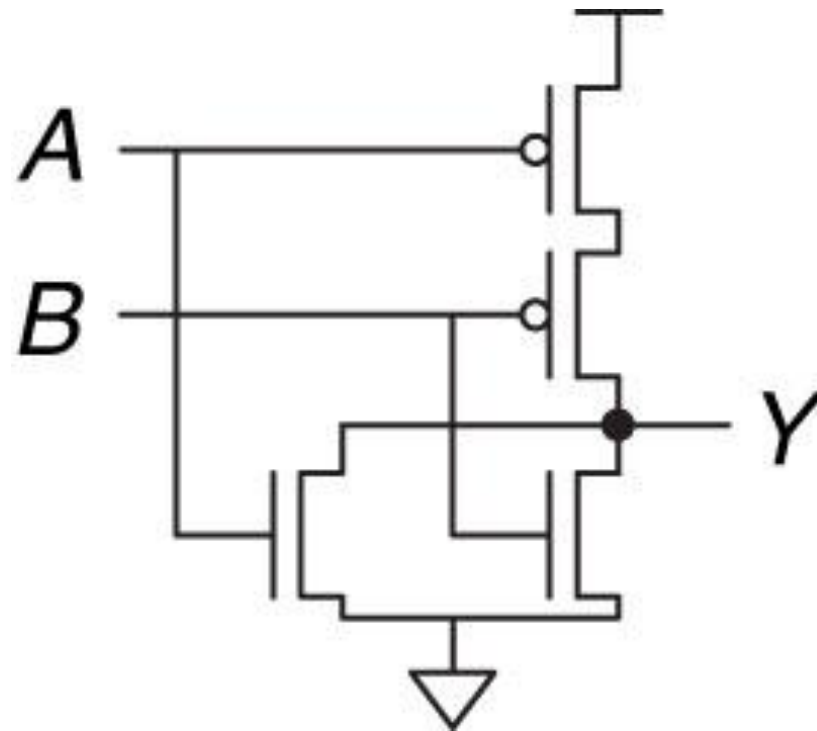


Figure 1.36 Two-input NOR gate schematic

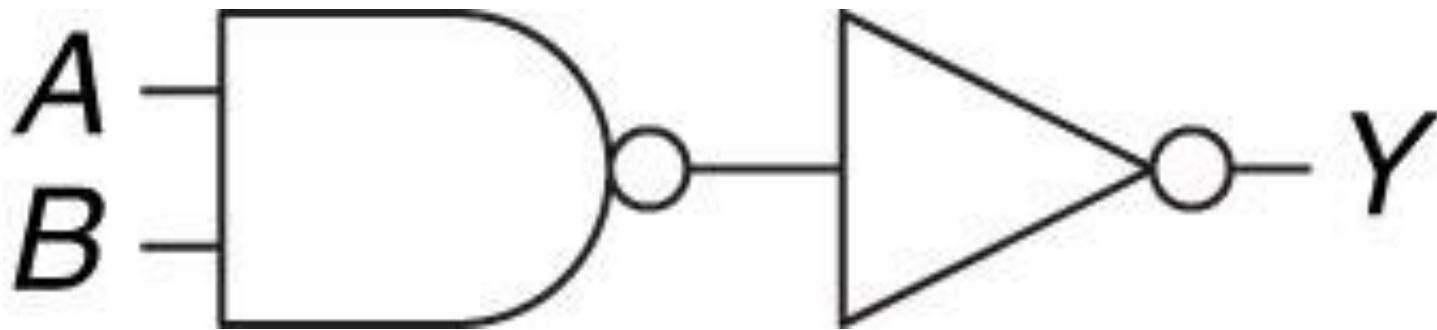


Figure 1.37 Two-input AND gate schematic

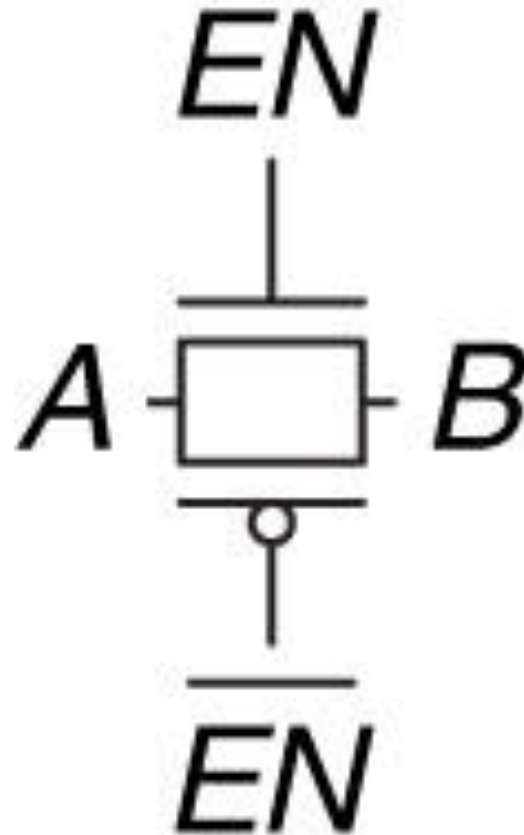


Figure 1.38 Transmission gate

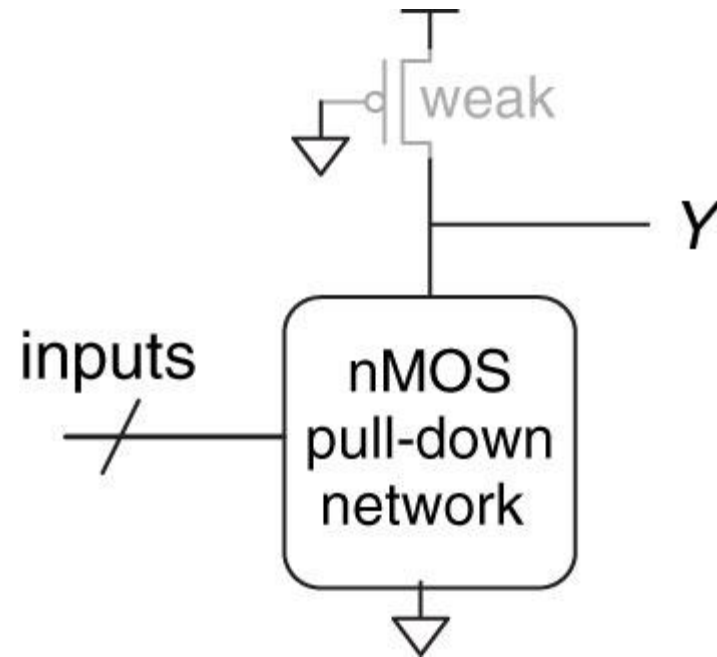


Figure 1.39 Generic pseudo-nMOS gate

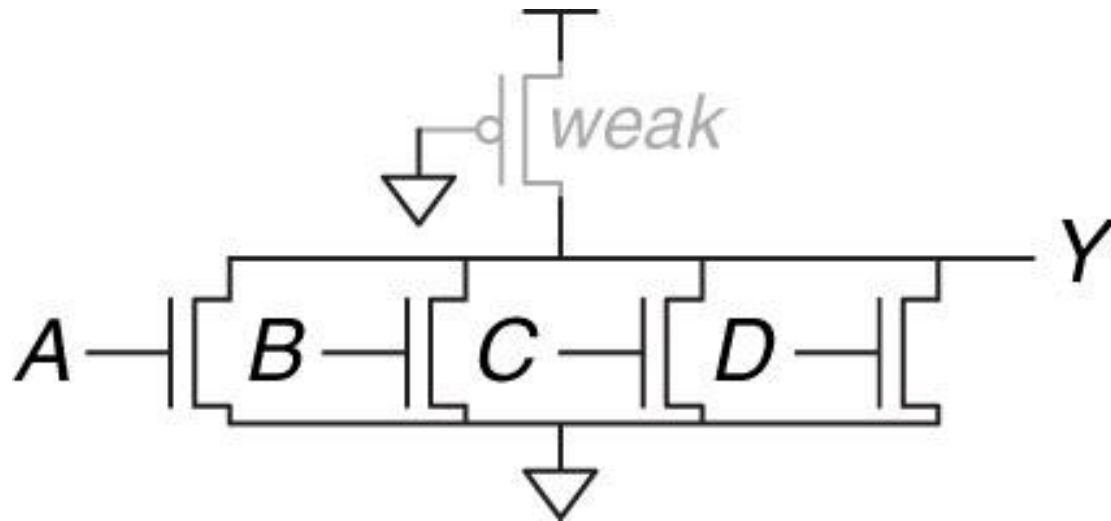


Figure 1.40 Pseudo-nMOS four-input NOR gate

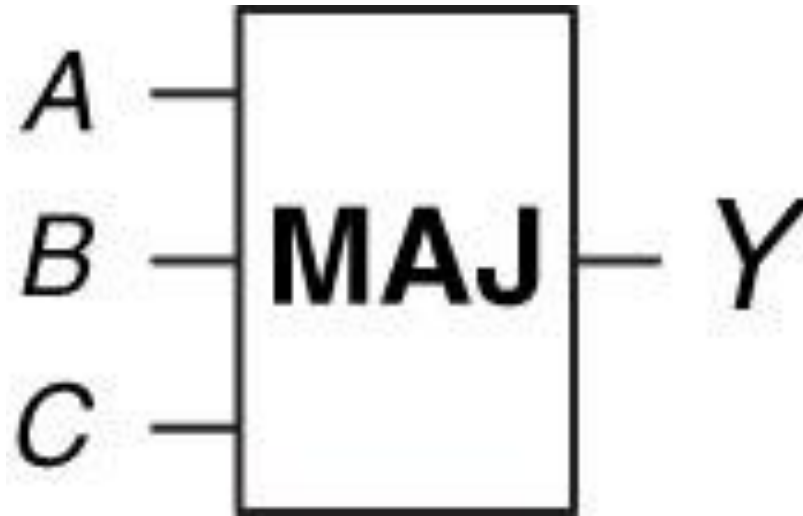


Figure 1.41 Three-input majority gate

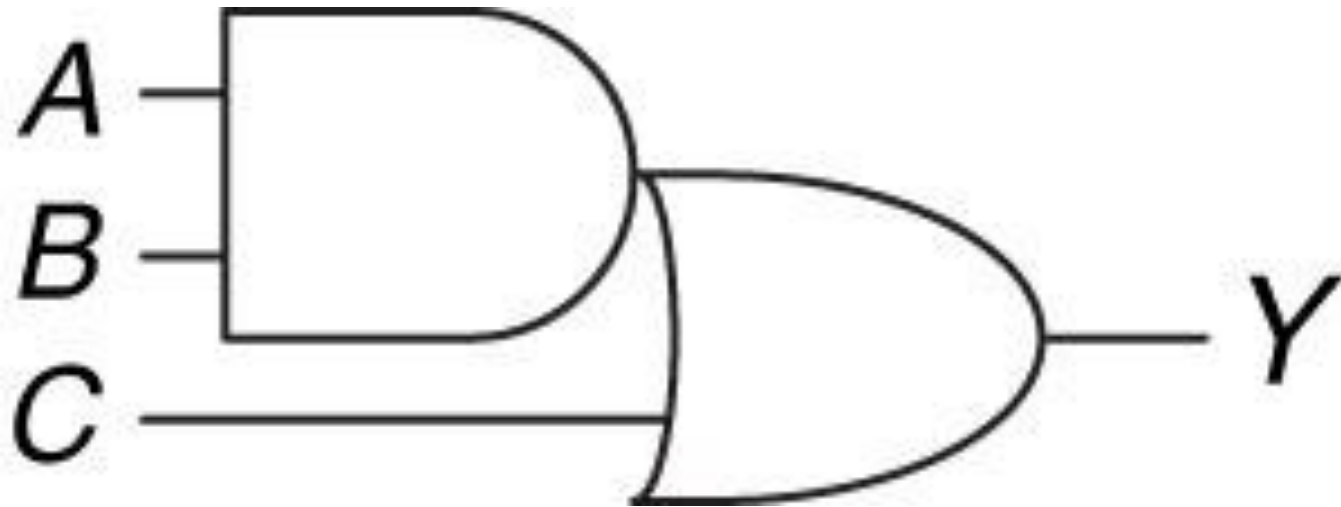


Figure 1.42 Three-input AND-OR gate

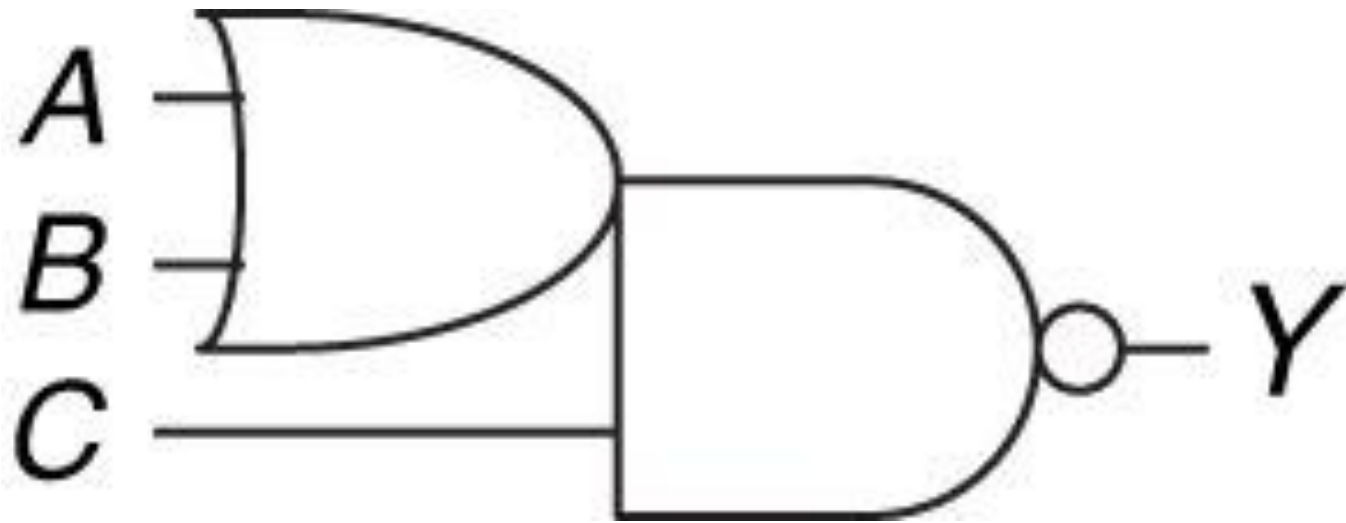


Figure 1.43 Three-input OR-AND-INVERT gate

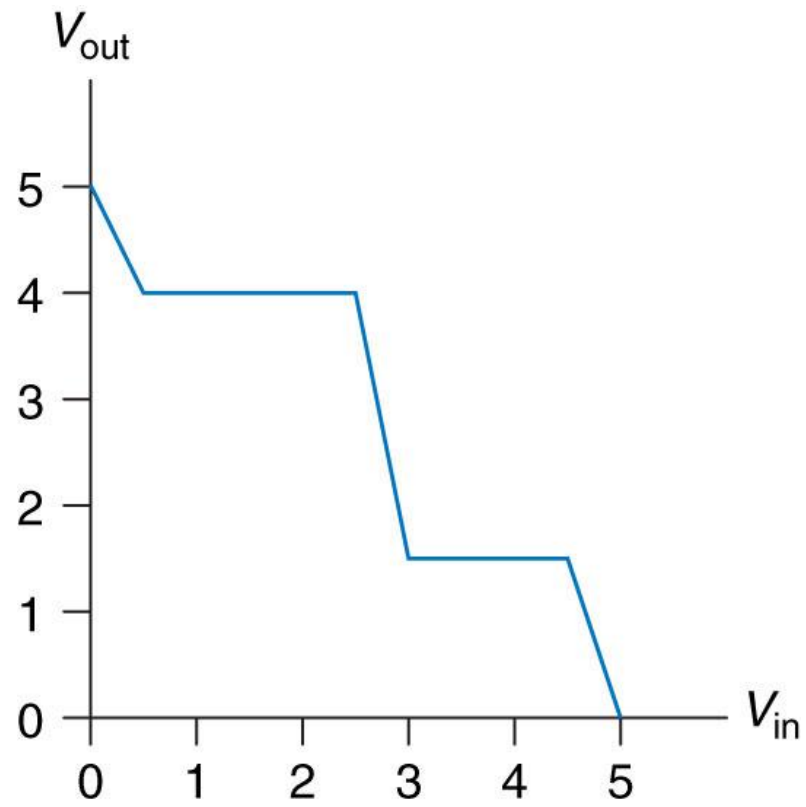


Figure 1.44 DC transfer characteristics

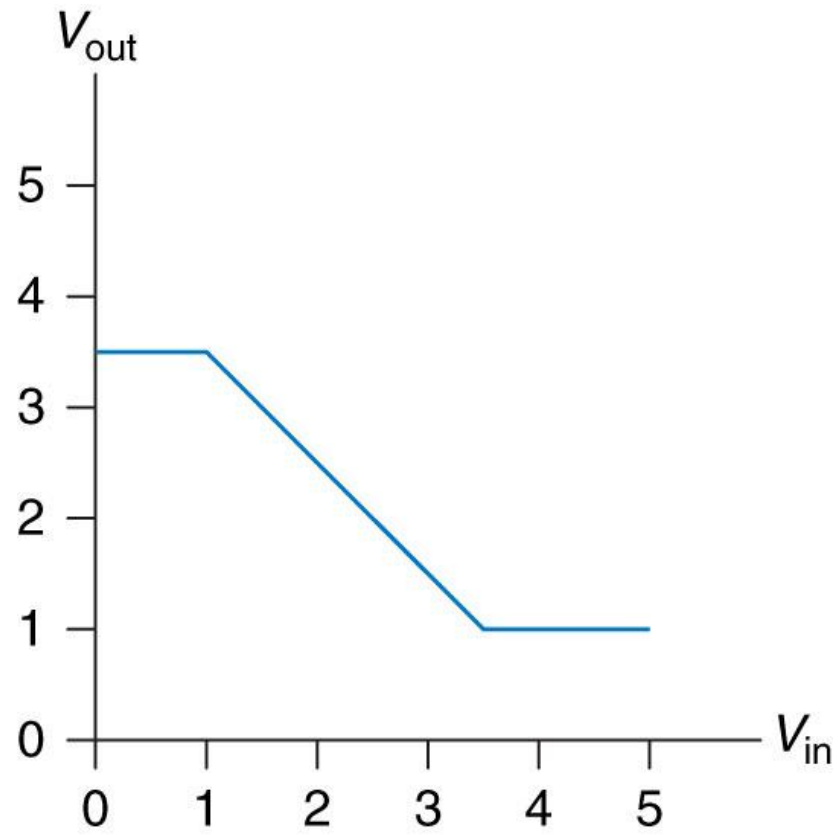


Figure 1.45 DC transfer characteristics

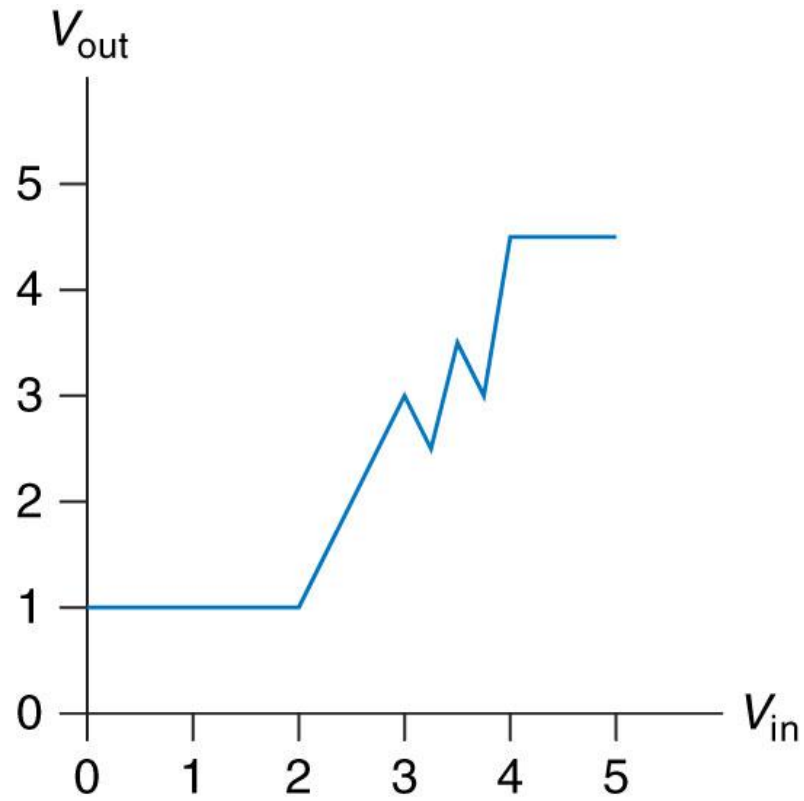


Figure 1.46 DC transfer characteristics

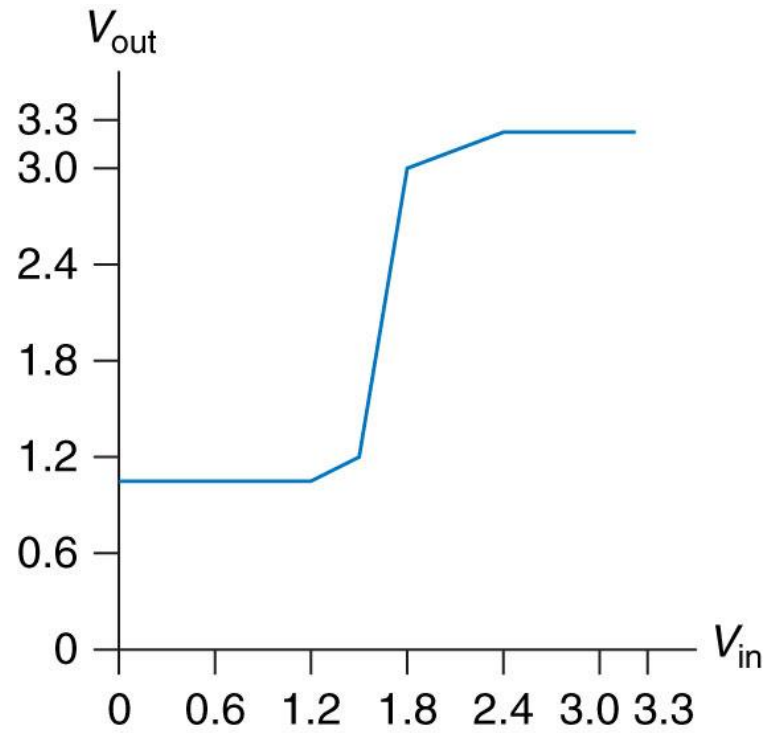


Figure 1.47 Ben's buffer DC transfer characteristics

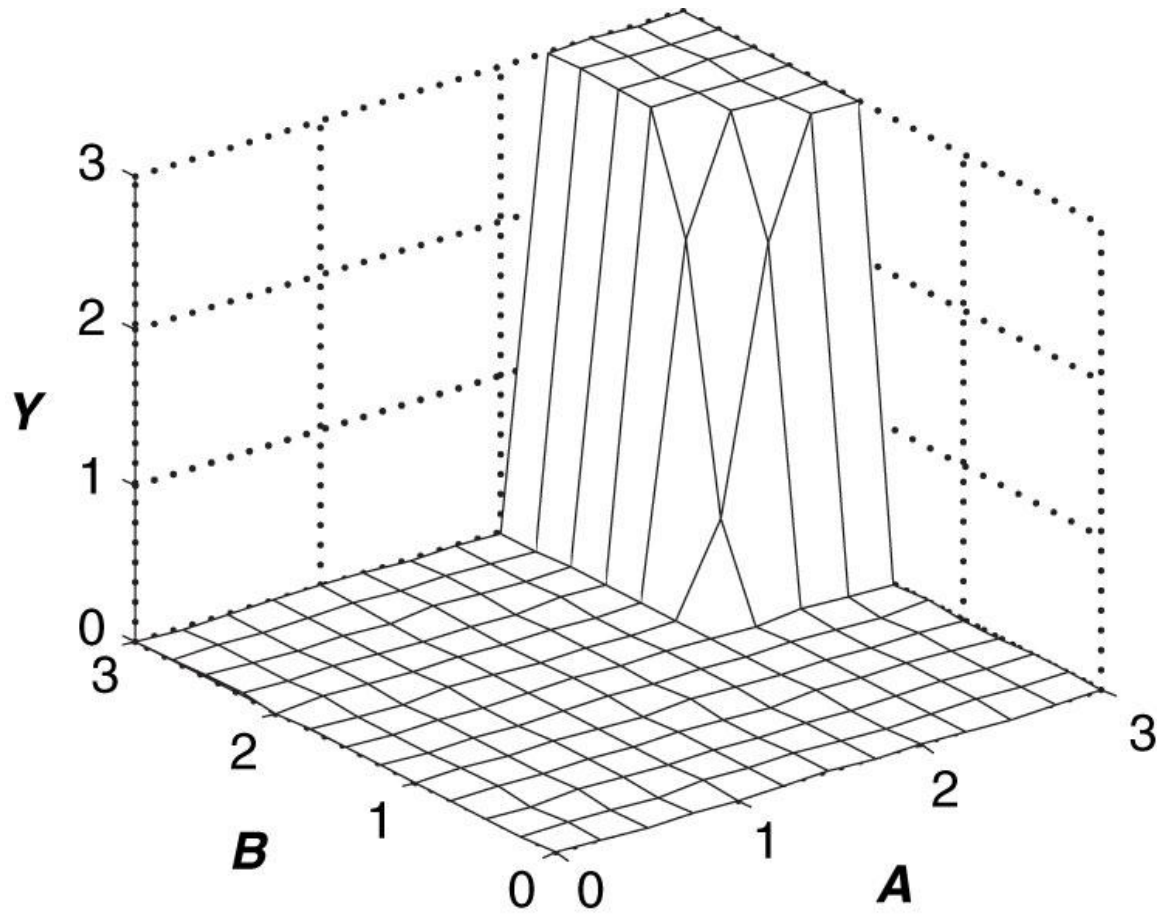


Figure 1.48 Two-input DC transfer characteristics

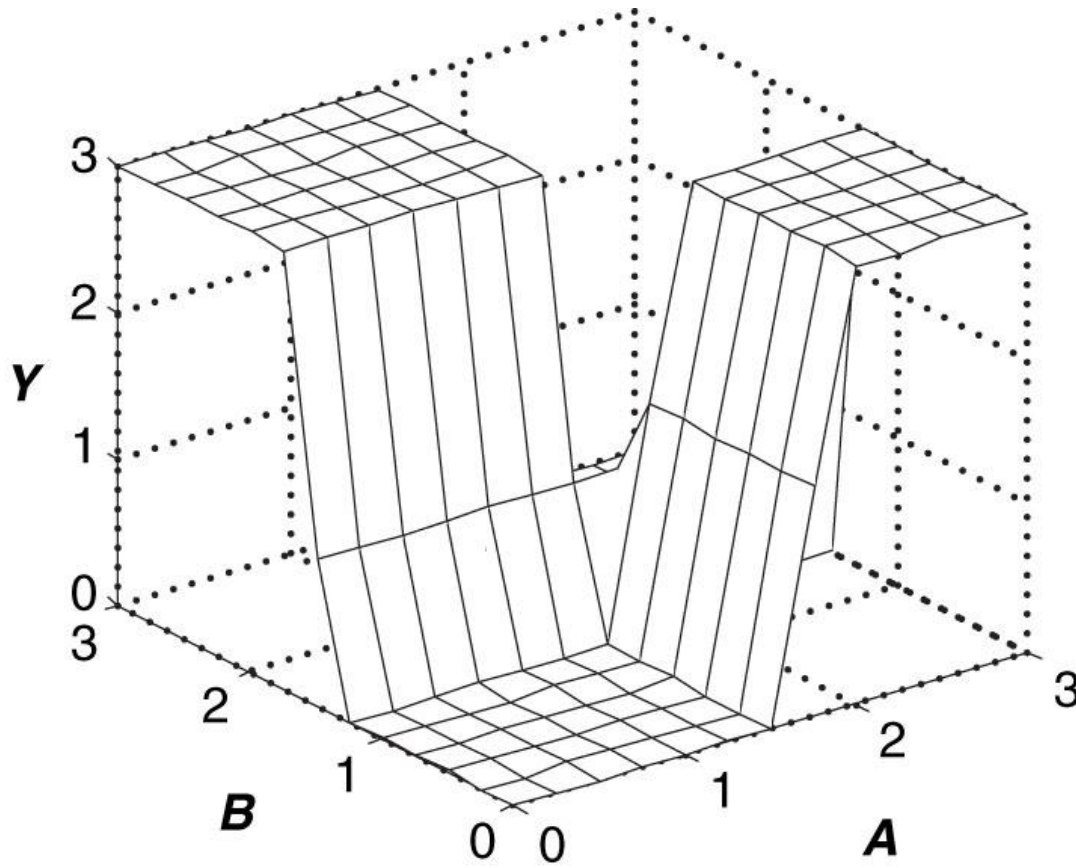


Figure 1.49 Two-input DC transfer characteristics

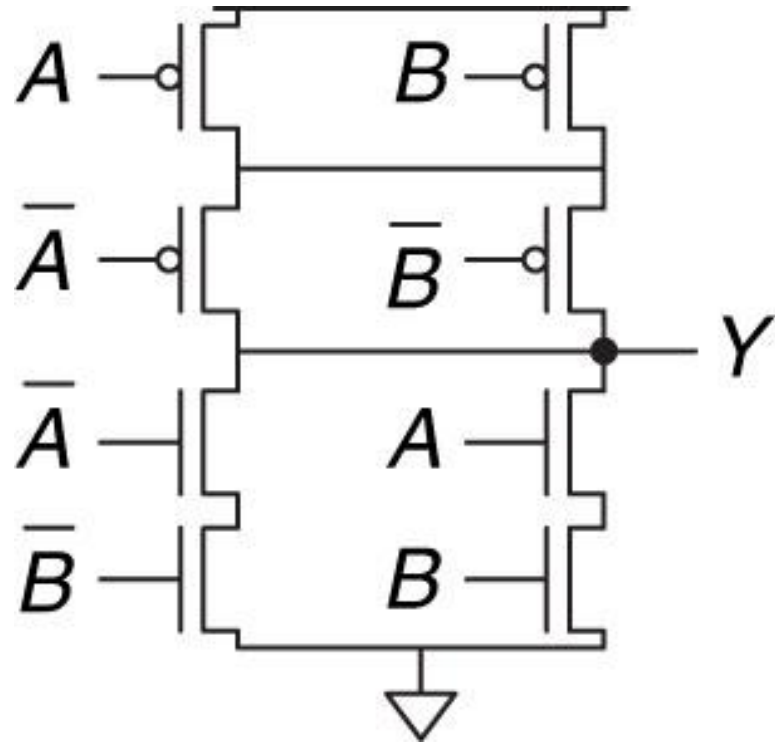


Figure 1.50 Mystery schematic

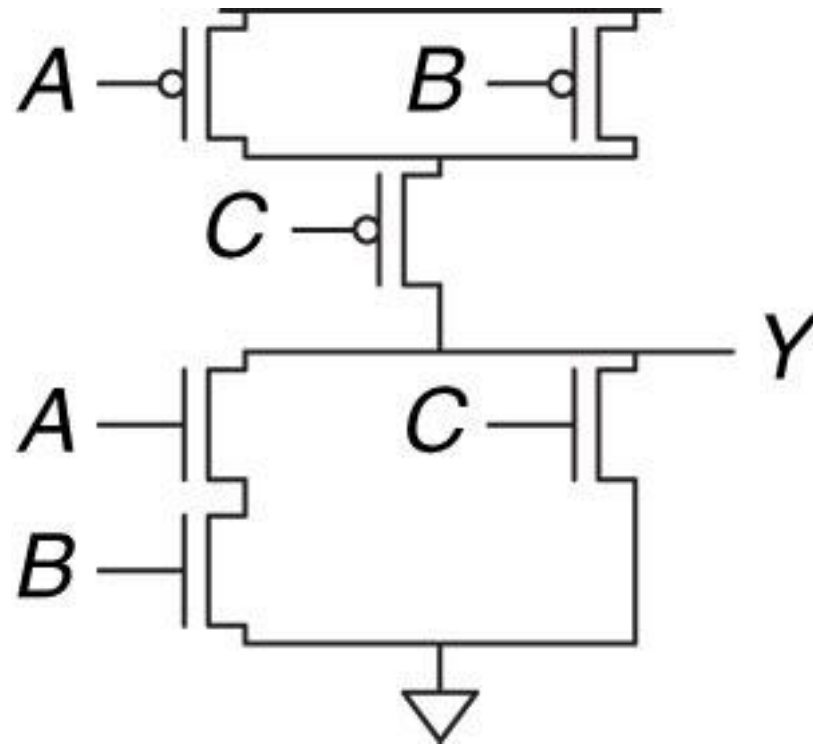


Figure 1.51 Mystery schematic

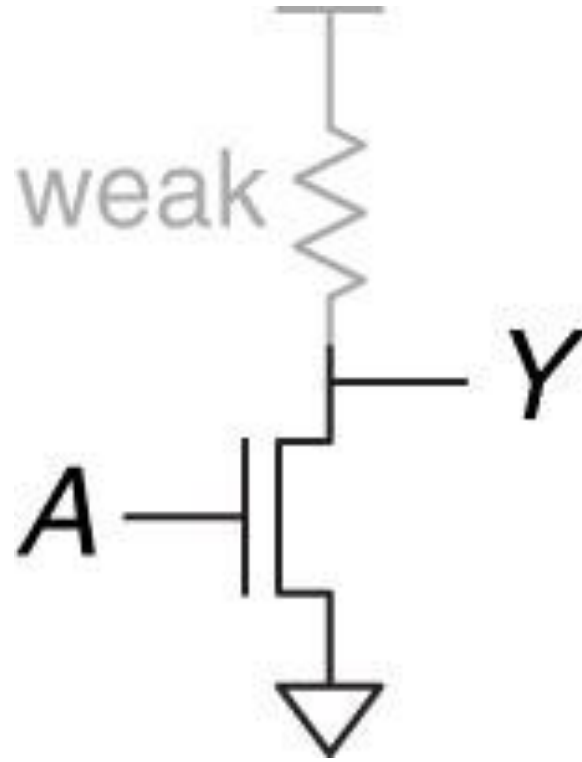


Figure 1.52 RTL NOT gate

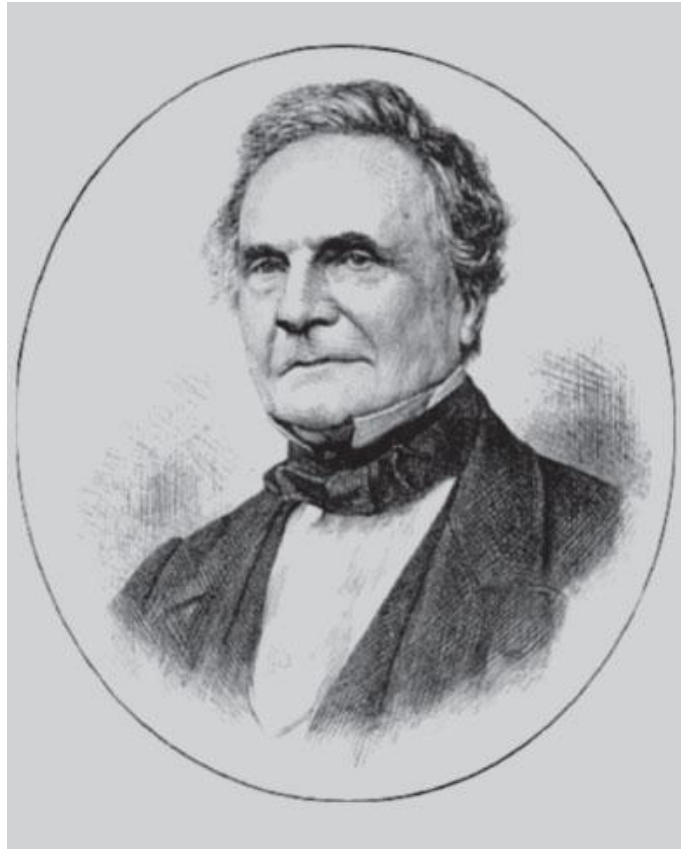


Figure M 02

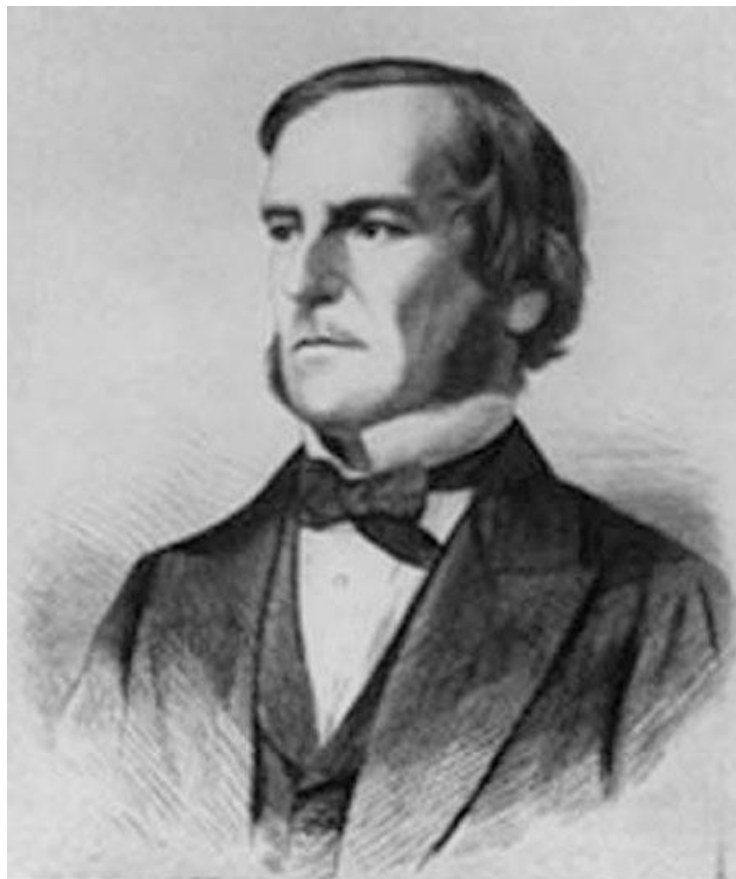


Figure M 03a



Figure M 03b

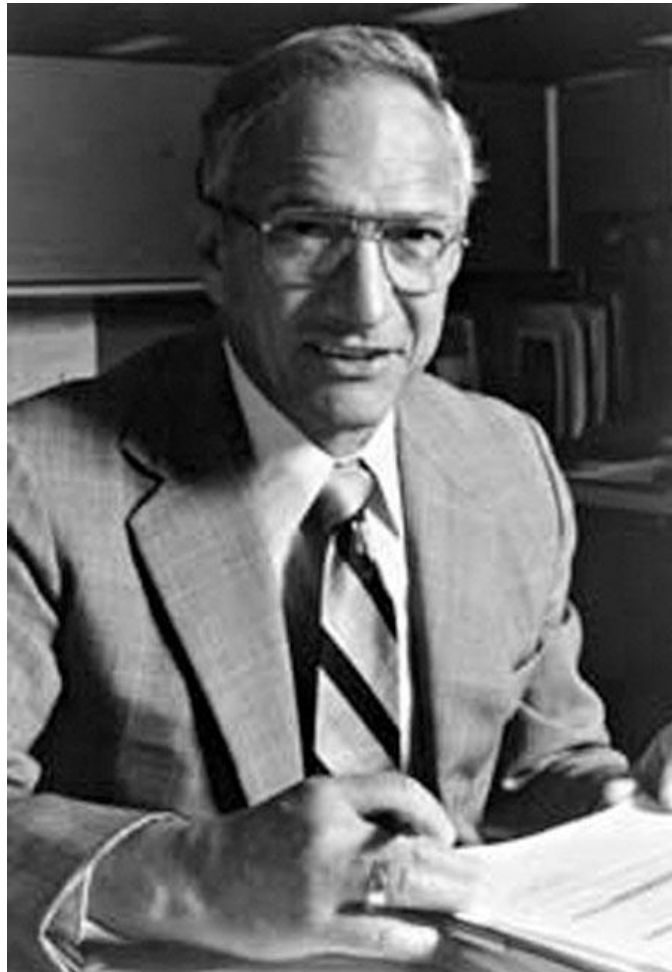


Figure M 04



Figure M 05

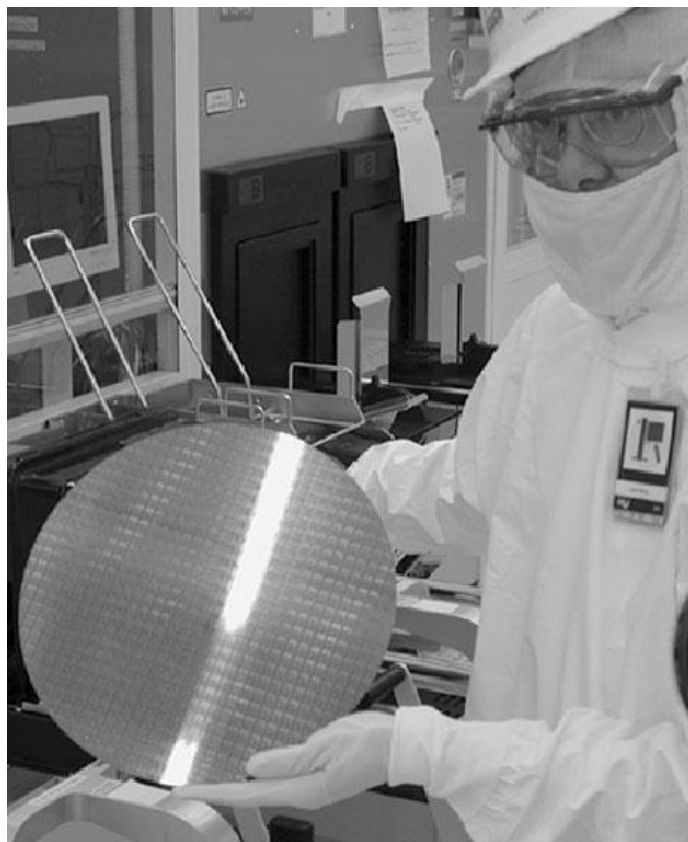


Figure M 06

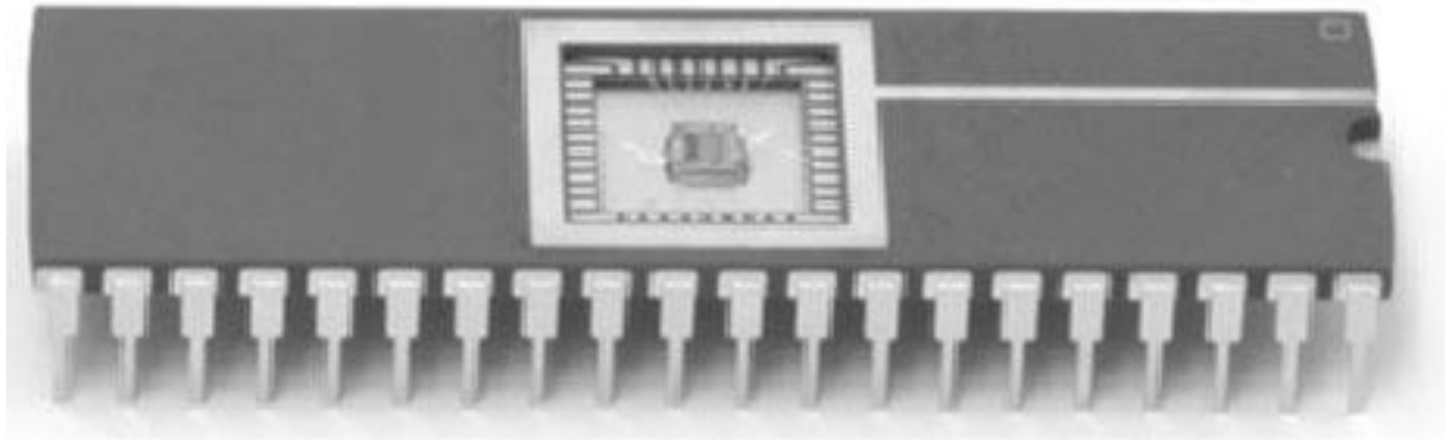


Figure M 07

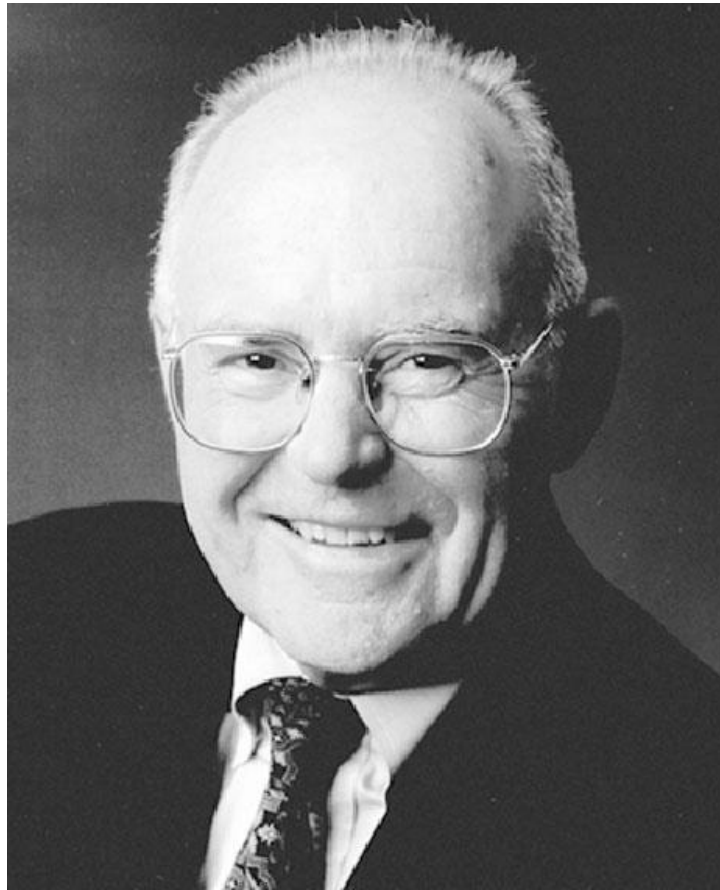
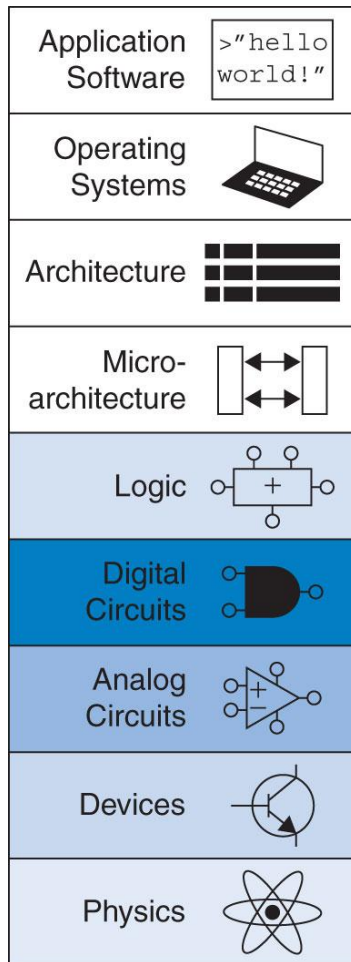


Figure M 08



Figure M 10



UNN Figure 1