2021 Edition

Chapter 10: Integrated Power Electronics

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Introduction

Although Power Electronics (PE) has far-reaching applications, the packaging technologies for PE circuits and systems are substantially common. This chapter focuses on the technologies for electronics packaging of the last few centimeters of electrical energy delivery to loads in high-performance computing, communications, mobile, automotive, industrial, medical and defense, with specific focus on System in Package (SiP) solutions that support loads and intellectual property (IP) blocks, such as CPU, GPU, FPGA, HBM and broader standalone loads in sensors, IoT and energy harvesting systems. As such, this Chapter is divided into four parts:

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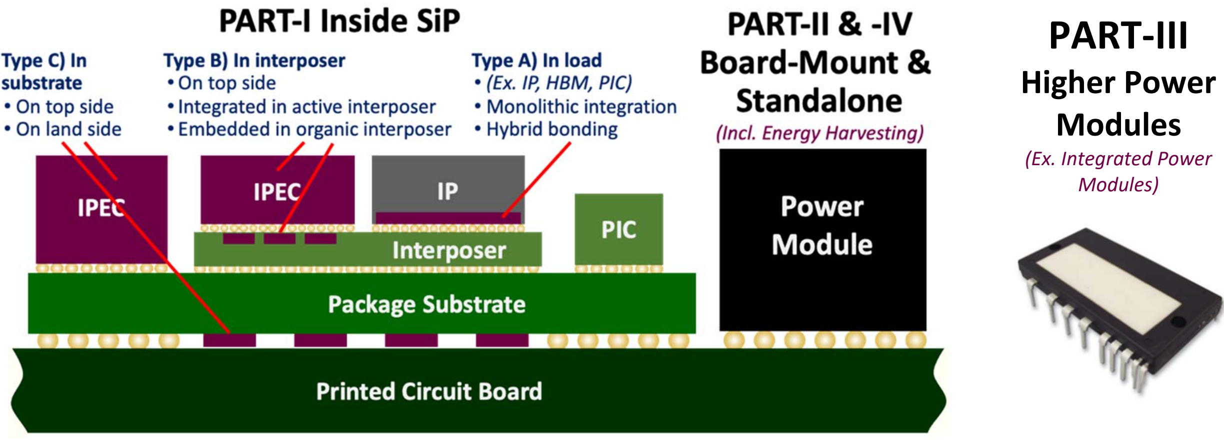
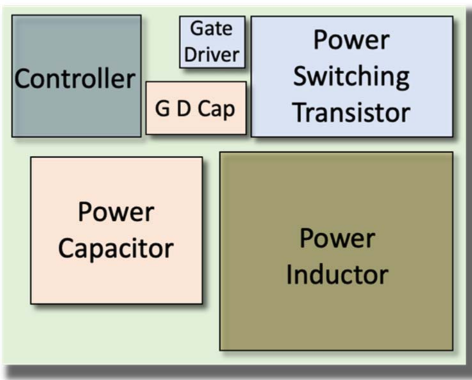
Contributors

An Integrated Power Electronics Component (IPEC), as used in this chapter, is defined in Figure 1. The IPEC embodies the primary functions of power conditioning as represented by power switching semiconductors, passive capacitor and inductor energy storage elements, a semiconductor gate driver with associated capacitor, and a controller. The IPEC may be implemented in its entirety as a standalone system component as discussed in Sections II, III and IV, or partitioned with portions, such as the power switching and control, implemented within IPs while energy storage is implemented within lower-cost real estate, such as interposers, as discussed in Section I.

The identification of the existing electronics packaging technologies and future development needs build from Section I to Section III and, though there is substantial commonality among the packaging technology approaches, redundancy in discussions is limited. Therefore, it is recommended that the reader move sequentially from Section I to Section III. Section IV is an evolving topic and will be expanded in the next revision of the HIR with closer alignment to Section II. Also, Chapter 10 primarily focuses on ≤48V/100A power conditioning. However, the basic technologies are applicable to much higher power levels. A graphical description of the areas addressed by each Section is shown in Table 1. The highlighted "IPEC" is described below.

Table 1. Graphic Description of Chapter Contents





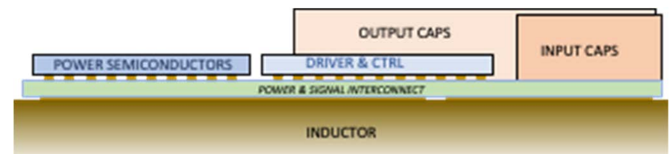


Figure 1. The "Integrated Power Electronics Component," IPEC, represents the electrical components and functions required for electronic conditioning of electrical energy delivered to the load(s). The IPECs may be partitioned and integrated in multiple ways within the System in Package, or be a standalone power electronic circuit for board-level power supply.

Heterogeneous Integration (HI) must be inclusive of power conditioning and delivery. While it is possible to supply power adjacent to one or more IP devices at the present time, such delivery will be impractical in the future to support the necessary speed and densities envisioned for heterogeneously integrated systems. Power delivery is one of the most critical elements that cross-cuts all application areas and clearly requires its own chapter in the roadmap. It is hoped that readers understand the PE packaging approaches, problems and technologies and can assimilate and morph solutions into their own IP packaging approaches to further deeper levels of integration.

Heterogeneous Integration also provides significant advantages to power electronics, as it permits integration of wide bandgap (WBG) power devices, e.g. GaN, with silicon control, logic, and memory devices, and with evolving passive devices. System-in-Package (SiP) and standalone power supply designers can use HI to address the primary challenges of power electronics: space, heat generation and electrical noise creation affecting communication, computation and sensor circuits. The challenges are divided into four categories: (1) reducing power converter size; (2) decreasing power path impedance; (3) delivering power efficiently; and (4) distributing clean, high-quality power at multiple voltages ranging from 48V to ≤1V to multiple levels of stacked packages. To reduce PE circuit size and path impedance, and achieve higher power processing densities, components need to be smaller and integrated closer together. Higher switching frequencies reduce component size and require closer location of components, which in turn reduces path impedance and radiated and coupled electrical noise. However, higher switching frequencies increase heating from increased power loss. Coupling the increased heating with densification greatly increases thermal densities and localized high-temperature regions. The densities are then limited by the practical worst-case junction temperatures of the semiconductors and longer-term reliability of packaging materials. The challenges are addressed in each Section of the Chapter specific to the packaging approaches addressed in that Section with the overarching focus on increasing frequency, reducing path impedance, increase efficiency and improve thermal management.

The reader is encouraged to contact any of the committee contributors to further discussions and answer questions. Also, please consider joining the committee to participate in the 2022 expansion and revision of this HIR Chapter by contacting Prof. Doug Hopkins, dchopkins@ncsu.edu, or Prof. Patrick McClusky mcclupa@umd.edu. Your input is greatly appreciated and needed.

Topical Discussion #1 – 3D Heterogeneous Integration of Actives and Passives for Discrete Power Modules

The power electronics community faces an escalating demand for efficient and integrated high-density power supplies for future computing needs. In order to meet this demand, power module technologies have made dramatic advances in the past decade, with advances in wide bandgap devices, innovative topologies, and more importantly with 3D power packaging technologies with advanced materials and process integration. Some of the advances include innovative multilevel and multiphase converter topologies with hybrid converters, high-density and thin passive components with higher efficiency at high frequencies, superior die-attach materials, thermal and thermomechanical reliability performance with high-Tg laminates, and high-power interconnects with innovative plated interconnects that can handle high currents. In spite of these advances, multiple challenges are foreseen in the future to meet the required targets of 1 W/mm^3 for low-power (1-30 W) and 0.1 W/mm^3 or >1000 W/in^3 for higher power (30 – 300 W) at efficiencies of above 95% to minimize thermal management challenges. This requires advances on all fronts: Designs, Materials for Packaging, Passives, Heat Spreaders and Die-Attach amongst others.

Need for thinner and vertically-integrated power delivery for efficient power supply is pushing the volumetric density and form-factors of future power modules. Higher switching frequency is critical for higher bandwidth, faster load transient response, and higher voltage scaling speed for better energy saving by dynamic voltage and frequency scaling. Higher current is required to meet the demand for higher functional integration. New topologies that can balance the voltage and current stresses while achieving higher switching speed and meeting the density, efficiency and electromagnetic compatibility with minimal EMI issues are required.

Surface assembly of passives is still the most common approach today in spite of its higher parasitics and lower volumetric efficiency and reliability challenges with solder interconnects. However, as the passives dominate the volume of the module, there is an increasing need to integrate passive component substrates. Both capacitors and inductors need to reach higher power-handling and efficiency in thinner form-factors for future power modules to meet the power density, size, weight and thickness targets. Because of their dominance in converter volume, passives may be used as the substrates themselves. Such examples to effectively utilize the substrate volume include the magnetic-embedded substrates and silicon trench capacitor substrate modules. Future magnetic materials are expected to deliver higher current/phase and higher frequencies with lower losses. Trench capacitors are becoming prevalent in replacing MLCCs because of their silicon scaling and integration advantages in spite of their limited volumetric densities with deep trench electrodes. Innovative nanoelectrodes will soon supersede trench capacitors in terms of performance.

The prevalent approach for power modules is to embed active switches and controllers in a leadframe or laminate with embedding or direct-plated off-chip interconnects. In all the approaches, 3D components on package with innovative through-via copper interconnects and thinner components are the key. These include copper clip interconnects and plated through-laminate or through-mold vias. The package design challenge is to balance the often conflicting electrical, thermomechanical and thermal management requirements. For example, high currents dictate the use of large amounts of copper; however, such large copper induces tremendous thermomechanical stresses on the thinned WBG devices. The materials challenge is to ensure long-term reliability in a high-temperature environment for an extended period, given the large number of disparate materials and their interfaces required. This requires high-temperature polymer dielectrics as well as polymer laminates, and CTE-matched heat-spreaders that co-exist with devices for addressing the local hot-spots from WBG heat dissipation. Pressureless assembly of devices with superior die-attach materials will be another key requirement.

Topical Discussion #2 – Heterogeneous Integration of Embedded Integrated Voltage Regulators

Fine-grain power management significantly improves energy efficiency (performance-per-watt) by up to 73%[1,2] by supplying the minimal voltage required at any given time to each load. It requires Integrated Voltage Regulators (IVRs) located in close proximity to the load to bypass the majority of the power distribution network (PDN) and associated impedance. Printed circuit board (PCB) mounted voltage regulators (VRs) cannot supply accurate voltages for fine-grain power management due to their high PDN impedance.[3] The way forward is PCB-mounted DC-DC converters that step down the system bus voltage to an intermediate voltage, which is then input to IVRs that perform voltage regulation.

The IVR challenges are to significantly reduce the interconnect resistance and parasitics between separately manufactured components (e.g., power transistors, gate drivers, controllers, capacitors and inductors), each made using their optimal manufacturing process, and to significantly reduce the z-dimension to enable integration in close proximity to the load. Monolithic integration cannot meet these IVR challenges.

Heterogeneous Integration (HI) refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics.[4] A potential solution is for IVRs to employ two levels of HI to enhance functionality and improve operating characteristics:

1) Disaggregate and tightly re-integrate separately manufactured components in an integrated power electronics component (IPEC) that provides multiple precisely regulated voltage outputs over a wide range (0.5-1.8V range) with increasing input voltage (3-5V),[5] current density (10-20A/mm^2) and switching frequency (5-50MHz), with high reliability, low thermal resistance and low cost in an ultra-thin z-dimension (100µm or less). Note: "IPEC" is synonymous with "VR chiplet," but does not have a chiplet standard interface.
2) Integrate IPECs in SiPs immediately under the load die, as shown in Figure 2, similar to silicon bridges, to provide vertical current flow for each voltage rail to its load from the PCB through the package substrate to the load die, minimizing lateral current flow and associated parasitics and significantly improving the PDN and fine-grain power management. Capacitors may be integrated in the load die and/or in the IPEC. SuperMIM capacitors, comprised of thin layers of different high-k materials each of few Angstroms thick stacked in a repeating superlattice, provide a 5x increase in MIM capacitance. Inductors may be integrated into the IPEC or into the package substrate.[6]

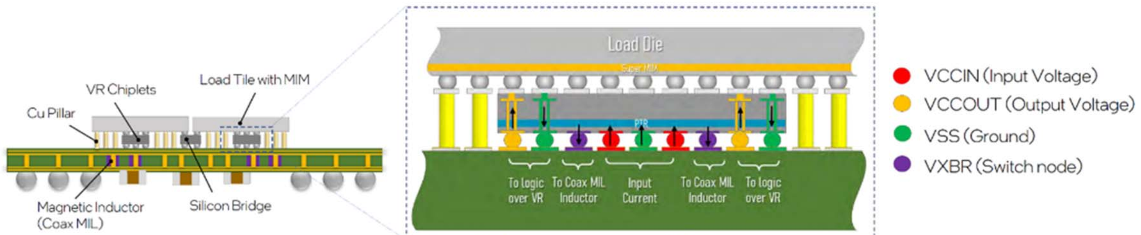


Figure 2. IPEC integrated below the die[6]

Required R&D includes panel-level packaging (PLP) employing a portfolio of state-of-the-art heterogeneous integration technologies (e.g., pick-and-place, die bonding, micro-transfer printing, RDL, through-substrate vias, sort/test, etc.); Electronic Design Automation (EDA) tools and Process Design Kits (PDKs) for heterogeneous integration; optimization of separately manufactured components for IVRs, including power transistors, gate drivers, controllers, inductors and capacitors; integrating arrays of separately manufactured components in IPECs customized for advanced topologies; and stacking separately manufactured components.

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Section I. Embedded Integrated Voltage Regulators

Glossary of Terms

BEOL	Back End of Line	MIM	Metal Insulator Metal
BSPDN	Back Side Power Distribution Network	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CoWoS-L	Chip on Wafer on Substrate - LSI	MTP	Micro-Transfer Printing
CPU	Central Processing Unit	PCB	Printed Circuit Board
CZT	Cobalt Zirconium Tantalum (CoZrTa)	PCPU	Power of CPU
DBHi	Direct Bonded Heterogeneous Integration	PDN	Power Distribution Network
DC	Direct Current	P_{in}	Input Power
DTC	Deep Trench Capacitor	PLP	Panel-Level Packaging
EMI	Electro-Magnetic Interference	PMIC	Power Management Integrated Circuit
EMIB	Embedded Multi-chip Interconnect Bridge	P_{out}	Output Power
ESL	Equivalent Series Inductance	PSiP	Power Supply in Package
ESR	Equivalent Series Resistance	PwrSoC	Power System on Chip
FIVR	Fully Integrated Voltage Regulator	RDL	Redistribution Layer
FPGA	Field Programmable Gate Array	R_{mb}	Motherboard Resistance
FSPDN	Front Side Power Distribution Network	R_{pkg}	Package Resistance
GaAs	Gallium Arsenide	sFOCoS	Stacking Fan-Out Chip on Substrate
GaN	Gallium Nitride	SiC	Silicon Carbide
GPU	Graphics Processing Unit	SiP	System in Package
HBM	High Bandwidth Memory	SKU	Stock Keeping Unit
HEMT	High Electron Mobility Transistor	SOC	System on Chip
HI	Heterogeneous Integration	VCCIN	Input Voltage
I_{out}	Output Current	VCCOUT	Output Voltage
IPD	Integrated Passive Device	V_{out}	Output Voltage
IPEC	Integrated Power Electronics Component	VR	Voltage Regulator
IVR	Integrated Voltage Regulator	VRM	Voltage Regulator Module
L/S	Line / Space	VSS	Ground
LDO	Low Drop-Out	VXBR	Switch Node

I.1. SUMMARY

Fine-grained power management significantly improves energy efficiency (performance-per-watt) by up to 73%,[1,2] by supplying the minimal voltage required at any given time to each load. It requires Integrated Voltage Regulators (IVRs) located in close proximity to the load to bypass the majority of the power distribution network (PDN) and associated impedance.[3] Printed circuit board (PCB) mounted voltage regulators (VRs) cannot supply accurate voltages for fine-grain power management due to their high PDN impedance. The way forward is PCB-mounted DC-DC converters that step down the system bus voltage to an intermediate voltage which is then input to IVRs that perform voltage regulation.

The IVR challenges are to significantly reduce the interconnect resistance and parasitics between separately manufactured components (e.g., power transistors, gate drivers, controllers, capacitors and inductors), each made using their optimal manufacturing process, and significantly reduce the z-dimension to enable integration in close proximity to the load. Monolithic integration cannot meet the IVR challenges.

The success of silicon integration at low power levels has been driven by the ability to integrate at competitive prices more complex systems than could be accomplished with discrete elements: multi-phase and distributed power conversion can be implemented with no significant added cost relative to single-phase converter architecture. Additionally, complex monitoring, protection, margining, etc., can be easily implemented when the whole system is contained in a single silicon device. Unfortunately, such capabilities do not easily extend to higher current/voltage levels, as silicon devices are limited by the process utilized, so that they cannot address the diverging requirements imposed by higher-power applications. Heterogeneous Integration (HI) enables the coexistence of differently optimized technology within an assembled unit, while still benefiting by reduced electrical distances, dense signal paths and high-current advanced interconnects, thus providing similar system-level benefits as are achieved by silicon integration.

Heterogeneous Integration (HI) refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved

operating characteristics.[4] A potential solution is for IVRs to employ two levels of HI to enhance functionality and improve operating characteristics:

- Disaggregate and tightly integrate separately manufactured components in an integrated power electronics component (IPEC) that provides multiple precisely regulated voltage outputs over a wide range (0.5-1.8V range) with increasing input voltage (3-5V),[5] current density (10-20A/mm^2) and switching frequency
(5-50MHz) and high reliability, low thermal resistance and low cost in an ultra-thin z-dimension (100µm or less). Note: "IPEC" is synonymous with "VR chiplet," but does not have a chiplet standard interface.
- Integrate IPECs in SiPs immediately under the load die (Figure 1), similar to silicon bridges, to provide vertical current flow for each voltage rail to its load from the PCB through the package substrate to the load die, minimizing lateral current flow and associated parasitics and significantly improving the PDN and fine-grain power management. Capacitors may be integrated in the load die. SuperMIM capacitors, comprised of thin layers of different high-k materials each of few Angstroms thick stacked in a repeating superlattice, provide a 5x increase in MIM capacitance. Inductors may be integrated in the package substrate.[6]

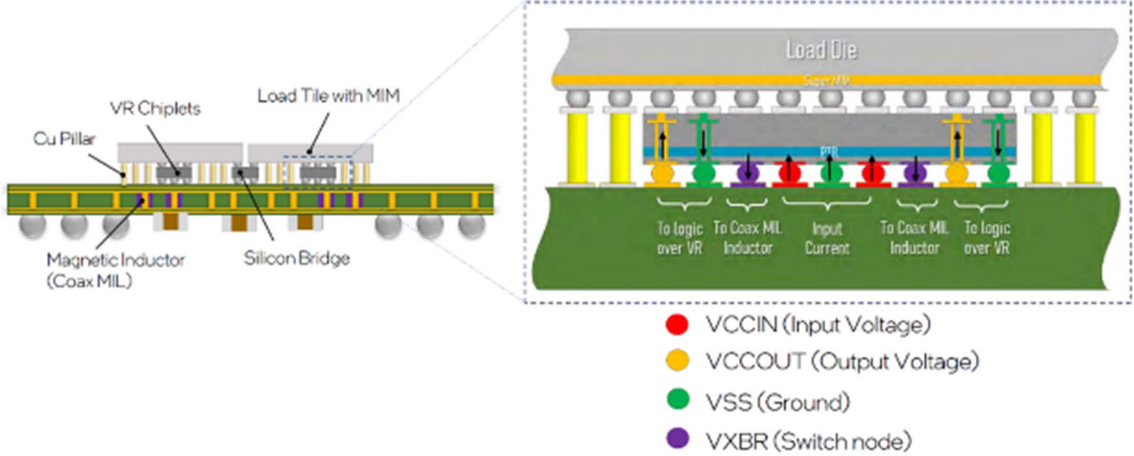


Figure I-1: IPEC integrate below die[6]

I.2. REQUIREMENTS

This section discusses the following requirements for IPECs:

- Modularity
- Fine-grain power management employing multiple buck regulators with fast transient response
- Low-impedance power distribution network (PDN)
- 0.5V to 1.8V output voltage
- 5-50MHz switching frequency
- 3-5V input voltage
- 10-20A/mm^2 output current density
- <100 µm thickness
- High system efficiency
- Ultra-low thermal resistance
- High reliability
- Cost effective: panel-level processing (PLP), high yield, known good die, modularity

Some of these requirements cannot be quantified in a "roadmap," because they must meet a "threshold" (i.e., be "good enough") which varies with application. For example, IVRs must have high reliability and be cost effective, but the specific reliability and cost targets are different for, say, mobile versus automotive applications. Similarly, IVRs must provide high efficiency, but specific efficiency targets depend upon the application whose goal is to maximize overall system energy efficiency (performance-per-watt) as opposed to IVR efficiency. Table 1 summarizes the IPEC requirements for IVRs. Over time the input voltage, switching frequency and output current density increases, the thickness decreases and output voltage range does not change much. In addition, as increasing numbers of phases are integrated in each IPEC, IPEC reliability improves and there's continuous improvement in reducing thermal resistance and cost.

Table I-1: IPEC Requirements for IVRs

Metric	Generation			
	1	2	3	4
Input voltage (V)	3	3	5	5
Switching Frequency (MHz)	5 – 10	10 – 50	5 – 10	10 - 50
Output current density (A/mm^2)	10	20	10	20
Output voltage (V)	0.5 - 1.8			
Thickness (µm)	<100			

PCB-mounted DC-DC converter requirements are discussed in Section II of this chapter. IPEC requirements for IVRs include the following:

Modularity: IPECs are small, modular building blocks for integration in SiPs having multiple loads, each with different power delivery requirements. SiPs are increasingly disaggregated SoCs (Figure 2)[7] that integrate multiple CPU, FPGA, custom accelerator, cache, memory, I/O, networking and other "chiplets" (also knowns as "tiles" or "IP blocks"). The SiP power delivery requirements vary widely depending upon the application, which include high-performance computing and data centers, mobile, automotive, aerospace and defense, Internet of Things (IoT), and medical, health and wearables (discussed in other chapters in the Heterogeneous Integration Roadmap). The SiP body size ranges from <100mm^2 (10x10mm) to >10,000mm^2 (100x100mm); the number of load die range from 2 to >10; the number of voltage rails/phases range from <10 to >100; and the SiP current demand ranges from <10A to >1,000A. Similar to the general heterogeneous integration approach of re-using die, mix-and-matching them to build a family of different SiPs, the power delivery approach is to integrate a number of IPECs in different SiPs to meet specific current demand and voltage rail/phase count requirements and re-use IPECs in a wide range of SiPs for many different applications. IPECs may be readily integrated into a wide range of packaging technologies, including 2D, 2DO organic-based, 2DS inactive silicon or glass-based, and 3D architectures (Figure 4).[8] Refer to Chapter 21 SiP and Module System Integration and Chapter 22 Interconnects for 2D and 3D Architectures of this Heterogeneous Integration Roadmap. The IPEC input voltage is 3-5V to meet applications which use both:

- 3-5V system buses, such as mobile and IoT
- Higher system bus voltages with multi-stage DC-DC conversion, since single-stage conversion is impractical with increasing input voltages and switching frequencies and decreasing output voltages.[9] Multi-stage DC-DC conversion (Figure 3) uses one or more PCB-mounted DC-DC converters to step down a higher system bus voltage (12-48V) to an intermediate voltage (3-5V) input to the IVRs as discussed in Section II of this Chapter. The IVRs supply many 0.5-1.2V rails to the many loads in the SiP. For some rails, LDOs (low drop out linear regulators) integrated on the load die provide additional voltage regulation. The PCB-mounted DC-DC converter may still supply some rails directly to the load die.[10]

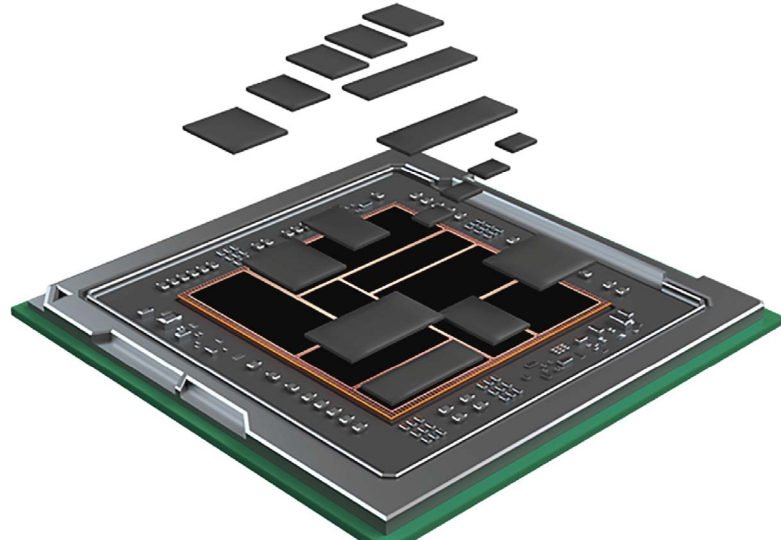


Figure I-2: Disaggregated SoC[7]

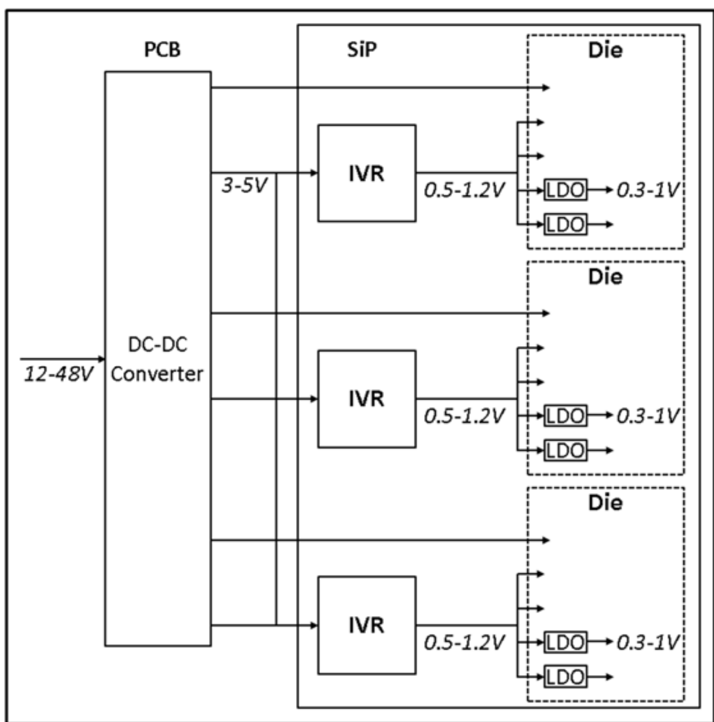


Figure I-3: Multi-Stage DC-DC Conversion[10]

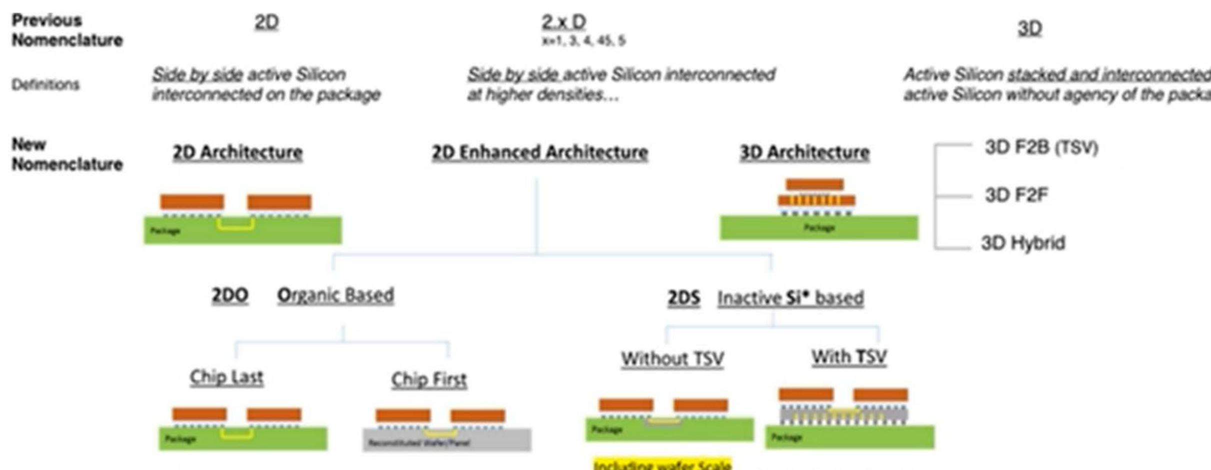


Figure I-4: Package Architectures[8]

Fine-grain power management employing multiple buck regulators with fast transient response significantly improves energy efficiency by operating each load at its minimal voltage required at any given time. Load power dissipation is highly dependent on voltage, increasing more than quadratically with supply voltage when considering thermal degradation and leakage power in addition to dynamic power. For <10nm processes, power increases by 3% for every 10mV increase in supply voltage.[11] Hence, precise voltage regulation is required because margins reduce the performance and power efficiency.[12] Fast Dynamic Voltage Frequency Scaling (DVFS) changes the voltage and switching frequency individually for each load on the fly (Figure 5) in response to rapid changes in the workload or operating conditions (e.g., temperature and aging).[13] DVFS varies the voltage between low levels to minimize power consumption during standby operation, to high levels to maximize performance during peak operation. DVFS requires many independent voltage regulators to supply multiple voltage domains with very accurate voltage levels, and fast transient response[14] to multiple loads (Figure 6). The historical increase in power rail count (Figure 7) will continue with integration of an escalating number of cores (Figure 8).[3] DVFS significantly increases the SiP performance and decreases its power consumption.[1]

Adaptive Body Bias (ABB) is used to adjust the device body voltage to reduce leakage current. Whereas DVFS is effective to address dynamic power consumption, it is less effective in reducing leakage power; ABB is effective

in lowering leakage power consumption. ABB has been shown to reduce leakage current exponentially while DVFS reduces leakage linearly.[15] With ABB, a voltage is applied between the source or drain and the substrate to change the threshold voltage (Vth) of a transistor – forward-biasing to reduce Vth to provide a faster, leakier transistor, and reverse-biasing to increase Vth to provide a slower, less-leaky transistor. ABB can be applied to the whole chip or, with Fine-Grain Body Biasing (FGBB), can be applied separately to regions of a chip such as to each core on a multicore processor.[16]

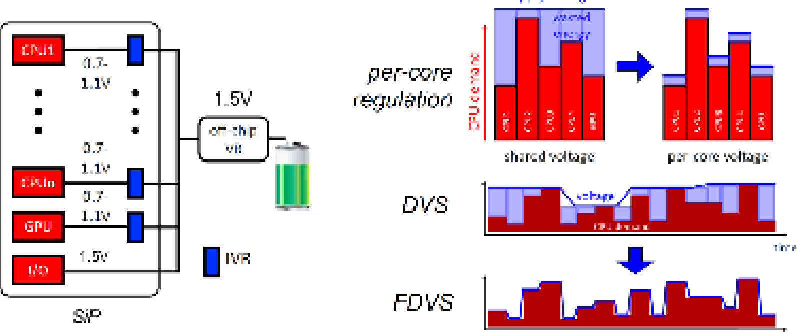


Figure I-5: Fast Dynamic Voltage Scaling[14]

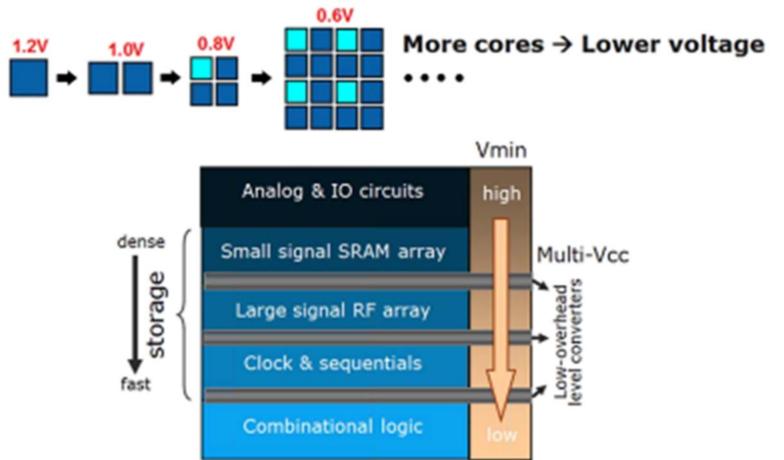


Figure I-6: Multiple Voltage Domains[1]

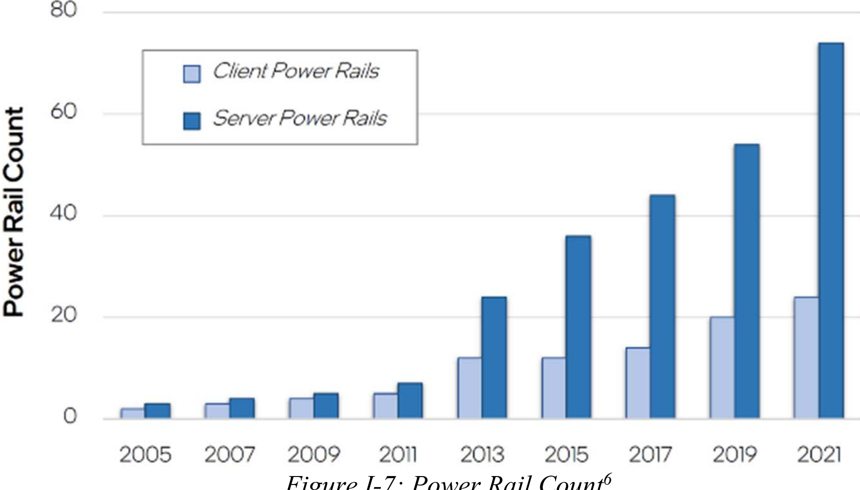


Figure I-7: Power Rail Count[6]

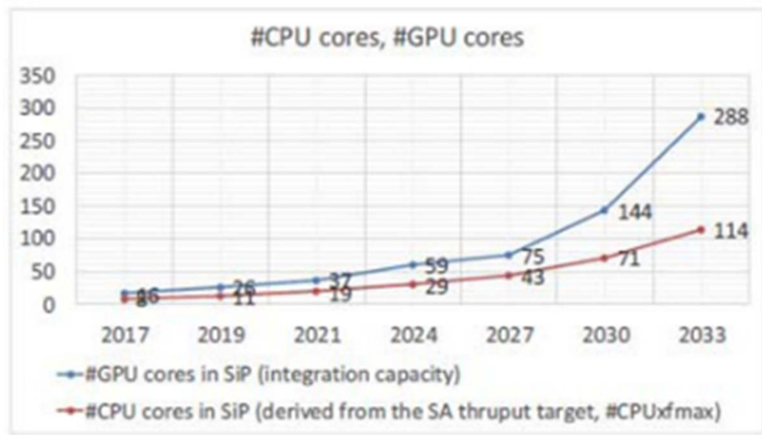


Figure I-8: IRDS projection of number of CPU and GPU core in an 80mm² area[3]

Low impedance power distribution network (PDN): Low-impedance PDNs are needed to supply loads with voltages within a tightly controlled operating range, and this need is escalating with advanced CMOS nodes having the operating voltage in close proximity to threshold voltage. For example, a 20mV variation is a much larger percent variation when the operating voltage is 500mV versus 900mV.[17] Load current consumption can change dramatically from cycle to cycle, and spikes in current draw cause the voltage to droop.[3] Voltage overshoots and undershoots must be minimized during load changes and input power supply fluctuations. A voltage that is too low can cause timing issues resulting in failure, and a voltage that is too high results in excessive power consumption and compromised reliability. There are penalties for adding generous guardbands.[17] The voltage regulator's bandwidth and the PDN's impedance[18] determine the amount of voltage droop in response to a load change. A steeper load line (Figure 9) results in significant power loss due to an operating voltage that is significantly higher than the minimum voltage required.[19] The PDN's impedance must be kept low across a wide range of frequencies by minimizing inductive, capacitive and resistive parasitics, and its voltage gradient across spatially distributed voltage domains must be minimized. In addition, routing losses in the path from the voltage regulator to the load must be minimized since they have a quadratic dependence on current. PCB-mounted VRs cannot supply accurate voltages for fine-grain power management due to their high PDN impedance (Figure 10 and Figure 11), so the way forward is PCB-mounted DC-DC converters that step down the system bus voltage to an intermediate voltage, which is then input to IVRs that perform voltage regulation and bypass the majority of the PDN impedance (Figure 12 and Figure 13). Since IVRs supply low voltage (<1V) and high current (10's to 100's of amps), the IVR-to-load PDN must have minimal series resistance and inductance.

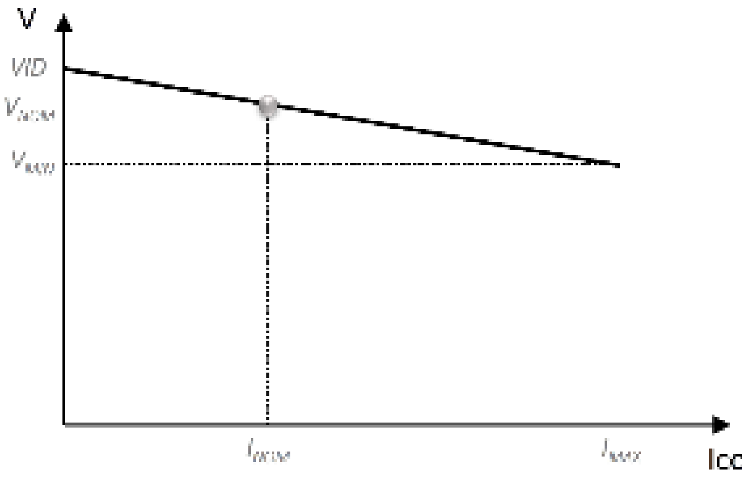


Figure I-9: Load Line[20]

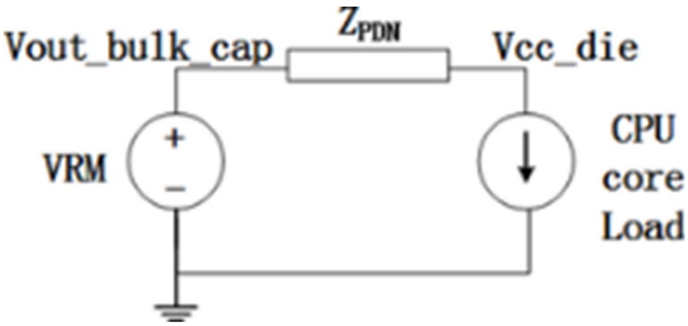


Figure I-10: High Impedance PDN Due to External VRM[3]

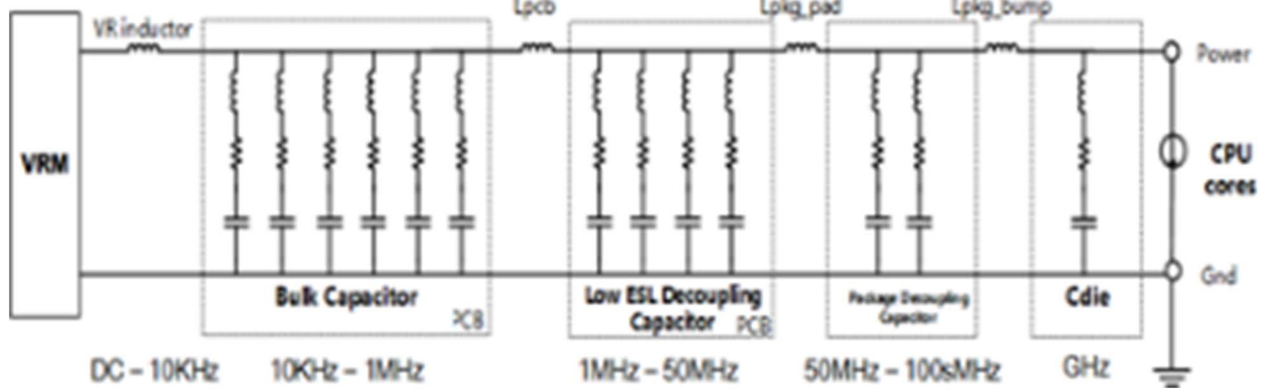


Figure I-11: PDN With External VRM[3]

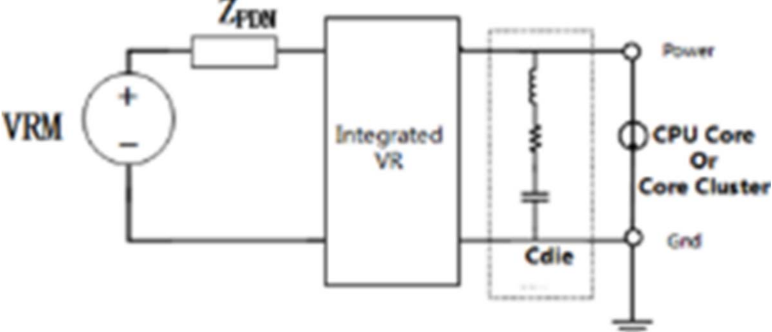


Figure I-12: IVRs bypass PDN bottleneck[3]

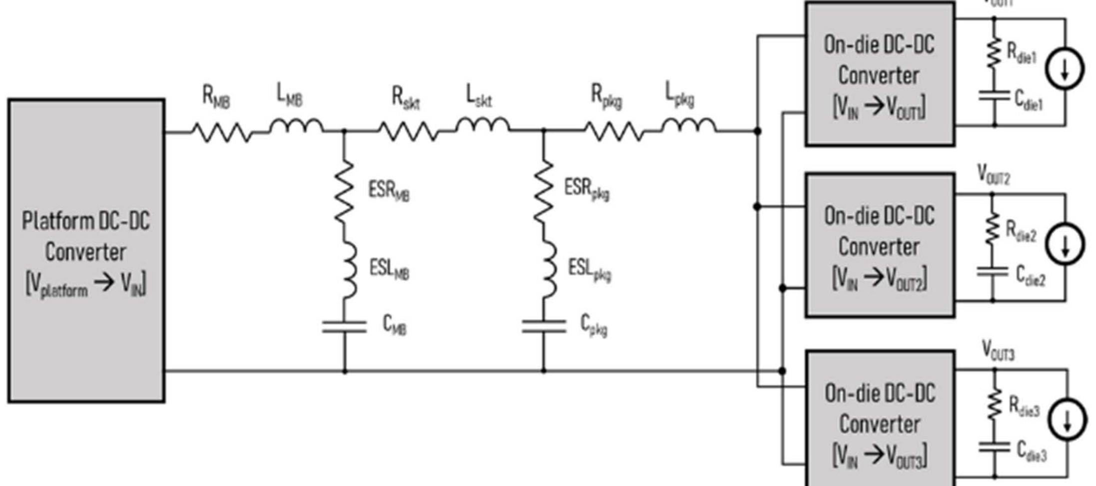


Figure I-13: IVRs Supplement VRMs[5]

Input voltage in the 3-5V range[5] is needed to balance being low enough to support high switching frequency and high enough to reduce the PDN's routing loss for support of escalating output power (Figure 14) and reduce the

number of power/ground pins, which compete with I/O. Additional factors that determine the optimal IVR input voltage include the proximity of the first stage DC-DC converter to the IVR and whether the first stage is regulated versus unregulated and centralized versus distributed.[21,22]

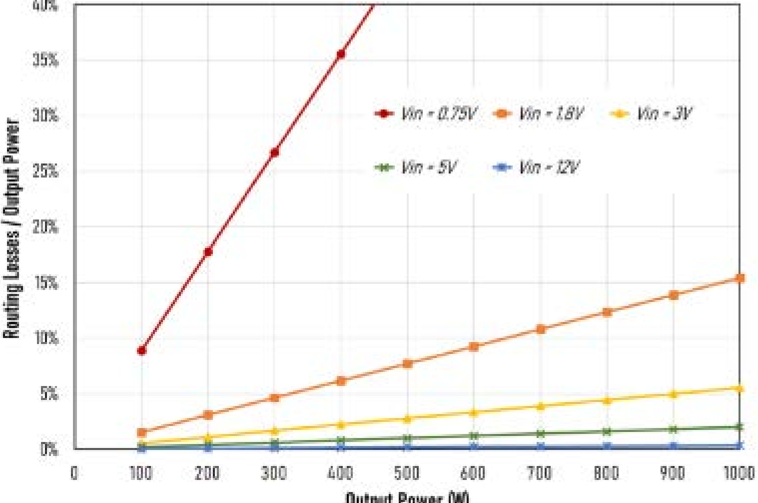


Figure I-14: Routing Losses[5]

Switching frequency in the 5-50MHz[5] range is needed to balance being low enough to support low duty cycles (output voltage divided by input voltage) and high efficiency, and high enough to reduce the size of the inductors and capacitors and to increase the control loop bandwidth (which is approximately 10% of switching frequency), improving transient response. Low-bandwidth VRs require additional decoupling capacitors to make up for their slow response time.

Output voltage range in the 0.5V to 1.8V range is needed to support SiPs integrating a diversity of load die made using different process nodes and having different voltage requirements. Input voltages of 0.5V to 1.2V are typical for digital loads (the lower voltages to minimize power consumption during power-saving operating modes and the higher voltages to maximize performance during peak operating modes) and 1.2V to 1.8V for analog loads.

Output current density in the 10-20A/mm^2 range is needed to keep up with escalating SiP power density. The power density trend in the last decade (Figure 15) will continue with CMOS scaling to 5nm, 3nm, 2nm nodes and beyond and heterogeneously integrating many diverse die in large-area (>100x100mm) substrates. High-end SiPs will draw more than 1,000A in the near future, driving the need to achieve high current density for other IVR components.

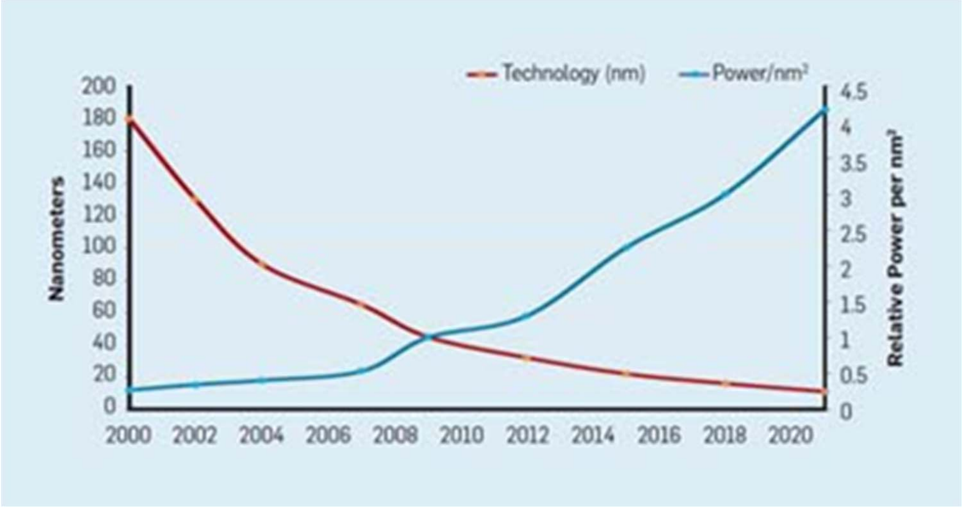


Figure I-15: Transistor scaling and chip power density trend[3]

Ultra-low thermal resistance is needed to facilitate heat removal, which is a major challenge and limiting factor, since (i) IVRs share the SiP's limited thermal envelope with the load die, and (ii) IVRs having high current densities

are located in close proximity to loads having high power densities, which are forecasted to increase to >2W/mm^2 average with >9W/mm^2 hotspots (Figure 16).[23] IVRs must not exacerbate these hotspots and will require thick copper interconnects to minimize thermal resistance.

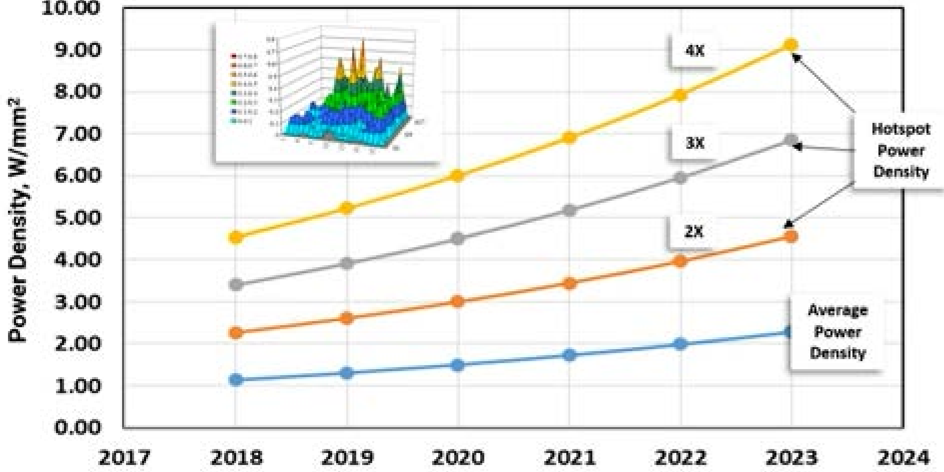


Figure I-16: Load Die's Power Density Trend[23]

High system efficiency is needed to maximize SiP performance-per-watt, which is the key performance metric, as opposed to maximizing the IVR efficiency. Counter-intuitively, IVR efficiency that is lower than PCB-mounted VR efficiency may be acceptable due to IVRs improving fine-grain power management and the PDN network. The voltage accuracy (i.e. minimized voltage variation) at the on-die power grid has far greater impact on energy efficiency than VR conversion efficiency,[24] and the reduction in PDN routing losses can be more than enough to offset the voltage regulator's conversion losses. For example, a 97% efficient first stage followed by an 88% efficient second stage voltage regulator (i.e., 85% combined efficiency) provides higher system efficiency than a single stage 90% voltage regulator (Table 2). In addition, SiP performance-per-watt can be increased with short-duration peak current operating modes for individual loads. Due to the short duration, IVR efficiency is not important during these peaks. (The challenges is maintaining high reliability during peak operation). Lastly, system energy proportionality (whereby energy consumption scales with workload) is important and requires multi-phase IVRs with phase shedding, whereby IVR phases are progressively turned on/off depending upon workload.

Table I-2: System Efficiency - Single Stage PDN vs. Dual Stage PDN[5]

Parameter	Single Stage PDN	Dual Stage PDN
CPU Power (P_{CPU})	100 W	100 W
Output Voltage (V_{OUT})	1 V	1 V
Output Current ($I_{OUT} = P_{CPU}/V_{OUT}$)	100 A	100 A
VR2 Input Voltage (V_{IN2})	1 V	3V
VR2 Efficiency (η_2)	100%	88%
VR2 Input Power ($P_{IN2} = P_{CPU}/\eta_2$)	100 W	113.6 W
PDN Current ($I_{PDN} = P_{IN2}/V_{IN2}$ or I_{OUT})	100 A	37.9 A
Package Resistance (R_{PKG})	0.5 mΩ	0.5 mΩ
Package Losses ($P_{PKG} = I_{PDN}^2 \times R_{PKG}$)	5 W	0.7 W
MB Resistance (R_{MB})	1 mΩ	1 mΩ
MB Losses ($P_{MB} = I_{PDN}^2 \times R_{MB}$)	10 W	1.4 W
Routing Losses (P_R $P_{PKG} + P_{MB}$)	15 W	2.1 W
VR1 Output Power ($P_{OUT1} = P_{IN2} + P_R$)	115	115.7 W
VR1 Efficiency (η_1)	90%	97%
VR1 Input Power ($P_{IN1} = P_{OUT1}/\eta_1$)	127.8 W	119.3 W
System Efficiency ($\eta_{sys} = P_{CPU} / P_{IN1}$)	78.3%	83.8%

IVR power loss is due to conduction loss, switching loss and charge loss (Figure 17). The challenges for 3-5V input, high current density IVRs are to (i) minimize the conduction loss by minimizing the power transistor's on-

resistance and interconnect resistance, and (ii) minimize the switching loss by minimizing the parasitics in the gate drive and power loops (Figure 18)[25] to minimize the turn on/off time, dead time and loop inductance. The interconnects are a major limiter, because to achieve high efficiency along with high current density requires integrating in a minimal footprint (i) high current interconnects (VCCIN, VCCOUT, VSS, VXBR as shown in Figure 1), (ii) gate distribution with ultra-low parasitics, and (iii) control, protection and monitoring interconnects to each phase. Charge loss is moderate with 3-5V voltage input and moderate switching frequency but becomes substantial with increasing input voltage and switching frequency. The tradeoff is between minimizing conduction loss versus switching loss, since increasing the power transistors' gate periphery reduces its on-resistance (conduction loss) but increases its switching loss and vice versa.

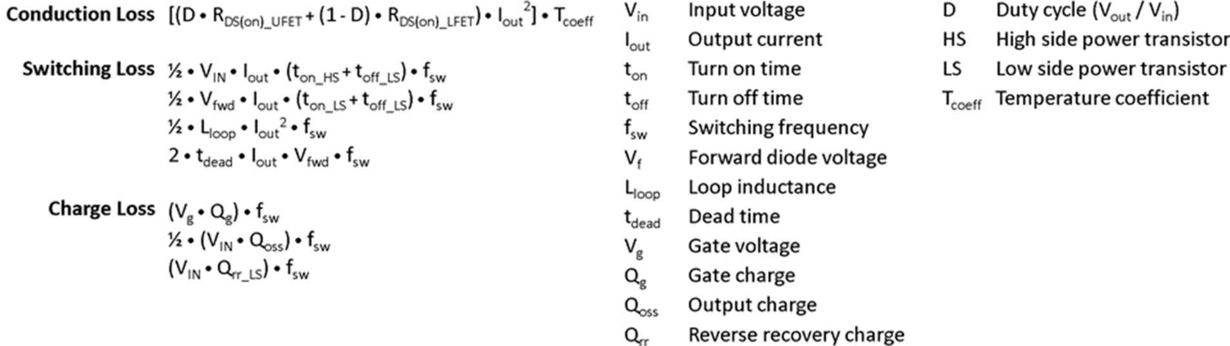


Figure I-17: Buck Regulator Power Loss Equations

Figure I-18: Parasitics in Gate Drive and Power Loops[25]

High reliability is needed to ensure operation at all times in the safe operating area, which is typically well below the rated voltage, maximum allowable junction temperature and maximum allowable current density, and meet reliability standards, such as IPC-9592B: Requirements for Power Conversion Devices for the Computer and Telecommunications Industries.[26,27] High reliability requires using proven materials and manufacturing processes and employing structures that minimize stresses and coefficient-of-thermal-expansion (CTE) mismatches.

Low cost is necessary for IPECs to be used in a wide range of SiPs and applications and not limited to only high-performance applications that can afford price premiums. Low cost requires:

- **Panel-level processing (PLP):** Embedded Chip or Fan-Out are promising technologies to integrate the separately manufactured IVR components into an IPEC that can be mounted within the SiP. Manufacturing these IPECs on panels that have three-times the area of wafer-level processes (Figure 19)[28] and use inexpensive panel area rather than expensive semiconductor area for the high-current interconnects, are required to meet low costs. Historically, high-performance "compute" applications (e.g., CPUs, GPUs, FPGAs and HBMs) have been the market drivers for heterogeneous integration. These applications require very high interconnect density (to increase bandwidth, decrease latency and improve power efficiency) and ultra-fine (<1µm/1µm) line width/space (L/S) design rules. PLP challenges for the compute applications are (i) providing ultra-fine L/S and (ii) since each panel contains a large number of die, very high volumes are required to make the business case for PLP manufacturing facilities. In contrast to compute applications, IPECs require interconnects having much higher current density but lower interconnect density, so coarse (>10µm/10µm) L/S design rules are sufficient. IPECs are an attractive market driver for PLP since they do not require ultra-fine L/S and address large markets having very high volumes.
- **High yield:** Complex HI SiPs will require IPECs with multiple IVRs, each having multiple separately manufactured active and passive components. Utilization of multicomponent PLP to achieve low costs can only be successful with high IPEC module yields. Since a complex IPEC will have multiple bare chips as well as passive devices, these components must have intrinsically high yields prior to subsequent integration. In addition, the integration process must have high yields and must use mature, well-proven materials and manufacturing processes and relaxed design rules.
- **Known good die:** IPECs need to be tested and binned prior to integration in the SiP.

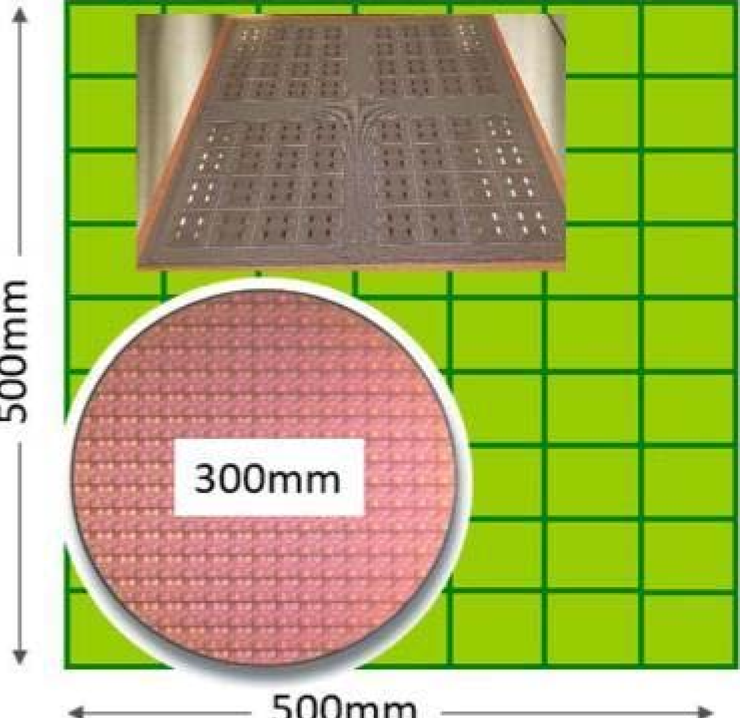


Figure I-19: Dimensional difference between 300mm wafer and 500x500mm panel[28]

Ultra-thin z-dimension: The IPEC must be thin (<100µm) to facilitate integration in close proximity to the load die in a wide range of package architectures.

I.3. EXISTING SOLUTIONS AND CHALLENGES

Existing solutions and their challenges for meeting the requirements described above are:

Converter topology technologies include:

- Low-drop out (LDO) linear regulators, which are limited to regulating the output voltage close to the input voltage since their efficiency is proportional to output voltage divided by input voltage.
- Switched-capacitor converters, which use capacitors for energy storage, are well-suited for a fixed input to output voltage conversion ratio but suffer from low efficiency when the conversion ratio deviates from the optimal.
- Switched-inductor voltage regulators (buck converters),[29] which use inductors as the energy storage element, are widely used for regulating an output voltage that is much lower than the input voltage.
- Advanced topologies, including multi-level buck converters and hybrid and resonant switched-capacitor converters,[30] improve performance and reduce voltage requirements but require an increased number of power transistors, gate drivers and passive components.

PCB-mounted VRs have historically been used for the vast majority of today's VR applications, but they are inadequate for supplying accurate voltages for fine-grain power management[3] due to their high PDN impedance which adds tens of millivolts extra voltage guard band, limited number of power rails and slow transient response. PCB-mounted VRs, discussed in more detail in Section II, include the following:

- Discrete power components (i.e., power transistors, gate drivers, controllers, capacitors and inductors), each separately manufactured using their optimal manufacturing process, are mounted on the PCB. This solution is very low density due to the number of discrete components and low (<1MHz) switching frequency, resulting from high parasitics between the components and high switching loss, requiring bulky passive components.
- Power management integrated circuits (PMICs) monolithically integrate power transistors, gate drivers and controllers along with a host of application-specific power management functions. Their inductors and capacitors are mounted on the PCB. Given the conduction versus switching loss tradeoff, PMIC's switching frequency decreases (requiring bulky passive components) as their input voltage and/or output current increases. PMICs for smartphones typically support 2.8-5.5V input voltage with multiple phases and independent outputs, and they can support up to approximately a total 20A output current with <1MHz switching frequency or up to 10 MHz switching frequency with <1A output current. PMICs for up to 48V input support low output current at <1MHz.
- Integrated regulators (like PMICs) monolithically integrate power transistors, gate drivers and controllers, and their inductors and capacitors are assembled on the PCB. Since they target a wide range of applications, they (unlike PMICs) do not integrate application-specific power management functions. Given the conduction versus switching loss tradeoff, they support high output current at low switching frequency or vice versa.
- Power stages integrate separately manufactured power transistor and driver die in a package. Their controller, inductors and capacitors are mounted on the PCB. High-current applications parallel multiple power stages in a multi-phase buck converter. They are optimized to provide high output current and high efficiency, so their switching frequency is typically less than 1MHz, requiring bulky inductors and capacitors.
- Power Supply in Packages (PSiPs) integrate controller, power transistor, and gate driver die along with the inductors and some of the capacitors in a package (with additional capacitors mounted on the PCB). Existing PSiPs range from small packages which support low input voltage and output current to bulky packages which support higher input voltage and output current. PSiPs can be paralleled to support higher output current. Given the conduction versus switching loss tradeoff, they support high output current at low switching frequency or vice versa.

Challenges include simultaneously increasing both the switching frequency to 5-50MHz and current density to 10-20A/mm^2 while also significantly reducing the z-dimension to less than 100µm. Incremental improvements in PCB-mounted VR technology cannot meet these challenges, so new disruptive technology is needed.

Monolithic integration technology is well-suited for low-voltage power components, such as controllers and capacitors, but poorly suited for integrating power components that require higher voltages and current densities. Monolithic integration technologies include the following:

- Integrating LDOs on the load die are well-suited for rails where the output voltage is close to the input voltage but have unacceptably low efficiency for large voltage step-downs.
- Integrating switched-capacitor converters on the load die are well-suited for rails where the output voltage is an optimal ratio of the input voltage but have unacceptably low efficiency if the ratio deviates from the optimal.
- Integrating buck regulators on the load die are limited to low (<2V) input voltage and low current density due to advanced CMOS processes' ultra-thin gate oxide.
- Integrating in a power supply on chip (PwrSoC) all the different components for a buck regulator (i.e., controller, gate drivers, power transistors and passives), which is also limited to (i) low voltage for high switching frequency and (ii) low current density. Examples include a 100 MHz 2-stage PSiP implemented in 130nm CMOS which provides 87% efficiency for 1.5V input, 1V output and 1A output per phase (4 phases) with a 1.5A/mm^2 current density;[31] a 100MHz IVR PMIC implemented in 40nm CMOS with integrated thin-film inductors which provides 82% peak efficiency for 1.8V input and 0.85V/20A/16-phase output in a ~15mm^2 chip scale package;[32] and a 50MHz 3-level buck converter implemented in 65nm CMOS which provides 50% efficiency for 5V input and 0.6V, 0.7A output in a 1.875x1.25mm die.[33]

The challenge is to significantly increase current density for 5V input and high switching frequency.

Power transistor technologies include the following:

- **MOSFETs** (metal oxide semiconductor field effect transistors) made with advanced CMOS processes have an excellent on-resistance • gate charge figure of merit (FoM) due to their short gate length, so can support high switching frequency; however, their thin gate oxide limits their input voltage to approximately 1V. Increasing the input voltage to 1.8V requires a cascade configuration (Figure 20) which increases conduction loss, limiting current density and making it impractical to further increase input voltage. Power MOSFETs employ a laterally or vertically diffused region near the drain to support higher voltage and are widely used in PCB-mounted VRs. Given the conduction versus switching loss tradeoff, lateral MOSFETs for 3-5V input can support high switching frequency (up to 10MHz) but only for low output current (<1A). To supply higher output current, their switching frequency is low (typically <1MHz). Vertical MOSFETs support higher input voltage and output current but also with typically <1MHz switching frequency. MOSFET performance is asymptotically reaching its limit.

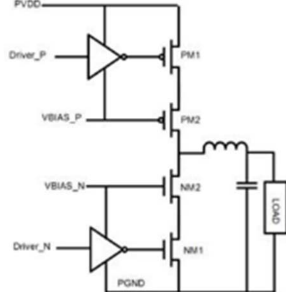


Figure I-20: Cascode configuration for IVR power stage[3]

- **GaN HEMTs** (gallium nitride high electron mobility transistors) provide a superior FOM compared to MOSFETs (Figure 21), so are increasingly used in PCB-mounted medium voltage (100V+) DC-DC converters for applications including consumer power adapters, audio, wireless charging, motor drives and server/telecom power supplies. GaN-on-silicon HEMTs offer the potential to be manufactured in trailing-edge silicon fabs, extending the useful life of these fabs. A 5V, 10 MHz buck regulator that co-packages a GaN power transistor die, a silicon gate drive die and capacitors for the power stage in a 4x4mm^2 package (Figure 22) supplies 22A output current with 83% efficiency for 5V-to-1V (Figure 23). Roughly 50% of the low-side power transistor's resistance is due to the device itself and the other 50% is due to the die metal, package and board interconnects (Figure 24). The challenges are to (i) significantly increase the power stage's current density from 1.4A/mm^2 (22A/16mm^2) to 10-20A/mm^2 and increase its efficiency and/or switching frequency by reducing the interconnect resistance, gate routing parasitics (Figure 25) and power routing parasitics (Figure 27) and (ii) significantly reduce the power stage's z-dimension.[34]

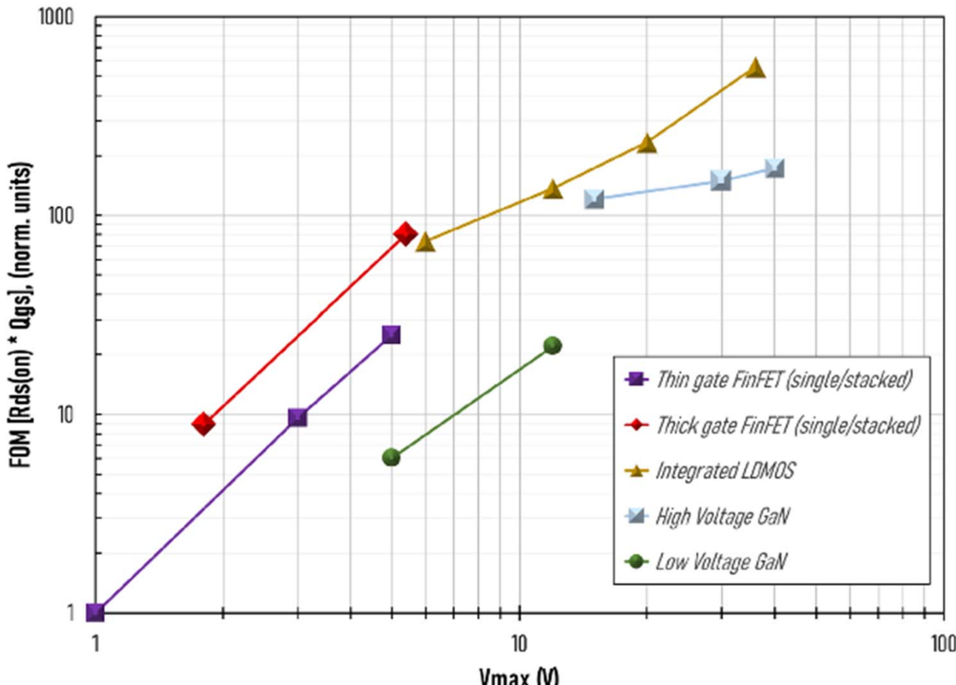


Figure I-21: Figure-of-Merit Comparison[5]

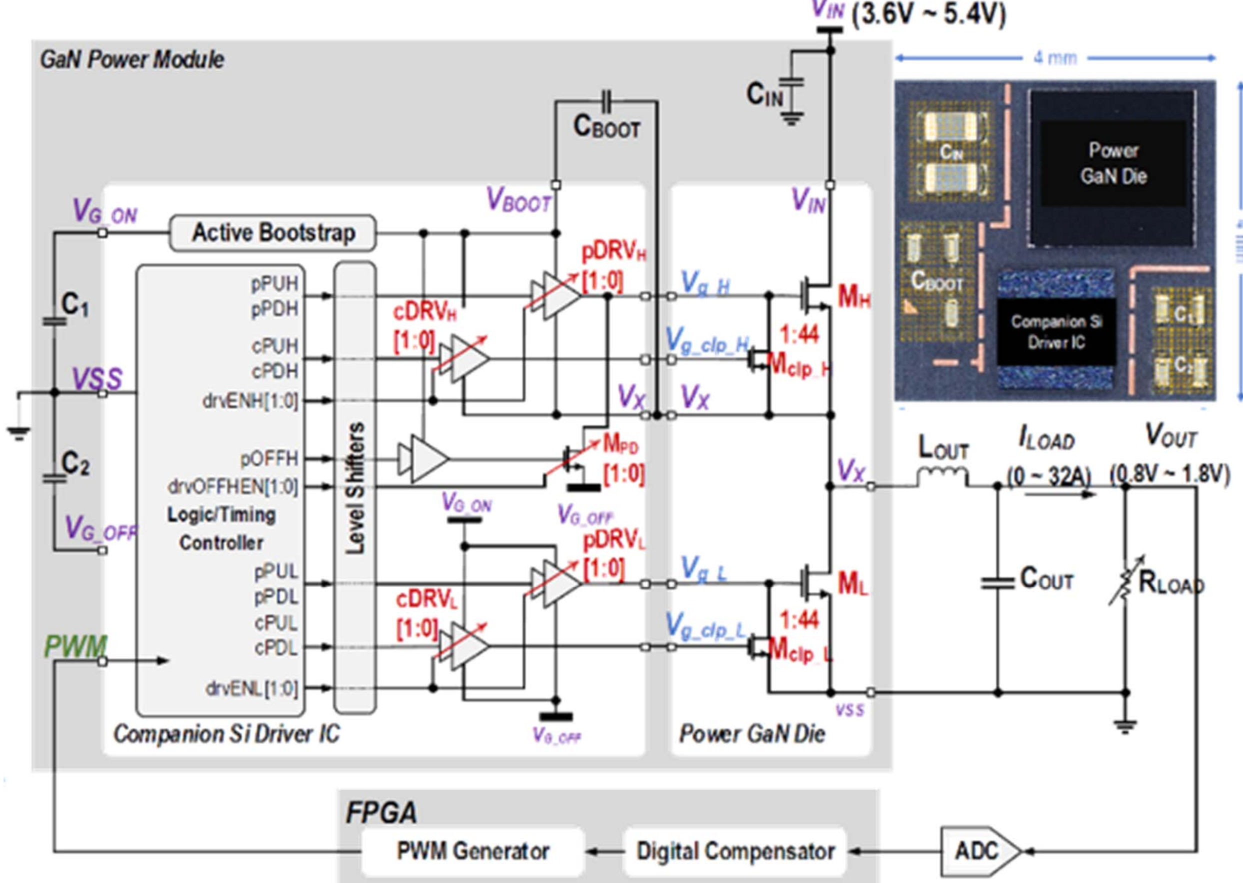


Figure I-22: 5V, 10MHz GaN Buck Regulator Power Stage[34]

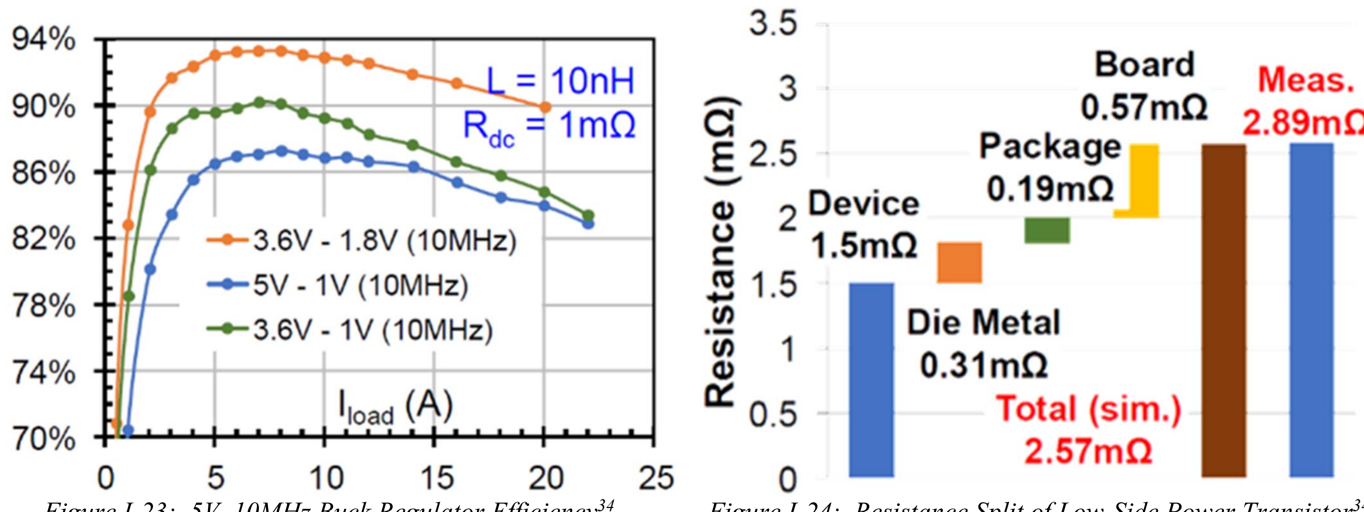


Figure I-23: 5V, 10MHz Buck Regulator Efficiency[34]

Figure I-24: Resistance Split of Low-Side Power Transistor[34]

Figure I-25: Impact of Gate Routing Resistance[34]

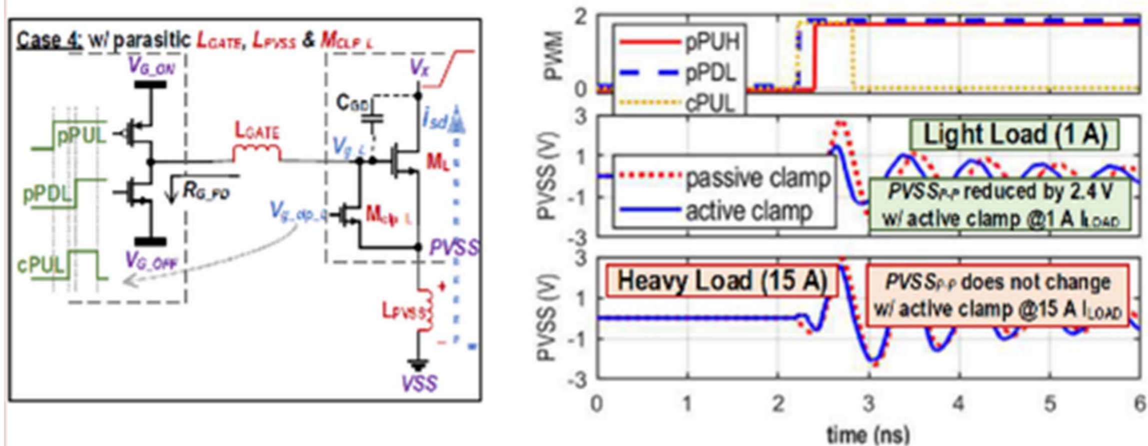


Figure I-26: Impact of Power Routing Parasitics[34]

- **GaAs pHEMTs** (gallium arsenide pseudomorphic high electron mobility transistors), a mature technology widely used for RF applications, have superior FOM compared to MOSFETs for low-voltage applications.[35] GaAs-based power stages have the same challenges as described above for GaN-based ones (i.e., reducing the interconnect resistance, gate and power routing parasitics and z-dimension, as opposed to improving intrinsic device performance). GaAs high-volume production currently uses 150mm wafers, although it's possible to scale GaAs to larger wafers. Few, if any, companies are presently working to commercialize use of GaAs pHEMTs for power conversion.
- **SiC** (silicon carbide) serves high voltage 600V to 3,300V applications, such as electric vehicle drive trains and charging, solar inverters, rail traction, servo drives and AC power supplies. SiC does not provide an advantage over MOSFETs for 3-5V input voltage.

Integrated capacitor technologies include electrolytic capacitors, ceramic capacitors and silicon capacitors and are discussed in detail in Section II of this chapter.
Integrated inductor technologies which are currently in commercial products include the following (Table 1).[36] The challenges associated with the current version of each technology are also outlined.

- Discrete magnetic composite-core inductors as single inductor or in a magnetic inductor array attached using surface mount technology on the land side of the package substrate (Figure 27). Key challenges for this technology are the need for lower height profile and the need for improved inductance vs dc resistance – this parameter should be measured in nH per milliOhm.
- Embedded, air-core inductors (Figure 28) integrated in the organic microprocessor/SOC package substrate. As the number of inductors required increases for more complex granular power requirements (i.e. more separate loads on SOC or processor chip), this technology will require a reduced footprint for each inductor – this could compromise the benefit of the solution due to increased dc resistance and poorer nH/mOhm.
- Coaxial magnetic composite core inductors integrated in the package substrate (Figure 29).
- Air-core inductors on silicon or as part of the 2.5D/3D heterogeneous integration structure. This solution may suit very low inductance requirements (1nH approximately) that will be required for IVRs operating at or above 100MHz. It could make use of RDL and bump/solder ball interconnect to provide the required inductance. The challenge may be achieving sufficiently low dc resistance. EMI may also be an issue in terms of effects on nearby on-chip circuitry. This technology has the potential to effectively deliver an inductor array platform for granular power distribution.
- Thin-film, magnetic-core, planar inductors fabricated on silicon, made using Permalloy or CZT. This technology is currently available from only one high-volume foundry with other foundries, and the wider supply chain, beginning to engage. Currently the technology is delivering solenoid inductors in high volume – these are currently limited in terms of nH/mOhm (less than 1.0) and in terms of saturation current (less than 1 amp dc), unless used in coupled inductor format (up to 2.5 to 3 Amp dc). This technology has the potential to deliver an effective inductor array platform for highly granular power distribution.

Table I-3: Comparison of metrics for integrated inductors[36]

Inductor Metric	Composite Core (This Work)	Air Core Inductor [2]	Composite Core [7]	Composite Core [12]	Thin Film Magnetics [11]	Thin Film Magnetics [13]
Inductance	2.5 nH	1.2 nH	3.0 nH	374 nH	3.9 nH	120 nH
DC Resistance	12 mΩ *	7 mΩ *	12 mΩ *	24 mΩ	39 mΩ	270 mΩ
Imax	8 A	8 A	4 A	2.5 A	1.25 A	0.4 A
L/Rdc	208 nH/Ω *	171 nH/Ω *	250 nH/Ω *	1558 nH/Ω	100 nH/Ω	444 nH/Ω
Area	0.4 mm²	2 mm²	0.5 mm²	6 mm²	0.5 mm²	0.9 mm²
Current Density	20 A/mm²	4 A/mm²	8 A/mm²	0.41 A/mm²	2.5 A/mm²	0.44 A/mm²
Energy Density	200 nJ/mm²	19.2 nJ/mm²	18 nJ/mm²	195 nJ/mm²	6.1 nJ/mm²	10.7 nJ/mm²
Peak Q (Freq)	33 (90 MHz) *	24 (140 MHz) *	18 (100 MHz) *	29 (10 MHz)	15 (100 MHz)	14.5 (15 MHz)

* Includes the parasitic routing impedance from the powertrain to the inductor and from the inductor to the load.

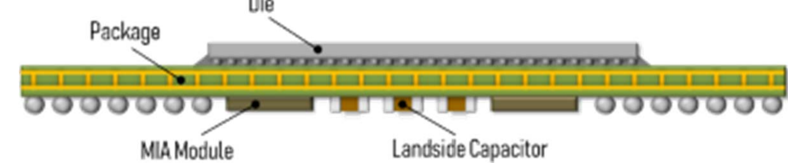


Figure I-27: Cross section view showing magnetic inductor array (MIA) on package land side[37]

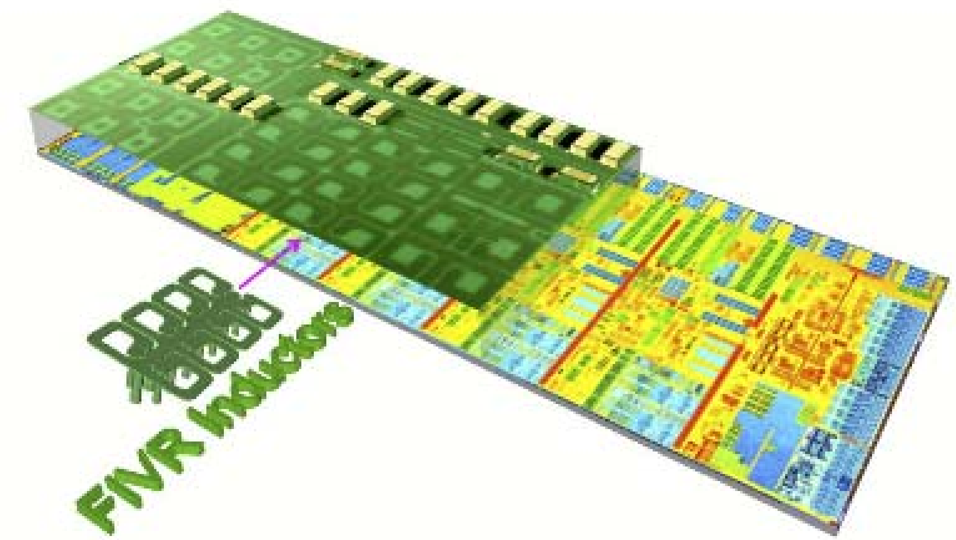


Figure I-28: Bottom view of package substrate integrating inductors[38]

Fully Integrated Voltage Regulators (FIVRs), introduced by Intel in their Haswell processor in 2014, have demonstrated the merits of improving fine-grain power management and the PDN.[39] Intel's 10nm Icelake mobile 9-28W TDP processor, introduced in 2019, attaches several magnetic inductor array (MIA) modules as landside components to the processor's package (Figure 27) to minimize output voltage ripple and enable single-phase operation during light loads to increase efficiency. A typical Intel processor can have over 100 inductors. The magnetic inductor arrays are used sparingly for phases that are active during typical workloads in which the processor spends the majority of its time. Additional air-core inductors are active only during peak workloads which draw the maximum current but only for a small amount of time.[37] The challenges are to increase input voltage (from 1.8V to 5V) and current density and reduce cost.

Backside Power Delivery Network (Figure 30), such as Intel's PowerVia technology, improves voltage droop characteristics, allowing for faster transistor switching while enabling denser signal routing on the top of the chip compared to a conventional Frontside Power Delivery Network.[40,41] IVRs are still needed to supply the backside power delivery network.

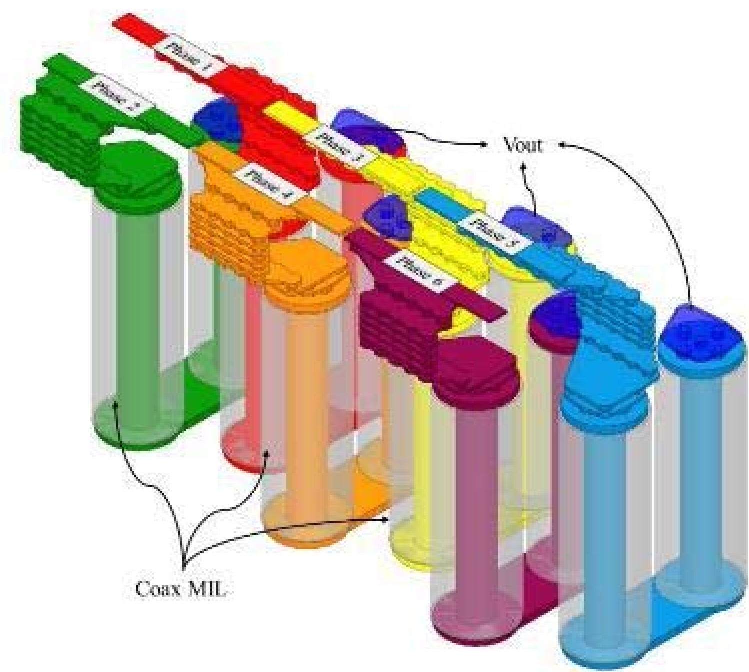


Figure I-29: Array of coaxial magnetic composite core inductors used in a 6-phase IVR[36]

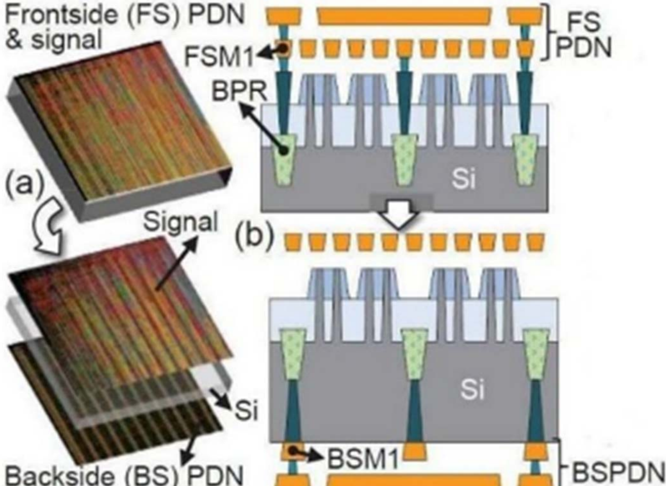


Figure I-30: Backside Power Delivery Network (BSPDN)[40]

I.4. POTENTIAL SOLUTIONS

To support a wide range of voltage rails, phases and current demand, N-number of IPECs may be integrated in the SiP using one or more of the packaging architectures (Figure 4), such as the following:

- Integrate IPECs on the active side of the load die using 3D stacking. An example is Ferric Semiconductor's stacked IVR (Figure 31), which stacks on the load die (i) an IVR die that integrates the power transistors and control circuits made using TSMC's 28nm CMOS with integrated inductors in the CMOS back-end-of line (BEOL) metal interconnects, and (ii) a Deep Trench Capacitor (DTC) die having low Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL). The stacked IVR supports a 2V input voltage.[42]
- Integrate IPECs on the backside of the load die. Challenges include compromising thermal management for load die using backside cooling and integrating TSVs in the load die to interconnect the IPEC outputs to the load and the IPEC inputs from the interposer.
- Integrate IPECs in an active interposer under the load die. An example is a CEA-LETI's demonstration vehicle that integrates in a 198mm^2 65nm CMOS interposer with six 2.5V switched-capacitor

converters, one under each of the six load die (Figure 32).[43,44,45] 2:1 conversion efficiency is 82% for 1A output and 50% for 5A output. The interposer has micro-bumps (10µm diameter, 20µm pitch) and through-silicon vias (10µm diameter, 40µm pitch).

- Embed IPECs in cavities in the package substrate, form interconnects using semi-additive panel-level build-up processes, and attach the load die on top, similar to Intel's Embedded Multi-chip Interconnect Bridge (EMIB) process (Figure 33). Similar to embedding many (10 or more) EMIB die in the package substrate (Figure 34 and Figure 35)[53] to interconnect load die, embed many IPECs in the package substrate between the interconnect bridges to place IVRs in close proximity to the load die.
- Bond IPECs to the load die similar to IBM's Direct Bonded Heterogeneous Integration (DBHi), which directly bonds a silicon bridge to and between die using copper pillars and housed in trenches machined in the laminate substrate (Figure 36).[46] Its major difference from Intel's EMIB is that DBHi has C4 bumps formed on the chip pads that attach to the substrate and micro bumps formed on the bridge pads, while EMIB forms both C4 bumps and micro bumps on the chip pads, a more complex process.[47]
- Embed IPECs in organic-based packages, such as:
  - Amkor's S-Connect process (Figure 37), which embeds semiconductor die and integrated passive devices (c) and silicon bridge die (d) in an RDL interposer, made using silicon, glass or an epoxy mold compound, with an ASIC (a) and HBM (b) on top.[48]
  - ASE's Stacking Fan Out Chip on Substrate (sFOCoS) (Figure 38) whose test vehicle embeds a ~6x6mm silicon bridge die with 0.8/0.8µm interconnects and 55µm micro-bump pitch into the fanout organic RDL layers. The fan-out chip module size is 27x14mm and the package dimension is 40x30 mm.[49]
  - TSMC's Chip-on-Wafer-on-Substrate-LSI (CoWoS-L) (Figure 39), which embeds an LSI in an organic substrate with high-density RDL interconnects. The LSI may be an integrated passive device (IPD) in addition to a local silicon interconnect.[50]

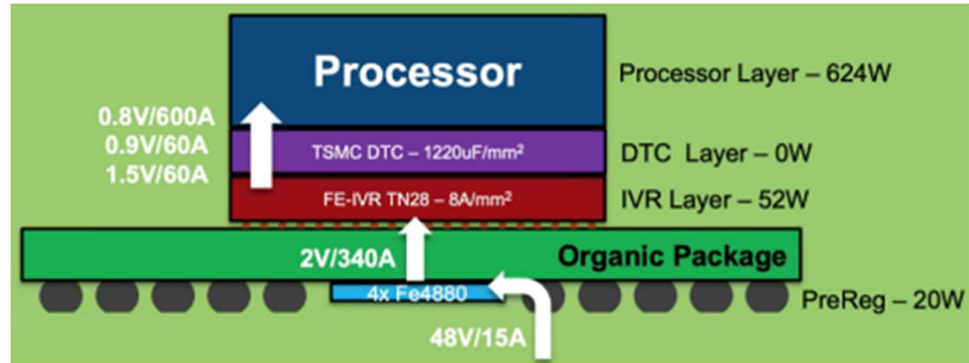


Figure I-31: Ferric Semiconductor's Stacked IVR[42]

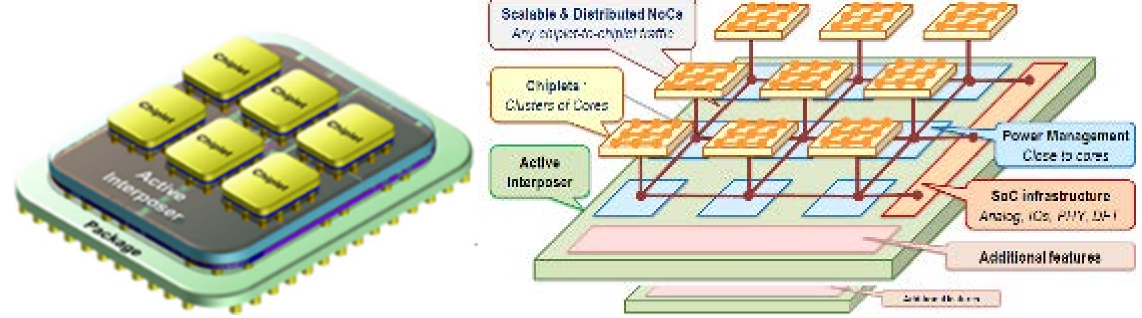
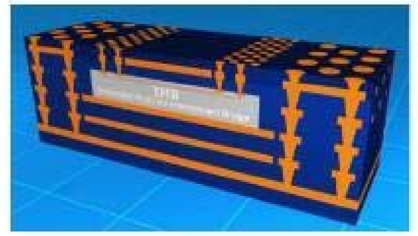


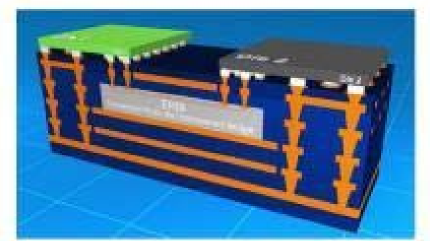
Figure I-32: 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer

1) HDI substrate build-up to cavity layer

2) EMIB Die embedding into cavity



3) EMIB interconnect and HDI substrate FLI formation



4) Die attach onto EMIB substrate

5) EMIB functioning as D2D interconnects

Figure I-33: EMIB die embedding process[28]

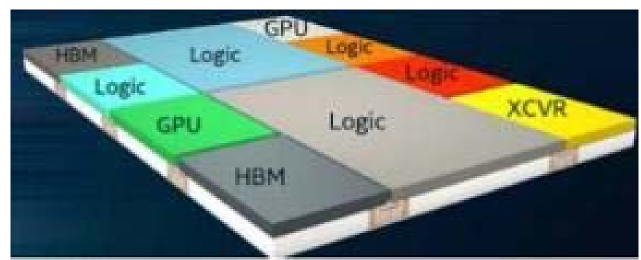


Figure I-34: Silicon bridge die[28]

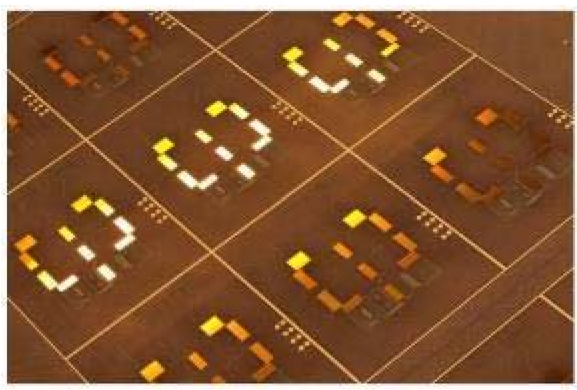


Figure I-35: 10+ EMIBs embedded in package substrate[28]

Figure I-36: IBM's Direct Bonded Heterogeneous Integration (DBHi) [46]

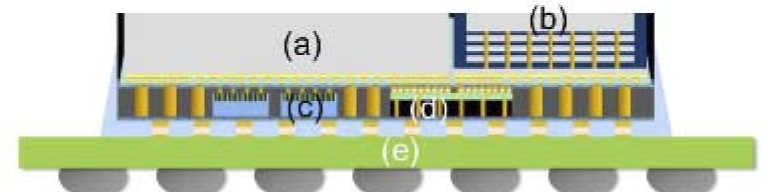


Figure I-37: Amkor's S-Connect Process[48]

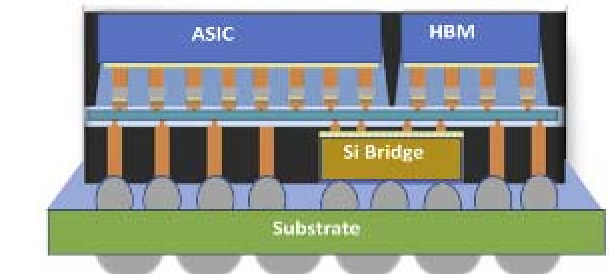


Figure I-38: ASE's Stacking Fan-Out Chip on Substrate (sFOCoS) [49]

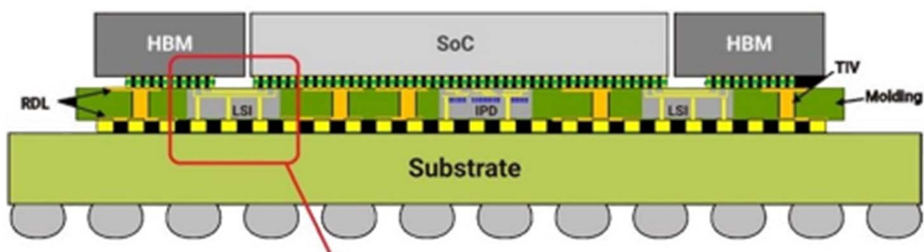


Figure I-39: TSMC's CoWoS-L[50]

One potential IPEC solution disaggregates separately-manufactured semiconductor die into small, very thin chips (called x-chips) that are transferred to large area panels which serve as the heterogeneous integration platform. An example of a 4-phase buck converter power stage IPEC, where each phase is sized for the integrated inductor (e.g., ~2A continuous and ~6A+ peak current) and the IPEC is constructed as follows:

- GaN, GaAs or silicon power transistors are disaggregated into large arrays of small (e.g., 275x280µm), thin (<15µm) x-chips (Figure 40), which densely pack the source/drain fingers to minimize RDS(on) • Area, connect gates to both sides of the power transistor and minimize lateral current flow (e.g., <100µm) in the thin metal layers made using a semiconductor wafer fab. The last step in the semiconductor wafer fab process is passivation openings to top metal, and the passivation openings are arranged for subsequent RDL interconnects using coarse (>10µm/10µm) L/S design rules to the source, drain and gate (Figure 41). CMOS gate driver x-chips are similarly manufactured on separate silicon wafers.
- Gate driver x-chips are transferred to the top side (Figure 42) of an ultra-thin, large area glass or ceramic substrate with through-substrate vias with their active side facing up towards the load die (Figure 43).
- Power transistor x-chips are transferred to the bottom side of the substrate (Figure 44) with their active side facing down towards the package substrate.
- Since the gate driver and power transistor x-chips are ultra-thin and small, it's straightforward to use RDL for interconnections.

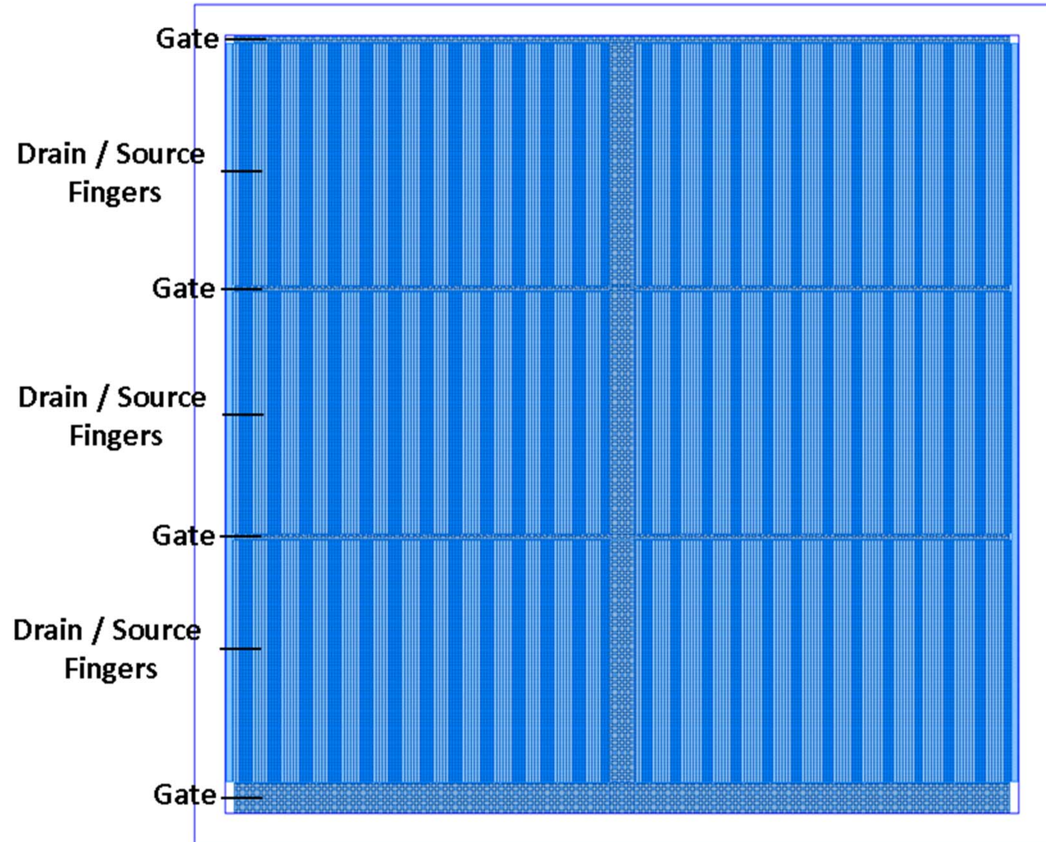


Figure I-40: Top view of 275x280μm x-chip's densely-packed source/drain fingers[10]

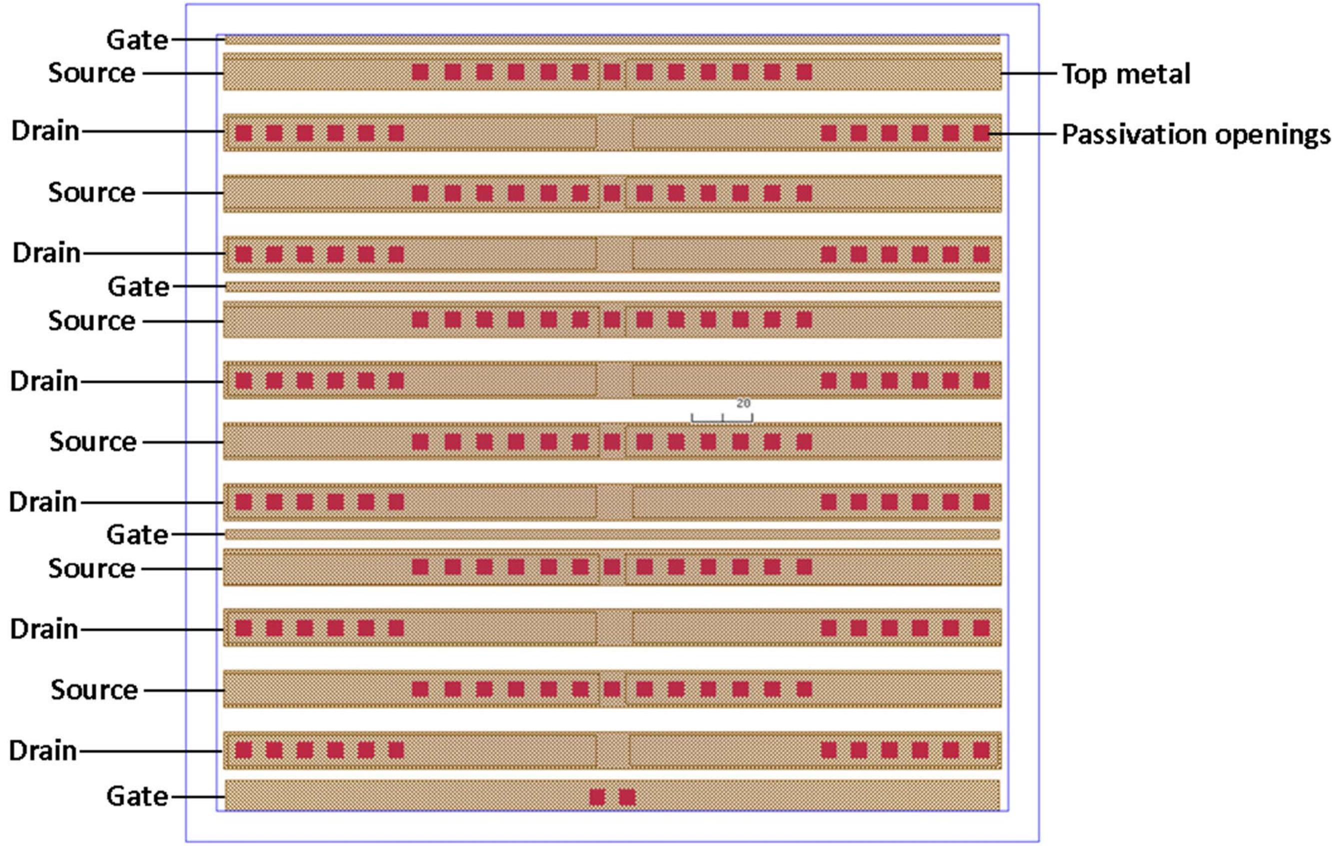


Figure I-41: Top view of 275x280mm x-chip's passivation openings to top metal[10]

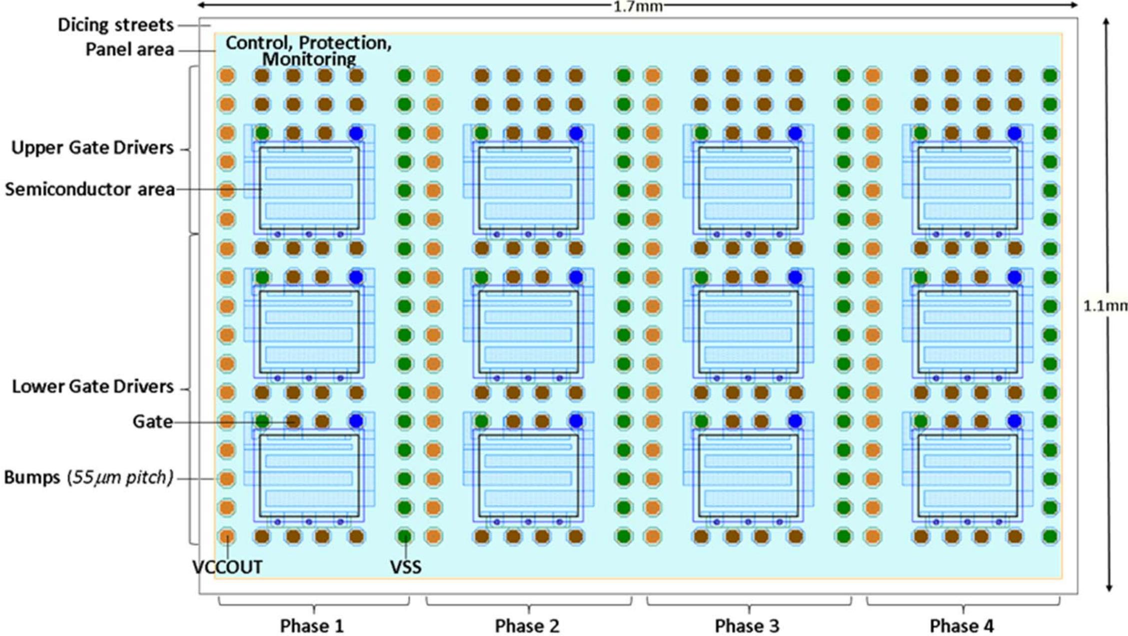


Figure I-42: IPEC Top View[10]

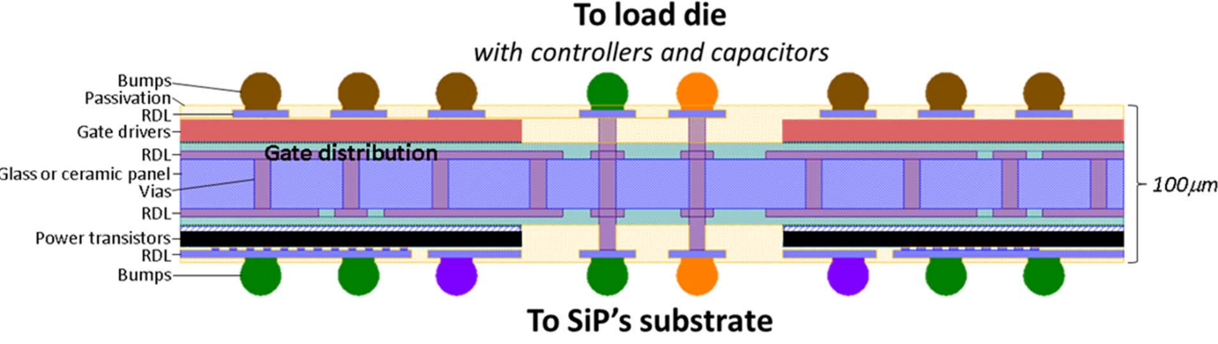


Figure I-43: IPEC Cross-Section View[10]

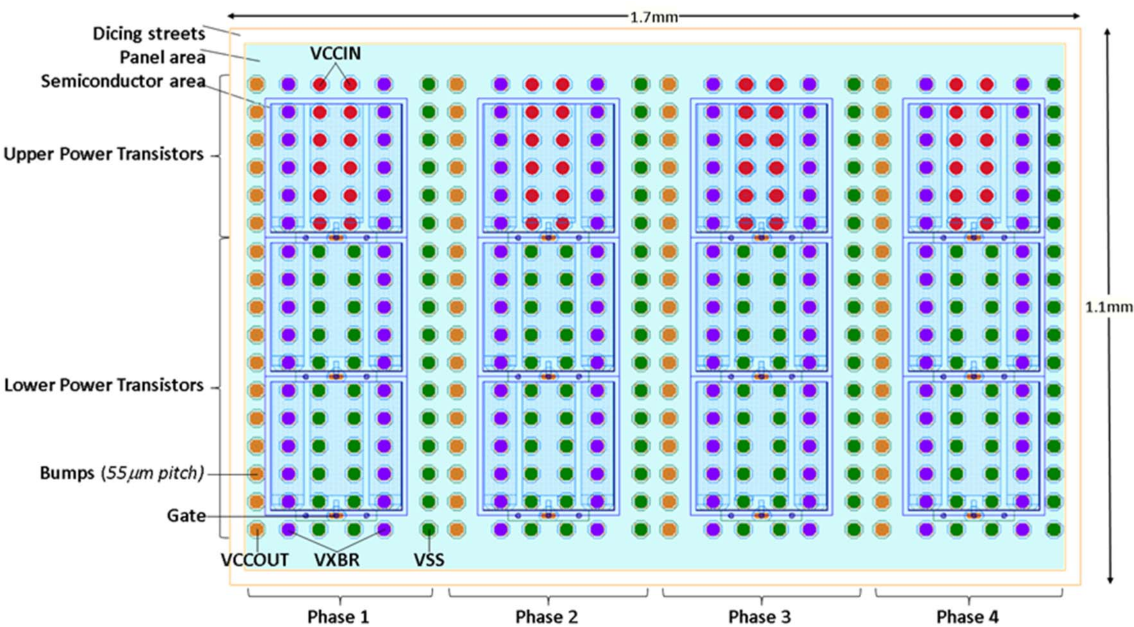


Figure I-44: IPEC Bottom View[10]

This example shows the following benefits of this heterogeneous integration approach:

- Tightly coupling separately manufactured components: The interconnection distance between the power transistors and gate drivers is just slightly more than 100µm which significantly reduces the parasitics and switching loss.
- Reduced electrical and thermal resistance to support high current density: Multiple thick RDL interconnects made using panel-level processing supplement the semiconductor die's thin interconnects made using wafer-level processing. Thick PLP RDL is used for all high-current interconnects as well as gate distribution and routing of the control, protection and monitoring signals. Lateral current flow in the thin semiconductor die's interconnects is minimized.
- Cost reduction: The majority of the interconnects consume substrate area (Figure 43) rather than semiconductor area (Figure 1). Substrate area is significantly lower cost than semiconductor area. In this IPEC example, the gate driver and power transistor semiconductors fill less than 25% and 50%, respectively, of the substrate area.
- Known good die (KGD): The IPECs can be tested and binned, for example into five different SKUs (Stock Keeping Units), one SKU with four good phases plus four SKUs with just three good phases (Figure 45).

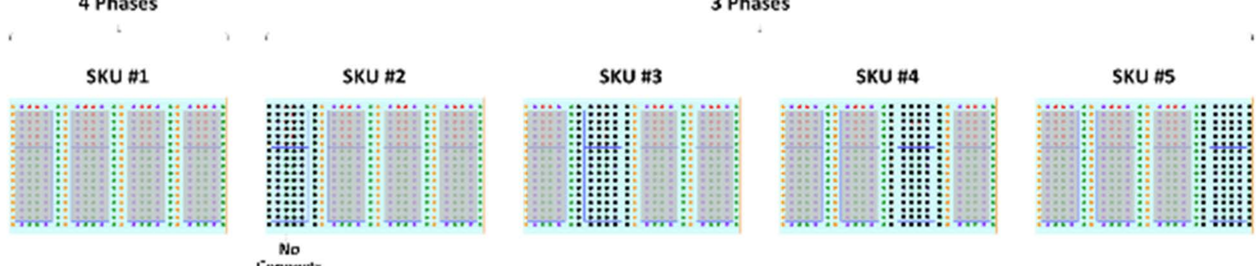


Figure I-45: IPEC Binning Options[10]

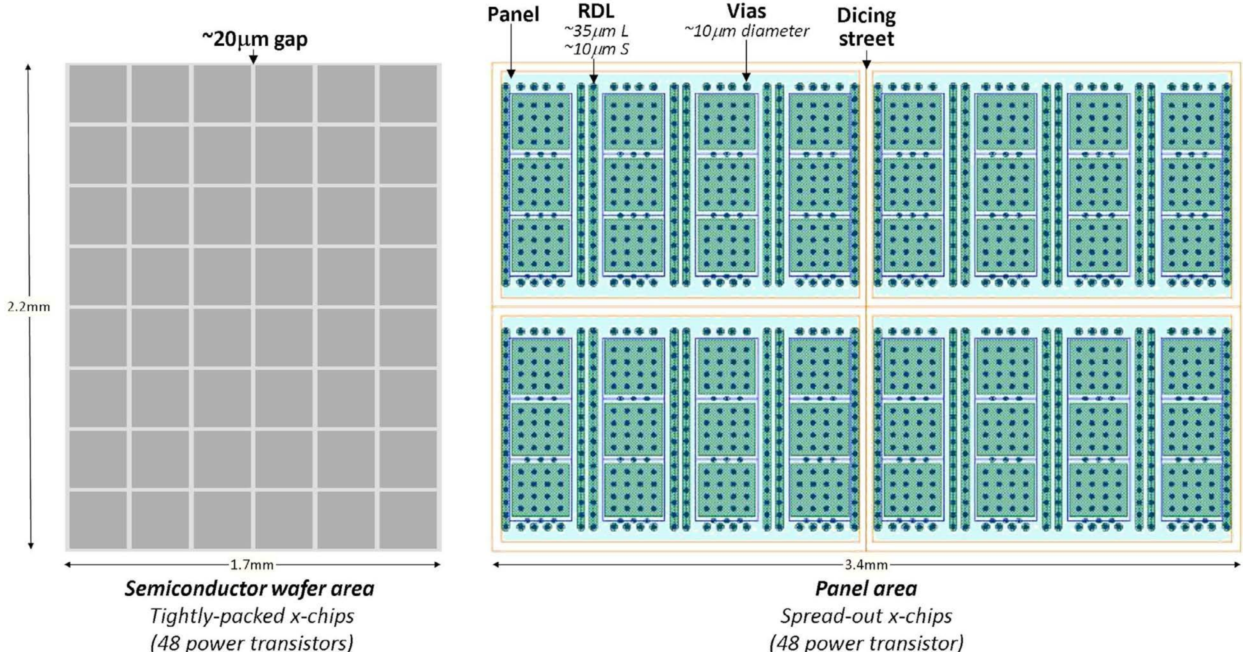
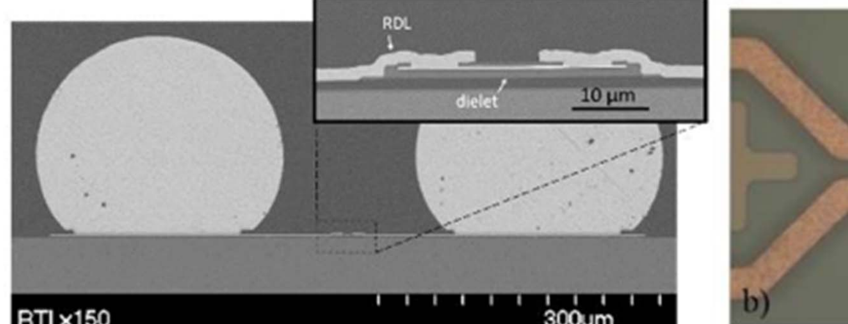


Figure I-46: MTP spreads out x-chips tightly packed on semiconductor wafers on panels[10]

An example of a potential method for manufacturing IPECs is to use micro transfer printing (MTP), a massively parallel pick-and-place process that efficiently transfers large arrays of ultra-thin (<15µm), small, separately manufactured components from one or more source wafers to destination silicon wafers or large-area glass or ceramic substrates.[51,52,53] A fully automatic ISO 4 class clean room system transfers up to 50x50mm arrays of x-chips from source wafers (up to 300mm) to destination wafers (up to 300mm) or panels (up to 450x450mm).[54] By customizing the post spacing of the MTP system's stamp, x-chips tightly packed on the source wafer (maximizing source wafer

utilization) are efficiently spread out on the panel (Figure 46). Placement accuracy is +/-1.5µm (3 sigma), which resolves the critical position accuracy requirement for the RDL interconnect process.[55,56] Die shift issues are eliminated since x-chips are held in place with a thin adhesive layer underneath with RDL on top and no epoxy mold compounds are used. Examples of MTP applications include fan-out packaging of microdevices (Figure 47),[57] GaN/RF-SOI SPST switch (Figure 48)[58] and GaN HEMTs on silicon (Figure 49).[59] An example of a foundry that offers high volume MTP capabilities is X-FAB.[60]



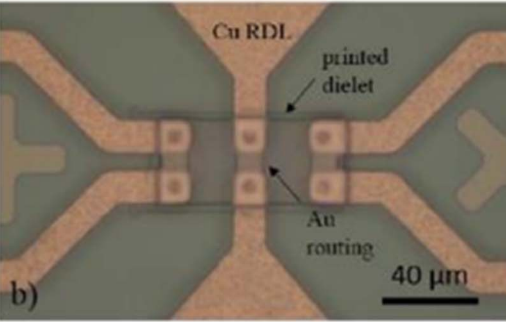


Figure I-47: Fan-out packaging of microdevices made with MTP[57]

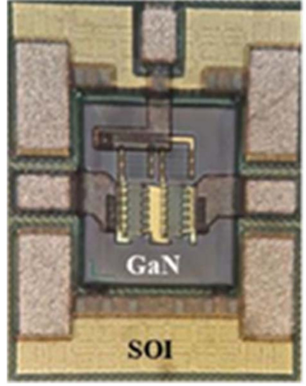


Figure I-48: GaN/RF-SOI SPST switch[58]

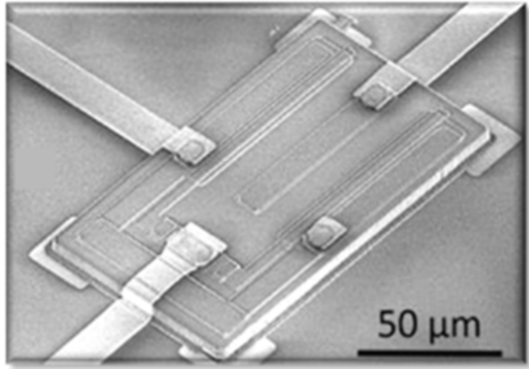


Figure I-49: GaN HEMTs on silicon[59]

Integrated inductor technology options that have recently been proposed and show promise include:

- Small footprint (0201 – 0.2mm x 0.1mm) discrete inductors, using high frequency (100MHz+) polymer-loaded composites or fired magnetic material, with low profile (less than 0.1 to 0.3 mm). These components can be used in a PSiP platform, either as surface-mount devices [MuRata], or with copper terminations, embedded in the SOC organic substrate or package [Taiyo Yuden].
- High frequency ferrite cores embedded in 2.5D/3D heterogeneous integration structure using BEOL interconnect processing to provide windings [IMEC].
- Vertical coaxial magnetic composite core inductors (Figure 29) integrated in the package substrate by plated-through holes drilled in the package substrate and encapsulated with a composite magnetic material [Intel].
- Embedded magnetic-on-silicon inductors embedded in PCB substrate or package [Wurth].
- Embedded thin film CZT combined with copper windings in PCB substrate or package [Tyndall].
- Electroplated planar copper windings with electro-deposited magnetic core [Enachip].
- Vertical inductors based on thin film CZT deposited on the sidewalls of low-profile electroplated copper pillars [Tyndall].

I.5. REQUIRED R&D

R&D focused on IPECs is needed in the following areas:

Panel-level packaging (PLP) employing a portfolio of state-of-the-art heterogeneous integration technologies (e.g., pick-and-place, die bonding, micro-transfer printing, RDL, through-substrate vias, sort/test, etc.) for prototyping and volume production. Prototyping should be done using manufacturing flows that are representative of volume production. A state-of-the-art PLP foundry would enable and stimulate R&D. The cost of building such a PLP foundry

is on the order of $0.1B versus $10B for a state-of-the-art wafer fab and would leverage decades of experience and technologies from PCB, flat panel display and solar panel manufacturing.

Electronic Design Automation (EDA) tools and Process Design Kits (PDKs) for PLP heterogeneous integration. Tools are required for the holistic co-design optimization, simulation and integration of separately manufactured IVR components. A variety of stack-ups, layer maps and models, including measured versus modeled correlation and improving load energy efficiency through improving the PDN and fine-grain power management is required. PDKs for the diverse IVR components and heterogeneous integration method which provide design guidelines and incorporate the results of reliability testing and analysis (so it's known when, how and why various IVR components fail during high current density and high-frequency operation). Tools should also include cost modeling to identify and resolve early in the IPEC design cycle roadblocks and trade-offs in cost and yield among various heterogeneous integration options. Such cost modeling can build upon the substantial activity-based cost modeling, which breaks down a process flow into all of its cost components (e.g., labor, materials, capital and yield), that has been done for chip-on-interposer on substrate and fan-out on substrate.[61]

Optimization of separately manufactured components for IVRs, including power transistors, gate drivers, controllers, inductors and capacitors. Key R&D for power transistors include employing compound semiconductors (GaN and GaAs), which have very low gate and output charge and no reverse recovery charge, and minimizing their on-resistance • area figure-of-merit, optimized for 3-5V operation. Key R&D for IVR inductors, which requires a multidisciplinary approach with considerations of 3D inductor design, magnetic material synthesis and processing, integration and assembly into packages, substrates and interposers, include:

- Increasing dc nH/milliOhm beyond 1.0 (up to 5.0 to 10.0).
- For magnetic core solutions, increasing the saturation current up to 5 to 10Amps dc.
- Exploiting the vertical direction to provide reduced footprint, ultra-low dc resistance inductors – to produce a useful, single vertical inductor (either air core or with magnetic core) using discrete, embedded components, plated through holes in PCB or the RDL/bump interconnect in a 2.5D interconnect system.
- Exploring integrated inductor arrays in interposers or substrates for complex granular power architectures.
- Consider the EMI implications of integrated inductors and appropriate solutions.
- Utilize the "parasitic inductances" within the system architecture, either with or without magnetic material enhancements, which is the "holy grail" for integrated inductors.

Integrating arrays of separately-manufactured components in IPECs customized for advanced topologies, such as a 3-level buck converter (Figure 50), 4-level buck converter (Figure 51) or hybrid series-capacitor tapped buck converter (Figure 52), which improve performance and reduce voltage requirements but require an increased number of power transistors, gate drivers and passive components.

Stacking separately-manufactured components, such as power transistors, to increase their gate periphery, reducing conduction loss, or capacitors to increase bypass capacitance.

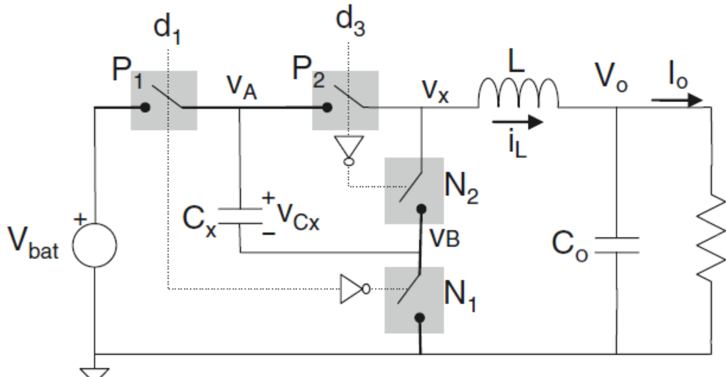


Figure I-50: 3-Level Buck Converter[62]

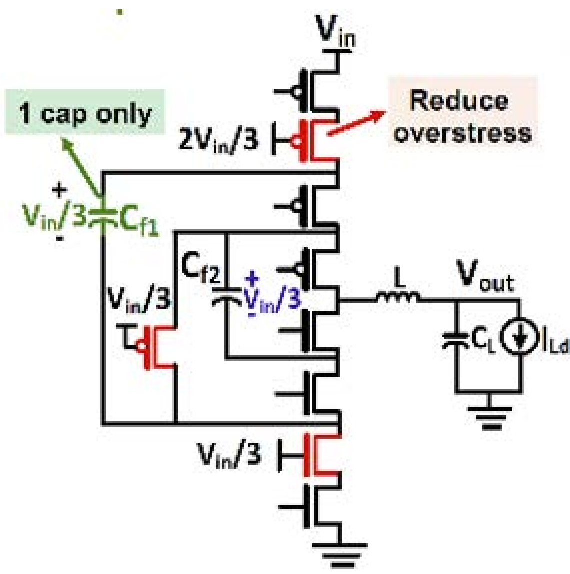


Figure I-51: Modified 4-Level Buck Converter[29]

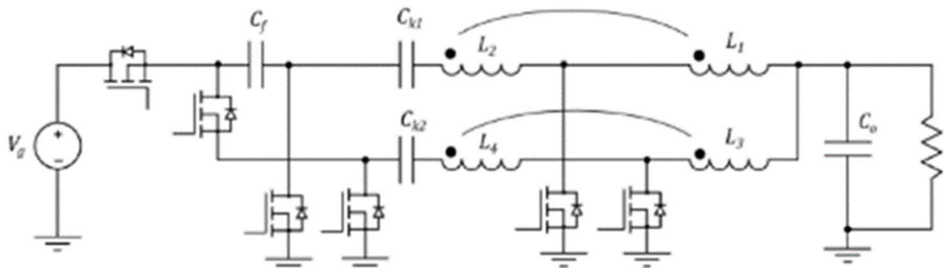


Figure I-52: Hybrid Series Capacitor Tapped Buck Converter[5]

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Section II: Power System-in-Package (SiP) Modules

II.1 POWER MODULE TOPOLOGIES

Technology Drivers and Topologies: Power SIP modules are designed to deliver the output voltage at the target current levels and load transients. They deliver power to most of the loads in the system, including the majority of the processors, RF modules, analog and sensor chips and others. They, however, are limited by their impedance bandwidth because of their distance from the load. For load transients that demand low impedance over a MHz, they fall short in the response time and lead to excessive switching noise. Hence, package-embedded decoupling capacitors are used to deliver charge for shorter transient times. In spite of the increasing trend to package integrated power delivery through IVRs (integrated voltage regulators), stand-alone on-board power SIP modules play an important role in delivering power to most of the system components. They consist of switches, drivers and controllers, along with the storage elements such as passives. If multiple power switches and control logics are integrated on the same chip, they are known as PMICs (power management integrated circuits). Applications and requirements for voltage regulators are classified in Table 1. Specifically, the key parameters that matter for optimizing power management are:

- Input supply voltage (Vin)
- Load voltage (Vout)
- Load current range (I)
- Efficiency over the current range (Efficiency)
- Load di/dt (di/dt)
- Load voltage regulation and dynamic requirements (DVFS)
- Supply voltage noise (Ripple)

Metrics

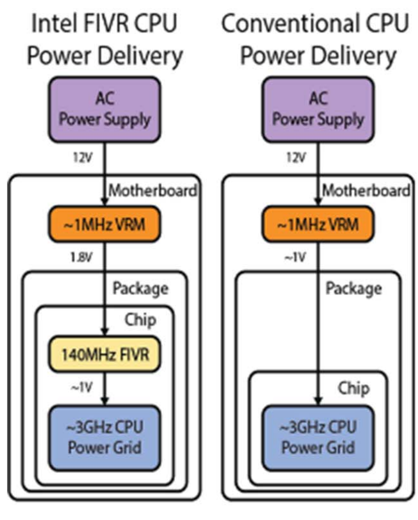
Table II-1: Power Module Applications and Typical Design Parameters

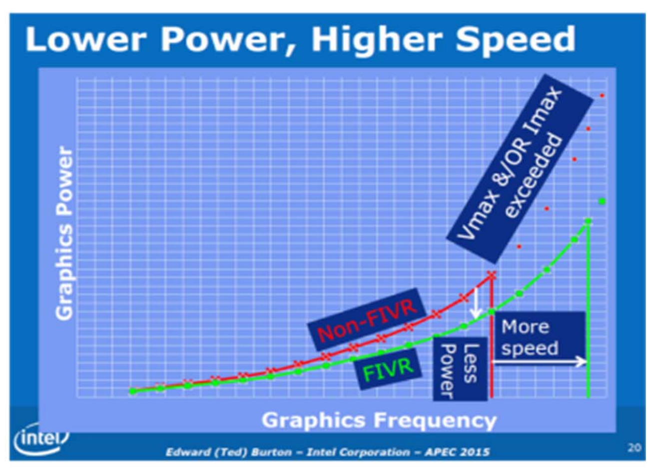
Application	Vin	Vout	I	Efficiency	di/dt	DVFS	Ripple
Server processor	12-48 V	~1 V	~100 A	High at high current	High	Low	Medium
Graphic processor	12-48 V	~1 V	100's A	High at high current	Low	Low	Medium
AI accelerator	12-48 V	~1 V	100's A	High at high current	Low	Low	Medium
Mobile processor	2.3-5 V	~0.4-0.8 V	~5 A	High 10 mA to 3A	High	High	Medium
HBM Module	3.3-5-12 V	~1 V	~10 A	High at high current	Low	Low	Medium
Optical module	3.3 V	~0.4-0.8 V	~10 A	High at high current	Low	Low	Small
Cell Baseband processor	5-12 V	~1 V	~5-20 A	High at high current	Low	Low	Small

Different applications have dramatically different needs. Table 1 is a collection of typical requirements, though it should be considered as a guideline, since real products have a much broader range of specifications. If we look at these key applications, we can therefore formulate the architectural needs to satisfy the requirements for each of them. For example, a relatively fixed ratio of input to output voltage with low di/dt may be well served by a single-stage buck converter if Vin/Vout is <5. As the ratio increases, a resonant L-C converter may be preferable; if di/dt is larger, then a two-stage architecture will yield better efficiency if the second stage has high bandwidth. If high efficiency is required across a wide range of currents, then phase-shedding and/or different operating control modes are also required.

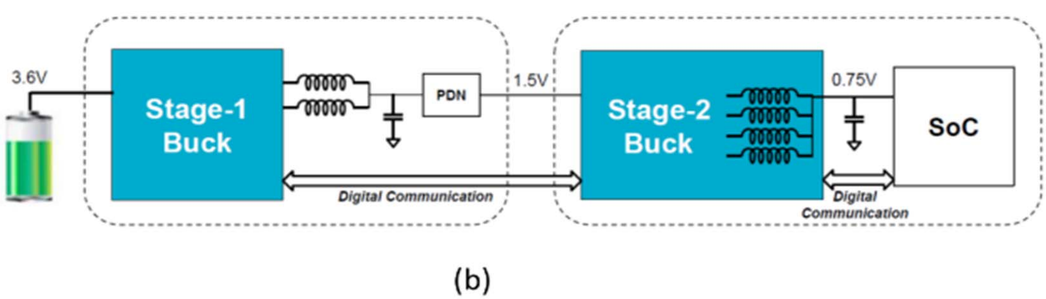
Existing Solutions and Challenges

Topology Advances: Significant improvements in topologies and architectures for power conversion are being developed in response to new packaging technologies (2.xD and 3D) as well as the broader adoption of new semiconductor processes (GaN and SiC). We may divide this section into main areas of applications: AC/DC, Medium Voltage Server applications, High Performance Computing (HPC), and Mobile applications.





(a)



(b)

Figure II-1: Multistage power conversion (a) on-board and on-chip stages using FIVR (left), conventional on-board only (center) and performance improvement chart of FIVR vs. conventional (right); and (b) two stage Buck architecture with Stage 1 on–board and Stage 2 in package [3].

1. Power SIP in High Performance Computing (HPC):

This application is predominantly covered in Section I. Only a brief overview of on-board power modules is provided here. The need to reduce losses in the motherboard/socket interconnect, as well as provide better and more granular regulation to the processor cores, is driving the industry to a two-stage approach, so that the processor socket is fed with a higher voltage at lower current, thus reducing the impedance constraints on the Power Delivery Network (PDN). Integrating the second stage conversion within the package and/or SoC die requires extreme miniaturization of the passive components. The switching frequency needs to be higher than 100MHz, thus allowing very small inductors, which are realized as either air-core in the device substrate or using a thin-film magnetic material.

As processor supply voltages in newer process nodes are no longer around 1V but rather approaching 0.5V, a single stage DC-DC converter with discrete components mounted on the circuit board can no longer provide reasonable efficiency, due to both increasing conversion ratio and the need to bypass the lossy PDN. A high-frequency, fully integrated voltage regulator (IVR) needs to be implemented at the load to provide the required response to transients and to achieve switching frequencies that may exceed 100 MHz. Low-voltage transistors are required, thus making it impractical to interface directly to the battery. In the case of a single-chip SoC, the IVR must be integrated within the package or within the chip (Figure 1(a)). In the case of a Heterogeneous Integrated SiP, the IVR must be integrated within the SiP (Figure 1(b)). A two-stage architecture thus provides a higher-performing solution, while the integration of high-frequency passive components allows for size and cost-effective implementation of multiple distinct power domains, further improving system efficiency (https://www.realworldtech.com/power-delivery/).

2. Medium Voltage Server Applications:

This is comprised of two parts: AC/DC converters and the DC-DC converters that serve the Intermediate Bus Architecture (IBA):

AC/DC Converters: The use of GaN devices has increased the operational frequencies of AC/DC converters, thus allowing significant reduction in their size, and forcing improvements in efficiency to allow cost-effective dissipation of the heat generated, challenged by the higher power density achieved. Current state-of-the-art products achieve power densities exceeding 30W/in^3 at the complete board level for 65W converters for consumer applications [4]. More of these advances will be reported in Section III.

IBA DC-DC Converters: The shift of intermediate bus architecture from 12V to 48V and the trend to continuously reduce the supply voltage to the processor cores requires a redesign of architectures for DC/DC conversion, from the most common standard multi-phase buck converter to a two-stage architecture, where one stage is typically tasked with providing a large voltage ratio conversion with high efficiency, while the other stage manages the accurate regulation of the supply voltage. The example in Figure 2 shows a pre-regulator, which absorbs the variability of the supply, followed by a fixed-ratio converter with high efficiency. Alternatively, one can utilize a resonant capacitive converter for the first stage (as shown in Figure 3), followed by a low-voltage DC-DC converter (not shown) to provide final regulation [5-7]. By utilizing a cascaded resonant converter, high peak efficiency of 99%, full load efficiency of 97.9% with driver loss, and peak power density of 4068 W/inch^3 was demonstrated [8]. The topology for the second stage is typically a multi-phase buck, which has been developed with up to 128 phases to achieve low ripple at the load.

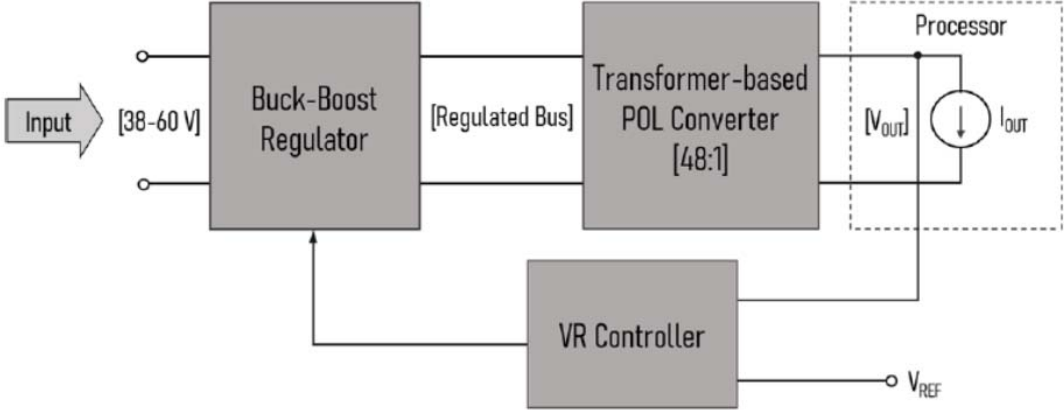


Figure II-2: A two stage power converter with pre-regulator that absorbs transients from the input supply [9].

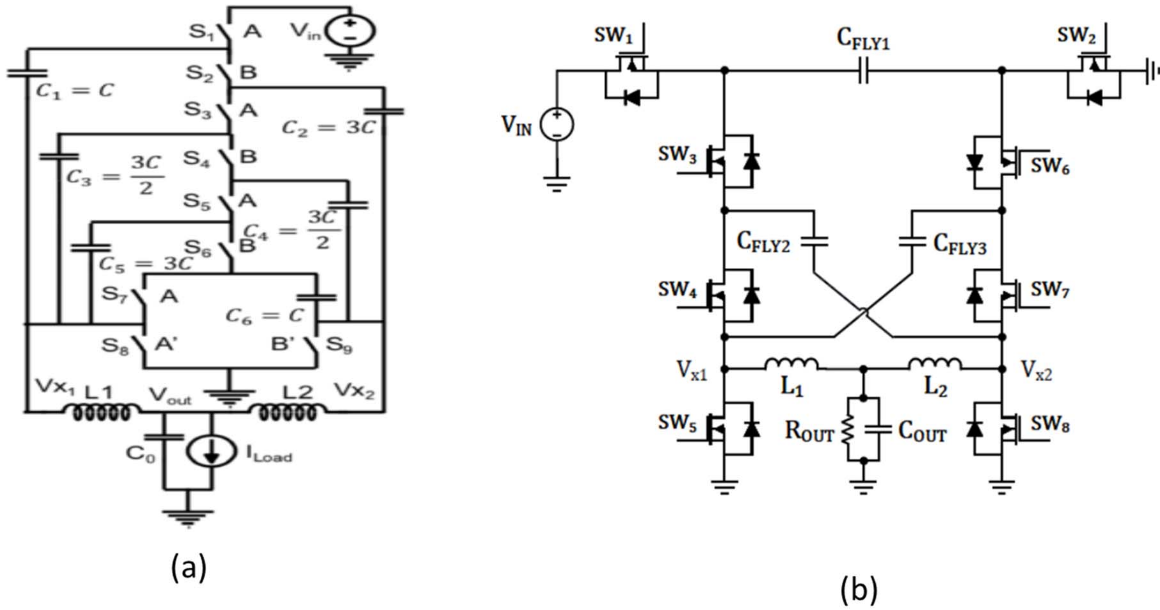


Figure II-3: Cross-Coupled Series-Capacitor Quadruple Step-Down Buck Converter [10]

A lot of effort in recent years has been devoted to co-optimizing step-down architectures for efficiency, size and thermal management. These include resonant versions of Series/Parallel and Dickson/Ladder switched-capacitor

topologies, switched-tank converters and merged topologies, where a switched-capacitor converter leverages the inductor of a traditional buck stage to control the current slew rate in the capacitors. All of these architectures attempt to improve overall efficiencies by either reducing the RMS value of the current in the passive devices and/or implementing Zero-Voltage and Zero-Current Switching (ZVS, ZCS) to reduce switching losses in the transistors. A list of relevant resources can be found in J. Stauth's presentation at PwrSoC 2021 [11] or [12].

As the power consumption of high-performance processors increase from ~100W to ~1,000W, the physical implementation of the system becomes more and more critical, since lateral flow of current in the PC board is very inefficient and the extraction of the heat generated becomes more challenging. As already pointed out in Section I, vertically stacking the Power Management with the load becomes a preferred solution, as demonstrated in the Tesla Dojo implementation, where power is delivered from the bottom, signals flow horizontally, and heat is mostly extracted from the top of the stack. Co-designing the power converter with the load becomes more critical to enabling an effective module integration.

3. Mobile Processors:

Mobile processors create additional constraints on the Power Management design: high-efficiency requirements typically extend over three orders of magnitude of load current, and over 7 orders of magnitude if we consider Idle and Off modes. When "off", the processor's power management needs to draw less than 1 µA; idle modes may vary, depending on applications; and when the processor is powered up, its current consumption may span between a few mA and up to 10 A. In the past, the most common architecture was based on a multi-phase buck with direct connection to the battery and various control schemes to optimize performance, including near time-optimal transient response. Multiple operating modes allowed efficiency to remain relatively flat across the three orders of magnitude of the current range, by including phase shedding and PFM (Pulse Frequency Modulation) at low current (hysteretic, fixed-on-time, etc.). Various improvements to the traditional buck topology have been proposed to improve the performance and efficiency, including multi-level "flying capacitor" architectures [13]. These are illustrated in Figure 4 [13, 14].

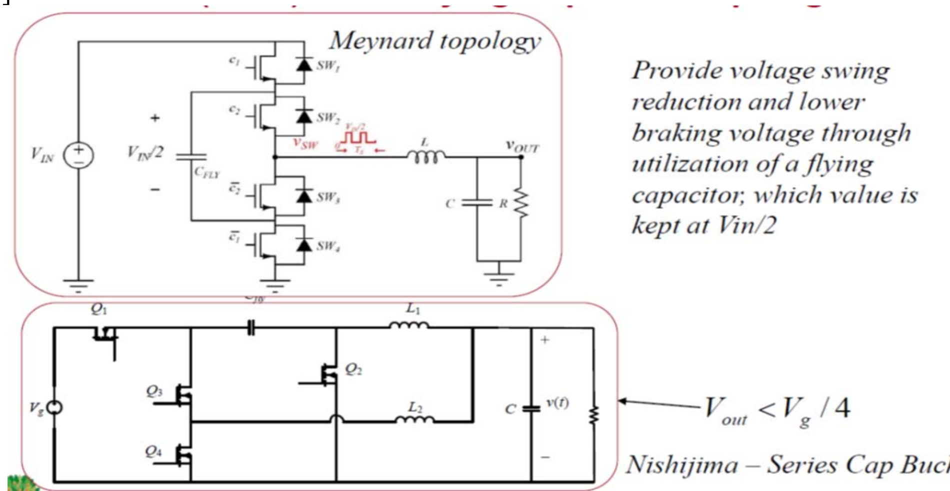


Figure II-4: Multi-level conversion with double step-down two-phase convertor for VRM

4. Power modules for wireless charging:

Another area of innovation in mobile devices is related to wireless charging, where the need to minimize I^2R losses is forcing an increase in the rectified voltage out of the receiving coil, followed by a high-efficiency switched-capacitor converter to bring the voltage down to a level compatible with the battery charger, as illustrated in an example in Figure 5.

Figure II-5: Wireless charging system with high-voltage rectified voltage and high-efficiency switched cap converter

Table 2 and Table 3 provide performance metrics for 5V POL, 3.6 V Battery, 12V and 48V power modules, respectively, including all components.

Table II-2: 5V/3.6V Power Module Performance Metrics

Metric (5V POL Module)	**Generation**			
	Current[1]	**2**	**3**	**4**
Output voltage (V)	0.6-4.0	0.4-4.0	0.4-4.0	0.4-4.0
Switching Frequency (MHz)	3-4	5-6	10	10
Output current density (A/mm^2)	0.1	0.12	0.15	0.2
Thickness (mm)	1.2	1.0	0.9	0.8
Peak Efficiency @1.2V (%)*	86	87	88	88
Metric (3.6V Battery)	**Generation**			
	Current[2]	**2**	**3**	**4**
Output voltage (V)	0.9	0.8	0.6	0.5
Switching Frequency (MHz)	3-6	Two-stage	Two-stage	Two-stage
Output current density (A/mm^2)	0.1	0.2	0.4	2
Thickness (mm)	0.8	0.6	0.6	0.4
Peak Efficiency @Vout (%)**	84	82	82	82

[1] TI TPSM82823; **Converter efficiency is not improving significantly, because size is the focus*

[2] TI TPS62861; ***Converter efficiency is not improving, because of lower Vout, and system efficiency is the true metric*

Table II-3: 48V Power Module Performance Metrics

Metric (48V to processor)	**Generation**			
	Current[3]	**2**	**3**	**4**
Output voltage (V)	~1			
Switching Frequency (MHz)	0.3-0.5			
Output current density (A/mm^2)	0.1			
Thickness (mm)	4.5			
Peak Efficiency (%)	87			
Metric (48V to POL)	**Generation**			
	Current[4]	**2**	**3**	**4**
Output voltage (V)	3.3-12	1.8-5	1.8-5	1.8-12
Switching Frequency (MHz)	0.5	1.5	3	5
Output current density (A/mm^2)	0.1	0.3	0.7	>1
Thickness (mm)	2.5	2.5	1	1
Peak Efficiency (%)	91	91	92	92

[3] Vicor PRM + VTM; [4] Vicor PI352x-00

II.2 SIP POWER MODULE INTEGRATION

Introduction

Wide Band Gap (WBG) devices such as SiC and GaN enable higher power densities and faster transitions in the power switch. However, in order to benefit from these advances, it is critical to minimize the loop between the gate driver and semiconductors while ensuring that the system parasitic inductances are low. Embedding of actives and passives became very important in power applications to increase power density and efficiency along with miniaturization of power modules, using Si devices for low power and wide bandgap GaN and SiC devices for high power. The associated changes in the layout and interconnection structure brings advantages in board-space saving, parasitics reduction, and thermal dissipation. Multichip packaging and active-passive integration offer the advantages of shorter interconnects without the use of long wires, and thus improved electrical performance, reduced package thickness if thin components are available, and enhanced thermal performance.

Metrics

Table II-1 Performance metrics

Parameter	Value
Resistance between driver and switch	< 1 milliohms
Inductance between driver and switch	< 50 pH
Package thermal resistance from Junction to Case	<1 C/W
Package thickness	<0.2 mm per active device layer
Power density (Area)	1 – 5 W/mm^2
Power density (Volume)	1 W/mm^3

Existing Solutions and Challenges

Integrated Drivers

The need to reduce parasitics in the interconnect elements of power transistors and their drivers was recognized early by the industry. Particularly challenging is the inductance that is developed by the connections among separate dies when they are separately packaged, as it creates ringing on the switching nodes and can make it difficult to properly control the turn-off behavior of transistors. This issue led to the creation of DrMOS, originally implemented by co-packaging the discrete MOSFETs of a half-bridge with their drivers in a leaded package with a split power frame, and later utilizing more complex frames to further reduce parasitics. An example of this implementation is illustrated in Figure 6. This approach delivered good performance for silicon implementations running at switching frequencies below 1MHz. Similar implementations were developed for GaN FETs (see Product Specifications of TI LMG5200), where the drivers and power FETs are co-packaged, as shown in Figure 7. Yet, the small parasitic capacitance and higher frequencies afforded by GaN FETs cause the interconnect parasitics to limit the achievable performance, even when the drivers are placed in the same package.

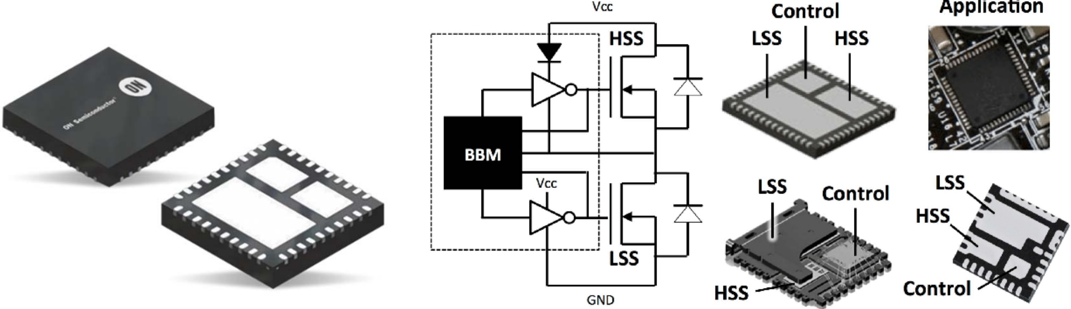


Figure II-6: Control, high-side switch and low-side switch integration in leadframe packages.

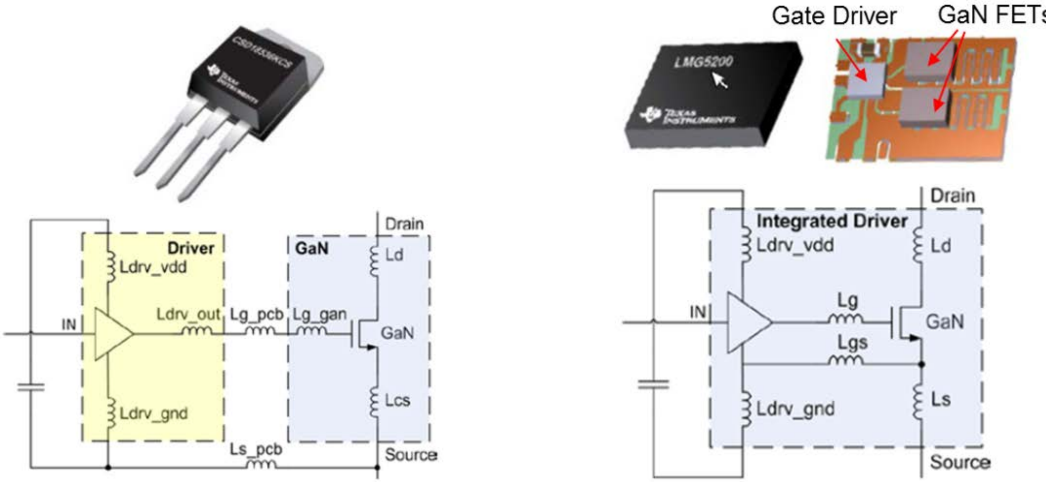


Figure II-7: Integrated GaN drivers and switches on the same package.

Monolithic Integration: In order to benefit from GaN ICs, companies such as EPC and Navitas seek to monolithically integrate driver, logic, FETs, and other functions to make a system-on-chip half-bridge [15, 16]. GaN manufacturers have thus developed GaN processes that allow the integration of multiple FETs on the same die, thus enabling the implementation of drivers and power transistors in the same die. This technology significantly reduces key losses associated with discrete packaging methods by eliminating some of the interconnections. For example, since the gate drive and FETs are integrated on a single die, gate loop inductance can be eliminated resulting in a reduction in gate loop loss. The benefits are shown through the gate loss comparison in Figure 8.

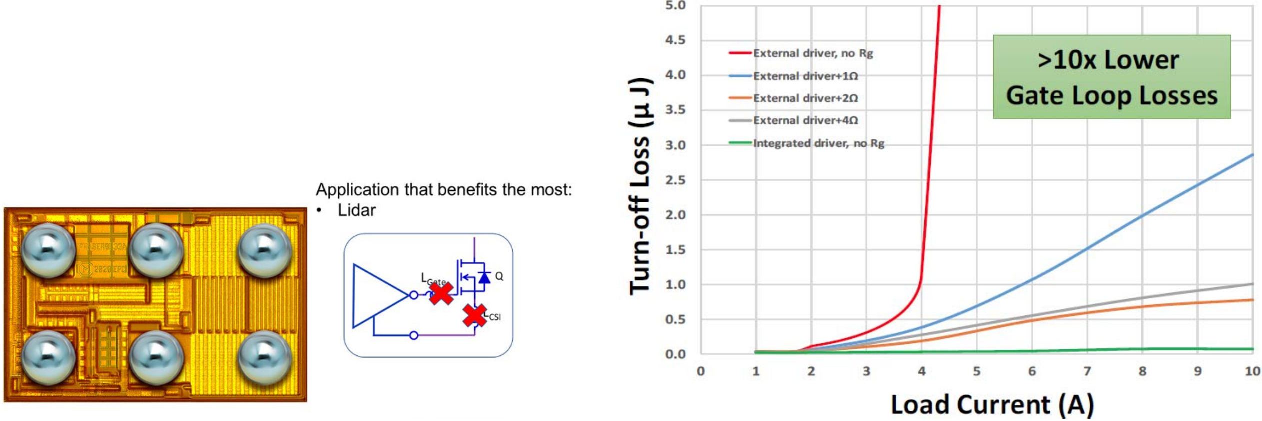


Figure II-8: Gate loop loss comparison of monolithic ICs with external drivers.

2D Leadframe Package Integration: Most power devices are packaged in discrete low-pin-count packages such as a leadframe package that offers low cost and has high current carrying capability. In the same way that SiPs are achieving higher density, lower cost and higher performance by heterogeneously integrating multiple device types into one package, multiple power devices can be integrated into a common package. This could include power switches, gate drives, PMUs and passives. This concept has been advanced by Texas Instruments and others to reduce circuit footprint and increase performance. Figure 9 and Figure 10 illustrate the integration of various power devices onto standard leadframe packages with thick Cu I/Os and large die pads. The upper-left portion of Figure 9 depicts a GaN power FET and a Si gate driver wire bonded in a leadframe package. The two circuits to the right of that incorporate a high-side power switch, a low-side power switch and the controller within the leadframe package. The two circuits on the right depict the integration of two power ICs and an integrated passive device (IPD), which can be mounted over the power ICs, or mounted under them (lower figure). These integrated power packages reduce the circuit footprint and thickness, eliminate Bill-of-Material burden for the customer, reduce parasitic inductances and better addressing thermal resistance. Complex Multiphysics co-design that solves the thermal, electrical and thermomechanical models concurrently is needed to achieve the heterogeneous integration. Supply-chain readiness is another key aspect that must be addressed.

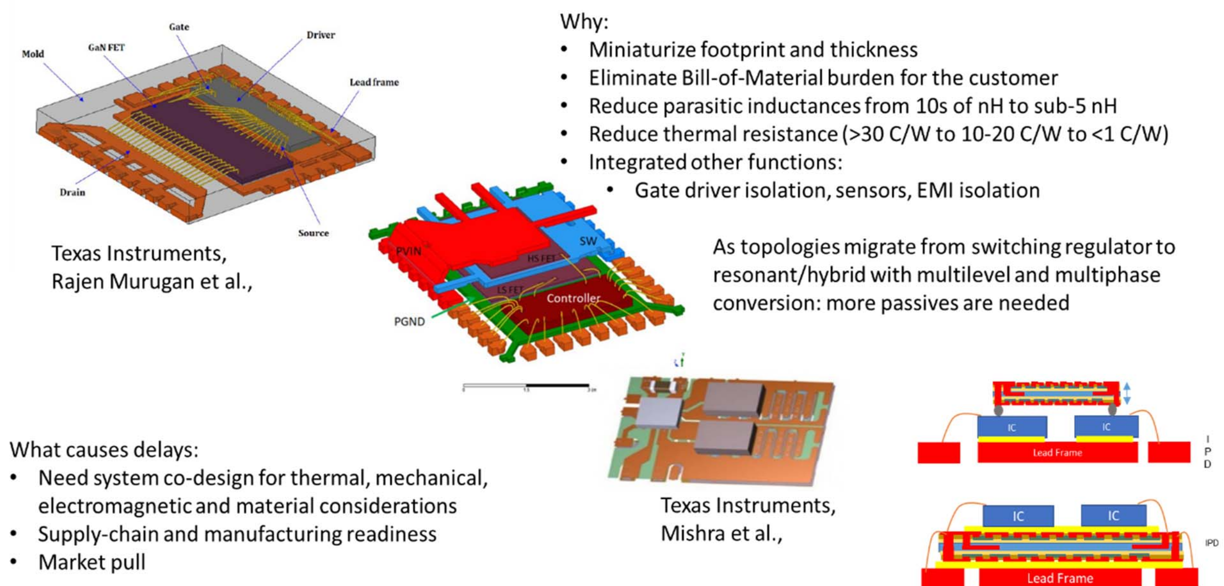


Figure II-9. Evolution of leadframe packaging.

3D leadframe packages: Although chip stacking within a package and in a package-on-package (PoP) have been used for logic and memory chips, the stacking of power devices in power conversion circuits has generally not been done due in part to the increased thermal load in a smaller area. Texas Instruments has developed PowerStack, a 3D power packaging technology not only for its 2:1 footprint reduction but also for its electrical and thermal performance. Figure 10(a) depicts a cross-section of a power block with the high-side and low-side MOSFETs stacked using thick Cu clips using Texas Instruments PowerStack technology. The source of the low-side die is attached the foundational pad of the lower Cu clip of the leadframe which provides the ground connection for the low-side MOSFET as well as a low resistance thermal path. The middle Cu clip provides the drain contact of the low-side MOSFET and the source contact of the top-side MOSFET as well as being the voltage-out lead. Finally, the top Cu clip connects to the top-side MOSFET drain contact and forms the voltage-in lead. The gate contacts are wire bonded (not shown). Stacking the high-side and the low-side power switches in power conversion circuits such as a synchronous buck converter not only reduces circuit board footprint by about half, but minimizes interconnect distances providing lower circuit inductance, lower resistance on all current paths, increased converter efficiency and lower thermal dissipation. Figure 10(b) illustrates the footprint savings for stacking the two power MOSFETs (40% reduction) and forming a one-package power block, and for integrating the controller along with the stacked MOSFETs (60% reduction), both compared to a three-package configuration.

The electrical and thermal advantages of the PowerStack 3D stacking are illustrated in Figure 10(c). The schematic on the left depicts the circuit diagram of two side-by-side MOSFETs in one MCM package and the same devices stacked in a PowerStack package. The side-by-side version (on the left) has high parasitics on all four connections. The center schematic highlights the parasitics that are eliminated in going to the 3D stack – the low-side source to ground parasitics and the high-side source to the low-side drain parasitics. Finally, the schematic on the right depicts the resulting reduced parasitics of the 3D stacked configuration. This provides for higher current levels, higher switching rates, reduced conduction, reduced switching losses and reduced thermal dissipation. Also critical to stacking power die is providing an optimal, low thermal resistance path since the thermal dissipation from both MOSFETs are additive. The PowerStack does this by directly attaching the large ground clip to a top-side pad on the PCB, putting thermal vias under the ground pad and using the board's buried ground planes for improved thermal spreading to improve thermal performance (Figure 10(c)).

High thermally conductive epoxy mold compound: Epoxy molding compounds with higher heat dissipation capacity and lower coefficient-of-thermal-expansion (CTE) are favorable for thermal management of high-power devices. More compact structures, such as embedding with higher power density, implies higher heat generation that needs to be managed without affecting the reliability and the performance of the components. Even with high silica filler loading, the thermal conductivity of standard mold compounds is between 0.9 to 1 W/mK. For applications requiring higher thermal conductivity, different types of resin materials in combination with high K fillers such as boron nitride, boron carbide, and aluminum nitride are used. More recently, carbon-based additives are being looked at for improving thermal conductivity. A mold compound with 8.7 W/mK was formulated by incorporating high-purity graphene without impacting melt viscosity. The properties of the advanced high thermal conductivity mold compounds are reported in [17].

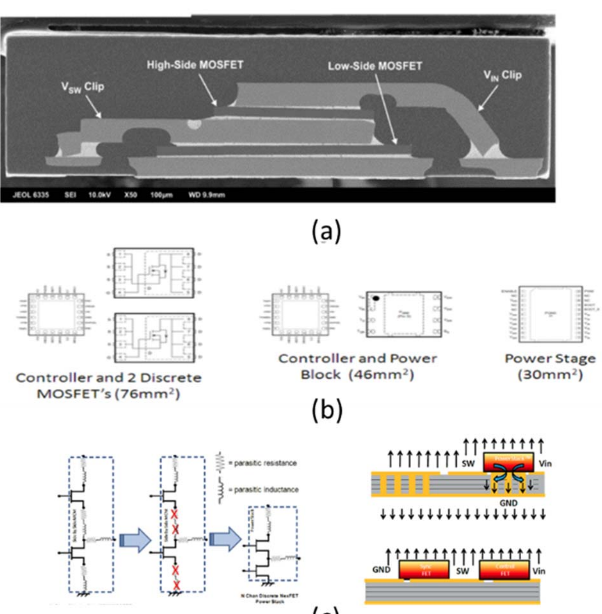
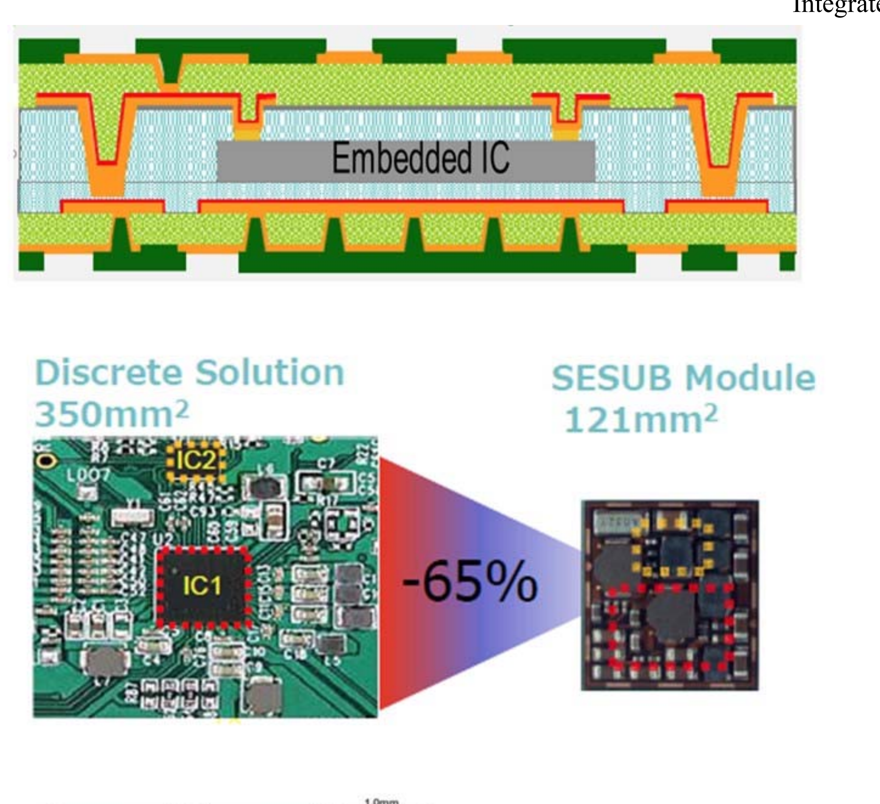


Figure II-10. Advantages of Texas Instruments Leadframe Power Module SIP Integration [1] [2].

Texas Instruments' GaN flip-chip-on-leadframe: The key advance in heterogeneous leadframe integration is the combination of wide bandgap devices with CMOS gate drivers. In addition, the devices are flip-chip assembled instead of wire-bonded. One such key advance is Texas Instruments GaN half-bridge power stage for 48V-PoL applications. It consists of two GaN FETs with a gate driver. Figure 10 compares the circuit schematics of this integrated packaging method with standard discrete assembly, showing the differences in the number of parasitic elements. The gate loop inductance, which affects ringing and overshoot in switching, can range from 5nH-20nH for the standard packaging method, whereas that of the package with integrated driver is reduced to 1nH-4nH [2]. This type of low-inductance package, which results in less power dissipation during switching and safer operation of the devices, is required to realize the GaN switching performance.

Laminate-Embedded Modules: Conventional SiP modules have discretely-packaged ICs that are surface mounted on a PCB, creating a long electrical distance between ICs. With embedding, the electrical distance between ICs can be substantially shortened within the SESUB, as shown in Figure 11. These short signal and power lines reduce the parasitics R, L, C associated with the interconnections, and alleviate noise emission issues. Embedding of ICs in the package reduces the overall footprint of the package by bringing the dies directly underneath the surface-mount passive components. This reduction of footprint makes it attractive for mobile applications. The via interconnects provide significantly reduced parasitic inductance and resistance, while providing a thin profile and high-density packaging. It also enables 3-D stacking of components, and enhanced primary and secondary thermal management for power devices with high local heat flux and temperature-sensitive devices such as capacitors. Embedding, thus, permits integrated thermal management, allowing optimal performance of heatsink technologies by removing packaging interfaces [18]. The planar design also allows flexibilities of (1) double-sided cooling and (2) system integration of gate drive circuits. The electrical and thermal performance benefits are shown in Figure 13. The materials include: a) High-Tg laminates, b) High-thermal conductivity and low-CTE molding compounds, c) High-temperature interfaces, d) Barriers to oxygen, moisture and other ions, and e) Low-CTE or low-stress conductors. These are discussed in Figure 13 [19, 20]. Chips are sintered to a copper lead frame with premachined cavities where the lead frame provides mechanical support, enhances thermal spreading and distributes corresponding electrical potential to the bottom electrode of the chips. A silver sinter die-transfer film is used to form a well-defined homogeneous contact layer in the cavities. The chip top-side metallization is accessed by laser drilling the FR-4 material and electroplating with copper to form the copper via. The thermal interface material has a thermal conductivity of 5 W/mK.



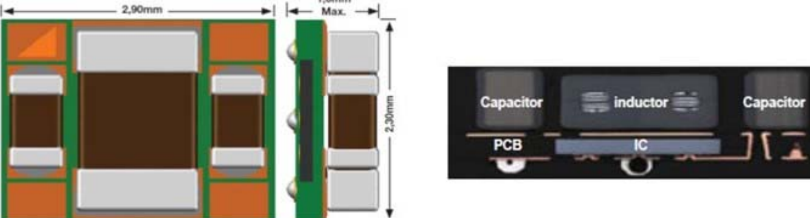


Figure II-11. Texas Instruments' MicroSiP DC-DC module [14] and TDK's SESUB Package.

Table 5 summarizes the key properties for advanced high-Tg epoxy resins. Laminates from these substrates are used to demonstrate embedded power modules. The laminate consists of high-conductivity ceramic particles to improve thermal conductivity. The IC is embedded in the resin structure, and subsequent build-up processes including via formation are simultaneously carried out on both top and bottom sides of the substrate to make the package structure. The leakage current is within 10nA up to 4kV at room temperature and is below 100 µA for >1.5kV at 250°C. Reliability studies indicate that the power module operation does not degrade on thermal cycling between -55°C to 125°C for 1000 cycles and thermal aging at 150°C for 2000 hrs [21]. For non-aged modules, the breakdown strength of the material is between 5.34 and 6.51 kVrms, while after thermal cycling the breakdown strength range drops to between 4.73 and 4.2 kVrms.

The concept of die embedding into laminates was first explored in the "HERMES" EU project for power applications. The Texas Instruments MicroSiP module is one of the first miniaturized DC-DC converters that uses active die-embedding technology using the Embedded Component Packaging (ECP®) process as developed by AT&S. A high-performance power management device is embedded in a laminate substrate, and discrete passive components are assembled onto the top side of this substrate, as shown in Figure 11. This embedding technology increases the power density, saves board space for the device footprint, and reduces the interconnect length [13]. These features that active-embedding brings are particularly important in miniaturized systems such as portable or wearable electronics. SESUB (Semiconductor Embedded Substrate) is TDK's state-of-the-art substrate technology which has embedded ICs in a PCB substrate. SESUB offers several advantages over standard SiP structures, such as board space saving, reduced parasitics, improved thermal management, and low profile. Power-die embedding has also been advanced by ASE's a-EASI technology where the thermal performance is enhanced with the exposed copper pad. The package is thinner and the parasitic inductance is also reduced with this. The next step is then to stack multiple dies on either side of the leadframe or side-by-side. These are illustrated in Figure 12.

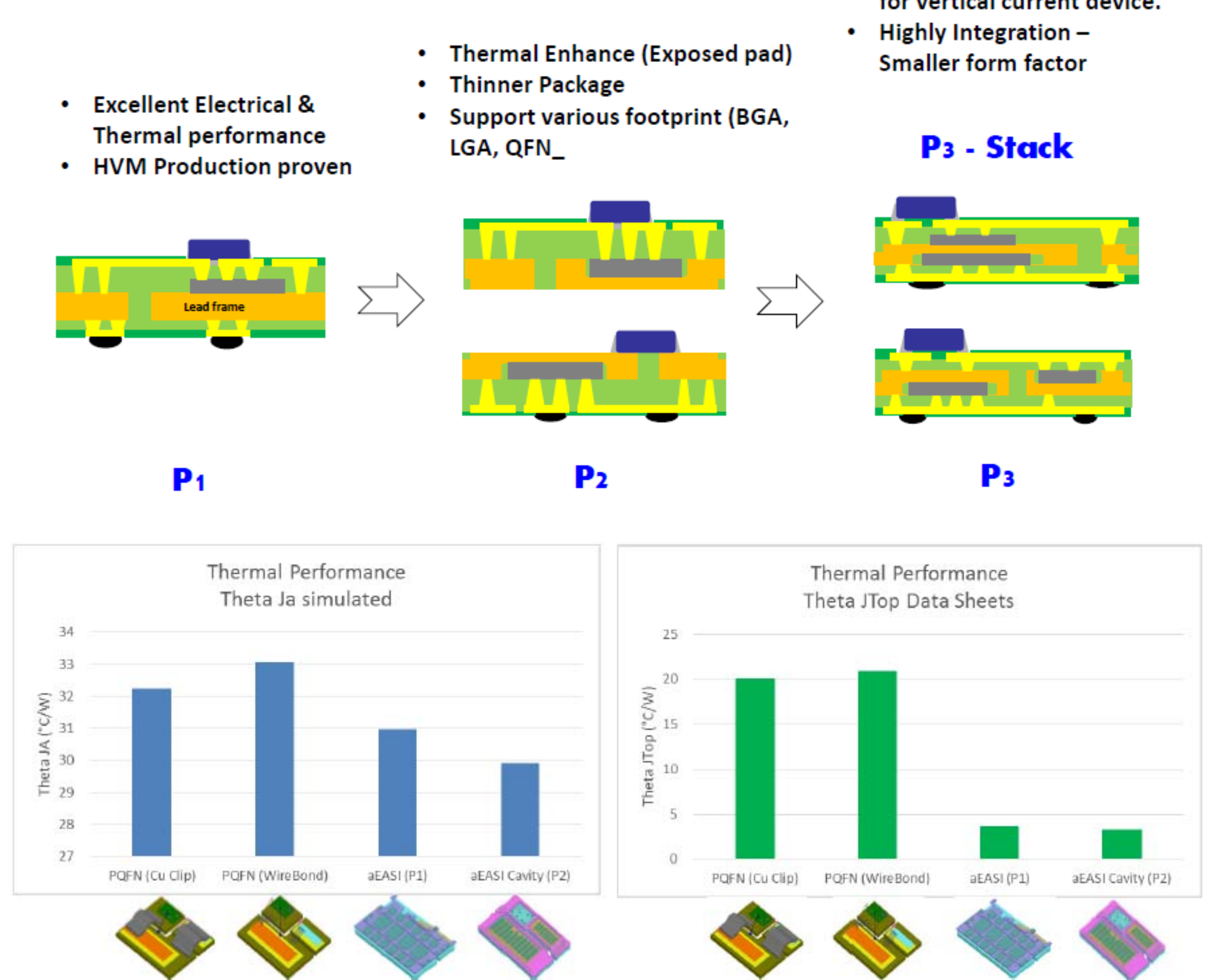


Figure II-12: ASE's advances in embedded packaging for lowering the parasitics, thermal resistance and package thickness.

The AT&S ECP® process has also been applied by GaN Systems to package their new 650V/30A GaN-on-Si HEMT transistors. The improved performance is summarized by Rainer Frauwallner (AT&S) in Figure 13. The Schweizer Electronics p2 Pack power embedding technology is another extension of this, with embedded dies, where bond wires are replaced by direct galvanic contacts with Cu-filled vias to minimize the package inductance. This substrate is then further embedded into PWBs of 575mm x 583mm in size for direct integration of drivers and control systems. Schweizer's p2 Pack power module is one of the first packages to enable co-integration of power, control and driver ICs in a single package in a thickness of less than 1.4 mm. Panel-based power embedding has begun to emerge in a big way for analog products, starting with low power, then high power, and in the future many others that include integration of many devices. These panels don't require BEOL tools, materials and processes. The panels can be manufactured outside the IC foundry. Embedding by AT&S for low power and by Schweizer and Fraunhofer for high power, both in board-like large panels, are examples of ePFO. These are extended to kW embedding, which is the key focus of Section III.

Figure II-13. Improved thermal management and electrical parasitics with embedded packages (GaN systems).

Table II-5 Material Properties [11]

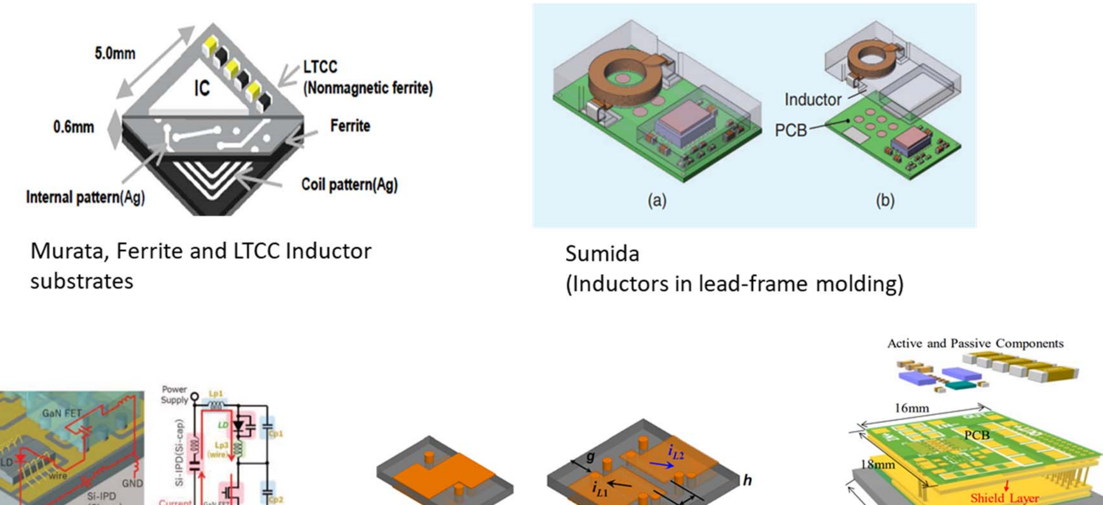
Parameter	Value
Thermal conductivity	8 W/mK
Tg	270 ^{0}C
Modulus	30 Gpa
CTE	9/22 PPM/^{0}C
Water sorption	0.27 %
Dielectric strength	5.6 kV @120 um

Table II-6 Material properties of prepeg material system [12]

Parameter	Value
Tg (DSC)	200 ^{0}C
Tg (DMA)	220 ^{0}C
CTE	38 ppm/^{0}C
Peel strength	>1.4 N/mm
Thermal conductivity	0.7 W/mK

Package-Embedded Passives: With the trend to 3D packaging, the prevalent approach is to embed active switches and controllers in the laminate, followed by surface assembly of passives. However, since the passives limit the volume of the module, there is an increasing trend to have passive component substrates. Both capacitors and inductors are embedded in substrates or packages for the power modules. In some cases, they are used as the substrates themselves. Examples are the magnetic-embedded substrates by Virginia Tech, ferrite-substrate power modules by Murata, and silicon trench capacitor substrate modules by Murata. Selective examples of these are illustrated in Figure 14. Integration of capacitors and inductors in single-phase and multi-phase IVRs will be the key to meet the power density, size, weight and thickness targets of future products. Higher switching frequency is critical for higher bandwidth, faster load transient response, and higher voltage scaling speed for better energy saving by dynamic voltage and frequency scaling. Higher current is required to meet the demand for higher functional integration. Low current (< 1 A/phase) and high-frequency (> 50 MHz) IVRs tend towards wafer-level integration, while high current (> 3 A/phase) and low-frequency switching (>1-20 MHz) with fewer phases tend to utilize

package-integrated IVR (Figure 15). A schematic cross-section of both approaches is also shown in the figure. Future magnetic materials and heterogeneous integration is soon expected to meet higher current/phase and higher frequencies at the same time.



Murata, Ferrite and LTCC Inductor substrates

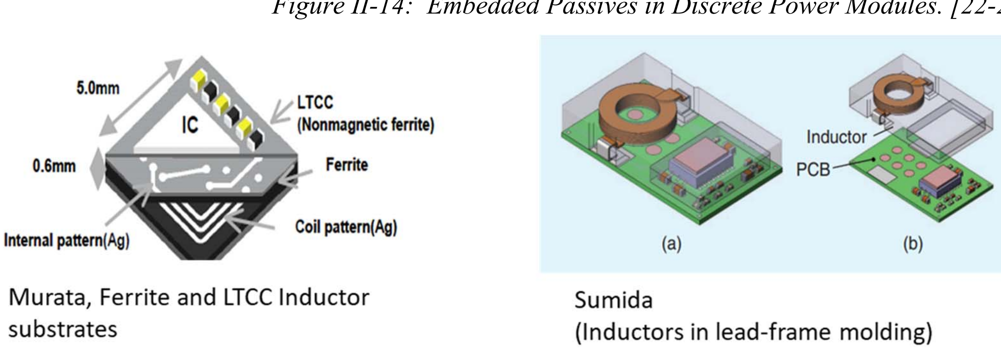
Sumida (Inductors in lead-frame molding)

Modules on silicon capacitor substrates; Murata's LIDAR modules

Virginia Tech (Inductors in laminate)

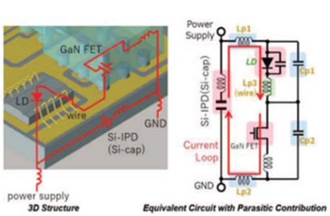
GaN DC-DC converter with substrates-embedded inductors

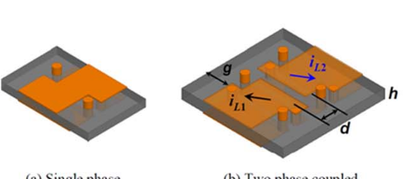
Figure II-14: Embedded Passives in Discrete Power Modules. [22-26]

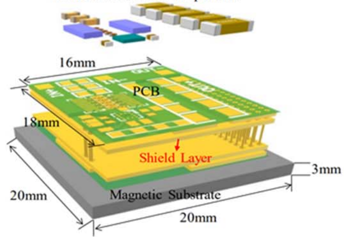


Murata, Ferrite and LTCC Inductor substrates

Sumida (Inductors in lead-frame molding)







Modules on silicon capacitor substrates; Murata's LIDAR modules

Virginia Tech (Inductors in laminate)

GaN DC-DC converter with substrates-embedded inductors

Figure II-15: Integrated inductors for wafer-level and package-level integration. The number of phases are shown in the figure. [27] [Bottom right figure is from Ferric Inc]

II.3 POTENTIAL SOLUTIONS AND REQUIRED R&D

Table 2 and Table 3 provide the projected performance metrics for power modules that support different application segments. A summary of such projections is also shown in Figure 16. This report provides the reported advances in form-factor, thermal resistance and parasitics that drive these key technologies. The key solutions are in different categories:

- Component Performance: There is a continuous need to advance the volumetric density of passives without sacrificing their efficiency and power handling. This has been the biggest challenge in the miniaturization of medium-sized power modules. In addition, heterogeneous integration of active devices is another key challenge.
- Substrate Materials: High Tg (>250°C) substrates with low moisture absorption, resistance to electrochemical migration at high temperature and humidity.
- Devices with copper termination and laser compatibility: For embedding, it is critical to form galvanic connects (electroplated copper) onto the device terminations. Analog devices come with aluminum metallization that needs specific barriers towards copper.
- Assembly: Backside metallization of dies has to be compatible with direct bonding on copper leadframes or packages. This is traditionally achieved with solders, though they suffer from long-term electrical stability issues that forced the industry to look for silver or copper die-attach materials. Pressureless assembly of dies with nanosilver and nanocopper is a key challenge that the industry is facing.

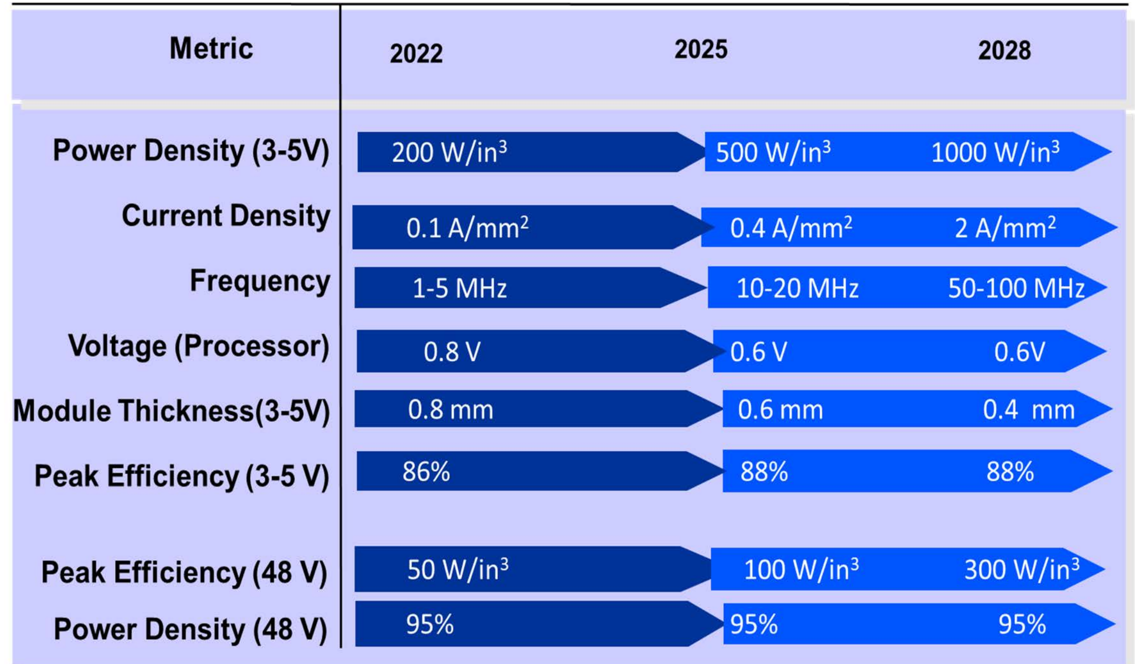


Figure II-16: Projected performance metrics for power modules.

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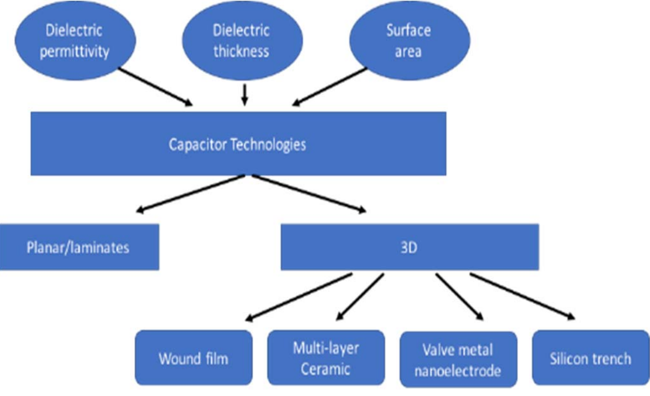
II.4 Passive Components:

II.4.A Capacitors

Capacitors are the key storage components in the power delivery network. They are essentially used to filter the output voltage noise and maintain a smooth power supply. High-frequency switching in the active IC can lead to large voltage spikes or transients because of the inductance and resistance parasitics. Such transients in the voltage across the power-supply rails can limit maximum allowed current transients. Excessive switching noise limits the dynamic switching speeds and power-efficient designs. Decoupling capacitors are used along the power delivery network to reduce the magnitude of the voltage spikes and maintain a stable voltage. These decoupling capacitors are essentially charge reservoirs that act as local power supplies. They help supply charge when there is a droop in the voltage and absorb it when there is a spike. This helps level out the fluctuations and maintains a constant voltage across the power and ground planes. As the frequency increases in high-speed digital circuits, decoupling capacitors are needed



FigureII-17. Summary of capacitor technology classifications and the three main design parameters affecting their capacitance level.

to supply large current surges during very short time intervals, with values approaching 500 A/ns. In order to minimize the degree of intervening interconnection impedance parasitics, decoupling capacitors should be placed as close to the IC as possible. Package-embedded capacitors have lower parasitics and improve the electrical performance at higher clock speeds (>350 MHz). Capacitors are also increasingly utilized as storage elements in switched-capacitor or hybrid power converters.

Multiple approaches are used at different levels of the power delivery chain (Figure 17), based on the current and voltage rating, equivalent series resistance (ESR), frequency stability, capacitance density, thickness and integration options. Capacitors affect the size, design constraints and the overall performance of the power delivery network.

Table 7 compiles the key performance metrics of a capacitor.

Table II-7: Comparison of Capacitor Technologies.

Performance Parameters	MLCC	Silicon Trench	Ta capacitors
Capacitance density	20 μF/mm^3	10 μF/mm^3	20-30 μF/mm^3
Thickness	125 - 500 μm	100 μm	50-75 μm
ESR	5-10 mΩ.× μF	5 mΩ × μF	50 mΩ × μF
Frequency stability	>100 MHz	10-100 MHz	10-100 MHz
Leakage current	0.1 μA/μF	0.1 μA/μF	0.1 μA/μF
Integration	Die-side or landside assembly/embedding	Silicon- integrated	Wafer or package-embedding

1. Existing Solutions and Challenges:

Capacitors comprise two electrodes that are isolated with a thin dielectric. The key electrode requirements are conductivity, high Schottky barrier for low leakage, and easy processing on various substrates for surface area, while the key dielectric requirements are dielectric strength, low thickness with no defects, and permittivity. Various capacitor structures are formed through different combinations of dielectrics and electrodes, as illustrated in Table 7.

Planar capacitors can either be made from certain polymer films or laminate materials, thin-film oxides, or sometimes composites of polymer and inorganic fillers. Oxides are deposited onto a metal using either physical or chemical vapor deposition, and then the top surface is metallized to form the counter electrode. These capacitors are ideal for 3D integration due to their planar design, but often have low capacitance values in the range of 10-50 nF/mm^2. Therefore, their use is mainly in on-chip or package build-up layers.

Surface-Mount MLCCs: Multi-layer ceramic capacitors (MLCCs) are a type of 3D capacitor that can have very high volumetric densities due to their multilayer stacking of high-permittivity ceramic layers. By making use of stacked and planar electrode layers in parallel, MLCCs can maintain very low ESR and ESL values. They have been the workhorse for board-level modules with very high volumetric densities due to their multi-layer stacking of high-permittivity ceramic layers. The relative permittivity of the ceramic layers can range from <40 for $CaZrTiO_3$ (class I paraelectric dielectrics) to >5000 for $BaTiO_3$ (class II ferroelectric dielectrics). Class I dielectrics do not change much in polarizability at different DC voltages or temperatures, whereas class II dielectrics can be strongly affected by both but achieve very high volumetric densities. MLCCs maintain very low impedance values (5 milliohms x microfarad) due to their combined benefits from low DC resistance from nickel electrodes and high capacitance. For this reason, they are the most widely used type of capacitor technology. Densities of 2 μF/mm^2 with ~100 micron films are now utilized for package-embedded decoupling with densities of 20 μF/mm^3. In one such example, a 0.13 mm thick, 0.22 μF capacitor with only a 0.6 mm • 0.3 mm footprint is available, leading to about 20 μF/mm^3. Several companies are now providing such high-density options at ~0.1 mm thickness, including Murata, Taiyo-Yuden, AVX, and Samsung. In terms of footprint, new ultra-small options have recently become available, using only a 0.25 • 0.125 mm area. At a slightly larger footprint, a 10 μF capacitor in a 1 • 0.5 size with 20 μF/mm^2 has a thickness of 0.5 mm. Typical area densities and footprints with different voltage ratings are compiled in Table 2. Such advances are feasible by reducing the dielectric thickness with finer barium titanate particles and also thinning the nickel electrodes with finer nickel particles. These systematic advances are recently compiled by Murata, as shown in Figure 2. These are surface-assembled onto the land-side or die-side of the substrates as illustrated in Section I. The downside is lower voltage capability, as noted above.

Inserted MLCCs: Smaller footprints and thinner form factors are needed to accommodate miniaturized, fine-grain power management with ultra-short interconnection lengths. Traditionally utilized as surface-mounted devices

Table II-8: Comparison of densities, thickness and voltage ratings for leading-edge capacitors.

Thickness Voltage	0.5 mm	0.4 mm	0.3 mm	0.2 mm	0.1 mm	0.05 mm
1-3 V					0.94 μF/mm^2	
4-5 V	20 μF/mm^2	8 μF/mm^2	6 μF/mm^2	2.75 μF/mm^2	0.44 μF/mm^2	0.2 μF/mm^2
6-10 V	8 μF/mm^2	8 μF/mm^2	4.4 μF/mm^2	2 μF/mm^2	0.44 μF/mm^2	
11-25 V	2 μF/mm^2		0.1 μF/mm^2		0.03 μF/mm^2	
26-50 V	20 nF/mm^2					
51-100 V						
>100 V	5 nF/mm^2					

(SMDs), discrete MLCCs are becoming so thin that embedding within the package is possible. This is accomplished by assembling the capacitor inside substrate cavities, followed by planarization, via-drilling and via metal contacts

with electroplating. Thinner layer MLCC technologies with high capacitance at lower voltage ratings for consumer electronics have been exclusively developed with Ni BME technology, making this, by far, the most common capacitor type. Copper inner electrodes have also been commercialized for high-frequency RF capacitors to achieve high Q.

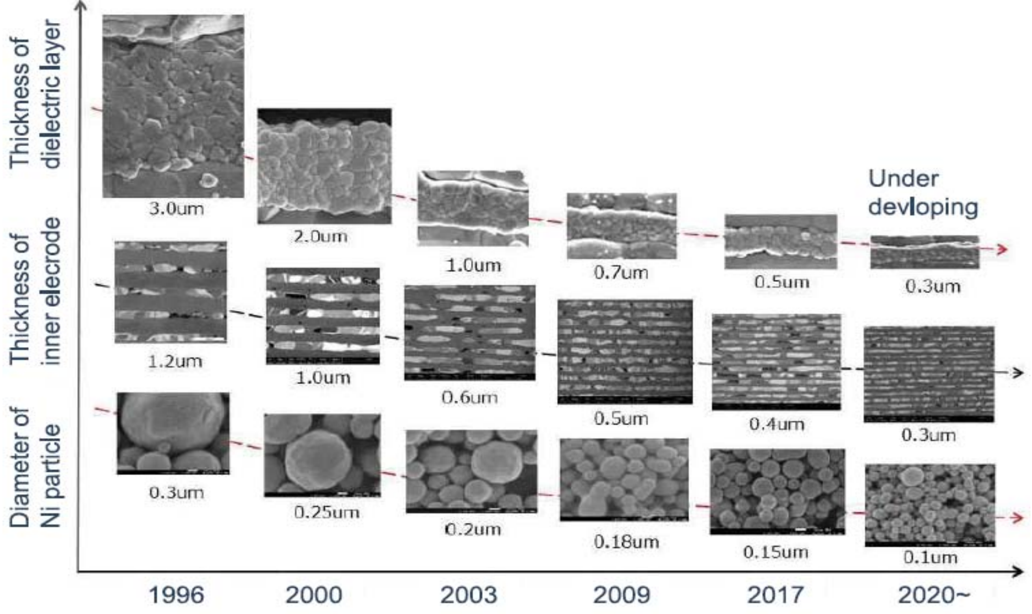
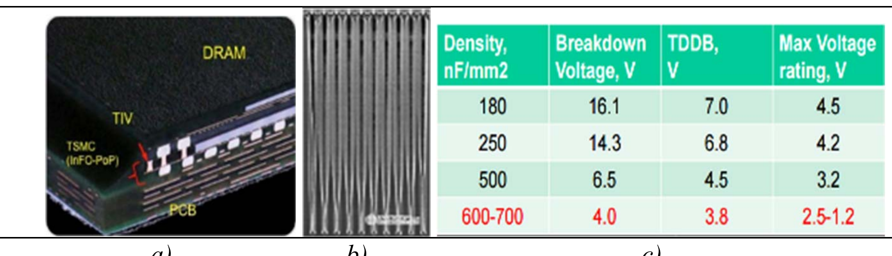


Figure II-18. Multilayered ceramic capacitor advances from Murata, with thinner dielectrics and electrodes from finer particles [1].

Anodized High-Surface-Area Capacitors include mainly the metals tantalum and aluminum, which can form relatively high-permittivity oxide dielectrics down to nanometer-scale thicknesses. Additionally, since the oxide (Al_2O_3 or Ta_2O_5) is formed directly on any surface topography in a very controlled anodization process, the capacitors can make use of very high surface areas. Such capacitors can achieve densities exceeding that of MLCCs. The counter electrode or cathode is formed with a conducting polymer or manganese oxide. They are particularly suited for low-frequency decoupling where large capacitors are needed, and a single electrolytic capacitor can replace several MLCCs. Particulate electrodes (eg, tantalum) or etched aluminum foils are well-recognized for achieving high capacitance volumetric density. However, they are not able to compete with MLCCs yet [2, 3]. They usually feature higher equivalent series resistance (ESR). The high ESR arises from the low conductivity of the cathode materials used in high-surface-area capacitors.

Trench Capacitors: These are silicon-integrated capacitors that are becoming more viable candidates because of advances in silicon thinning, embedding or assembly with high reliability. These are also emerging as the mainstream

option because of their silicon fab compatibility, and continual escalation in capacitance density to that comparable to MLCCs. They are formed with CVD or ALD dielectrics on deep silicon trenches. One other strategy for increasing silicon trench capacitor density is using different dielectric materials. Si_3N_4 can be thermally grown on silicon in a nitrogen-rich environment, instead of SiO_2, providing a slight increase in permittivity and thus higher capacitance values. Similarly, alumina and hafnia are emerging as suitable candidates because of their high permittivity.



Density, nF/mm2	Breakdown Voltage, V	TDDB, V	Max Voltage rating, V
180	16.1	7.0	4.5
250	14.3	6.8	4.2
500	6.5	4.5	3.2
600-700	4.0	3.8	2.5-1.2

a) b) c)

Figure II-19. (a) TSMSC InFO-PoP in Apple A10 processor (b) TSMC deep-trench capacitor structure (c) Current and projected capacitance densities and voltage ratings for the silicon capacitors [4]

Table II-9: Comparison of densities, ESR, current-handling and operating conditions of high-voltage capacitors. (Source: Datasheets from companies)

	Polymer film caps ECI HT1		CDE 550C Aluminum Caps	KEMET Ni BME C0G		TDK CeraLink PLZT Ceramic		Advanced electrodes and dielectrics
mF/cc	0.7	0.085	>6	1	0.6-0.012	5.5	5.5-2	10
V	400	600-2400	200-500	500	1000-3000	400	500-900	400-1000
ESR (mΩ x mF)		60	16-228	3-5	3-5	10-12	10-12	<5
Irms (A/ mF)	1	5.2	5-31	50		12	12.5	50
Temp		125-150 C	105	125	125	150		105-150

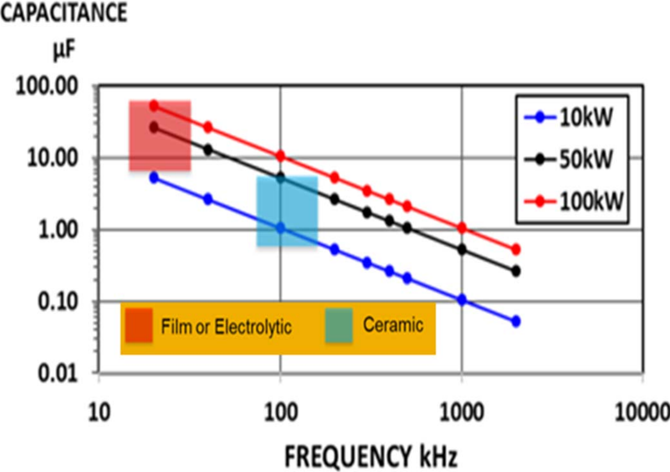


Figure II-20: Capacitor requirements for 400 V DC link applications and technology options. (Source: KEMET, modified from Prof. R. Kennel, Technical University, Munich, Germany).

High-voltage capacitors: In the quest for more efficient power conversion, hybrid and switched-capacitor power converter topologies have been developed. To achieve the high efficiencies desired, low-loss ceramic capacitors have been developed for the LC tank. In the high-voltage domain beyond 400 V, polymer film capacitors are popular due to their ultra-high stability and reliability. Polymer dielectrics are very stable, have high dielectric breakdown strengths, and feature self-healing, making them ideal for the highest power applications. Estimation of capacitor needs for high-voltage and high temperature, based on Equation (1), is illustrated in Figure 21.

$$C = \frac{P_{Load}}{U_{Ripple}\left(U_{Max} - \frac{U_{Ripple}}{2}\right) 2\,\pi\, f_{Rect}} \quad (1)$$

Higher capacitance densities are available with multilayered ceramic capacitors, with densities exceeding 5 µF/cc for 500-900V operation. A new class of dielectrics, based on antiferroelectric material, with relative permittivity >1000 at high voltages, are also developed to achieve 5 µF/cc with 600-1000V by TDK. $CaZrTiO_3$ (class I paraelectric dielectrics) are also pursued for this application because of their stable permittivity and reliability performance at high temperature and voltage gradients.

Assembly Technologies: Passive components are fabricated with tin finish for solder assembly. Nickel barriers are used to form stable intermetallics with no long-term electromigration issues. For high-power passives that support currents of several Amperes, new advances have been introduced by close partnership between component and materials companies. One such advance is the copper-saturated solders for complete conversion to Cu_3Sn intermetallic with no further thermal migration issues with copper interfaces. Known as Transient Liquid Phase Soldering (TLPS), such high-temperature interconnects use solder pastes that are loaded with copper particles to form stable intermetallics. While leaded X7R stacks are available from several companies for lower-temperature applications, KEMET offers C0G leadless stacks. One major advance for bonding leaded stacks is Transient Liquid Phase Sintering where a low melting point metal or alloy is reacted with a higher melting point metal or alloy at a relatively low temperature. The resulting TLPS interconnect cannot be re-worked but has a higher temperature capability than the lower melting point metal or alloy. This technology can be used to replace high melting point (HMP) Pb-containing solders in leaded stacks and has facilitated the development of leadless stacks mentioned earlier [5]. More recently the TLPS technology has been used to embed passive components in circuit boards and substrates [6]. This approach can achieve high shear strengths with thin joints that lead to the lowest parastics. For embedded or inserted inductors, interconnects are formed through direct laser-drilled vias and copper plating over the capacitor pads. The key requirement in this case is the availability of capacitors with copper terminations for easy process integration.

Roadmap Projections:

With several capacitor solutions available, a combination of them is required to address the total power supply solution. For higher voltages > 250V, electrolytic and film capacitors are currently preferred for these applications. However, for higher temperatures ≥200°C, only MLCCs are widely available [7]. This trend is illustrated in Figure 21. Furthermore, the increased use of WBG semiconductors switching at higher frequencies favors smaller ceramic capacitors over these other bulk capacitor solutions [8]. The high capacitance density of MLCCs, aluminum electrolytic capacitors and Ta capacitors make them more suitable for lower-voltage decoupling applications (12-200V).

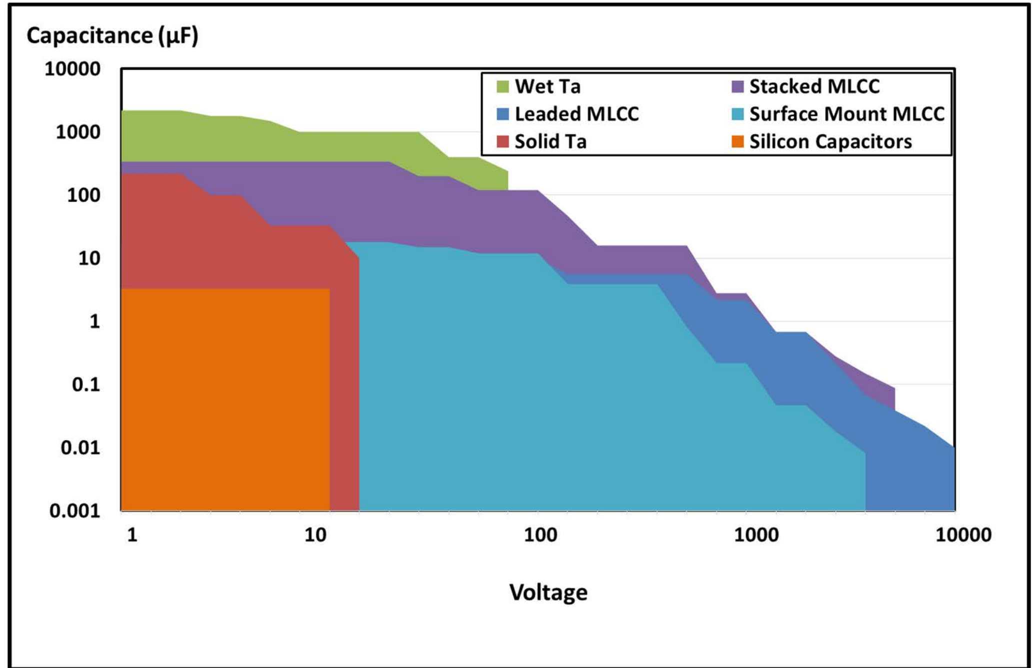


Figure II-21: High Temperature (200°C) Capacitor Types. (Source: KEMET)

For lower voltages (0.8 - 12V), the power delivery capacitor network involves on-chip film capacitors, package power-ground planes with polymer dielectrics, embedded or surface-assembled trench capacitors and MLCCs for

decoupling, and electrolytic capacitors on the board for low-frequency noise filtering. Materials with high permittivity that can sustain high frequencies and be processed at 10-100 nm are always of need. Certain multicomponent oxides and nanoscale grain-boundary capacitor structures are known to feature giant polarization but only sustain low frequencies. Such materials are of interest if they can be extended to MHz frequencies while retaining low leakage. Inserted capacitors are emerging as a key option to achieve better decoupling performance at reduced package footprint.

Key challenges with inserted MLCCs include component thickness, copper terminations for via formation, and reliability from high stresses. The advantages in scalability to thinner components and compatibility with embedding have been driving trench capacitors to the forefront, taking a bit of the MLCC business. Trench capacitors are becoming prevalent for replacing MLCCs because of their silicon scaling and integration advantages in spite of their limited volumetric densities with deep trench electrodes. Innovative nanoelectrodes will soon supersede trench capacitors in terms of performance. Trench capacitors tend to dominate the future high-performance power supply applications. However, the trend to higher volumetric densities may also create new solutions such as carbon nanofiber or porous nanosilicon capacitors with densities of 1-3 µF/mm^2 but only from less than 30-50 micron electrode thickness, resulting in densities of up to 100 µF/mm^3. ALD titanium nitride appears to be the ideal low-ESR electrode solution for achieving < 5 milliohms x microfarad. However, alternative approaches are of high interest. The overall trend in capacitor evolution is illustrated in Figure 22.

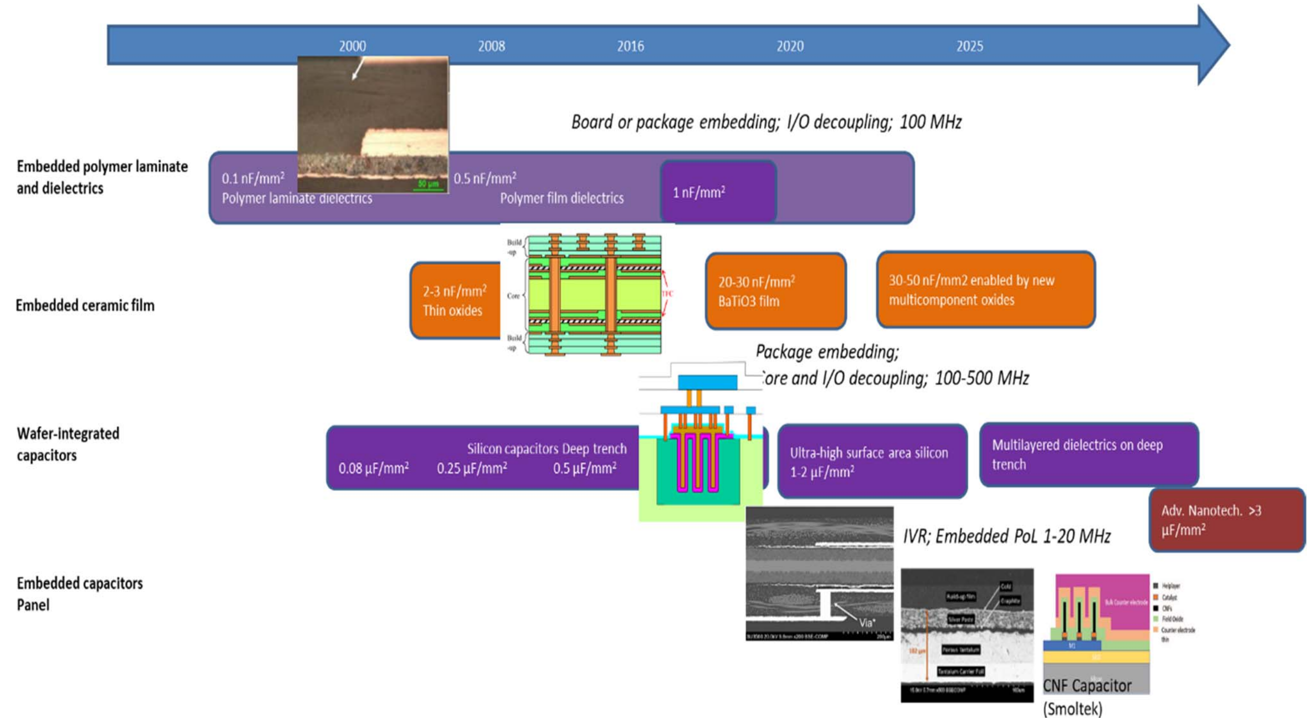


Figure II-22: Capacitor roadmap showing the trend in evolution and future projections.

II.4.B Inductors

Most power converters in PDNs often utilize switching regulator technologies. The input/output voltage conversion ratio is determined by the on/off time of the upper and lower switches. During the on-time, the current rises as energy is stored in the magnetic field of the inductor, which is then released during the off-time at a different voltage than the input. The inductance value of the inductor needs to be large enough to mitigate the amount of current rising and falling that occurs over each period. Any leftover ripple can be mitigated with the use of a decoupling capacitor at the output. The inductors in board-level power modules are briefly described in the section. A short summary of magnetic component advances as transformers for high-density isolated converters enabled by wide bandgap switches is also provided.

Metrics

The key metrics are inductance per area, inductance per DC resistance (nH/milliOhm), current-handling, and power loss (large-signal AC loss + DC loss). The properties of ideal inductors are benchmarked with existing inductors in Table 10.

Table II-10: Inductor performance metrics and emerging need

	Discrete (Ferrite or Metal powder)	Magnetic composites – substrate-embedding	Nanomagnetic films: On-chip	Need
L/Rdc nH/milliohm	15-25	5-10	0.1-0.2	>10
Q	>20	<10	5	>20
Current-handling Thickness	0.01 – 0.1 A/mm^2 200- 500 microns	0.1 – 1 A/mm^2 50 - 200 microns	5-10 A/mm^2 25 microns	5-10 A/mm^2 25-50 microns core
Cost	Low	Low	High	Low

Table II-11: Performance of existing magnetic materials and the need for future

	Thickness Microns	Coercivity A/m	Resistivity m Ohm cm	Saturation Flux (Tesla)	Permeability
Mn,Zn ferrites	>100	3-5	10,000	0.6	5000
Nanocrystalline and amorphous flakes	>15	3	110	1.2	15000
Electroless thinfilms	3-5	10-20	100	1	<<1000
Plated thin films	2-100	20-80	35	1.3	~1000
Flake composites	25-500	100-200	10,000	0.8	100-150
Nanomagnetic films	1-10	10	200-300	1.5	200-500

Existing Technologies and Solutions

The desired magnetic properties for the ideal inductor core are: 1) high permeability, 2) high saturation magnetization and 3) high-frequency stability. Typical properties of magnetic materials are compiled in Table 11, and are briefly introduced here. The maximum current that an inductor can handle is directly related to the reluctance of the magnetic core, while inductance is inversely related to the reluctance. Reluctance is directly proportional to the length of the core and inversely related to the cross-sectional area. Toroids with an airgap feature the lowest reluctance and high inductance. Soft magnetic materials with high permeability are widely used in power inductors to increase the inductance without increasing the footprint or coil length of the inductors. In order to increase current handling, thicker cores with larger field anisotropy (the field at which inductance starts to saturate with applied field) are desired.

Magnetic Materials: Ferrites have been widely used as the magnetic cores for low frequency applications such as transformers. The ceramic properties of ferrites provide high resistivity (> 1 Ω*m) resulting in low eddy current loss for thicker cores. However, the low field anisotropy (Hk) of ferrites limits them to low-frequency applications (~1 MHz). Ferrites also have low saturation magnetization (<0.5 T) and low permeability (μ), which lead to low inductance volumetric density and low current handling when used as the inductor cores.

Soft ferrites have been widely used as the magnetic cores for low-frequency power applications such as transformers. They contain iron oxide (Fe_2O_3) in addition to other transition metals such as Mg, Mn, Zn and Ni. Because of this partial cancelation in magnetic moments, ferrites have lower saturation magnetization (<0.5 T) as compared to metal-based magnetic materials (~1 T). This limits them in high-power applications. However, their magnetic softness and high resistivity make them attractive for inductor and transformer applications. Alloy ribbons are other materials candidates for low-frequency power applications. As compared to ferrites, magnetic metals show higher saturation magnetization and higher permeability. The advanced properties enable miniaturization of transformers. However, the low conductivity of metal elements deteriorates the eddy current loss. To reduce eddy current losses, low-conductive elements such as boron and phosphorus are added to make magnetic metal-alloys such as Metaglass (FeSiBCuNb alloy) ribbon from Hitachi Metals, Ltd. These are suited for low-frequency isolated DC-DC converters with transformer topologies.

Magnetic alloys (Metglas®) from Hitachi show good soft magnetic properties such as low coercivity, low core loss and high permeability. The good soft magnetic properties are the results of absence of grain boundaries and crystal magnetic anisotropy in amorphous alloys. Another example is VITROPERM®, an iron-based nanocrystalline material with soft-magnetic properties: high saturation flux density ≥ 1.2 T, permeability can be adjusted in the range from 400 to 800,000, excellent thermal stability over a wide temperature range, low core losses and low coercivity, and low or zero saturation magnetostriction. VITROPERM products are available as ribbon in thicknesses from 14 µm to 20 µm and widths from 2 mm to 66 mm. Because of their high eddy currents, they are more suitable for lower frequencies as transformer cores and common mode chokes. Thin power inductors from Taiyo Yuden, Tokin, Murata, and TDK often use metal powder cores.

The magnetic fields of a toroid are directed within the plane of the core and the eddy currents are orthogonal to the plane; aligned magnetic flakes have emerged as the key innovation in magnetic materials, in order to increase the permeability. These powder inductors can achieve high inductance and high saturation current while retaining a small size. The low thickness profile enables them to be embedded into substrates and provide high power densities. Figure 5 lists the performance of these inductors.

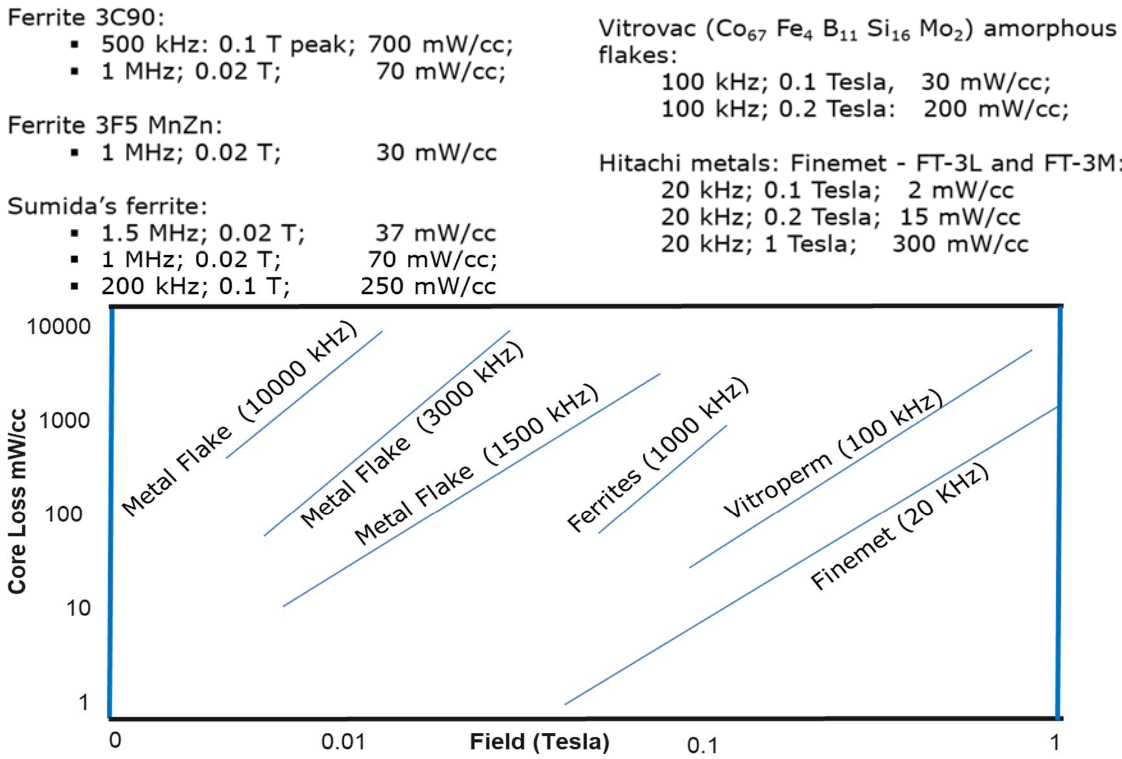


Figure II-23: Power losses in metal-based magnetic cores for low to medium frequencies.

Metal-based particle or composite magnetic cores are suitable for medium-frequency applications with higher current-handling than ferrites. These composites consist of high permeability and high saturation magnetization (Ms) metal particles that are isolated by thin native oxides or polymer for low eddy current losses at high frequency. Permeability and frequency stability are the two properties that can be achieved by engineering the metal particle shape and size in the composite. Saturation magnetization, on the other hand is an inherent material property. At high frequency, permeability starts to drop as losses such as eddy-current and ferromagnetic resonance losses start dominating. By engineering the shape of magnetic particles, the high-frequency losses can be reduced [9, 10]. The ferromagnetic resonance frequency (f_{FMR}) occurs when the frequency of the external applied field matches the frequency of magnetic spins inside particles. At this frequency, magnetic spins begin to resonate, causing imaginary permeability to rise while the permeability begins to droop. For applications where high DC-bias is constantly applied to the inductors, the high Ms prevents saturation of magnetic cores. The composites can easily be scaled to thick layers for high-current handling. Typical particle materials that are used in such cores are Molypermalloy powder cores, High Flux, kool Mu®/Sendust, Iron or NiFe flakes, and XFlux®. By utilizing coupled inductor designs and modified solenoid topologies, higher performance is continually achieved.

Sputtered film inductors are most suitable for on-chip integration. By using the standard CMOS-compatible manufacturing processes, magnetic inductors with small profiles can be integrated with ICs using back-end compatible process options. Ferric, Inc demonstrated magnetic thin-film inductors that are integrated into the ICs, as shown in Figure 24. The inductors allow a shorter path for the power to be delivered to the ICs, resulting in a lower I^2R loss. The magnetic materials in the inductors are made of amorphous cobalt alloy with low coercivity (< 1 Oe) and high saturation field (~25 Oe). The magnetic films are separated by thin insulation layers, in order to suppress eddy current loss. The multilayered magnetic films show high permeability of 600 up to 100 MHz. Inductors with the films as magnetic cores show stable inductance until 100 MHz.

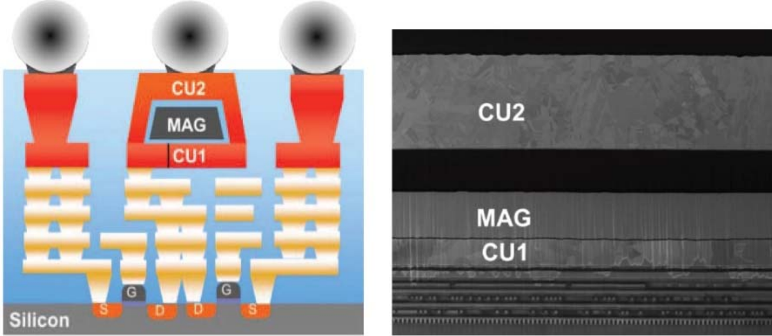


Figure II-24: Left: Illustration of magnetic thin-film inductors integrated with ICs; Right: SEM cross-section of magnetic thin-film inductors integrated with ICs. (Ferric Inc)

Inductor Topologies

Based on how the magnetic cores are integrated with copper windings, magnetic-core inductors are categorized into two types. One is the Magnetic-Copper-Magnetic (MCM) inductor where copper windings are sandwiched between two magnetic layers. Strip-line and spiral inductors come in this category. The other type is Copper-Magnetic-Copper (CMC) inductors where the magnetic cores are enclosed within the copper windings. Toroids and solenoid inductors come in this category. Solenoid inductors can generate uniaxial magnetic field inside the winding loops and prevent unwanted electromagnetic (EM) interaction with other components. The solenoid inductors show high current handling when the uniaxial magnetic field travels along the hard axis. This requires magnetic cores to have uniaxial anisotropy. This can be achieved easily by applying uniaxial external magnetic field during the deposition of magnetic cores. Various inductor component performance metrics and footprint are shown in Table 12.

For higher voltage conversion from 12 V to 1V that delivers 30-100 A with GaN Point-of-Load power converters, a larger case size of 60-1000 mm^3 is used. DC resistances are 0.13 to 0.25 milliohms to maintain high current needs within a 10-20% drop. The Irms is determined so that the temperature rise is within 20-40°C. These typical values for a part number are compiled in Table 13.

Planar Transformers with Isolated DC-DC Converters: Isolated DC-DC converters are an essential building block in many of the distributed power systems such as computers and servers in telecommunication systems, adapters for laptops and chargers for consumer electronics, power conversion architecture in renewable energy, and battery management systems for electric vehicles. Compact and highly-efficient power conversion has been the singular focus in the evolution of isolated DC-DC converters. There are two main approaches in achieving the miniaturization of isolated DC-DC converters: one is increasing the switching frequency of the device, and the other is employing novel transformer technology such as planar magnetics. In the DC-DC stage of power conversion, an increase to switching frequency means a reduction in volume of passive components such as inductors, transformers, and capacitors, which leads to higher power density and lower cost for the converter. However, the increase in operating frequency is generally limited by losses and permissible temperature rise of switching components, which has long been the technological bottleneck of Si-based switching devices . Recent advances in GaN-on-Si switching devices opened up various paths for innovation in isolated DC-DC converters. The other critical aspect of an isolated DC-DC converter, such as the resonant converter, is the transformer. Apart from the switching-related losses of the devices, magnetic components in isolated DC-DC converters themselves are various sources of losses such as core loss, winding loss, and additional ac losses due to high-frequency effects, which account for a significant portion of the total converter loss. Moreover, the transformer and inductor are generally the biggest components in isolated DC-DC converters which take up a large footprint area of the converter PCB substrate. Thus, the transformer or inductor has been the critical hindrance to high-efficiency and miniaturization of isolated DC-DC converters.

Table II-12: Inductor performance metrics and footprints for low-value inductors.

Current handling Thickness	0.6A	<=2A	2.6-2.7A	<=4A	<=5A	<=7A
<=0.4mm	1.5 mH/1.28 mm^2 (Murata) 350 mΩ LQM18PN_B0					
<=0.5 mm		0.15 mH/3.8 mm^2 (Coilcraft) XFL2005-151ME 85 – 98 mΩ 1.6-1.8 A				
<=0.6 mm	1mH/4 mm^2 150-170 mΩ 0.7 – 1 A (Coilcraft) **XFL2006-102ME_**		0.47 mH/2.4 mm^2 (Murata) DFE201210U 3-4 A, 42 mΩ			
0.7 mm			240 nH/1.28 mm^2 (Taiyo Yuden) 75-100 mΩ 0.65 mm MCFE1608TR24MG	0.47mH/5 mm^2 (Murata) 3A, 53 mΩ DFE252007F-R47M#		
0.8 mm		DFE252008C 0.47µH/5 mm^2 2.5 A 60 mΩ (Murata)	0.47µH/1.28 mm^2 (TDK) 54-60 mΩ TFM160808ALC 1000 nH/1.28 mm^2 128-160 mΩ (TDK) TFM160808ALC-1R0MTAA		0.24 µH/5 mm^2 (Murata)	
1			240 nH, 30 mΩ 1.28 mm2 3.0 A DFE18SAN_G0	37 milliohms 2.4 A, 0.42µH/4mm^2 (Coilcraft) EPL2014	0.47 µH/5mm^2 27 milliohms DFE252010F (Murata)	0.24 µH/5 mm^2 16 mΩ (Murata) DFE252010F-R22M#

Table II-13: Typical performance metrics and footprints for moderate-value inductors from Coilcraft.

Case Size	Inductance (nH) *(Tolerance: ±20%)*	DCR ± 17% (mΩ)	SRF typ (MHz)	Isat (A)			Irms (A)	
				10% drop	20% drop	30% drop	20°C rise	40°C rise
SLC7649S-360KL_ 7.3 x 4.6 x 2.6 mm	36	0.17	1150	100			56	74
LC1175-700ME 10.8 x 7.5 x 7.2	70	0.24	179	83.0	100	100	58.0	76.0
SLC1480-111ML 13.46 x 12.95 x 8 mm	110	0.18	130	110	128	130	64.0	83.0

Traditionally, transformers and inductors in isolated DC-DC converters were discretely implemented with conventional cores for each component. This requires additional accessories for wire windings as shown in Table 14. Conventional wire-wound components are still widely used in industry products due to their well-established and straightforward design process, but they suffer from bulky size, low repeatability, and high-profile. In order to increase the power density and reduce the parts count, various integrated magnetics designs were proposed, which combined the inductor component into the transformer core by using additional windings, or by utilizing the leakage inductance (Table 14 (b)-(c)). However, these wire-wound designs are far from mass production processes which generally increase the fabrication cost and suffer from low-repeatability. More recently, planar magnetic components are widely accepted in products in the 0.1kW to 5kW range due to their advantages of low-profile, high power density, good thermal characteristics, and ease of manufacturability. Planar designs are implemented with either discrete or integrated components, which in the latter case require extra effort in the sophisticated design and fabrication of the transformer.

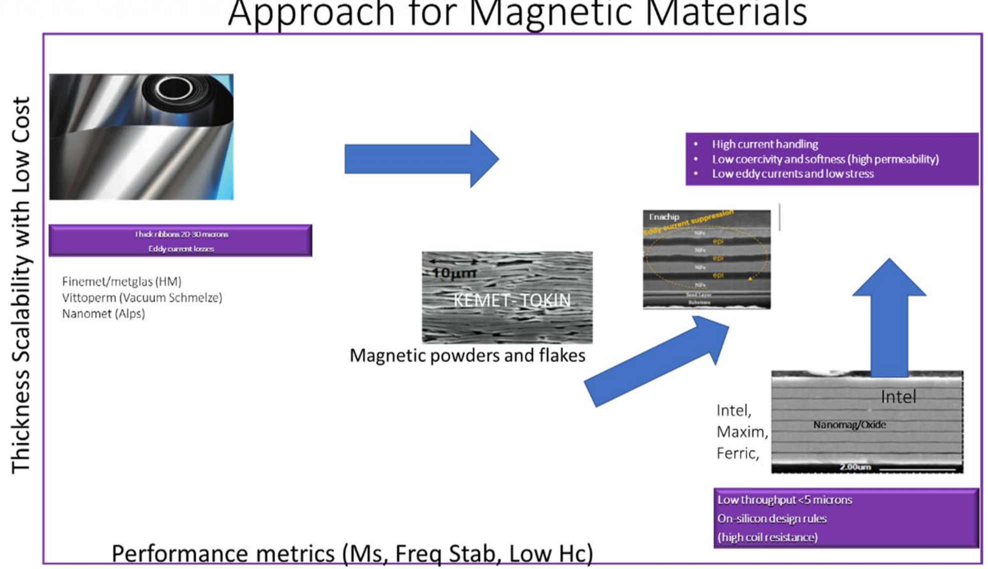
Table II-14: Trend to planar transformers in isolated DC-DC converters.

Method	**Wire-wound integrated**	**Wire-wound planar core**	**PCB winding planar core**
Structure			
Power	1kW	3.3 kW	5 kW
Profile	> 19-34 mm	16 mm	20 mm
Leakage inductor	Integrated	Integrated	Integrated
Process	Manual (Litz wire)	Manual (Litz wire)	Thick Cu PCB
Repeatability	Low	Low	High
Ref.	[11]	[12]	[13]

Substrate-embedded transformers are also advancing in isolated miniaturized low-power (ex. 500-mW) power supplies. One such example is TI's 5 kV RMS isolated DC/DC converter (UCC12050) with ~0.27 cc, and 60% efficiency, along with low capacitance between the primary and secondary windings that results in low EMI. The high isolation protects the IC against severe voltage spikes.

II.5 ROADMAP

The primary focus is to enhance the inductance density and current handling with lower losses. These metrics can be written in terms of L/R ratio, A/mm^2 and losses given in mW/cc or Quality factor or power efficiency. The required metrics are compared with the state-of-the-art in Table 10. The key enabler for this is advances in magnetic structures and processes that can enhance permeability at high frequencies, while retaining high Ms and low core losses with low hysteresis. While such materials are well-known, the key is to process them in the required geometries in a scalable and low-cost process.



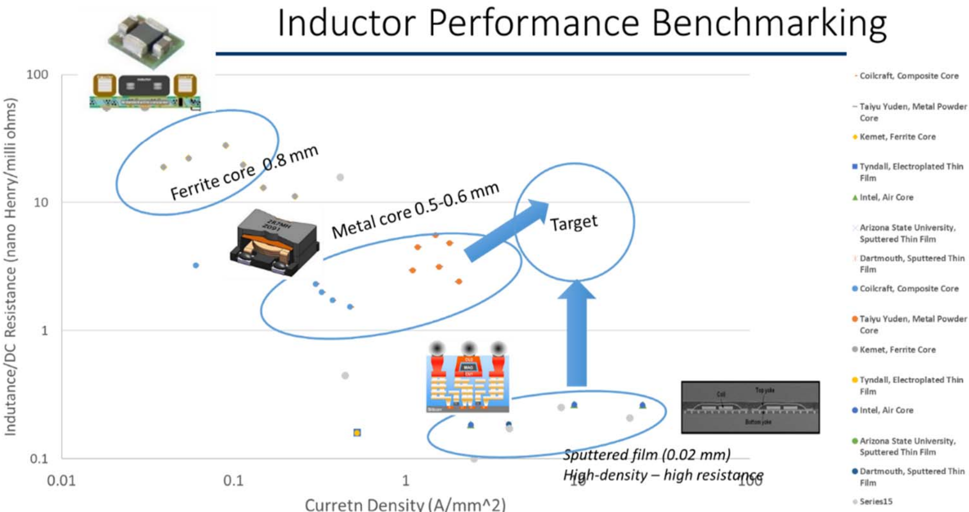


Figure 25: Inductor metrics with key technologies and trends.

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Section III: Integrated High-Power Systems

III.1 INTRODUCTION

Section III focuses on power electronics packaging technologies for systems of 100V to >1500V, and 1kW to 100kW. Example applications include traction drives in transport systems, photovoltaic and wind-energy converters in renewable energy systems, power supplies in consumer products, data centers, etc., and broader power electronic systems supporting areas such as aerospace. A strong focus is on systems interfacing with board mount power (Section II). The packaging technologies can follow traditional levels of packaging as may define power semiconductor modules, intelligent power modules that integrate gate driver and protection circuits, and power converter modules that further integrate passive component functions to define complete standalone converters and inverters. The traditional Levels of Packaging (1 through 3) are also defined in the power electronics industry as "component-" "board-" and "box-level" packaging. "Packaging" is understood to be a "design process" that follows "manufacturing design rules" that incorporate the engineering science areas of chemical, electrical, mechanical, and thermal engineering. "Power Electronics Packaging" crosscuts all application areas that need processed electrical energy to support information processing systems. Section III identifies technologies and provides metrics and trends that will foster new design rules over the next five, ten and fifteen years, and suggest a pathway for research and development for Integrated High Power Systems. Section III does not address discrete power semiconductor packaging nor high-power-semiconductor multichip modules.

Intelligent Power Modules (IPMs)

The IPM is an early attempt to integrate more functionality into simpler power semiconductor modules. Functionality, such as gate drivers, gate isolators, desat, avalanche and short-circuit protection circuits, thermal sensors, and some level of control are integrated into these modules. Circuit partitioning and product modularization based on performance and manufacturing cost determine the integration approach. The IPMs are most closely associated with these applications as mentioned by manufacturers:

- Home appliances: fans, air purifiers, washing machines, air conditioners, refrigerators, vacuum cleaners.
- Industrial: pumps, compressors, HVAC, elevators.
- Automotive: AC compressors, oil pumps, on-board charging in electric vehicles.

III.2 CHALLENGES IN CIRCUIT ARCHITECTURES

High Power Conversion Topology and Architecture Issues:

- High current converters, either AC-DC or DC-DC, are multi-phase, and phases must be reasonably balanced. Factors affecting balance:
  - Component matching
  - Power Interconnect matching
  - Thermal gradients between phases
  - Design techniques to mitigate phase balancing often impact efficiency
- Power interconnect (low-voltage loads, switching nets)
  - Short traces to loads or power connectors
  - Thick metal interconnect – 5 to 20 oz (0.175mm to 0.7mm) copper availability
  - Area reduction for metal interconnect of switching nodes to improve radiated emissions
- Thermal management
  - Integrating liquid cooling into the substrates and module housings
  - ACS Immersion
  - ACS Cold plates
- Power density and spatial constraints

Example: Open Compute Project Rack and Power PSU definition for each 3kW AC-DC PSU that plugs in parallel within the V3 Power shelf (density is about 2kW/L). See Figure 1.

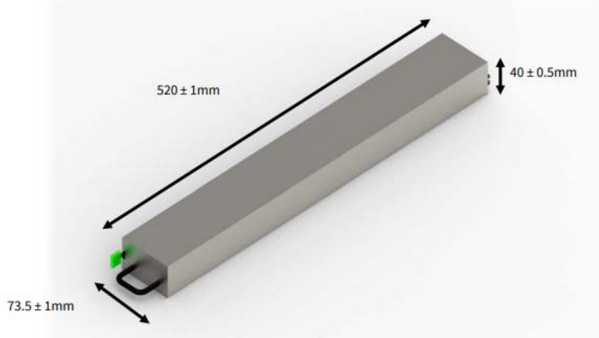


Figure III-1: Image from Open Compute Rack and Power Report.

The 100 kW Server Racks will require 2X 50 kW V3 Power shelves with a 6 kW PSU in each slot. Power density will increase another 60% in next-generation systems. Proposed footprint is 94mm X 40mm X 506mm (density increase to 3.2 kW/L).

Table III-I – Circuit Architectures Metrics

	2010	2015	2020	2025
Input Voltage	110-220VAC	220-270 VAC	220 - 480VAC	480VAC or 1000 VDC
Rack Power	10 kW	24 kW	67 kW	>100 kW
Efficiency	94%	96%	97.00%	97.50%
Rack Current	45A	90A	120A	200A

III.3 CHALLENGES and EXISTING SOLUTIONS

1. Size Reduction with WBG Power Semiconductors

The ultimate unachievable goal for power conversion is to produce a converter with zero volume having zero loss at no cost. All advances move toward this singularity. For smaller sizes and higher densities, components need to be made smaller and moved closer together. To achieve lower losses, conductive losses in components need to be continually reduced, and any stored energies, for example in junction capacitances and interconnect inductances, need to be routed to supply the load. To achieve reduced costs, the parts count must be reduced, the fabrication must be simplified and the level of integration of passive and active devices must be increased. The most practical approach is to address what is the highest contributor to volume, loss, and cost, which is the switching power semiconductors.

The improvement in power efficiency that comes from using wide bandgap (WBG) semiconductors is now well understood and accepted. Power losses are a combination of the following three factors: on-state loss, off-state loss, and switching loss. Increasing levels of doping decrease the on-state resistance but also lower the breakdown strength. The higher intrinsic breakdown strength of wide bandgap devices means they can be doped more heavily while still maintaining the needed breakdown strength. This results in lower on-state resistance and correspondingly lower on-state Joule heating losses. The wider bandgap of SiC and GaN reduces intrinsic carrier concentration, thus lowering the reverse leakage current and reducing already low Joule heating losses in the off-state. The higher saturation electron drift velocity of the SiC and GaN lead to faster switching speeds, with lower capacitance and thus lower switching losses. These increases in efficiency reduce the power losses, so less heat needs to be removed and integrated cooling systems can be smaller. Required cooling system size is also reduced by the ability of these WBG devices to operate at higher temperatures. Typically, SiC devices are chosen today for higher power applications, due to their higher breakdown strength and thermal conductivity. The Al(Ga)N/GaN devices are preferred for high frequency applications, although developments are occurring to increase the power levels of GaN devices and increase the frequency of SiC devices.

In addition to improved efficiency, Al(Ga)N HEMT (High Electron Mobility Transistor) devices can operate at higher frequencies. Higher-frequency operation permits the use of smaller passive components, thereby reducing overall converter size. The Al(Ga)N HEMT devices are also typically grown in thin epi-layers and thus can be used with thinned wafers, reducing packaging thickness and increasing the ability to embed GaN in substrates and printed circuit boards. The lack of and high cost of bulk GaN material has limited the development of vertically conducting GaN devices. If the use of GaN is limited to planar (HEMT) devices, the current through each device is limited. Research is currently being conducted toward developing vertical devices in epi-GaN [1,2] on heterogeneous

substrates to address this issue, and it is expected that these devices will become available in the next 2-5 years. Research is being conducted to develop GaN HEMTs at higher voltages, with 1200 V devices expected to be available in the next 2 years [3]. Alternatively, planar GaN can lead to high levels of functional integration, adding on drivers, sensors and making monolithic serial (totem pole, half bridge) structures. Two n-channel devices in series form the unit switching cell for a synchronous buck converter.

As SiC and GaN reach increasing levels of commercial penetration, research is now focusing on devices made from semiconductors with even larger bandgaps, such as diamond and GaO [4,5]. These ultra-wide bandgap devices promise even greater efficiencies and switching frequencies than GaN and SiC. However, they are more difficult to dope, which makes creating junctions and contacts for devices more difficult. It is anticipated that many of these new devices will be released in the next 3-10 years. More details are available in the International Technology Roadmap for Wide Bandgap Power Semiconductors (ITRW) [6].

Table III-2 – Expected Developments in GaN and SiC.

	2 years	5 years	10 years	15 years
1200 V GaN HEMT devices	X			
Vertical GaN power devices	X	X		
Gallium Oxide Based Power Devices		X	X	
Diamond Based Power Devices			X	X

2. Novel Device Interconnection Approaches

Miniaturized and stacked packages handling ever larger amounts of power have higher power densities, and the heat generated in the package must be discharged through a smaller backside surface area. Furthermore, limited access to the devices within a substrate renders traditional convection-cooled heat sinks mounted on the back of the package ineffective. Therefore, new approaches and materials are needed for packaging and interconnect. In particular, the smaller packages have led to a drive for replacing wirebonds with flip-chip and other direct-bonding approaches that allow double-sided cooling. Finding reliable attach materials, however, has proven to be a challenge, as new soldering and sintering methods have been developed and studied, but their long-term reliability is still uncertain.

Another interconnection development driven by the package size reduction has been the development of multifunctional electrical and thermal conduits such as through-substrate vias and through-silicon vias that are designed to extract heat from the central regions of the package while establishing electrical connections between layers of the package. The following section will discuss recent developments in package approaches, interconnections, and thermal management for embedded power electronics and will complement similar efforts by PSMA in their Power Technology Roadmap [7].

Multiple advances in packaging methods have characterized the progress of power electronics integration in the past decade. A few major packaging developments include: (i) planar interconnects; (ii) flip-chip bonding; and (iii) chip embedding [8]. Planar technology has been used in the industry and has resulted in developments in stacking and interconnection. Exploration of flip-chip technology has yielded methods of converting standard dies to a format compatible with their technology, useful in an industry that still favors aluminum wirebonds [8]. Chip embedding has developed a variety of methods of embedding active, passive, and formed components into organic and inorganic substrates.

2.1. Planar Interconnects

Planar interconnects were created by both Siemens and Mitsubishi [8,9] for use in their vehicles' power modules in the early 2010s. Their one-layer approach to the planar interconnect scheme saw reductions of up to 50% in parasitic inductance [9,10]. Since these single-layer modules were introduced, the technology has matured significantly with the introduction of copper clip bonding and the incorporation of multiple layers. Copper clip bonding was developed to replace aluminum wirebonds due to better electrical and thermal conductivity. The electrical connections that double as heat conduction paths make copper clips an efficient way to reduce the size of the package, as shown in Figure 2 [11].

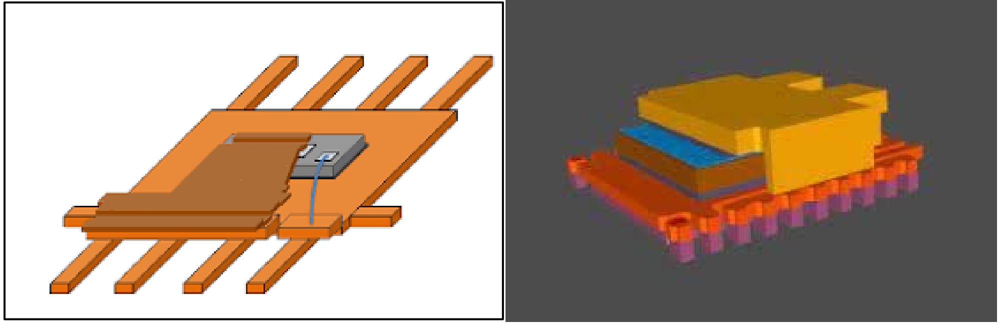


Figure III-2: Two power packages with Cu clip leadframes, leaded (left) and leadless (right) [11].

The multilayered approach has also made progress. For instance, one module laid the chips in a parallel arrangement between sheets of copper [12]. This approach to planar connections between the power electronics and the gate drivers consistently achieved improved thermal and electrical performance [12]. The multilayered approach consists of a cooler-substrate-die-substrate-cooler arrangement that allows for efficient cooling of both sides of the package, but leaves little room for variations in the heights of the die [13-15]. Height variations in the die cause some chips to be distant from the single DBC or PCB plate that forms the top of the package, which can affect the quality of their electrical and mechanical connections. Recent structures allow for planar connections of components of varying heights by employing copper spacers. The copper spacers are used to augment heights of the smaller chips and establish strong electrical and mechanical contact [16]. Reductions in parasitic inductance and the ability to incorporate a variety of components in planar packages has enabled the integration of power components, improvements in performance compared to traditional packages, and reduced package dimensions.

2.2. Flip-chip Interconnection

Flip-chip packaging techniques have also been pursued by academia [13]. The flip-chip approach seeks to eliminate aluminum wirebonds from the package by replacing them with solder bumps that have been deposited onto the chip pads. The die then becomes a surface-mount component where the solder ball array acts as a mechanical and electrical connection [17]. However, most commercially available SiC power devices, as well as most Si power devices, are not designed for such applications, instead favoring electrical connections via aluminum wirebonds. A number of companies have modified power devices designed for wirebonds using Chip Scale Packaging (CSP) and Fan Out Wafer Level Packaging (FO-WLP) technologies to form power devices that can be attached by flip chip solder bumps or BGA solder balls. Both IR and Fairchild use solder bumps to attach MOSFETs, eliminating wirebonds. Figure 3(a) shows IR's FlipFET structure that is a CSP with flip chip solder bumps and Figure 3(b) shows Fairchild's BGA MOSFET which is a FO-WLP slightly larger than the chip that brings the backside drain contact to the package topside surface [18]. Researchers have embedded multiple commercially available SiC power devices that were designed for wirebond connections into the package, including SiC Schottky diodes [19], and achieved up to 24% reductions in on-state resistance. Others have achieved as much as a 50% reduction in parasitic inductances [20], again without altering the die's functional properties. These results have demonstrated that the performance of SiC chips can be dramatically improved simply by adjusting the approach to packaging the components. More information on flip-chip packaging of power devices can be found in Chapter 8 on Single- and Multi-chip Packaging. Refer to Chapter 22 for a detailed discussion on interconnect covering 2D & 3D architecture and the interconnect pitch roadmap.

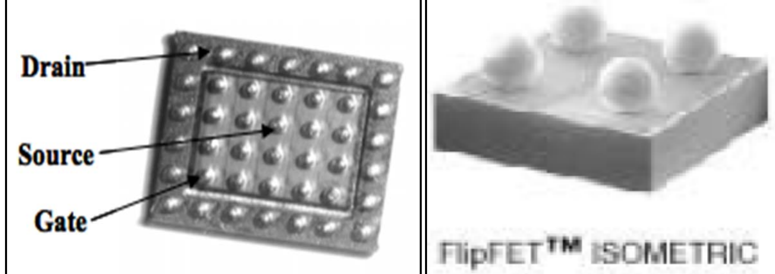


Figure III-3: Flip Chip Power Devices, a) IR's FlipFET CSP with flip chip solder bumps and b) Fairchild's BGA MOSFET FO-WLP [18].

2.3. Chip Embedding

Finally, chip embedding-based packages have made extensive progress [8,21]. Researchers have embedded active, passive, and formed components in layers of organic and inorganic substrates. One chip-embedding process uses sintered silver to attach IGBTs and diodes to a base substrate that has been metalized with copper. Afterward, the chips are embedded by lamination into a prepreg layer and vias are laser-drilled to the chip pads. The vias are then filled with copper and etched [22]. This process is representative of many chip-embedding techniques, which have flexibility in the order, layout, and species of chip that is embedded. IGBTs, diodes, MOSFETs, and myriad other components have been embedded face-up and face-down to achieve a more efficient module than was possible with traditional surface mount packaging methods [8].

Power chip embedding was pioneered by GE with their Power Overlay technology (POL) and Infineon with its MOSFET chip embedding technology used in its DrBlade power modules. The POL process bonded power FETs and diodes under a thick (25 – 50 µm) laminate film with vias preformed in the laminate. Thick plated-up Cu (50-100 µm) formed the topside pattern metal and filled the vias, contacting the power devices pads. The embedded structure was solder-attached to a backside Direct Bond Copper (DBC) metal-insulator-metal substrate. Figure 4 shows one of four POL IGBT modules and one of four POL diode modules that are used to form the 1200A, 600V, liquid cooled full bridge with six embedded IGBTs per module and six diodes per module [23]. The Infineon technology solder-attaches the power chips onto a thick copper leadframe. It then laminates a thick dielectric film over the chips and embeds them. An array of large vias is formed to the MOSFET power pad, one via is formed to the gate pad and large deep through-vias are formed to the backside leadframe. Thick Cu is plated in the vias and on the top surface and patterned to form the module circuit. Figure 5 shows a cross-section of an Infineon 48V embedded chip half bridge with two MOSFETs shown embedded [24].

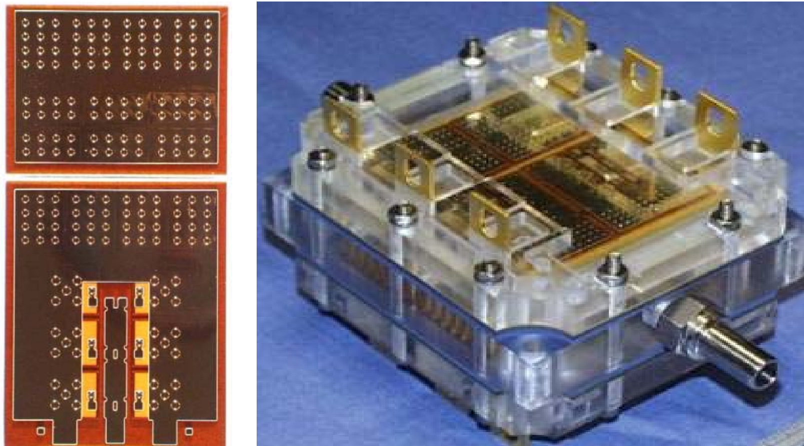


Figure III-4: GE Power Overlay power modules; top-left six-diode module, lower-left six-IGBT module and right 1200A, 600V full bridge with four diode modules and four IGBT modules [23].

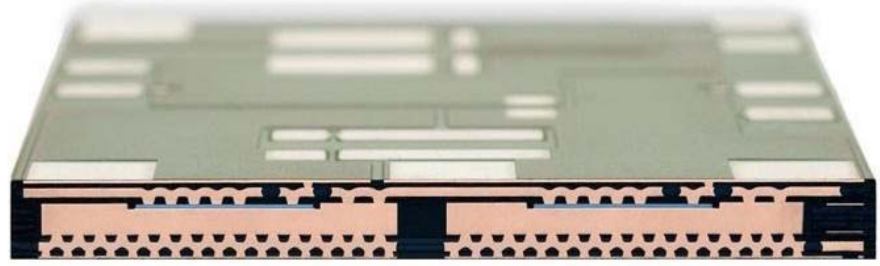


Figure III-5: Cross-section of an Infineon embedded MOSFET half bridge power module [24].

Other embedded-chip power module technologies include the TI MicroSiP^{TM} (Figure 6 [25]), AT&S ECP process, Schweizer Electronics p2 Pack (Figure 7 [26]) and Sarda Technologies PCB-embedded power technology (Figure 8 [26]). All of these embedded-chip power technologies eliminate wire bonds, replacing them with either direct metallurgical contacts, solder or brazing. Eliminating wire bonds improves electrical performance by reducing interconnect parasitic inductance and resistance by more than an order of magnitude. In addition, all of these

embedded power packaging approaches have smaller footprints and low profiles and lend themselves to double sided cooling discussed in more detail in section 6 below.

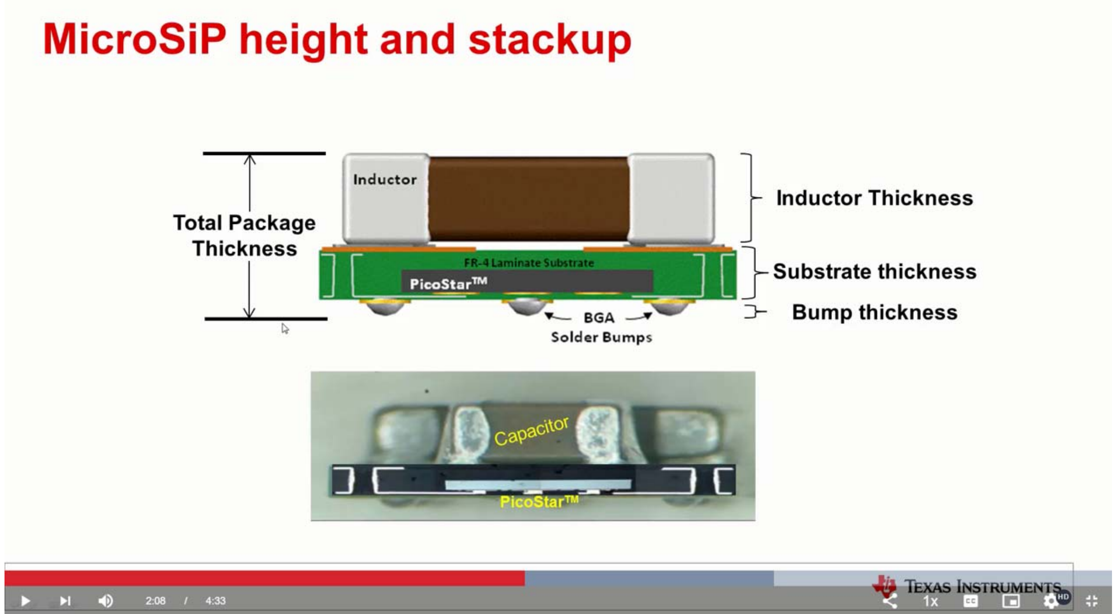


Figure III-6: TI MicroSiP embedded power chip packaging [25].

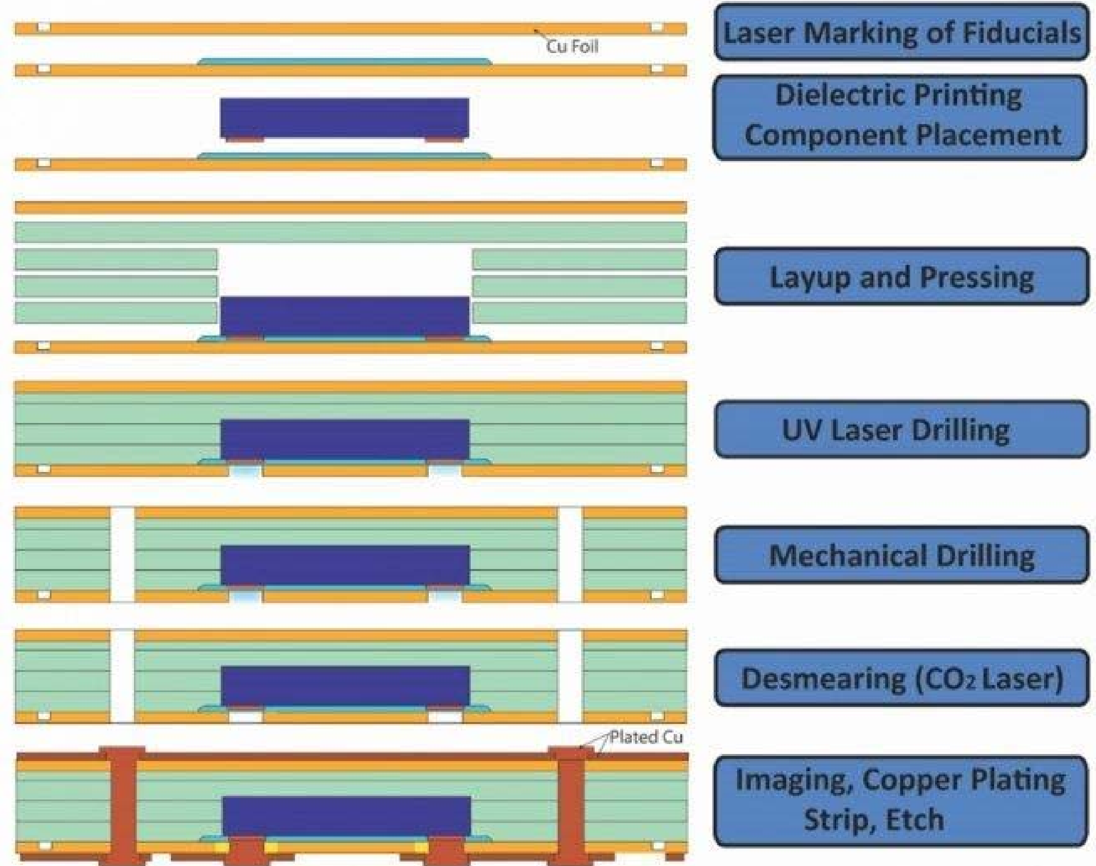


Figure III-7: AT&S Embedded Component Packaging (ECP™) process flow [26].

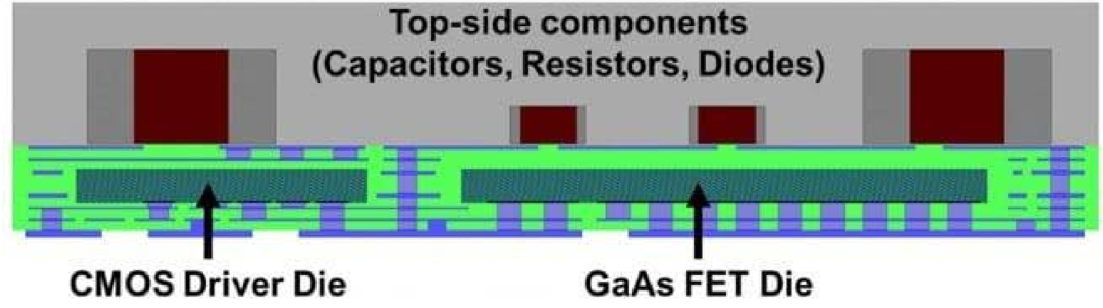


Figure III-8: PCB-embedded two-phase power stage with GaAs FET quad [26].

The replacement of wirebonds with interconnects such as TSVs, metal and flip chip solder bumps, and large-area solder and die attaches, is a prerequisite for reducing the size of the package. Standard solders, including the lead-free SnAg solder, are incapable of withstanding the thermomechanical stresses induced by the novel packages [27]. Furthermore, traditional wire bonds are bulky and inefficient. As a result, new die-attach methods and materials have been developed as replacements. The methods include high-temperature soldering, transient liquid-phase bonding, and sintered silver or copper [28].

3. Attachment Approaches and Materials

3.1 Metal-based Sintering

Metal-based sintering has been developed for large-area joints because of its ability to withstand the high temperatures and temperature cycling of power modules. Developing a high-quality connection between the sinter paste and substrate relies heavily on the treatment of the substrate. One report found that silver sintering on an Au-finished Si_3N_4 substrate gave adhesive strengths of up to 70MPa when applied with a 6MPa pressure [29]. It has also been demonstrated that silver sintering on an unmetalized but polished DBC substrate at 6MPa yields good adhesive strengths [30]. Furthermore, under thermal cycling, the degradation of these silver-based die attaches has been found to be minimal [31]. Research has also demonstrated that the incorporation of varying levels of molybdenum and silver-coated nickel particles allows for control of mechanical properties such as coefficient of thermal expansion and Young’s modulus [32]. After proving the viability of pressure sintering for die attach, one study demonstrated connections with shear strengths in excess of 15 MPa without elevated pressure application techniques [33] to enable less-strict manufacturing practices. While these results demonstrate that the pressureless silver sintering process has some viability, other authors have argued that the reduction in strength is due to a lower-quality interface that limits thermal conductivity of the materials [34], making it the less viable option. More research will need to be conducted on this topic to establish the best fabrication processes, but these preliminary results have demonstrated the potential of the materials to reliably replace the traditional aluminum wirebond. Research has moved away from silver sintering to copper sintering owing to the issues of silver migration under high voltage and temperature, along with the high cost of silver paste, especially nanoparticle paste. Low-temperature sintering of copper can provide similar levels of electrical and thermal conductivity at much lower cost. However, it requires sophisticated bonding equipment that allows processing in a reducing atmosphere and has a narrower process window than silver sintering. These aspects require additional work for scale-up and widespread adoption of the technology.

3.2. Transient Liquid Phase Sintering

Other promising die attach techniques have also been developed – first, through diffusion-soldering of copper-tin intermetallics. The intermetallic joints created by these techniques have exhibited melting temperatures of 676°C and 415°C (Cu_6Sn_5) with remelting temperatures well in excess of 400°C [27]. Their strength and thermal stability have made them candidates for the future of die attach along with silver-based sintering methods described above. Additionally, metal bumps have allowed further elimination of wire bonds in 3D packaging. A substrate-chip-bump-chip-substrate approach investigated in one paper demonstrated the effects of different bump cross-sections and material compositions on the thermomechanical reliability of the package. The authors used copper-molybdenum solders in a variety of shapes to directly attach the chips to one another. Their method proved to be electrically successful but had limited mechanical reliability under electrical cycling [35]. While the technique has been successful in the lab, there are issues for large-scale processing owing to the long curing times, up to 30 minutes, and narrow process window. Furthermore, the high stiffness of the materials can lead to die cracking. The batch-to-batch uniformity is also poor owing to the difference in the particle loading and size between batches, leading to yield

issues. Additional work is needed in process development and inspection (e.g. backscattering) to address these scale-up issues.

In summary, heterogeneously integrating the power electronics into the overall system requires the ability to embed the interconnections and stack devices. As such, wirebonds must be eliminated and replaced with through-silicon vias, through-substrate vias, metal bumps, flip chip solder bumps, large-area solder and die attaches, and direct copper interconnect patterning. Each of these technologies has seen extensive development over the last ten years, and continues to be further refined. Flip chip solder and metal bumps must be able to handle the levels of power they are asked to carry without suffering electromigration. Direct-copper interconnect patterning needs to have sufficient adhesion to the devices and sufficient thickness to handle high currents without enduring stress levels that cause fracture. Lead-free solders along with copper and silver sinter pastes are being developed for large-area solder connections to minimize thermomechanical stresses.

Another way to reduce size and promote heterogeneous integration is through combining separate functions into multifunctional components. Through-silicon and through-substrate vias must serve not only as electrical connections but also as thermal conduits. Embedded thermal management systems consisting of fluid-filled conductors can serve not only as coolers but also as power busses. Developments are underway in these areas but they need to be further enhanced.

4. Thermal Management

Embedded thermal management systems will require not only the development of complex integrated microfluidics but also simpler solutions. For example, higher thermal conductivity encapsulants as well as anisotropic conductive materials embedded near the heat dissipating devices can remove heat to the sides of the heterogeneously integrated system where it is easier to remove by external cooling elements. Furthermore, heterogeneous integration requires techniques to cool the power electronic devices without allowing heat from those high-loss devices to migrate horizontally or vertically to warm more temperature-sensitive electronics. Examples of the solutions being developed to address this problem are thermal metamaterials and thermal isolation materials. These materials combine a low thermal conductivity backbone, which minimizes undesirable heat spreading, with high thermal conductivity elements (e.g. traces or vias) that allow the heat to be safely moved along paths past the thermally sensitive components to the cooling units.

4.1 Thermal Metamaterials

Metamaterials are engineered materials that provide material properties that are not available in nature. Thermal metamaterials are assembled materials in sheet or stack form providing unique combinations of density and porosity and thermal conductivity. In the application of metamaterials to power packaging thermal requirements, the goal is to reduce hotspots with thermal spreading and to provide increased cooling of high-dissipation devices. For example, PARC has developed a metamaterial for a coating on cooling fins that is transparent to infrared, so radiant heat passes through it unobstructed while it reflects UV radiation providing 13°C lower radiating surfaces.

4.2. Thermal Isolation

In addition to the arrangement of high and low thermally conductive materials for the thermal path design, the "thermal distance" concept is proposed to measure the thermal coupling effect. The thermal distance is defined as the physical distance of the thermal coupling path between heat sources. To reduce the thermal coupling, the most common way for conventional wire-bonded power modules is to directly increase the distance between dies to preventing heating up by adjacent dies. However, this not only increases the form factor but also the electrical parasitics (e.g. resistance and inductance). For double-sided cooled power modules, the thermal distance can be increased by an interleave packaging structure while maintaining high power density and small form factor, as shown in Figure 9 [36]. The interleave structure is achieved by having dies soldered down on individual Cu bonding pads and adjacent devices soldered on different insulated substrates (top or bottom). On the other hand, powerful cooling components (e.g. heat sink and cold plate) are not merely desired because of enhancement of heat dissipation capability. Higher cooling capability can effectively remove the heat vertically from dies to cooling components with a smaller thermal spreading angle and therefore minimize the thermal coupling effect.

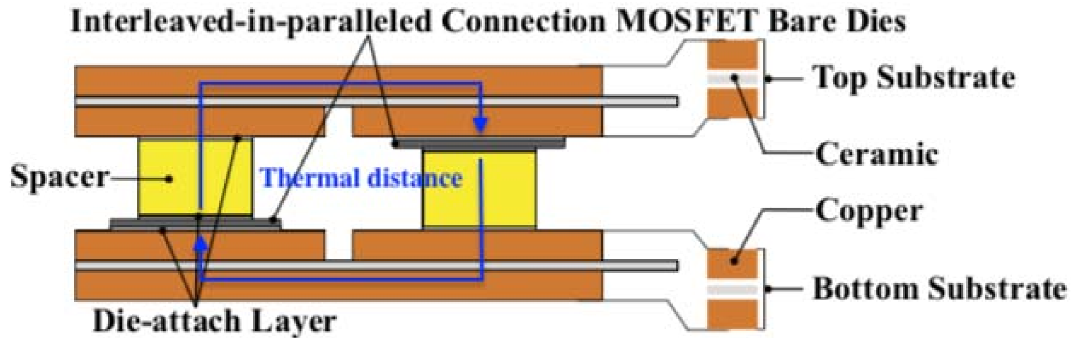
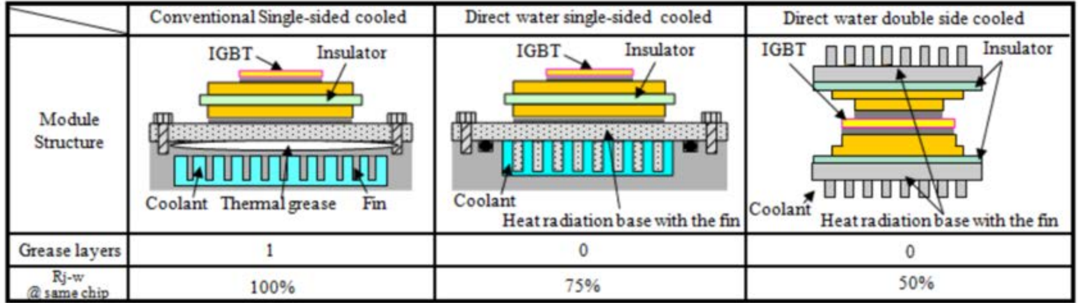


Figure III-9: An interleaved double-sided packaging structure [36].

4.3. Direct and double-sided cooling:

To meet the rapidly rising demand of power density, the double-sided cooled technique was proposed to effectively increase power dissipation capability while maintaining a small form factor. Compared with conventional single-sided cooled power modules, the advanced double-sided cooled power modules are equipped with top and bottom insulated substrates for building a sandwich structure (substrate/power devices/substrate). By mounting the cooling components (e.g. heat sink and cold plate) on the external surfaces of both substrates, the heat can be dissipated from power devices to the top and bottom sides of the module. To further enhance the current and power rating, the number of layers along the thermal path must be minimized. The direct-cooled power modules employ integrated heat sinks and eliminate the TIM layer (e.g. thermal grease). It not only results in better thermal performance by removing the bulk and contact thermal resistance of a TIM, but also avoids the TIM uniformity concern and degradation issue. The coolant can directly contact the integrated heat sink without extra fins in the cold plate, as shown in Figure 10 [37].



	Conventional Single-sided cooled	Direct water single-sided cooled	Direct water double side cooled
Module Structure	IGBT, Insulator, Coolant, Thermal grease, Fin	IGBT, Insulator, Coolant, Heat radiation base with the fin	IGBT, Insulator, Coolant, Heat radiation base with the fin
Grease layers	1	0	0
Rj-w @ same chip	100%	75%	50%

Figure III-10: An interleaved double-sided packaging structure [37].

Planar interconnection and chip embedding of power modules form ideal structures for implementing double-sided cooling. GE's POL embedded power technology (detailed earlier) is attached to a backside metal-insulator-metal substrate that has high thermal conductivity and can be directly attached to a heat sink or liquid-cooled heat exchanger. It also has a planar topside surface with thick patterned copper and multiple solid-post metal vias directly to the chip pads. Adding a thermally conductive, electrically insulating layer over the topside metal allows a second heat sink or heat exchanger to be attached to the topside, reducing junction thermal rise by 40% or more (Figure 11 [38]).

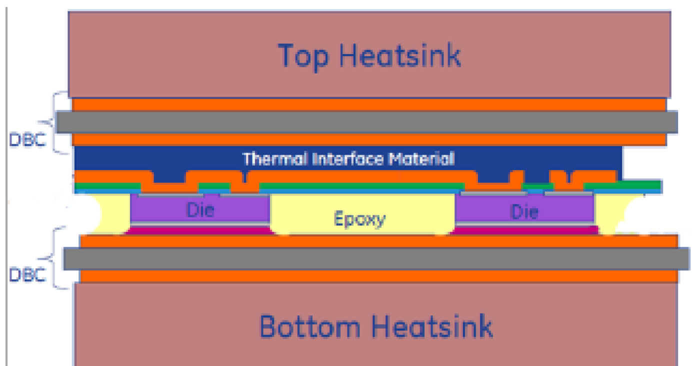


Figure III-11: A cross-section of the GE POL embedded power module with topside and bottom side cooling [38].

4.4. Advanced thermal management:

Advanced thermal management is critical for power electronics targeting the EV/HEV market with its higher voltage requirement (see Chapter 5). A power converter will require an effective thermal conductivity greater than 500 W/m-K at a target price around $1/kW in the next 10 years. The accelerated incorporation of WBG technologies using SiC has allowed power modules to achieve better performance and cost targets. Even so, with the larger heat dissipation in power module packaging, increasing thermal conductivity is now of comparable importance.

Inductor cooling is also of high importance, as inductors are often the highest power-loss element in the converter, exceeding the losses of the switching devices, now that the switches utilize the more efficient wide bandgap materials. Research is addressing this issue in three ways. The first is through the development of materials with higher electrical conductivity than the current electroplated or printed copper and silver windings to minimize Joule heating. The second is through the development of substrates with integrated cooling channels. The third is through the development of hollow conductors through which coolant can flow to internally cool the windings.

Current packaging technology with Cu conductors, wire bonds, and solder attachments is evolving better thermal performance materials (e.g. Ag, graphene or diamond conductors with wire-free interconnects and sintered attachments). These changes cause the thermal performance to increase by a few hundred W/m-K, but there is an attendant cost increase in dealings with the new material and process technologies as well. Table 3 below provides an overview of the package development for the next 5 years and beyond. The key challenge in power modules is evolving towards better thermal performance for improved reliability at compatible cost. Currently, there is an extensive focus on using embedding technology for higher power handling. It helps to improve the thermal performance of the package through direct cooling at top and bottom sides of the die. In addition, embedding allows scalable solutions for a more heterogeneously integrated Power Module. Examples of the components to integrate in a package are the power diode, power FET, driver, passive components and sensors. There have been significant innovation activities to date allowing the embedding of a few components in a power module. Nevertheless, innovation is continuing to enhance integration by introducing more components (e.g. sensor or RF) in the power modules as a system solution. Further embedding is one of the key challenges in the development of future power modules with more functional integration that achieve better thermal conductivity with comparable cost. More discussion on Thermal Management can be found in Chapter 20, while a sampling of needed future material developments is listed in Table 3.

Table III-3: Interconnect and Thermal Management Developments Needed, and Timeframes.

	5 years	10 years
Interconnect	Ribbon bond, Flip-chip	Embedding, Direct Bond, Flexible Foil, Direct Metallization
Die Attach	Cu/Ag Sintering, Brazing	TLPS
Substrate Material (DBC)	Si_3N_4	Elimination of substrate with die on base plate
Thermal Interface Material (TIM)	TIM with higher Thermal conductivity	Elimination of TIM for direct cooling, double side direct cooling (die embedding on base plate)

4.5. High temperature materials:

One of the key advantages in the use of WBG devices in power modules is their ability to operate with high performance at very high temperatures. Table 4 shows the maturity and temperature tolerance of various semiconductor technologies [39]. Whereas Si can operate up to 250°C, its performance and operating life rapidly degrade above 125°C. WBG devices can operate with high performance to much higher junction temperatures. Allowing the junction temperatures of WBG power semiconductors to rise well above 125°C can not only allow them to operate in harsher environments such as an automotive engine compartment or in a hybrid or all-electric vehicle, the materials used in the power module must also be able to withstand the higher temperatures. This is particularly true of the embedded-chip approaches described above which utilize organic materials to encapsulate and to provide the interconnect dielectrics. At temperatures above 150°C, most organic materials used in chip embedding technologies have issues with Tg (excessive CTE), material softening, outgassing and material breakdown. Organic adhesives and encapsulants would be limited to 150°C to 175°C operation, and more stable organic films such as polyimide would be limited to 250°C to 275°C. Higher-temperature compatible organics need to be developed to use chip embedding technologies with WBG power semiconductors at higher operating temperatures. Alternatively, planar power interconnect would need to be done without organic materials (i.e. planar interconnect without embedding) or utilizing a chip embedding process where the organic materials are removed after the module is fabricated by, for example, etching or sublimation. Figure 12 shows a high temperature chip-embedding technology from the Center for Power Electronics Systems (CPES) at Virginia Tech [40]. It is targeting operating temperatures

in the 200°C to 300°C range to support the high-temperature capabilities of SiC power devices. It uses a ceramic window frame structure to form a low CTE, high temperature structure with the SiC power devices mounted into laser-cut openings in the ceramic.

Table III-4: Technical maturity and temperature tolerance of various semiconductor materials [39].

Material	Tech maturity	Temp tolerance (°C)
Silicon (Si)	Very high	125-250
Silicon-on-Insulator (SOI)	Medium	250-300
Gallium Arsenide (GaAs)	High	350
Gallium Nitride (GaN)	Very low	>500
Silicon Carbide (SiC)	Low	>750
Diamond	Very low	>800

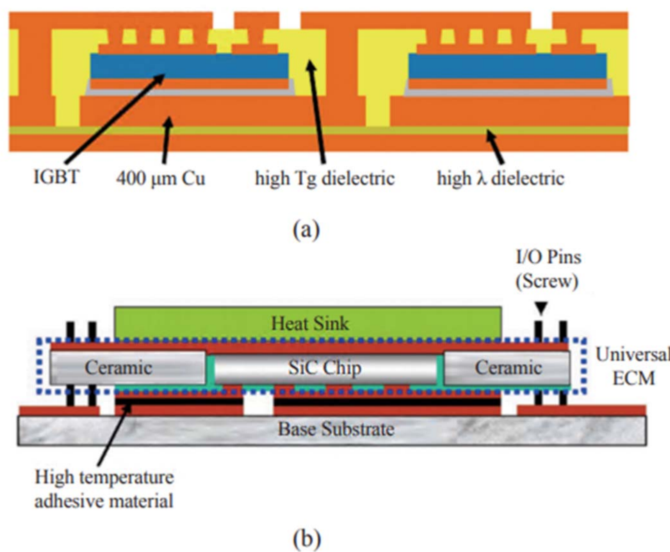


Figure III-12: High temperature SiC power module from Center for Power Electronics Systems (CPES) Virginia Tech, (a) embedded chip structure and (b) assembled embedded chip power module [40].

Substrate

Power module substrates usually contain a top conductive layer for routing and mounting semiconductor devices, another bottom conductive layer for stress management and mechanical ruggedness, and an insulating layer between two conductive layers. Insulated metal substrate (IMS), an organic substrate, consists of a polymer-based layer for insulating top and bottom conductors. IMS has a thin, low-modulus, and low thermally conductive insulating film, and thus a thick metal baseplate is required for mechanical support and thermal spreading. Low thermal conductance leads traditional IMS to low-power applications (e.g. LED). Due to good electrical isolation, high operating temperature, and high effective thermal conductivity, metal-clad plate ceramic substrates, e.g. direct bonded copper (DBC) and direct bonded aluminum (DBA) substrates, are commonly used for high-power modules. However, thermal-mechanical reliability issues were found at bond wire interconnections and the solder layers between ceramic substrates and metal baseplate due to high CTE mismatch [41,42]. To solve the reliability concerns, high thermally conductive epoxy resin-based insulating materials filled with ceramic fillers (e.g. BN, Al_2O_3, and AlN) were proposed for improving the thermal conductance and eliminating the solder layer between substrate and baseplate due to the IMS inherent baseplate [41,43]. It not only reduces the potential failure points but also the thermal interface, resulting in better reliability and thermal performance. The thermal conductance of the 10-W/mK 120μm-thick epoxy-based substrate with 5kVAC breakdown voltage (@ 60Hz) is comparable to 15-mil Al_2O_3 DBC [43]. Moreover, IMS has thickness flexibility on top and bottom conductors for optimizing thermal spreading due to low CTE mismatch between Cu and organic film that DBC doesn't have [43,44]. On the other hand, because of manufacturing and ruggedness considerations, the minimum standard DBC thicknesses of Al_2O_3 and AlN DBC are 0.38 mm and 0.63 mm, respectively. The corresponding breakdown voltages are 5.7 kV and 12.7 kV [45] which are overkill for applications lower than 1.7kV. Mitsubishi developed IMS power modules having 4kV and 2.5kV insulation voltages for 1.7kV and 0.65-1.2 kV applications, respectively [44]. In addition to the IMS structure, the multilayer availability and thickness flexibility of an organic insulating layer enable embedded technology and are advantageous to

heterogeneous integration. Embedded technology can realize perfect magnetic-field canceling by forming a very compact and thin current loop between two conductive layers, leading to an ultra-low parasitic loop inductance [46]. Panel-level manufacturing and packaging process provide organic-based packaging great competitiveness on cost compared with ceramic-based packaging while maintaining necessary design factors for the power module [43].

III.4 POWER MODULES (HIGH VOLTAGE)

Power (semiconductor) modules are important building blocks in power electronics systems. In Section III, we focus on medium voltage to high voltage, 200V, and above. The main applications for medium voltage ranging from 200V to 1500kV including traction motor, EV/HEV, PV system and UPS; and high voltage above 1500kV include transportation including railways, renewable energy sources like wind turbines, and the smart power grid, as shown in Figure 13 [47].

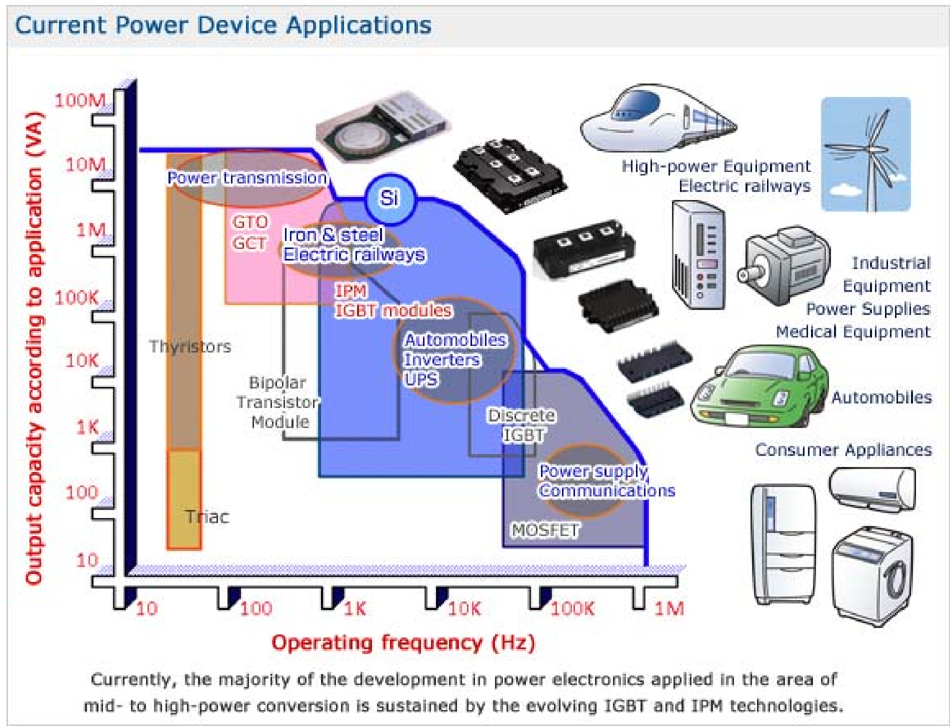


Figure III-13: Source: Mitsubishi Electric Power Device Technologies and Product Trends [47].

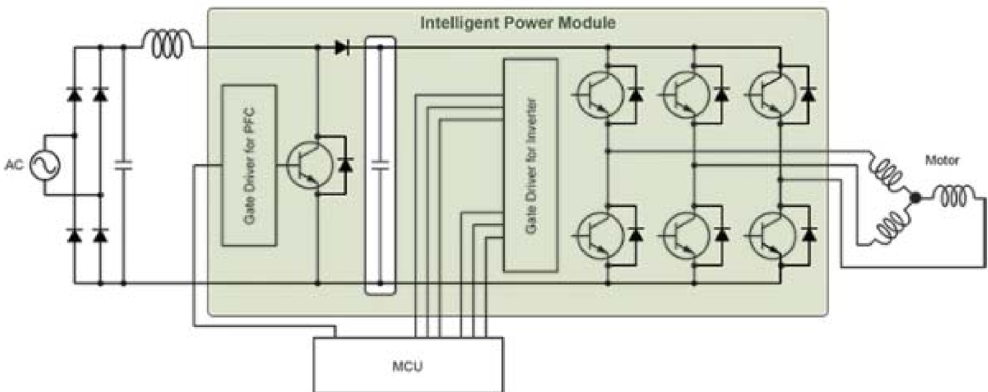


Figure III-14: Intelligent Power Module (IPM) circuit diagram. Source: ON Semiconductor [48].

An Intelligent Power Module (IPM) is an advanced, highly integrated solid-state power switch. It adds functions and value to power modules beyond the basic power switches and gate drivers in one module, to enhance the performance. It often integrates temperature sensors to protect against overheating, current sensors to detect and address overcurrent and short circuit conditions, sensors to detect under-voltage conditions, and gate-control logic to prevent high-side and low-side switches from conducting at the same time. Integrating these functions not only reduces power circuit board area and parts count, it improves performance by reducing interconnect parasitics between the various control functions and the power devices.

4.1 Metrics

Metrics	Expectation and Requirement
Topologies	The majority of the EV utilizes three phase Voltage Source Inverters (VSI) based on insulated gate bi-polar transistors (IGBTs), refer to standard inverter topologies in image below. Many alternative topologies like Current source inverter, Z-source inverter and three-level inverters are available. The requirements of three-level inverters to overcome the double capacitor banks and higher cost need more innovation.
Passive component	Passive components with superior frequency characteristics are embedded next to switching devices. E.g. Minimize parasitic inductance through direct contact for higher switching speed. *Figure III-15: HI-level module for automotive application [49]*
Sensorics	Integrate both temperature and current sensor into the component level for better monitoring and controlling of the system. Need breakthrough in compact size to integrate current sensor.
Electrical System	Example in Automotive Application: • Voltage: Expectation up to 1.7kV (Current 1.2kV) • Current: Low current. e.g. 500A max for 1.2kV • Efficiency: 98% as per WLTP (Worldwide Harmonized Light Vehicle Test Procedure) • Switching Frequency: 16-20kHz (Current 10-12kHz) Better heat dissipation for high operating temperature and lower thermal resistance, e.g. Dual side direct cooling with Rth 0.15 per 100mm die size Breakthrough in Immersion cooling, jet impingement and spray cooling.
Thermal System	*Figure III-16: Jet impingement double-side cooling design [50]* Water heat optimization for pressure drop 60mbar 10L/min New Fin design structure and microchannel heat sinks and heatpipes. Refer to the Thermal Chapter for details.
EMC Spectrum	Better balancing to avoid voltage/current spike current. EMI filter integration
Cost	Low cost. E.g. Package cost <$0.07/kwatt with dual direct cooling.
Form Factor	Small form factor. No standard and depending on application and the system requirement. E.g Chip embedded in the PCB
Integration	Components/sub-modules Integration Gate-Driver Integration – to achieve shorter conduction loop with lower parasitic parameters. Heat sink Integration Cooling Integration Busbars integration System Integration *Figure 17: Reference [51]*

Intelligent power modules are most closely associated with motor control, but they are used in uninterruptible power supplies, inverters, and renewable-energy systems. An example of an IPM from ON Semiconductor is shown in Figure 14 [48].

4.2 Challenges for Component Packaging

The typical package structure of a power module is shown in Figure 15 [52]. It consists of a few basic elements: Dies (Diode, IGBT or MOSFET), insulating substrate, base plate, interconnects, Die Attach, Thermal Interface Material (TIM), encapsulant, and case. It is critical to choose the right materials to assemble all the elements in a package.

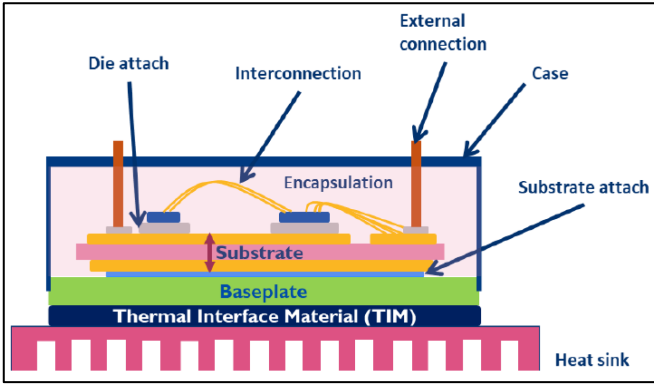


Figure III-18: Status of the Power Module Packaging Industry [52]. Source: Yole.

	Challenges	Existing Solution	Trend and required R&D
Interconnect	Challenges in resistivity and low inductance, thermal conductivity, high current density and TC requirement.	Al wire is widely used as a front metal interconnect. Some players used clip, ribbon bond, Cu wire, direct Cu plating or Cu sintering.[RF1]	Elimination of Wire Bond
Die Attach	Challenges in resistivity and low inductance, thermal conductivity and TC requirement. Elimination of lead solder and comply with ROHS Directive.	Die attached solution mainly solder paste and progressive conversion to Ag sintering.	Low Temp and pressure-less sintering. Cu Sintering. TLPS
Encapsulation	Challenge in high voltage ion mobility to meet HTRB performance. Comparative Tracking Index (CTI) equivalent to 600V.	Silicone Gel and epoxy compounds are commonly used.	Fast Cure epoxy. Material with high operating temperature stability
Substrate	Good electrical conductivity between the semiconductor components and terminals. Good electrical isolation to base plate and heat sink Good thermal conductivity material	Ceramic layer sandwiched with two metal layers. Common ceramic materials are Al_2O_3, $Zr\text{-}Al_2O_3$, AIN, Si_3N4 or BeO. The metallic material commonly is directly bond Cu or Al (DBC or DBA) Mainly used at bottom-side of the module for single side cooling and progressively used at top-side and bottom-side as well for double-side cooling structures.	Exploring different layers and materials. Merge substrate and baseplate as a single layer High performance Embedded Chip Power with direct power chip attached to DBCu substrate, planar, direct chip I/O connections to topside thick Cu interconnect and with double side cooling.
Baseplate	Good thermal conductivity	Widely used materials are Cu, Cu alloys or materials with high thermal conductivity.	Eliminate substrate to baseplate-attach material using direct DBC.

4.3 Challenges on Efficiency

Strike for >98% efficiency and lower cost requirements.

	Challenges	Existing Solution	Trend and require R&D
High-Speed Switching	Low loss. Reduce parasitic inductance.	WBG solution. SiC Diode, SiC MOSFET in EV/HEV market *Figure III-19: Source: Mitsubishi Electric Power Device Technologies* Planar Interconnect *Figure III-20: Reference [53]*	Use SiC in more markets. Hybrid Device – Future Integrated SiC with GaN HEMT in Power Module. Eliminate high interconnect parasitic by eliminating wire bonds and going to planar interconnect structures such as embedded chip power structures.
Thermal Management		Double-sided direct cooling with drain and source pads are connected to top and bottom DBC. *Figure III-21: Reference [54]* Stack Power module with thermally improved LTCC interposer *Figure III-22: Reference [55]*	Planar and embedded chip power modules with double sided cooling with low CTE, high thermal conductivity, dielectric substrates. SiC, AlN, composite structures with carbon nanotubes.
Thermo-mechanical	Overcome mismatched CTE of different materials in components package	Optimize material selection for integration	

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Section IV: Energy Harvesting

IV.1 INTRODUCTION

Energy Harvesting (EH) is competing with other power sources in the IoT (Internet of Things) world. Many different developments have shown the potential and benefits of EH [1, 2] compared to conventional energy supplies. However, the broad variety of EH sources, in combination with application-specific solutions, leads to multiple types of housings for the different transducer elements. In addition, energy storage, power management and radio components vary a lot depending on the envisaged application and operating scenario, resulting in a multitude of specialized device packaging and integration results.

A key challenge for a broader industrial adoption is a clear path towards standardized integration concepts. A clear advantage of today's batteries over energy harvesting is their prompt availability in different standardized form factors and voltage levels. Both criteria enable a rapid design of an IoT device without co-developing a customized power supply.

Energy harvesting (as described above) takes advantage of different expected ambient energy sources. A roadmap towards harmonized packaging and integration solutions needs a detailed analysis of specific as well as common requirements.

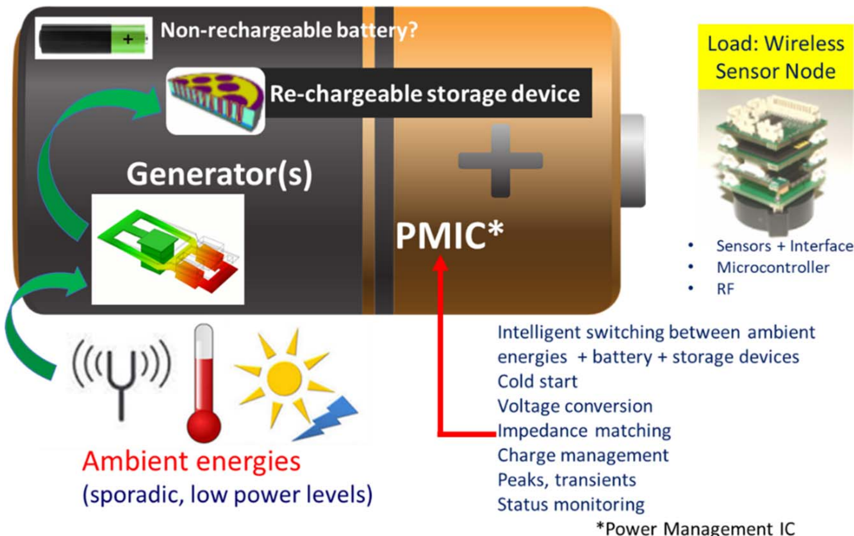

Figure IV-1. Replacing the function of a battery requires integration of a complex array of technologies. [illustrations courtesy of Tyndall National Institute]

The convergence of EH and packaging can be unique, since there are applications in which packaging must be carefully architected because it can actually become an integral part of the EH system. For instance, it is very common to utilize the packaging and geometry of a system solution to maximize power extraction from thermo-electrics, where power is maximized by the thermal differential on either side of the thermoelectric generator (TEG), and therefore the heatsinking capability of the overall packaging dictates much of the application's viability and/or operating life. Similarly, solar panels need to be embedded onto a surface (e.g. external IoT device housing) that has access to light energy, which is often outside the space made available for conventional energy storage elements. Kinetic EH can also be heavily dependent on packaging, whether it be a physical dynamo (electromagnetic principle) that must be accessible (at least by a shaft) to the mechanical energy source actuating it, or a microelectromechanical system (MEMS)-based, piezoelectric vibrational harvester that may rely on system packaging for the transfer of kinetic energy. Other even more forward-looking EH technologies, such as a triboelectric nanogenerator (TENG), which must derive its electrical energy from capturing charge generated by rubbing charged objects together (i.e., static electricity from friction), that must not only have packaging designed to integrate the EH, but also designed to generate friction of some form with the surrounding environment.

The field of EH is so complex, diverse and application-specific that we cannot address all of its current and envisioned technologies within the scope of this document; therefore, we will focus on the main energy harvesting devices based on vibration, thermoelectricity and solar cells, recognizing that a significant body of early conceptual work is then needed including a broad range of stakeholders for successful system integration. Further methods and more detailed considerations will be added in future versions.

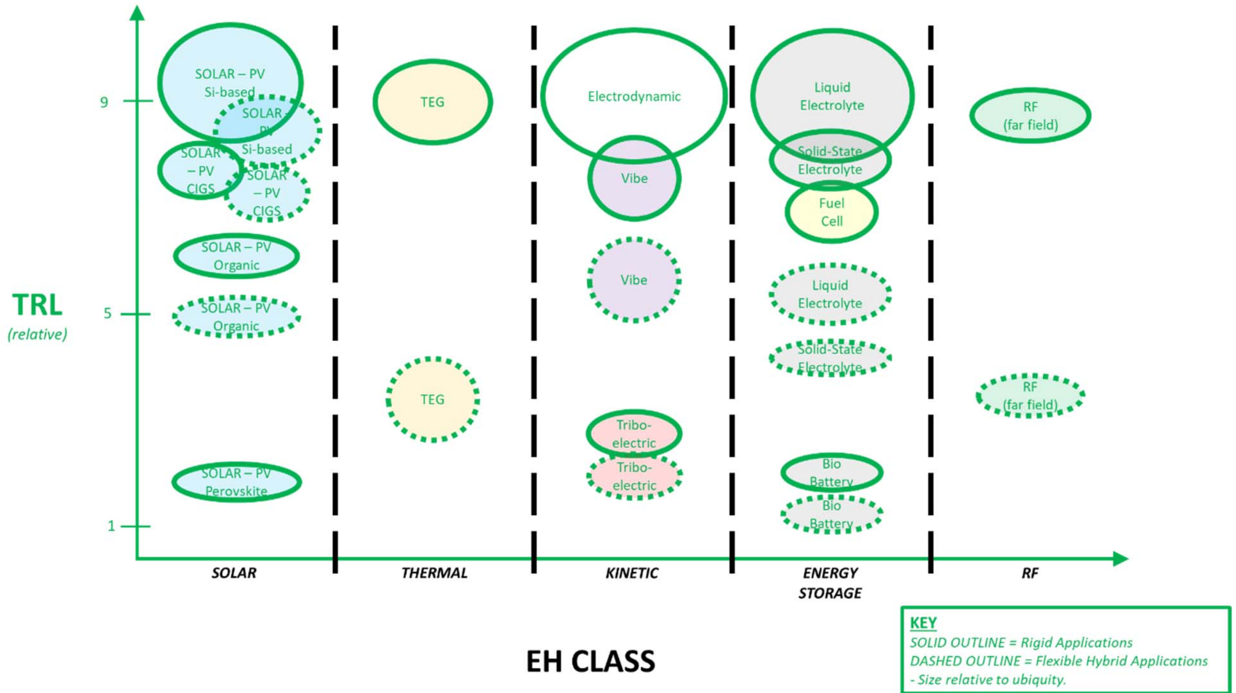

Figure IV-2: Technology Readiness Level (TRL) of current Energy Harvesting technologies.

IV.2 ENERGY HARVESTER-RELATED INTEGRATION CHALLENGES

A. Background

Energy harvesting is based on different physical effects and involves various transducers, resulting in a multitude of related integration challenges [3, 4]:

a) Kinetic energy: A spring-mass system translates the movement of bodies via a transducer (piezoelectric, electromagnetic or electrostatic) into electrical energy. In order to avoid losses between the harvester packaging and the energy source, a strong mechanical coupling is required without affecting the amplitude or frequency of the movement.

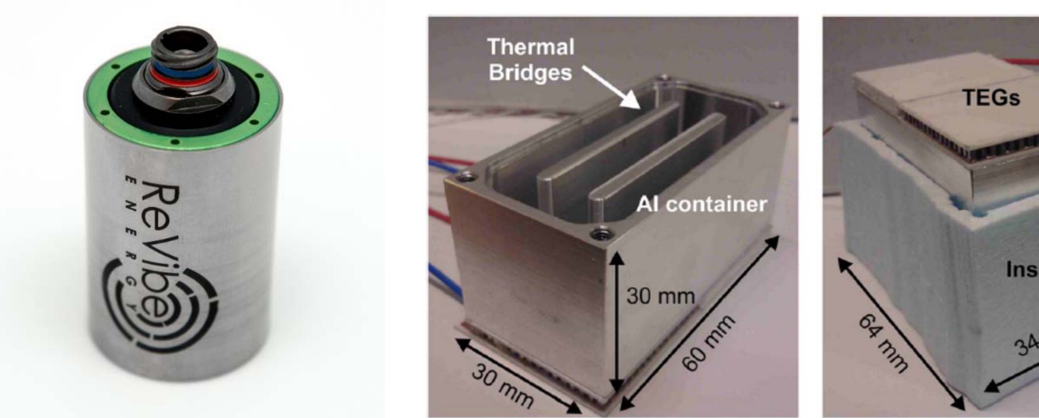

Figure IV-3: Kinetic energy harvester – Model D EVEH with the same size as D-sized battery [1].

Figure 4: Thermoelectric energy harvester using a heat storage unit [5].

b) Thermoelectricity: Ambient heat conversion into electrical energy via the Seebeck effect, the process may depend on local temperature gradients or heat fluctuations in time. Avoiding thermal energy losses requires heat conduction, thermal insulation and heat storage capabilities of components to be integrated into the overall packaging at the same time.

c) Solar cells: Radiant energy conversion via the photovoltaic effect requires the transparency of the packaging to electromagnetic radiation at the wavelengths of interest. Apart from further optical properties of windows

(reflection, scattering, diffraction etc.), the material has to be resilient to ingress over time or due to adsorption (e.g. water vapor).

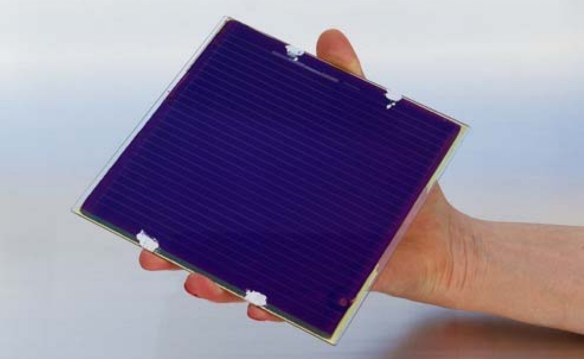

Figure IV-5: Solar Cell.
[Courtesy of Solliance Solar Research, photo by Niels van Loon, https://www.solliance.eu/2016/solliance-partners-present-first-semi-transparent-perovskite-module/ (last accessed 27/09/2021)]

d) There are other methods under investigation, ranging from triboelectricity [6], micro fuel cells [7], and using electromagnetic fields and waves [8] or acoustic waves [9]. However, these devices will be discussed in the next version of the roadmap.

B. Ambient Energy Sources: related integration challenges

Energy harvesting devices collect energy from the ambient energy source to which they are connected. This energy flow from the source to the drain may have a detrimental impact on the source itself or the surrounding system. Selected challenges:

a) Kinetic Energy is the energy a body possess due to its motion. Any additionally coupled parts will influence the mass, velocity, acceleration or frequency of the overall source. As a consequence, the normal mode or Eigen frequency of a body, a vehicle, a building, a machine, an animal or human being, will be distorted.

b) Thermoelectric devices generate electrical energy by allowing heat flowing through the Seebeck element. The heat flow leads to cooling on one side and heating on the other side. The resulting temperature change depends strongly on the characteristics of the heat source, e.g. thermal mass. Ambitious approaches may lead to unwanted energy fluctuation of the primary system.

c) Solar cells are not expected to influence the radiation source. However, accidental shadowing may lead to an unpredictable harvesting source and thermal management may be required depending on the source.

d) Other sources will be discussed in a later version of this document.

C. Heterogeneous Integration of Storage for Energy Harvesting

The power production profiles of most energy harvesting (EH) sources is largely variable due to their dependence on environmental conditions. For example, with outdoor solar PV, power production is high during daylight hours, but reduces to zero overnight. IoT sensor loads, on the other hand, usually have a well-defined power consumption profile, which peaks during data transmission. They may be configured to operate in low-power or sleep mode during periods of low power generation, but they generally need to maintain continuous operation at some minimum level of functionality and therefore require a continuous power source.

Due to this mismatch between power production and load demand profiles, energy storage is required in the same way as in large-scale renewable energy systems. Indeed, the same conventional battery technologies are used, but obviously at a much smaller scale. However, the current discharge rate of batteries sized based to match EH source and sensor load energy levels may be limited so that they cannot provide the high current peaks needed for data transmission. Supercapacitors provide a compatible solution in that case, where their higher power density enables them to supply the high current peaks while the higher energy density of the battery maintains continuous operation at average power levels.

Battery/supercapacitor technologies

Currently, low-capacity rechargeable (secondary) battery technologies suitable for combination with EH sources in IoT applications are largely based on NiMH and Li-ion coin and cylindrical cells [10, 11], with several manufacturers also providing laminated flattened form factors that are more compatible with electronics packaging [12, 13]. Going a step further, MEMS technologies have been developed to produce miniaturized batteries suitable for integration in electronic packaging [14]. Due to safety concerns with liquid electrolytes, technologies suitable for

integration of solid-state micro-batteries within electronic packaging are emerging. These include flexible batteries produced using screen printing techniques [15], PVD [16] and substrate thinning [17].

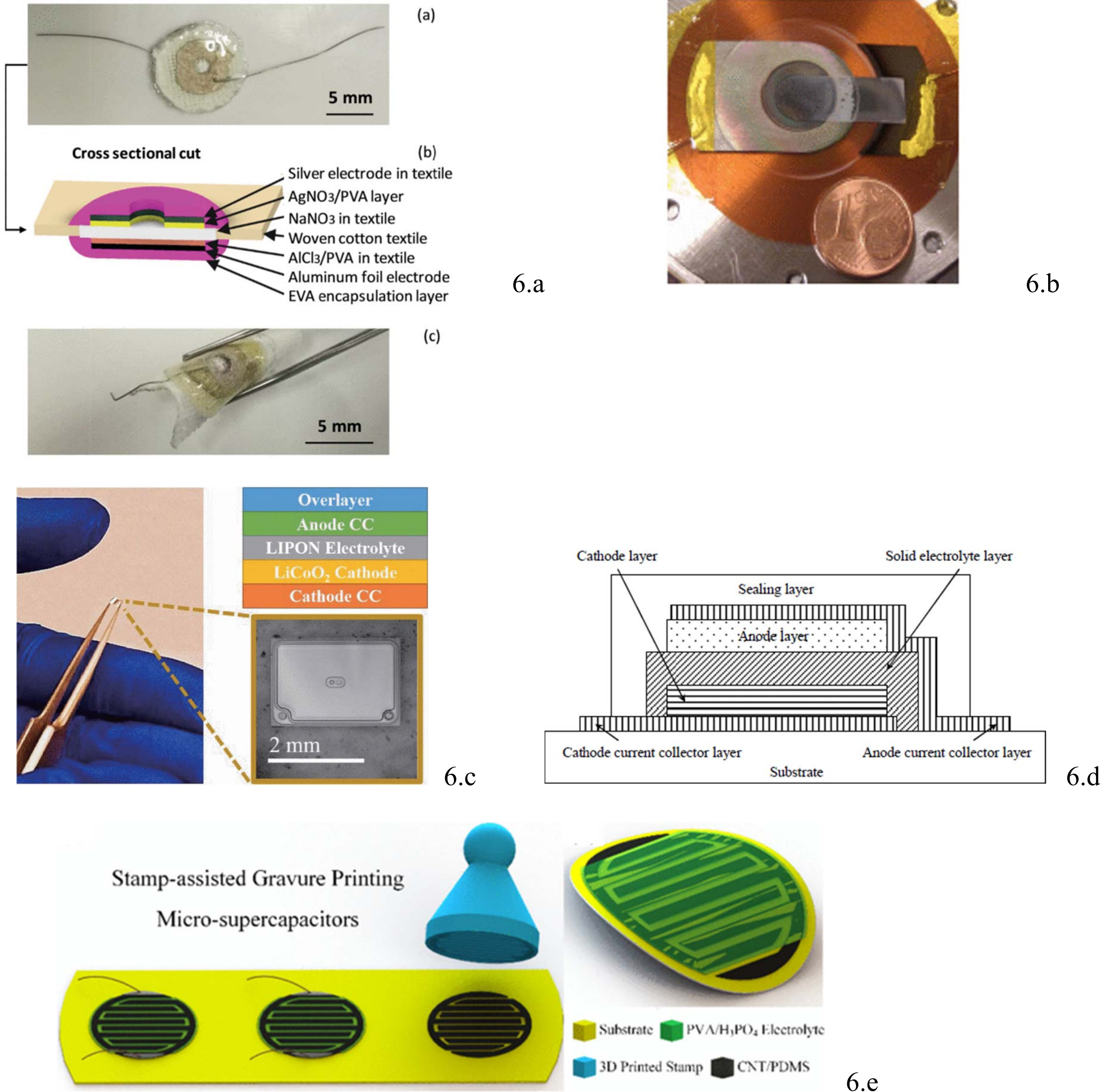

Figure 6: Flexible solid-state battery production technologies: (a) substrate release [15], (b) PVD [16], (c) 30 µm LIB produced by substrate thinning [17], (d) silicon compatible electrode build up [18], (e) gravure printed supercapacitor [22].

In addition to their form factor, solid state micro-batteries have a number of advantages that are appropriate to WSN energy needs. Thin film micro-batteries can deliver 250 Ah/cm^2 capacities for single layer cells, with peak currents of 5 mA/cm^2 possible for delivering up to 0.5 ms pulses every second. Trends in producing stacked cells decrease the footprint required for a given capacity. Solid state batteries exhibit very long lifetimes with 5,000+ cycles possible, particularly under conditions of shallow cell discharge. They have a stable output potential over the device lifetime. New electrode solutions suitable for integration on silicon are being developed [18] to address issues with high internal battery resistance.

Other approaches include a range of additive manufacturing solutions [19], and flexible fiber-shaped solutions [20, 21]. Similarly, technologies including inkjet printing have been applied to produce supercapacitors (also known as ultracapacitors or double layer capacitors) in form factors that are compatible with electronics packaging [22].

Commercial bare-die solutions have emerged [23], along with several Li-polymer offerings [24]. Paper-based supercapacitors and zinc-manganese so-called 'dry batteries' are also commercially available [23].

Integrated EH source/storage technologies: Examples include the integration of PV and battery cells within the same packaging, which opens the possibility of reducing or eliminating power conversion stages required to match

their operating voltages [25]. Roll-to-roll manufacturing has facilitated the integration of piezoelectric sources with supercapacitors and some power conversion circuitry [26]. Commercially, the integration of batteries and supercapacitors in one device provides an effective storage solution that can address the dynamic power profile of wireless sensor nodes [27].

IV.3 POWER MANAGEMENT ICS (PMICS) FOR ENERGY HARVESTING

The role of PMICs (Power Management ICs) in ultra-low power wireless IoT edge devices becomes particularly critical when multiple (primary, rechargeable and ambient) energy sources are available and complex conversion/storage operations are required to provide a steady voltage to the load.

Configurable parts are needed that cover different families of applications (e.g. buildings, machinery, smart mobility, wearables, implantables), each application in turn leading to a further sub-set of applications (e.g. wearables based on walking, running, work environment monitoring, health monitoring). Different families of devices may also be required for different power and voltage levels – e.g. switched capacitor circuits for narrow voltage ranges vs. inductive-based solutions for broader ranges. There is an increasing need for PMICs to be “software defined" and highly interoperable in order to work with the other generation and storage devices and the system load (microcontroller (MCU), transceiver and sensors typically) to maximize efficiency, use ambient energies when available and contextually minimize the device configuration to minimize the power consumed whilst meeting the application needs.

Features such as self-start, impedance matching, low quiescent current, efficiency at very light loads and wide input voltage range will be key for many applications, and such considerations should be taken into account when designing power management (discrete and IC) circuit blocks and power architectures.

Critical Features

a) *Efficiency*: Efficiencies > 90% are already being achieved but such a target becomes more challenging as the load power reduces to 10s of µW and below, where we anticipate many IoT edge devices will operate. The entire efficiency curve as a function of load needs to be examined so that multiple types of ambient energies are efficiently harvestable.

b) *Input and output voltage range*: Ambient energies from various sources deliver a very broad range of input voltages. For example, many low=temperature TEGs (thermoelectric generators) and EM (electromagnetic) vibrational transducers will generate only 10s of mV. Many piezo and triboelectric transducers provide 100s of V (at high impedance). No single PMIC can deliver the entire range but it is important that PMICs offer sufficient range to cater for variability and diversity in the ambient energy sources and transducers used. It also enables additional energy to be ‘drained’ from a battery/storage device at lower voltages. Configurable buck-boost topologies may prove popular. For applications where the input voltage is reasonable (several hundred mV, a few volts) and range is relatively narrow (e.g. some PV applications or a steady temperature source), switched-capacitor solutions may prove to be more efficient and lead to a smaller form factor (no external inductor needed).

c) *Cold start voltage*: The ambient energy source may be sporadic and retreat to relatively low operating voltage levels for a given period. This could result in sporadic engaging and disengaging of the energy harvesting source to the load and affect continuity of supply. PMICs may need to be able operate down to very low voltage levels (10s of mV) once cold-started.

d) *Cold start power source capability*: This is another much-overlooked feature. PMICs require a minimum amount of energy from a transducer (e.g. PV, vibrational, thermoelectric) in order to cold start. For many real-life applications, the ambient energies can be very low and this can impede the ability of the transducer to deliver power. Best available capability found to date is a few µW with emerging technology from Tyndall [28] indicating capability of operating to 1uW and potentially below.

e) *Quiescent current*: Many IoT devices often spend most of their time in quiescent mode. For such devices, battery life will be significantly impacted if the PMIC is a significant part of the overall device quiescent current. At present state of the art, PMICs can operate down to a couple of hundred nA [28] but this needs to get to 10s of nA for some applications.

f) *Impedance matching/MPPT*: Many applications using energy harvesting transducers will rely on the PMIC to provide impedance matching (e.g. MPPT – maximum power point tracking) to maximize the transfer of energy from the source to the load and/or storage device. PMICs will need to be capable of handling multiple types of transducers and have capability to auto-configure and dynamically modify the impedance as required accordingly as the ambient energy changes. Vibrational energy harvesting sources are particularly prone to

performance degradation due to changes in frequency, amplitude and acceleration of the ambient energy source [29].

IV.4 CHALLENGES AND SOLUTIONS ROADMAP

Emerging technologies in development to meet the above requirements in real applications include:

i. Novel power architectures efficiently converting ambient energies (often very low voltages/power) to usable levels at high efficiency
ii. Novel self-start circuits for device autonomy
iii. Ultra-low (10s of nW) quiescent current consumption platforms
iv. Innovative topologies (e.g. zero voltage switching, high frequency) to both maximize efficiency and minimize size of external components (e.g. magnetics or capacitors) over a broad range of input and output voltages and power levels
v. Digital control capability to dynamically configure sensors, MCUs and transceivers to only activate as needed
vi. Digital control capability to assure a steady voltage supply to the load from the combination of sources available (primary, rechargeable)
vii. 'Multi-source' capability, managing a broad variety of ambient energy types
viii. Integration/embedding of other components (e.g. magnetics and MCUs driving performance, cost/size reduction) at power source and system level in package or on-chip
ix. Simulation models at the device and system level to help developers understand how to optimize performance and operability of their parts based on the PMIC offering. This can also help PMIC developers with trade-off and configurability considerations (e.g. efficiency versus input voltage range)

Common integration challenges

The White Paper "Energy Harvesting for a Green Internet of Things" [1] discusses in detail the key elements for industrial adoption. With respect to overall integration challenges, the lack of common standards and specifications are key limiting elements for all energy harvesting devices to assure inter-operability and system-level optimization. Key challenges to be addressed are:

a) *Ease of integration*: State-of-the-art harvesting devices are packaged in application-specific housings. The weight and size are often unclear in the beginning, resulting in delays in the overall system design.
b) *Flexible components*: Some harvester components are already available in a flexible format. Examples are solar cells, thermoelectric generators, batteries and supercapacitors. Flexible materials are allowing the use of energy harvesters for bendable applications, such as wearables. Moreover, with flexible materials, a conformal application on rough surfaces is possible. However, the overall device-level flexibility is currently limited by the flexibility of the components themselves.
c) *Power output level and waveforms*: Each harvester differs in power output (voltage, current, frequency) and requires a specific energy management and storage solution. As a consequence, the internal cabling/interconnection varies significantly and external connectors are not standardized. Available data sheets from different suppliers are not yet comparable to those of batteries.
d) *Standardization and harmonized Data sheets*: In the absence of standards in terms of form factor, specifications, test conditions, operating environments, etc., developers are creating bespoke parts making it difficult to do 'like for like' comparisons as well as inter-connect parts and predict system level behavior. The EU EnABLES project has made an initial move towards standardization with some initial take-up by creating uniform data sheets for different component types [30]. However, it needs broad acceptance and adoption by the power IoT community for it to take root.

Roadmap Towards Commercial Off-The-Shelf (COTS) Energy Harvesting Devices

If stakeholders 'think about power' at the early conceptual stages of IoT solutions in co-designing and selecting components, data gathering, and processing architectures, significant battery life extension is possible. This is not just about minimizing power consumption – it extends to understanding the operating environment and what types of energies could be harvested and stored to extend battery life.

Based on state-of-the-art technology, there is a sweet spot from around 1 mW to a few hundred mW, where real-life ambient energies from reasonably sized harvesters can have a significant impact on the battery life. Figure 7 illustrates such extensions possible for thermoelectric, vibration and solar energies operating at common and moderate activation levels. Further improvements in the 10-30% region should be possible over the next 5 years as

well as a significant increase of the (frequency) bandwidth over which vibrational devices can operate effectively, moving to several 10s of % – all very much depending on the application.

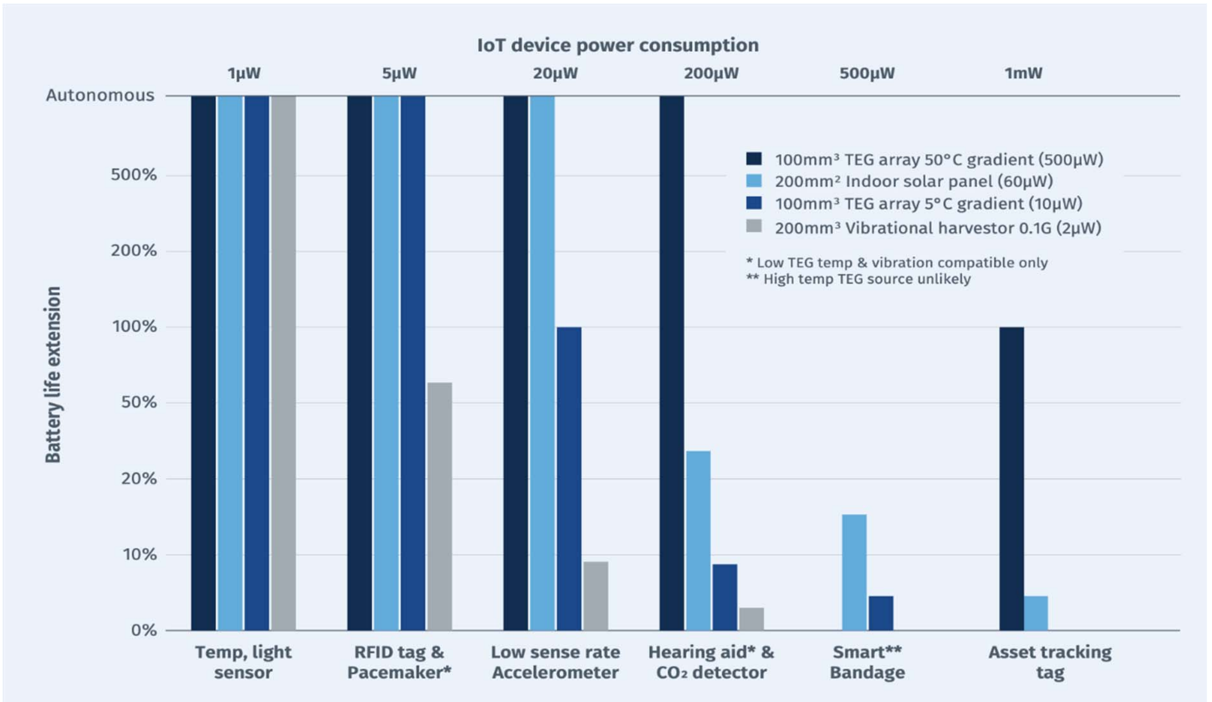

Fig IV-7. Battery life extension potential (courtesy of EnABLES position paper) [2].

At sub 100mW there is the double impact of less drain on the existing power source and increased viability of adding relatively small energy harvesting devices to significantly increasing battery life.

Future directions for EH devices can be briefly summarized by the following trends:

a) Next-Generation 2D integrated devices: Solar Cells and RF tags are compatible with 2D integration techniques such as roll-to-roll fabrication. This processing technology allows cost-effective integration of all components onto the same substrate. Flexible hybrid electronics (FHE) adds an additional element to facilitate the integration of EH solutions in application-optimized packaging. Conformance to atypical/asymmetric geometries can be further helpful for driving many of the same design objectives outlined above. When combined with insulating organic substrates (eg, polyimide), the properties of thermal/electrical isolation can facilitate denser integrated solutions (in terms of size, weight, and/or power metrics) while biocompatibility can facilitate medical/wearable environments. While much focus is on the application usage and environment, one should also note the major advantages FHE-based EH (and supporting components) can provide for integrating EH into high-volume processes (i.e. roll-to-roll, screen printing, etc.), which can greatly accelerate adoption thanks to the cost reduction enabled by economies of scale.

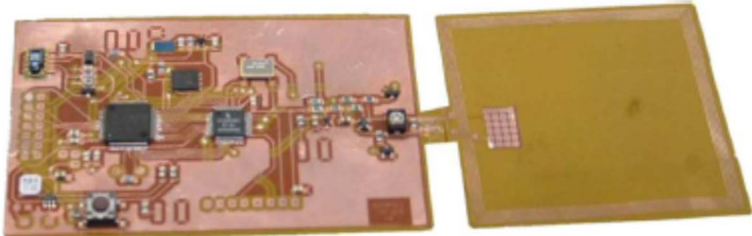

Figure IV-8: Flexible Tag Microlab, a 2D foil integrated system [31].

b) Next-generation 3D printed devices: Future 3D printed devices might consist only of printed parts, since active parts such as thermoelectric modules or electronic components will be printed in the same process.

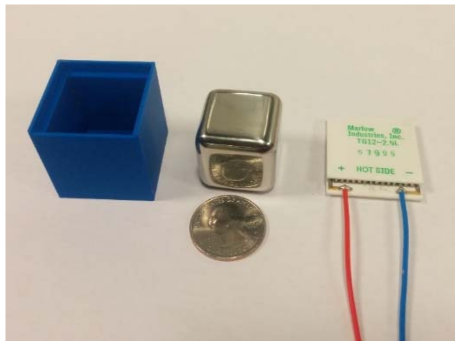
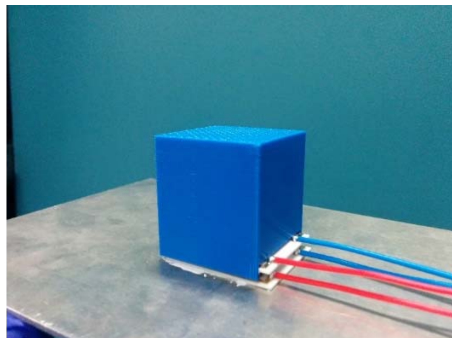

Figure IV-9: 3D Printed thermoelectric harvesting device [32]

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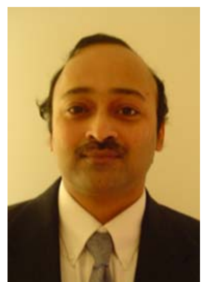
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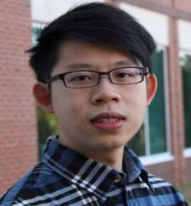
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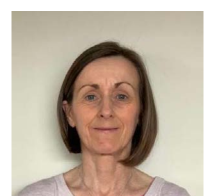
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