CHAPTER 10. TRANSISTORS and TRANSISTOR CIRCUITS:

10.1 INTRODUCTION TO TRANSISTORS

The transistor is a component of the form of a 'transfer-resistance' or 'trans-resistance', which is the reason for its name. It is a 3-terminal component. It has a low-resistance 'output path' between two of its terminals whose conductance is controlled by a high-resistance input (at the other terminal). The low-resistance output path is usually placed in series with other conductive components where it then serves to control the current through the string of components.

In the concept figure of 10.1-1(a), the controlled conductance is represented as being between nodes B and C. The input (control) node is at node A. One node (B) will be common to both the control input (A) and the output conductance. The bias between nodes A and B controls the conductance path according to whatever semiconductor effects relate to this bias. As V_{BC} increases the I-V_{BC} characteristics roll off to a relatively fixed current level like that represented by figure 10.1-1(b). In the fixed current regime the transistor then acts like a voltage-controlled current source $I(V_{AB})$, which is usually identified as the active regime.

In the active regime variations of node voltage V_C will have very little effect on the current level. So this node will be relatively 'stiff'. Because of its stiffness, node C is the favored choice as an output node.

Node B also can serve as output node since it is on the output path. But it is not as stiff as terminal C and since it is also one end of the controlling input then a variation in V_B will have an effect on I_C. The remaining node (node A) is only applicable to the input.

When the transistor is in the active regime the current level is a constant with respect to V_{BC} and slope (= dI/dV = conductance) = 0, which is exactly the behavior of an ideal current source.

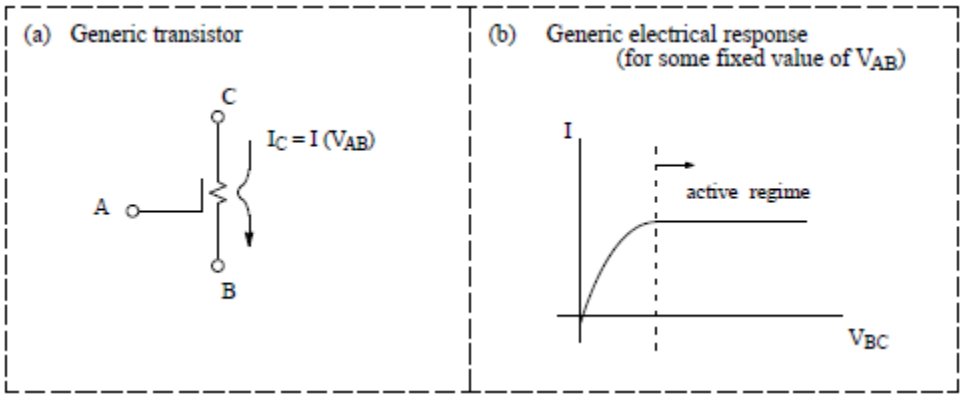


Figure 10.1-1. Conceptual transistor and its electrical characteristics

For use of the transistor in an amplifier it is necessary to translate it into an equivalent VCT (voltage-to-current transducer) as represented by figure 10.1-2. It is not expected that current level I_C will be linear with respect to the control V_{AB}, but we can accept linear approximations for small increments, not unlike the iteration methods used by software to assess non-linear device model equations.

The small-increment model for the transistor, also called the 'small-signal model' is of the form

$$i_C = g_m v_{AB} \tag{10.1-1}$$

where parameter g_m must be of the form of a conductance or *transconductance* (transfer conductance).

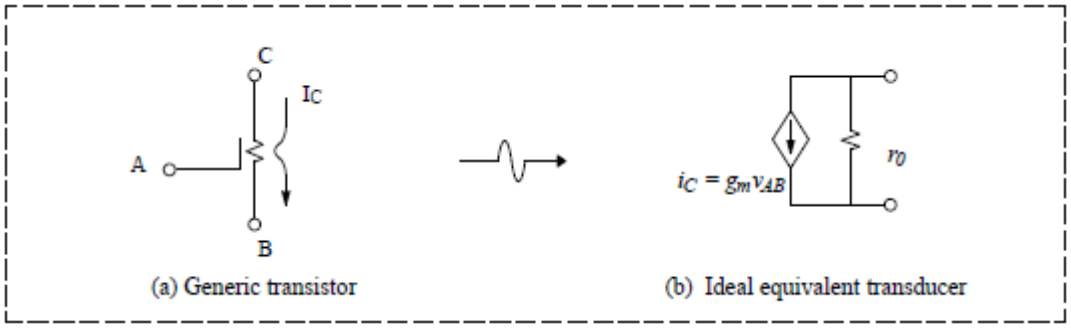


Figure 10.1-2. Small–signal interpretation of transistor as an idealized dependent current source

We also have to recognize that the current level I_C is not completely stiff and so the VCT must be softened to include an output resistance, as represented by figure 10.1-2(b). Output resistance r_0 is expected to be large, consistent with the ideal behavior of a current source.

Note the convention of the nomenclature. Lower case implies small-signal context. At the incremental level the conductances g_m and g_0 are the *slopes* of the two *I* vs *V* characteristics as represented by figure 10.1-3. And they are also lower case.

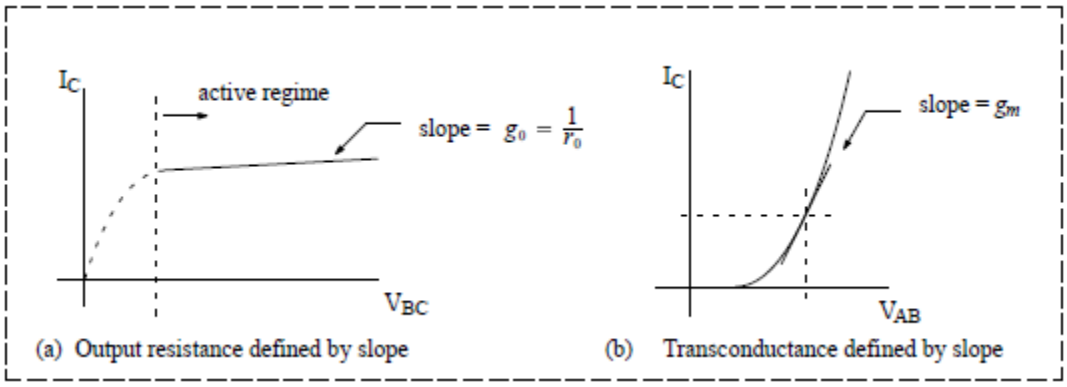


Figure 10.1-3. VCT parameters are slopes of the *I-V* characteristics in the (two) voltage planes.

A small incremental change in output current δI_C takes place with a small incremental (small–signal) change in the (input) control voltage δV_{AB}. In mathematics speak, this is expressed as

$$\delta I_C = \frac{\partial I_C}{\partial V_{AB}} \delta V_{AB} \qquad = g_m \times \delta V_{AB} \qquad (10.1\text{-}2)$$

This equation is of the same form as equation (10.1-1) as given for the VCT provided that we make the nomenclature small-signal correlation $\delta I_C \rightarrow i_C$ and $\delta V_{AB} \rightarrow v_{AB}$ and for which

$$g_m = \frac{\partial I_C}{\partial V_{AB}} \qquad (10.1\text{-}3a)$$

Its value depends on the bias point (a.k.a. operating point) at which the transistor is operated and it may be fairly large if the slope is steep.

On the other hand the output resistance r_0 is defined by the relatively small slope g_0

$$g_0 = \frac{\partial I_C}{\partial V_{CB}} \qquad (10.1\text{-}3b)$$

Its value also depends on the bias point at which the transistor is operated. The slope g_0 is relatively small as indicated by figure 10.1-3a.

There are a number of semiconductor, vacuum, and electro-optical devices in the transistor kingdom that have behavior like that indicated by these figures. But for semiconductors there are essentially only two species of transistor. These are devices for which:

(1) output conductance (and current) are defined by means of bias across a *pn* junction
(2) output conductance (and current) are defined by the effect of an E-field on a semiconductor substrate.

We call these two species:

(1) the 'bipolar-junction' transistor, (BJT)
(2) the field-effect transistor (FET).

Although each of these types of transistor may have similar roles within a circuit, each also has characteristics that make it particularly suited for certain tasks:

(1) The BJT is usually considered to be the 'heavy-lifter' of the transistor kingdom, oriented toward control of larger levels of current.
(2) The FET is usually associated with the light, fast action, particularly in the design of VLSI circuits.

The division is not emphatic and we can use BJTs in VLSI design and we can use FETs the size of an orange-juice can for circuits for which high-level current levels must be controlled.

10.2 THE BIPOLAR-JUNCTION TRANSISTOR

The earliest form of semiconductor transistor is the bipolar-junction transistor (BJT). An ion-implantation representation of its fabrication process is shown by figure 10.2-1. In comparison to figure 9.2-1 for the *pn* junction diode shows why the BJT is a natural evolution. The extra step relative to figure 9.2-1 yields a three-layer semiconductor device with two opposing *pn* junctions back-to-back, as shown by the inset to the figure.

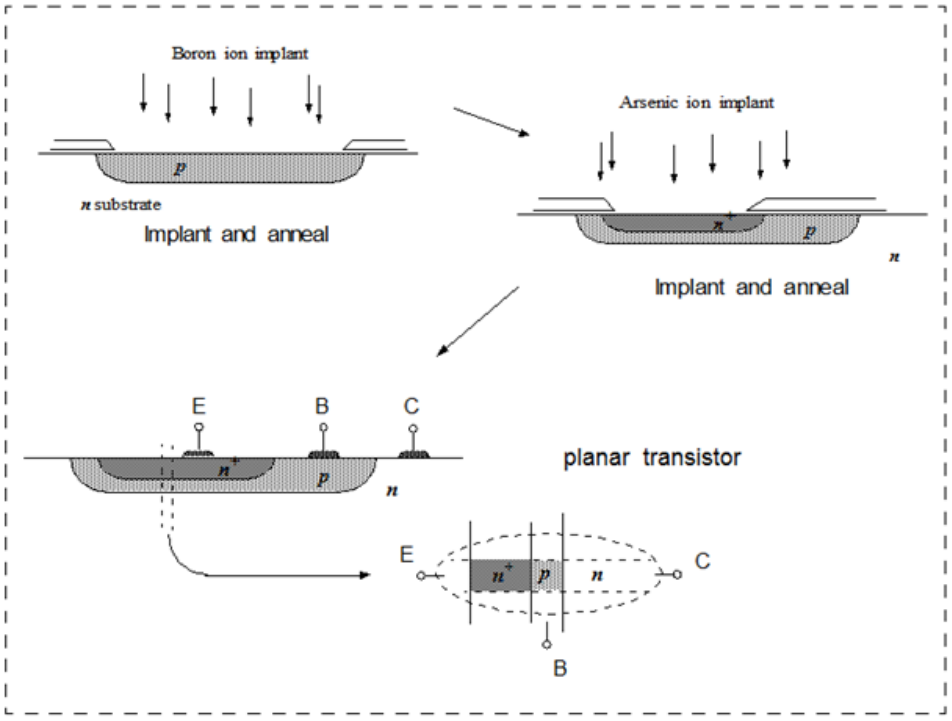


Figure 10.2-1 Fabrication and cross-section of a planar BJT (bipolar junction transistor)

An expansion of the inset is shown by figure 10.2-2 and identifies the appropriate junction biases and the resulting carrier flow for the BJT in active mode.

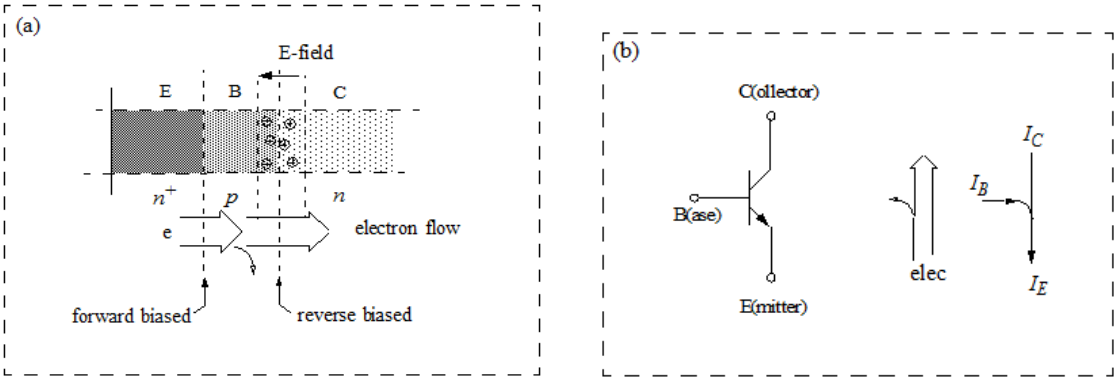


Figure 10.2-2a. Carrier injection and collection in the active mode bias
Figure 10.2-2b. Circuit symbol and corresponding carrier flow and node currents.

As represented by figure 10.2-2 the transistor is in active mode when the *pn* junction between E and B is forward biased and the *pn* junction between B and C is reverse-biased. These junction biases also correspond to bias order $V_E < V_B < V_C$. In part this bias order is indicted by figure 10.2-2b, which shows the circuit symbol and the corresponding carrier flow and current in the (*npn*) BJT.

The subscript nomenclature tells all. With forward bias of the B to E junction, charge carriers are injected through this junction and into the middle layer. And that is why node E is called the (*e*)*mitter* node. The middle layer is relatively thin, on the order of 1–2 μm thickness, so the injected charge carriers find themselves in the vicinity of the E–field that results from the reverse-biased B-C junction. The orientation of this field is exactly that which can snatch up the injected carriers and whisk them off toward node C. And that is why this node is called the (*c*)*ollector* node.

The emitter-collector process is very efficient. Efficiency is close to 100% (but not quite) when the emitter layer is the more heavily-doped one, as represented by figure 10.2-1.

The middle layer of the sandwich is called the *base* layer which is why the figure has the nomenclature shown.

Other bias orders besides the forward-active option can occur but are of relatively little functional benefit. Strictly speaking, the same emitter-collector process can take place if the transistor is electrically inverted but the resulting efficiency is lousy.

As should be evident, there is a choice of layer order. The one shown by figures 10.2-1 and 10.2-2 are in the *npn* order and transistors of this type are designated as *npn* transistors with circuit symbol as shown by figure 10.2-2b. If the *pnp* layer order is fabricated then the injected and collected charge carriers are holes instead of electrons. Holes are usually not as mobile as electrons and so the characteristics are slightly different. The key aspect of the *pnp* transistor is that its bias order is then flipped, and so its usage is flipped, as represented by figure 10.2-3.

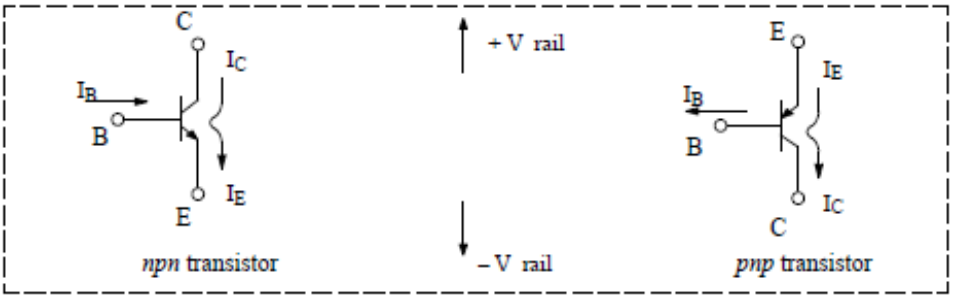


Figure 10.2-3. Nomenclature for the BJT. Since it is a three–layer device, there are two possible genders for the BJT, *npn*, and *pnp*.

Inasmuch as the *pnp* transistor is electrically complementary to the *npn* it is not uncommon for these two genders of transistor to be employed in sequence pairs so that the shortcomings of one will strengthen the other, much like what happens when the two genders of the human species decide to pair up.

Regardless of which gender is employed it is pretty obvious from the circuit symbols for figure10.2-3 and for figure 10.2-2 that $I_E > I_C$, even though we often assume that they are virtually equal. If we add up the currents, and obey Kirchoff's current law, which is the polite thing to do, then

$$I_E = I_C + I_B \tag{10.2-1}$$

But, we also assume that the transistor is a very efficient collector, so that

$$I_C = \alpha_F I_E \tag{10.2-2}$$

where α_F should almost be equal to 1.0, or maybe at least to 0.998. or maybe 0.95, or whatever. Ideally we can assume that the collector of a normally efficient transistor will collect almost 100% of the charge-carriers emitted by the emitter.

However equation (10.2-2) is put aside because it makes more sense to define a 'control' equation in which the output current I_C is controlled by input current I_B. That suggests that it is in order to combine equations (10.2-1) and (10.2-2) such that

$$\frac{I_C}{\alpha_F} = I_C + I_B$$

for which

$$I_C \times \left(1 - \frac{1}{\alpha_F}\right) = I_B$$

which we rewrite as $$I_C = \left(\frac{\alpha_F}{1-\alpha_F}\right) I_B \qquad = \beta_F I_B$$

Since α_F is very nearly equal to unity, then we expect β_F to be reasonably large. The equation that we therefore put to the most use is the *control* equation for the BJT

$$I_C = \beta_F I_B \tag{10.2-3}$$

where β_F is the *forward current gain*. The forward current gain is also referred to as h_{FE} in some of the older books, probably falls right after the section on alchemie.

A collateral control equation that is sometimes handy is

$$I_E = (\beta_F + 1) I_B \tag{10.2-4}$$

since $I_E = I_C + I_B$.

A typical value for forward current gain is $\beta_F = 100$. If we happen to be using transistors for high-current, high-voltage applications, the emitter–collector efficiency is reduced and β_F may only be about 25. In general, the *pnp* sister transistor is a little less efficient than the *npn*, and so this fact must be accommodated in circuit design where symmetry is important.

Otherwise all transistors may be assumed to be nearly alike, for which it is not unreasonable to default the forward current gain to $\boldsymbol{\beta_F = 100}$. After all they may have been gifted to you by your Mom or your Aunt Jane and did not otherwise include any performance characteristics.

10.3 BIASING OF SINGLE-TRANSISTOR BJT CIRCUITS.

In order for the *BJT* to exercise control over the current it must be emplaced in a path that is between the voltage rails and in series with other conductive components, like the circuit shown by figure 10.3-1.

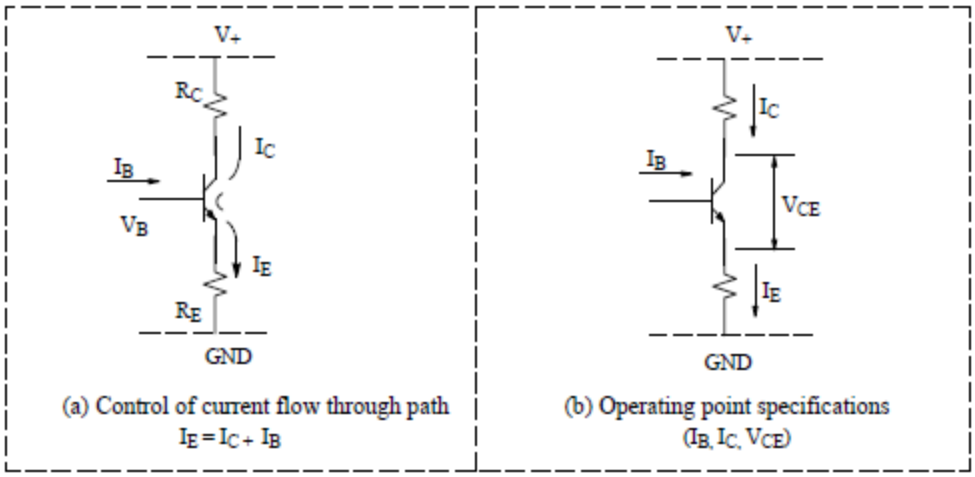


Figure 10.3-1. BJT deployed as a control element in a conductive path

Although this is not the only way in which we will deploy a transistor in a circuit, it is the most representative. As given by figure 10.3-1(a) it controls and defines the flow of current between the upper and lower voltage rails according to the biases that are applied and induced within the network.

The equilibrium current flow and voltages in and around the transistor are defined as its *operating point,* and we specify it by the values of (I_B, I_C, and V_{CE}).

Now if we should really attempt to solve this transistor circuit with the transistor as a real device, we would have to assume a bias across the junction and use it to find the current, then with this current, assess the junction equations to find junction voltage. With corrected junction voltage the current level would have to be updated. Then we would have to re-evaluate the junction voltage, - etc.
It would be an iterative process. And entertaining though this process might be the extra accuracy that we gain would be minimal. We are just as well off to accept a little slop and assume that the bias across a forward–biased *pn* junction is a value consistent with the current levels through the junction.

A typical *V*(junction) value for a forward-biased *pn* junction carrying currents at mA levels is

$$V\,(\textit{base-emitter junction}) \cong 0.7V \qquad \textit{accepted default} \qquad (10.3\text{-}1)$$

As indicated by figure 10.3-2, this corresponds to $V_{BE} \cong +0.7V$ for *npn*

Keep in mind that the *pnp* transistor will have <u>opposite</u> polarity (= –0.7*V*) across the base-emitter junction. But rather than be troubled about signs it is best to inspect the direction in which current is tasked to flow through the B-E junction and use it to identify the appropriate polarity. This form of analysis is exactly what was done with circuits with *pn* junction diodes, and we call it <u>inspection</u>. Software utilities do not have this luxury and so they have to try out different options, although at lightning speed. The emphasis, as before, is that the engineer cannot expect a formula to do his/her thinking. He/she must think and inspect.

Consider the following example.

EXAMPLE 10.3-1: Operating point analysis of a BJT (*npn*)

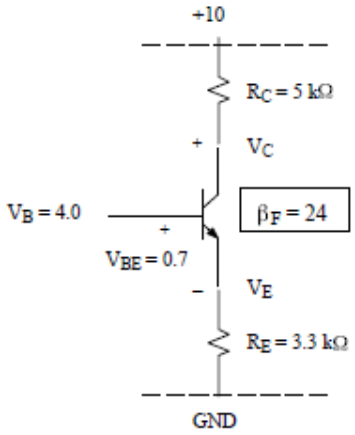


Figure E10.3-1a. *npn* transistor as a member of a string of conducting components.

SOLUTION: For $V_B = 4.0$ V and $V_{BE} = 0.7$V then

$$V_E = V_B - V_{BE} = 4.0 - 0.7 = 3.3\text{V}$$

Hopefully we do NOT need a calculator to do this little bit of math. Later we will simply blink twice and write down the value. (You need to get used to this quick math).

Naturally if we know the value for V_E we also know the current I_E for which

$$I_E = \frac{V_E - V_{EE}}{R_E} = \frac{3.3 - 0}{3.3} = 1.0\text{mA}$$

Note that the lower rail is sometimes labelled as V_{EE}. This option adds a little more flavor to the page collection of bias formulas even though the lower voltage rail usually = GND.

From the value of forward current gain β_F the value of I_B using equation (10.2-4) will be

$$I_B = \frac{I_E}{\beta_F + 1} = \frac{1.0}{24 + 1} = \underline{\textbf{.04mA}}$$

From which I_C is then

$$I_C = I_E - I_B = 1.0 - 0.4 = \underline{\textbf{0.96 mA}}$$

which could also have been accomplished by $I_C = \beta_F I_B = 24 \times 0.4 = 0.96\text{mA}$

Knowledge of the value for I_C gives V_C

$$V_C = V_+ - I_C R_C = 10 - 5 \times 0.96 \qquad = 5.2\text{V}$$

And consequently the last of the electrical facts needed to identify the operating point of the transistor is

$$V_{CE} = V_C - V_E = 5.2 - 3.3 \qquad = \qquad \underline{\textbf{1.9V}}$$

Be aware that these values are only approximates. They are predicated on the premise that $V_{BE} = 0.7\text{V}$. But otherwise these calculations are 'good enough'. Should more refinement be desired the analysis can be passed along to pspice or some other circuit simulation platform.

The values that are highlighted are the operating point for the transistor and has its best context in terms of the I-V output characteristics of the transistor shown by figure E10.3-2.

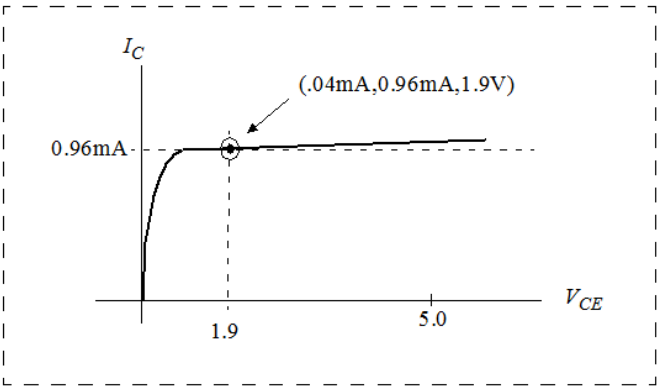


Figure E10.3-1b. Operating point of the transistor (for the example)

The operating point is (also) a graphical I -V point about which the signals passed to the transistor will wovulate.

EXAMPLE 10.3-2: Now make a modification to example 10.3-1. Change the value of R_E to 2.0 kΩ.

Following the procedure suggested by example 10.3-1the value of V_E is still 4.0 – 0.7 = 3.3 V, from which we can compute I_E , for which

$$I_E = \frac{V_E - V_{EE}}{R_E} = \frac{3.3 - 0}{2.0} \qquad = 1.65\text{mA}$$

(SOLUTION:) Proceeding as before, $I_B = \frac{I_E}{\beta_F + 1} = \frac{1.0}{24 + 1} = 0.066mA$

and then $I_C = I_E - I_B = 1.65 - 0.066 = 1.584mA$

Then we can find V_C, and V_{CE}, as

$$V_C = V_+ - I_C R_C = 10 - (5 \times 0.1.584) = 2.08$$

$$V_{CE} = V_C - V_E = 2.08 - 3.3 = -1.22V \quad ???!!$$

Wups! There is no way that V_E can be at a higher voltage than V_C!

So what is wrong? Well, it seems that there was a little precondition that was assumed, namely that the transistor was operating in the active mode. In the active mode the BE junction is forward biased and the BC is reverse–biased. In this case for which $R_E = 2.0$ kΩ .the transistor is left with *both* junction forward biased and there is no way that it could be in the active mode.

So for this case the control equation (10.2-3) is no longer valid and we cannot use either it or (10.2-4).

This shadow example makes the point that the transistor must be consistent with other elements in the circuit, and they can push the transistor into a mode for which the simplicity of equation (10.2-3) is wrecked. Courtesy of the graphical representation for the characteristics and V_{CE} = low we should realize that the BJT is tipped into a non-linear mode of operation.

We can assume a default of V_{CE}(min), usually elected as = 0.3V. Analysis thereto will realize an I_C = 1.28mA. But this option is a relatively useless exercise and a better use of time would be to undertake a bias-frame redesign. The BJT is intended to operate in the active mode if we are to take advantage of its control properties.

Keep in mind that we always (1) assume that the transistor is in the active mode. And if (2) this assumption fails, then the transistor is in a saturated (non-active) mode of operation and redesign is in order. It is a two-step process. If the transistor is biased correctly then the second step is unnecessary.

Now that we have tortured the transistor by assertion of an unreliable and incorrect bias option we might concede that more control of the base bias V_B will be accomplished by means of a voltage divider between voltage rails as shown by figure 10.3-3.

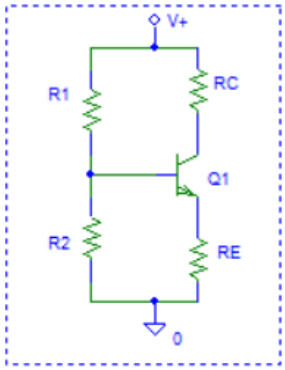


Figure 10.3-3. Four-resistor bias frame for the BJT.

The two resistors R_1 and R_2 form a voltage divider and which can be analytically simplified by its Thevenin equivalent shown by figure 10.3-4

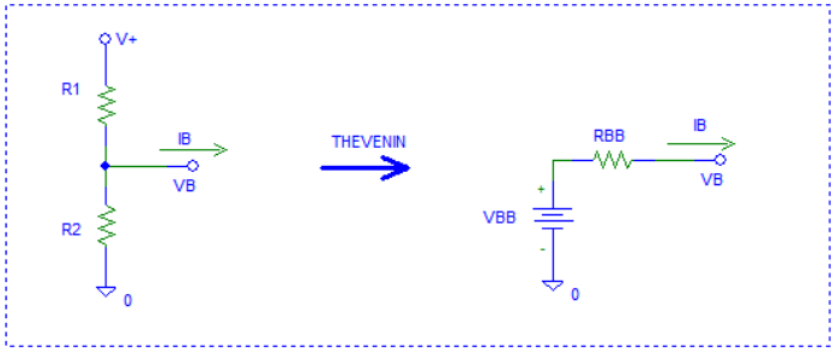


Figure 10.3-4. Thevenin equivalent voltage source to voltage divider

Fond memories of Thevenin equivalent analysis gives values for figure 10.3-4 of the form

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_+ \qquad R_{BB} = R_1 || R_2 \qquad (10.3\text{-}2)$$

The equivalent circuit for figure 10.3-3 is then of the form of figure 10.3-5.

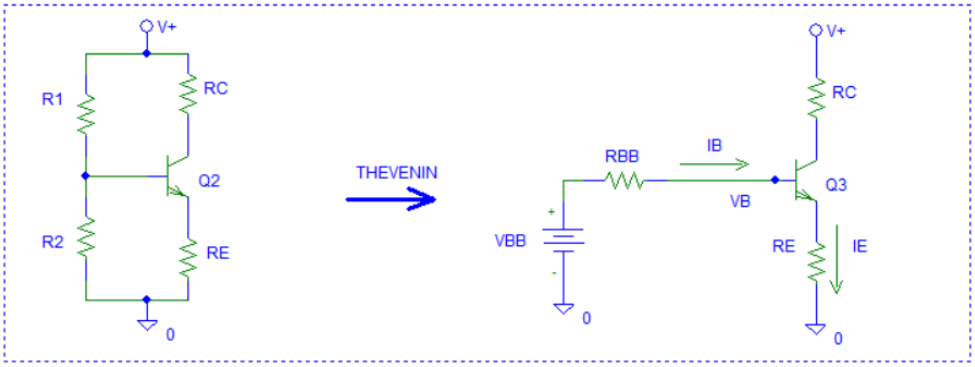


Figure 10.3-5 Thevenin equivalent to 4-resistance bias network for the *npn* BJT

for which V_{BB} is relative to the lower rail. Using KVL gives

$$(V_{BB} - V_{GND}) - I_B R_{BB} - V_{BE} - I_E R_E = 0$$

Once again it is assumed that the BJT is in the active mode. Turning the crank on the algebra we get

$$I_B = \frac{(V_{BB} - V_{GND}) - V_{BE}}{R_{BB} + (\beta_F + 1)R_E} \qquad (10.3\text{-}3)$$

If the lower rail is not at GND but at V_{EE} then it is in order to replace V_{GND} by V_{EE}.

We might note that if we bias a *pnp* transistor using the 4-resistance frame, as indicated by figure 10.3-6, then we have practically the same result as equation (10.3-3) for the base current I_B,

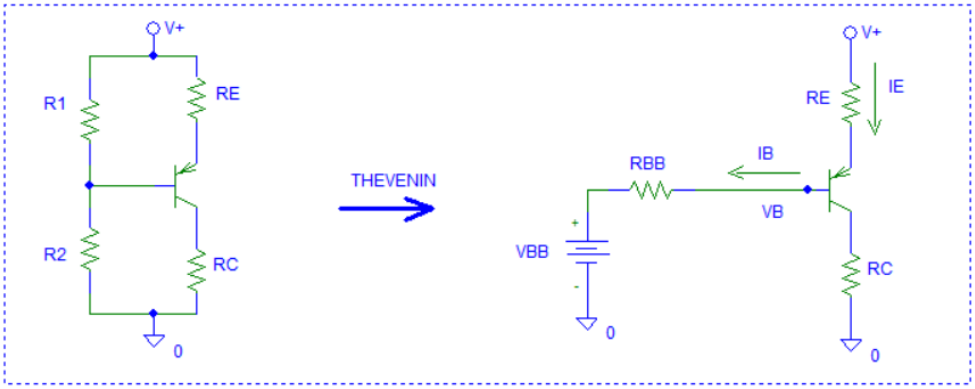


Figure 10.3-6 Thevenin equivalent representation for 4-resistance bias of *pnp* BJT

for which the recipe form will be

$$I_B = \frac{(V_{BB} - V_{EE}) - V_{BE}}{R_{BB} + (\beta_F + 1)R_E} \qquad (10.3\text{-}3)$$

In this instance, $V_{BE} = -0.7$ V since the *pnp* voltage biases and current flows are *opposite* to those for the *npn* transistor. If you check all of the signs, everything works out OK. Note that in this instance $V_{EE} = V_+$. For the *npn* transistor it is not uncommon for $V_{EE} = V_{GND} = 0$.

Let us consider an example:

EXAMPLE 10.3-3: Four–resistance bias frame. Determine the operating point.

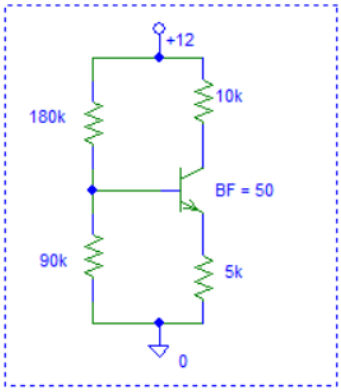


Figure E10.3-2. Example analysis of a 4-resistance bias frame for the BJT

SOLUTION: The voltage-divider attached to the base consists of resistances R_1 and R_2. Its Thevenin equivalent will have electrical characteristics

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_+ = \frac{90}{270} \times 12 \qquad = 4.0\text{V} \quad , \qquad R_{BB} = R_1 || R_2 \qquad = 180||90 \qquad = 60\text{k}\Omega$$

as reflected by equation (10.3-2). It is to your great advantage to do the mathematics by inspection, even if the results are a little sloppy.

Now, applying these numbers to the algebraic analysis culminated in equation (10.3-3), we get

$$I_B = \frac{(V_{BB} - V_{EE}) - V_{BE}}{R_{BB} + (\beta_F + 1)R_E} = \frac{(4.0 - 0) - 0.7}{60 + (50 + 1)5} \qquad = \mathbf{.0105mA}$$

Then we will find that

$$I_C = \beta_F I_B \qquad = 50 \times .0106 \qquad = \mathbf{0.523mA}$$

From the knowledge of I_C we can determine V_C and V_E:

$$V_C = V_+ - I_C R_C \qquad = 12 - 0.523 \times 10 \qquad = 6.76\text{V}$$

$$V_E = V_{EE} + I_E R_E \qquad = 0 + (0.523 + .0105) \times 5 \qquad = 2.67\text{V}$$

Then the output bias voltage V_{CE} is:

$$V_{CE} = V_C - V_E \qquad = 6.76 - 2.67 \qquad = \mathbf{4.09V}$$

And therefore the operating point is $(I_B, I_C, V_{CE}) \cong (0.105, 0.523, 4.09)$

As a reminder, these values are not exact. Even an educated guesstimate is not invalid, provided that you trek through the analysis mathematics at least once.

In example 10.3-2, note that $V_{CE} \cong 4.0$ V or $\cong 1/3\ V_+$. This is a reasonably good design, the criterion being that a V_{CE} of 1/3 of the voltage difference between the upper and lower supply rails. With this choice the swing space of the output signal will have margins which are sufficient to keep distortion reasonably low. Distortion analysis belongs to pspice or some other circuit simulation platform, but otherwise you may accept this criterion as good medical practice.

In this respect it is evident that when R_C is large the node voltage at V_C may be pushed down to a level for which the (*npn*) transistor is not in the active regime. Then neither the recipe equation (10.3-3) nor any of the rest of the electrical facts are valid.

For example, if $R_C = 20\ k\Omega$, then

$$V_C = V_+ - I_C R_C \qquad = 12 - 0.523 \times 20 \qquad = 1.35V$$

which is impossible! There is no way that V_C can be less than V_E. The transistor has been driven into saturation.

And although it is reasonably straightforward to determine an (approximate) operating point for a transistor in saturation via a default $V_{CE}(sat) = 0.3V$, this is a waste of time. If the transistor proves to not be in the active mode, we drop back and punt.

Consequently, whenever we assess a transistor circuit, we always make a snake check to affirm that it is in the active mode. The flag is the magnitude of V_{CE}, or better yet, the value of V_C relative to V_B, inasmuch as it is the bias V_{BC} that identifies whether–or–not the BC junction is in reverse bias as is required for the active mode.

This same process was introduced in Chapter 9 (*pn* junction), where we made an assumption about the operating state of the device. And then let an analysis confirm that it was true, - or not.

It is worthwhile to again acknowledge that rough analysis is adequate for performance assessments and design decisions, with follow-on by simulations for more refinement if needed.

In regard to estimates for circuits that include the BJT it is appropriate to acknowledge that β_F is usually sufficiently large so that a decent estimate of the current carried by the transistor can be accomplished via the approximation $V_B \cong V_{BB}$ and debiasing resistance R_E.
If β_F is large then $I_B \to 0$ and

$$\therefore \qquad I_C \cong I_E \cong \frac{V_{BB} - V_{BE} - V_{EE}}{R_E} \qquad (10.3\text{-}4)$$

Using this approximation on example 10.3-2

$$I_C \cong I_E \cong \frac{(V_{BB} - V_{EE}) - V_{BE}}{R_E} = \frac{4 - 0.7}{5} \qquad = \qquad 0.66\text{mA}$$

Compared to the answer ($I_C = 0.523$mA) using $\beta_F = 50$ the two values are not inconsistent with one another by a margin of approximately 25%.

Usually β_F is much larger than 50 For instance, if in example 10.3-2 we had let $\beta_F = 200$ we would have obtained a $I_C = 0.62$ mA, not much different than that for the quick rough analysis.

It is also worthwhile to take a look at a sister example for which we bias a *pnp* transistor. Consider the circuit represented by figure E10.3-3

EXAMPLE 10.3-3: Four–resistance bias frame, *pnp* transistor. Determine the operating point.

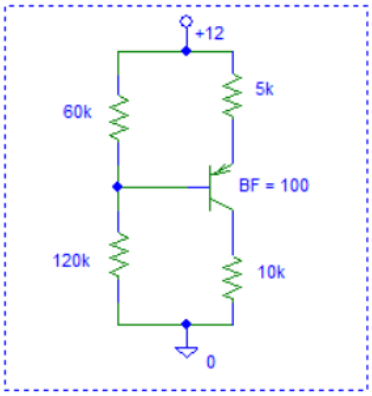


Figure E10.3-3. Four–resistor bias network with *pnp* transistor.

SOLUTION: Thevenin equivalent values for the R_1, R_2 string are evaluated as for any voltage divider:

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_+ = \frac{120}{180} \times 12 \qquad = 8.0\text{V} \quad , \qquad R_{BB} = R_1 || R_2 \qquad = 60 || 120 \qquad = 40\text{k}\Omega$$

(Once again: Do this analysis by inspection). Then apply the values to equation (10.3-4), for which

$$I_B = \frac{(V_{BB} - V_{EE}) - V_{BE}}{R_{BB} + (\beta_F + 1)R_E} = \frac{(8-12)-(-0.7)}{40 + (100+1)5} \quad = \underline{\textbf{-.00606mA}}$$

The negative sign indicates that the current is flowing out of the base, just like it is supposed to do. Taking this magnitude for I_B we get I_C and V_C and V_E, as follows:

$I_C = \beta_F I_B$ = 100 × (-.00606) = **- 0.606mA**

$V_C = |I_C|R_C$ = 0.606 × 10 = 6.06V

$V_E = V_{EE} - |I_E|R_E$ = 12 – (0.606+.0061) × 5 = 8.94 V

From which we find that V_{CE} will be

$V_{CE} = V_C - V_E$ = 6.06 – 8.94 = **-2.88V**

As expected, the polarity of this bias voltage is *opposite* to that for the *npn* transistor. The operating point Is then

(I_B, I_C, V_{CE}) = (**- 0.0061mA, -0.606mA, - 2.88V**)

An educated guesstimate is also valid provided that a grind trek through the (*pnp*) analysis mathematics is undertaken at least once. Using $V_{BB} - V_+ = -3.3$V the quick sloppy value of I_C would be -0.66mA.

10.4 SMALL–SIGNAL ASSESSMENT OF THE BJT and BIAS CONSIDERATIONS

Once the transistor is biased into an active state then it will control the output by applying a modulation to the input voltage and thereby end up modulating the output current I_C. We expect that the modulations are of sufficiently small amplitude so that equations (10.1-1) and (10.1-2) will be appropriate, with changes in subscripts to reflect that we are using a BJT, i.e.

$$i_C = g_m v_{BE} \qquad (10.4\text{-}1)$$

And for use of the transistor as a signal amplifier we must be equipped with the transconductance, g_m.

In order to determine the g_m indicated by equation (10.1-3a), it is necessary to identify a model for current I_C vs input bias V_{BE} . This requirement may be accomplished by means of a circuit model consistent with the BJT emitter-collector action, and one such is represented by figure 10.4-1.

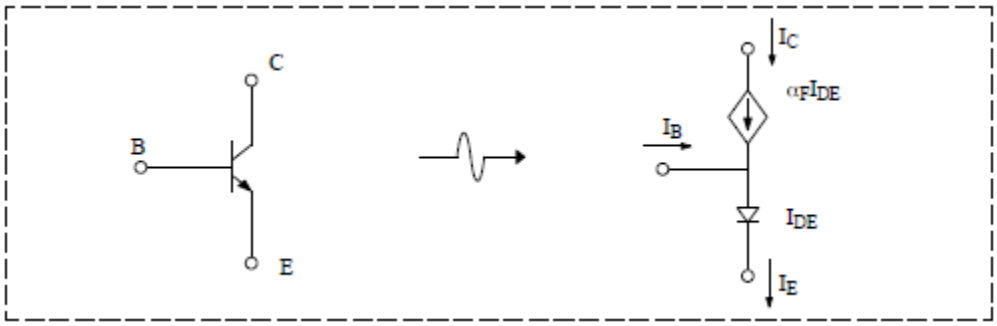


Figure 10.4–1: Circuit model for (*npn*) BJT

Figure 10.4-1 identifies that I_C is controlled by junction bias V_{BE} with analytical dependence

$$I_C = \alpha_F I_{DE}\left(e^{V_{VE}/V_T} - 1\right) \qquad (10.4\text{-}2)$$

This equation is also consistent with equation (10.2-2), for which coefficient α_F covers the efficiency context of the emitter–collector process and coefficient I_{DE} covers almost all aspects of the junction.

A more comprehensive model, the *Ebers–Moll model*, is represented by figure 10.4-2 and will accommodate the BJT in other options besides the active mode.

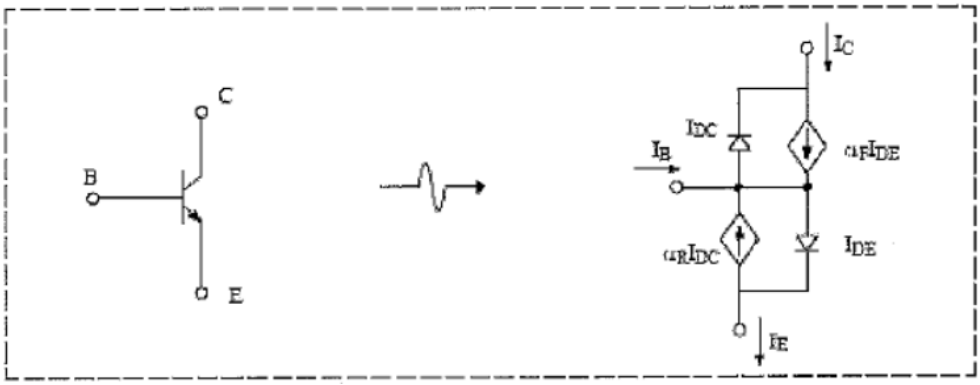


Figure 10.4-2: Ebers-Moll circuit model for the (*npn*) BJT

The parameter α_R is associated with efficiency of the emitter-collector process for the inverted BJT. The inverted mode is not usually as efficient as the forward emitter–collector process and so β_R typically is only about 0.5 (compared to 100 for β_F). The subscripts now take on the context of forward and reverse and this nomenclature is reflected by the listings of pspice BJT parameters.

The model represented by figure 10.4-1 and equation (10.4-2) is adequate for most back-of-the-envelope analyses. The more comprehensive device model is only in context of the parameter files employed by the circuit simulation software. Otherwise

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{\partial}{\partial V_{BE}}\left[\alpha_F I_{DE}\left(e^{V_{VE}/V_T} - 1\right)\right] \qquad = \frac{1}{V_T}\left[\alpha_F I_{DE} e^{V_{VE}/V_T}\right] \qquad \cong \frac{I_C}{V_T}$$

And therefore we adopt

$$g_m = \frac{I_C}{V_T} \qquad \cong \frac{I_C}{.025} \qquad = 40 I_C \qquad (10.4\text{-}3)$$

As has been noted earlier the thermal voltage $V_T \cong .025\text{V}$ assuming $T \cong 300\text{K}$. Equation (10.4-3) is taken as a benchmark for circuits that use the BJT for the signal transfer component.

Equation (10.4-3) also tells us that the operating point value of $I \cong I_C$ is all that is needed to determine the transconductance g_m unless we get crazy and operate at a wildly different temperatures than the norm.

Equation (10.4-3) shows that the transfer strength g_m is defined by the current through the transistor. So it is of some advantage and simplification to bias a transistor with a resistance frame which uses a current source, as shown by figure 10.4-3.

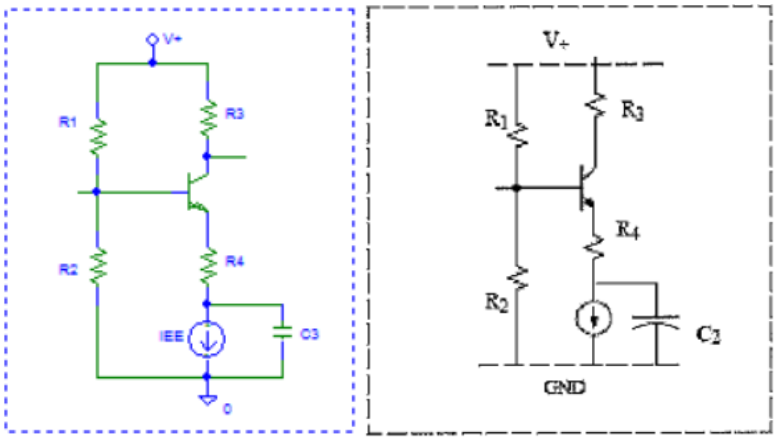


Figure 10.4-3. Bias network for a transistor using a current source to define operating point.

The bias frame shown by figure 10.4-3 also includes a *bypass* capacitance, C_2. Take note that C_2 has no effect on the operating point. Later in the analysis life it will serve as a bypass path for signals. Transistor circuits will always have capacitances located in and around the transistor to serve as signal conduits. Otherwise they may be ignored in the evaluation of the operating point.

Consider the following example:

EXAMPLE 10.4-1: Analysis of a BJT bias frame with current source. Determine the operating point.

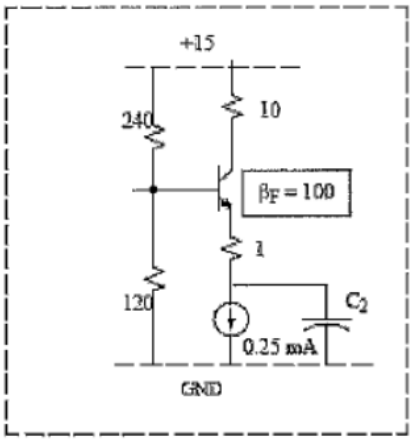


Figure E10.4-1 Example of *npn* transistor biased by a current source. (As a convention) all resistances are in kΩ and the current source is in mA.

SOLUTION: Since I_E is fixed by the current source the operating point is almost already specified. Assuming that the transistor is in the active mode then

$$I_B = \frac{I_E}{(\beta_F + 1)} \qquad \cong \frac{I}{\beta_F} = \frac{0.25}{100} \qquad = \underline{\textbf{.0025mA}}$$

As long as we are being quick and rough with the mathematics we might as well identify that

$$I_C \cong I_E = I(\text{current source}) \qquad = \underline{\textbf{0.25mA}}$$

so we can determine V_C by

$$V_C = V_+ - I_C R_C \qquad \cong 15 - 0.25 \times 10 \qquad = 12.5\text{V}$$

The node voltage at the emitter is given by

$$V_E = V_B - V_{BE} \cong (V_{BB} - I_B R_{BB}) - 0.7$$

And so we need to find V_{BB} and R_{BB}. And by inspection they are

$$V_{BB} = 5.0\text{V} \quad , \quad R_{BB} = 120 \| 240 \qquad = 80\text{k}\Omega$$

$$V_B = (V_{BB} - I_B R_{BB}) = 5.0 - 80 \times .0025 \qquad = 4.8\text{V}$$

And V_E is just one junction difference away from this value and so

$V_E = V_B - 0.7$ $= 4.8 - 0.7$ $= 4.1\text{v}$

so that V_{CE} is

$V_{CE} = V_C - V_E$ $= 12.5 - 4.1$ $= \underline{\mathbf{8.4V}}$

The operating point is then $(I_B, I_C, V_{CE}) = (0.0025\text{mA}, 0.25\text{mA}, 8.4\text{V})$

In the previous example we do NOT use the treasured recipe equation (10.3-3). It does not apply inasmuch as we have no idea what voltage will fall across the current source.

10.5 SMALL–SIGNAL EQUIVALENT MODEL OF THE BJT

If we use equation (10.4-3) as a guide, then for small signals the transistor can be conceptually replaced by a linear dependent current source like that indicated by figure 10.5-1

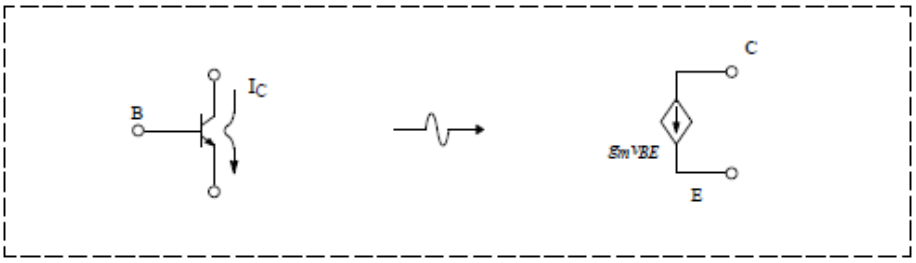


Figure 10.5-1. Ideal small–signal equivalent of the BJT. (Actually a little too ideal).

Don't get too attached to figure 10.5-1 inasmuch as the model is a little too ideal. From I-V_{CE} characteristics represented so far we know that the output terminal at C must have a finite output resistance/conductance. And we know that the model must include a finite resistance at node B since there is a finite base current I_B. These node resistances are represented and included by means of the hybrid-pi model of figure 10.5-2.

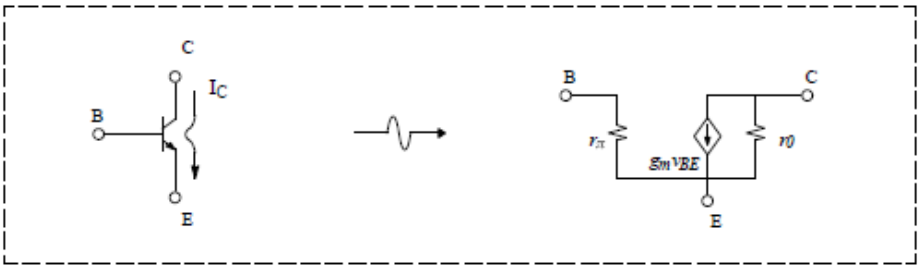


Figure 10.5-2. Hybrid-pi small–signal equivalent model of the BJT

The finite input resistance is a natural consequence of the junction since

$$I_B = \frac{I_C}{\beta_F} = \frac{1}{\beta_F}\left[I_{SC}\left(e^{V_{BE}/V_T} - 1\right)\right]$$

And therefore the slope at the input to node B is

$$\frac{\partial I_B}{\partial V_{BE}} = \frac{1}{\beta_F}\frac{\partial I_C}{\partial V_{BE}} = \frac{g_m}{\beta_F}$$

for which we identify a slope parameter

$$g_\pi = \frac{\partial I_B}{\partial V_{BE}} = \frac{g_m}{\beta_F}$$

and for which $r_\pi = 1/g_\pi$ is indicated by figure 10.5-2.

Output conductance g_0 is a consequence of the increase of I_C with respect to V_{CE}, as represented by figure 10.5-3 and the finite slope thereto.

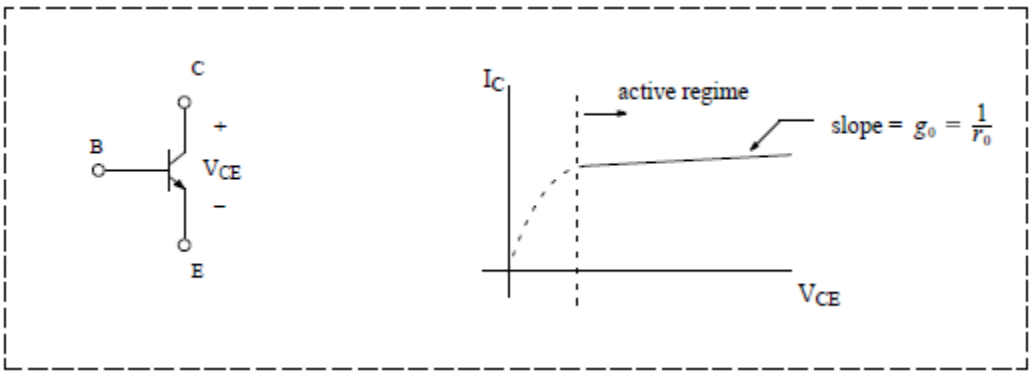


Figure 10.5-3 Output conductance and the Early effect.

This same context was identified in section 10.1. The output slope for the BJT is of the form

$$g_0 = \frac{\partial I_C}{\partial V_{CE}}$$

consistent with equation (10.1–3). By analyzing the operation of the emitter–collector processes and the junction depletion regions, the slope can also be shown to be proportional to the current I_C. This analysis was done so in some of the initial studies of the properties of the BJT by James M. Early and he reduced it to the form

$$g_0 = \frac{I_C}{V_A} \qquad (10.5\text{-}2)$$

where V_A is now called the *Early voltage*. The value of V_A is dependent upon transistor layer thicknesses and doping profiles. Typically it is about 50 - 100V.

The phenomenon is called the *Early effect.* James Early died in 1988 and so maybe it should now be called the 'late' Early effect.

Whenever a small–signal analysis is undertaken the hybrid–pi model is the model of choice for circuits that include BJTs..

The *pnp* transistor has exactly the same model and same directions of small–signal current as the *npn* transistor. This is to be expected since all of the polarities are flipped and so ratios will then all be of same polarity regardless of gender.

Figure 10.5-4. The small–signal model is the same for the *pnp* transistor as for the *npn* transistor

The hybrid-pi model may also be represented by means of a Norton equivalent form as represented by figure 10.5-5. The Norton form emphasizes the context of the BJT as a current-controlled transducer (CCT) defined by forward current gain β_F for which

$$i_C = g_m v_{BE} \qquad = (\beta_F g_\pi)\, v_{BE} \qquad = \beta_F\, (g_\pi v_{BE}) \qquad = \beta_F\, i_B$$

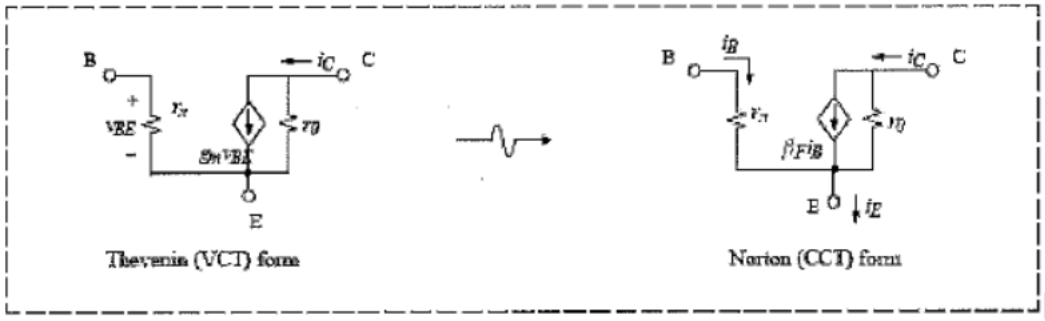


Figure 10.5-5. Options with the hybrid-pi model

As might be expected the CCT relationships of the small-signal model follow those of the macroscopic levels for I_E, I_C, and I_B, i.e.

$$i_C = \beta_F i_B \qquad\qquad i_E = (\beta_F + 1)\, i_B$$

And as a re-emphasis on nomenclature, the use of lower–case symbols for current, voltage, resistance and conductance all identify with the small-signal context of the circuit.

10.6 SINGLE-TRANSISTOR TOPOLOGIES with the BJT: THE COMMON–EMITTER CONFIGURATION

If a transistor is to be used as a signal transducer (a.k.a. amplifier element) it needs to be biased at an operating point for which it is in its forward active mode. It can then be translated into an equivalent, linear, small-increment (a.k.a. small-signal) model of the form(s) given by figure 10.5-5. The next step is to assess the basic circuit topologies and reformate them in terms of stages and building blocks.

The most direct single-transistor topology using BJTs is the one for which the control node is at the base and the controlled node is at the collector. The emitter is a shared (common) node. So the topology is designated as the common-emitter (CE) configuration and is shown by figure 10.6-1.

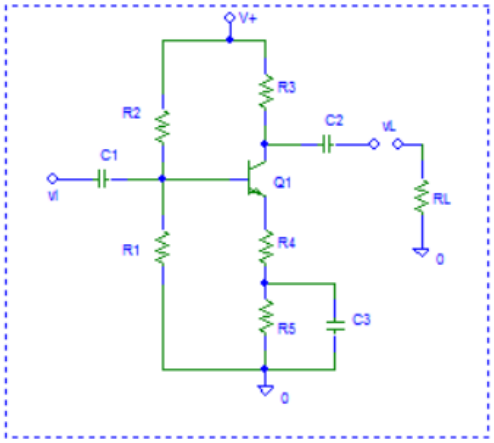


Figure 10.6-1. Common-emitter topology using an *npn* transistor. Small-signal input and output voltages are indicated by lower case symbols.

The CE topology is one for which the (input) signal v_I is passed to the base node through (input) capacitance C_1 and the output signal is passed to the load R_L from the collector node through (output) capacitance C_3. Since signals are time-varying, the capacitances serve as a low-impedance shunt paths for signals. Relative to the steady-state analysis the input and output capacitances are an open-circuit (high resistance) path, and hence leave the operating point analysis untouched.

As a re-emphasis on nomenclature, small-signal rms amplitudes are designated by lower case. Subscripts also have context. As represented by figure 10.6-1 v_L is the rms voltage amplitude across load R_L. If there is no load then the output would be designated as v_O (as in open).

In the topology of figure 10.6-1 it is necessary to acknowledge that capacitance C_2 serves to bypass resistance $R_{E2} = R_5$ in the emitter leg. Therefore only resistance $R_{E1} = R_4$ will contribute to the small signal topology. The only context which needs to acknowledge the entire resistance in the emitter leg, $R_E = R_4 + R_5$, will be for the operating point analysis, NOT the signal analysis.

For small-signal analysis the topology of figure 10.5-1 must be translated into a small–signal equivalent form using the transistor small-signal (hybrid-pi) model of figure 10.5-5. In making this equivalence it is in order to let the voltage rails be ideal voltage sources, in which case they have internal resistance ≅ 0. And so as far as a time-varying signal is concerned no signal appear across this zero resistance and the voltage rails have zero signal difference between them. In the translation to small-signal equivalent topology the voltage rails can then be treated as if they are a common rail and euphemistically renamed as an 'AC ground'. The small-signal equivalent topology then becomes considerably simpler than its physical topology as represented by figure 10.6-2:

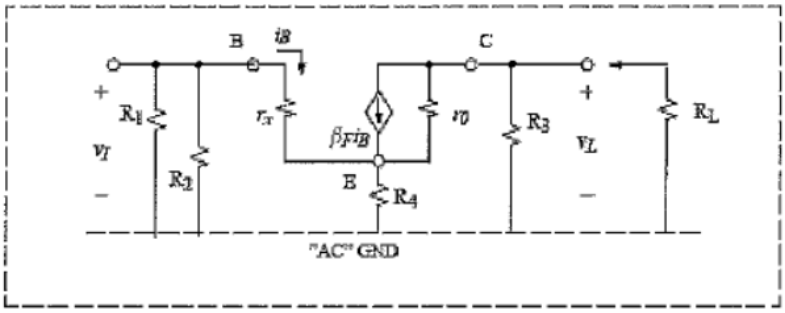


Figure 10.6-2. Two-port small-signal equivalent circuit to figure 10.6-1. The voltage rails have collapsed to a single 'AC' signal ground.

Also take note that the small-signal equivalent circuit does not show $R_{E2} = R_5$ because signals are shunted around it by capacitance C_2.

If we should want to abuse the simplicity of figure 10.6-2 then admittance paths due to the capacitances can be included. But it is best to let frequency context wait its turn. For now it is sufficient to assume that the signal frequencies are large and that the capacitances are sufficiently large so that they serve little function other than to shunt the signals to and around the physical nodes of the topology.

As a final simplification the topology is reduce to a building block characterized by input and output impedances R_{in} and R_{out} and a transfer function. The transfer function of choice is usually that of the voltage-voltage transducer (VVT).

The recipe is:

Find operating point: (I_B, I_C, V_{BE}) by equilibrium (DC) analysis. If the circuit is not in the active mode –punt (and redesign, if you are the designer.)	Find the small–signal parameters: For the BJT they are: (g_m, r_π, r_0) Construct small–signal equivalent circuit, analyze linear network	Find the two–port characteristics: $\left(R_{in}, R_{out}, \frac{v_L}{v_I}\right)$ We may find it easier to find some other transfer function besides v_L/v_I

In most cases it is not necessary to undertake the second part of step 2 since many of the single-transistor configurations have been worked over by many generations of EE students.

For the CE topology, we can best assess the circuit by making a minor approximation. We know that the resistance r_0 is large and therefore will make only a negligible contribution to currents in the emitter and the collector. Neglecting this small current, we can assess the signal voltage at node B (figure 10.6-2) by

$$v_B = i_B r_\pi + i_E R_4 \qquad = i_B r_\pi + (\beta_F + 1)\, i_B R_4$$

Therefore the resistance 'looking into' the base of the BJT transistor is

$$R_{iB} = \frac{v_B}{i_B} \qquad = r_\pi + (\beta_F + 1)\, R_4 \tag{10.6-1}$$

and is usually denoted as R_{iB}. The input resistance of the CE topology is then the paralleled set of resistances R_1, R_2, and R_{iB} (see figure 10.6-2) so that

$$R_{in} = R_1 || R_2 || R_{iB} \tag{10.6-2}$$

It is worthwhile to note that the resistance R_{iB} 'looking into' the base will 'see' resistance R_4 in the emitter leg multiplied by the factor $(\beta_F + 1)$. This factor is a benchmark inasmuch as emitter current is always $(\beta_F + 1)$ times that of the base current. The effect is therefore sometimes called 'emitter multiplication'.

Euphemistically it is also convenient to analyze the circuit from the point of view of the free charge carriers as they cruise the conductive thoroughfares within the network. In this case the charge carriers will 'see' the emitter multiplication effect as they flow into the base of the BJT. And consequently the same multiplication effect is true whether for *npn* or *pnp* transistors.

The collector of the transistor is a relatively stiff node in its own right but in the CE topology has an even stiffer resistance 'looking into' the collector, of magnitude

$$r_{out} = r_0 \left(\frac{r_\pi + (\beta_F + 1) R_4}{r_\pi + R_4} \right) \tag{10.6-3}$$

This result can be obtained by nodal analysis at the collector as represented by figure 10.6-3. Take note that any assessment of signal resistances at the output node requires that the input signal $v_I = 0$.

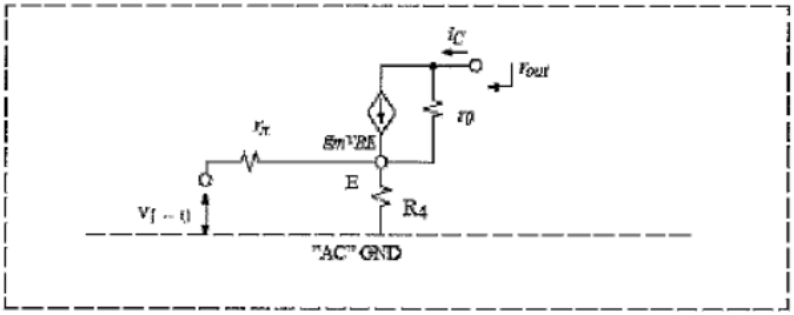


Figure 10.6-3 Assessment of the output resistance at the stiff node of the BJT.

Then nodal analysis at node v_C

$$i_C = g_m v_{BE} + v_C g_0 - v_E g_0 \quad = g_m(-v_E) + v_C g_0 - v_E g_0 \quad = v_C g_0 - v_E(g_m + g_0)$$

and at node E

$$0 = v_E(g_\pi + g_0 + G_4) - g_0 v_C - g_m v_{BE} \quad = v_E(g_\pi + g_m + G_4 + g_0) - g_0 v_C$$

The two equations can be simplified by neglecting g_0 when it is additive to g_π and g_m. Then

$$0 = v_E[(\beta_F + 1)g_\pi + G_4] - v_C g_0$$

$$i_C = -v_E g_m + v_C g_0$$

If v_E is eliminated between these two equations then

$$\frac{v_C}{i_C} = \frac{1}{g_0}\left(\frac{(\beta_F + 1)g_\pi + G_4}{g_\pi + G_4}\right)$$

which is the same as equation (10.6-3) if we multiply numerator and denominator by $r_\pi R_4$.

This algebraic exercise was entertaining but not one that we need to claim as SOP (standard operating procedure). Sometimes it is better to 'believe' rather than crawl through the process.

The output resistance is the set of resistances at the output node of the small-signal circuit and they are R_3 and r_{out} with common node v_C. Therefore the output resistance is

$$R_{out} = R_3 \,||\, r_{out} \qquad (10.6\text{-}4)$$

The resistance r_{out} also can be identified as that 'looking into' the collector. We might note that r_{out} also includes an emitter multiplication factor. In effect the emitter resistance $R_4 = R_{E1}$ induces a feedback effect that is reflected back to the other nodes when the transistor is in situ.

The voltage transfer function (a.k.a. voltage gain) may be obtained from

$$v_L = -i_C R_3 || R_L$$

But since $i_C = \beta_F i_B$, and since $i_B = v_B/R_{iB}$ then

$$v_L = = -\beta_F i_B \times R_3 \,||\, R_L \qquad = -\beta_F \left(\frac{v_B}{R_{iB}} \right) \times R_3 \,||\, R_L$$

Since $v_B = v_I$ and applying equation (10.6-1) gives

$$A_V = \frac{v_L}{v_I} = -\frac{\beta_F R_3 \,||\, R_L}{r_\pi + (\beta_F + 1) R_4} \tag{10.6-5}$$

Equations (10.6-1) thru (10.6-5) fulfill the recipe of the characteristics of the CE topology as a two–port network. But the degree of accuracy which they reflect is more than can be justified with the variations and approximations which accompany transistor devices. So it is in order to allow a few extra approximations and reduce the overhead.

Take note that r_{out} is typically much larger than R_3, on the order of MΩ whereas R_3 is typically on the order of kΩ. Consequently it is not a bad approximation to approximate R_{out} by

$$R_{out} \cong R_3 \tag{10.6-6}$$

Equation (10.6-5) can also be much simplified by dividing numerator and denominator by (β_F + 1), for which

$$\frac{v_L}{v_I} = -\frac{\beta_F / (\beta_F + 1) R_3 \,||\, R_L}{r_\pi / (\beta_F + 1) + R_4}$$

If β_F is assumed to be large then more approximations can be applied, i.e.

$$\frac{\beta_F}{\beta_F + 1} \cong 1 \qquad \text{and} \qquad \frac{r_\pi}{\beta_F + 1} \cong \frac{r_\pi}{\beta_F} = \frac{1}{g_m}$$

Then

$$\frac{v_L}{v_I} \cong \frac{-R_3 \,||\, R_L}{1/g_m + R_4} \qquad (10.6\text{-}7)$$

If we have a very strong transistor with g_m = large, the voltage transfer gain A_V reduces to

$$\frac{v_L}{v_I} = \frac{-R_3 \,||\, R_L}{R_4}$$

Equations (10.6-6) and (10.6-7) are usually accurate to within about 1–2%. Any further refinements might better be handed off to your friendly neighborhood circuit simulator.

In addition to these approximations it may also be of benefit to revisit equation (10.6-1) and apply the same approximations. Then

$$R_{iB} = r_\pi + (\beta_F + 1)\, R_4 \qquad = \beta_F / g_m + (\beta_F + 1) R_4 \qquad \cong \beta_F (1/g_m + R_4) \qquad (10.6\text{-}8)$$

Consider an example:

EXAMPLE 10.6-1: Analyze the following circuit topology and determine its two–port transfer characteristics (R_{in}, R_{out}, v_L/v_I)

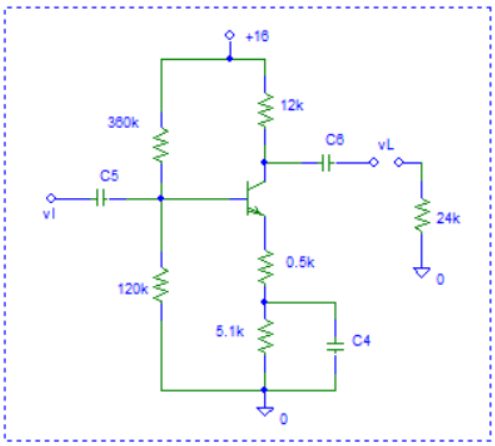


Figure E10.6-1. Resistances are in kΩ and capacitances C_1, C_2, C_3 are all assumed to be large.

SOLUTION: We have a 4–resistance bias network with the emitter resistance split into R_4 and R_5. The debiasing resistance in the emitter leg is therefore

$$R_E = R_4 + R_5 = 0.5 + 5.1 = 5.6\text{k}\Omega$$

The voltage-divider at the front end has Thevenin equivalents (by inspection)

V_{BB} = 4.0V $\qquad$ R_{BB} = 360 || 120 = 90kΩ

The base current I_B is then

$$I_B = \frac{V_{BB} - V_{BE} - V_{EE}}{R_{BB} + (\beta_F + 1)R_E} = \frac{4 - 0.7}{90 + (100 + 1) \times 5.6}. \qquad = .00503\text{mA}$$

For which

I_C = 100 ×.00503mA $\qquad$ = 0.503mA

As a snake-check, we should also find V_C, V_E and V_{CE} to confirm that the BJT is in active mode

$V_C = V_+ - I_C R_C \qquad = 16 - 0.5 \times 12 \qquad = 9.93\text{V}$

$V_E = V_{EE} + I_E R_E \qquad \cong\ 0.503 \times 5.6 \qquad = 2.85\text{V}$

for which $\qquad V_{CE} = 9.93 - 2.85 = 7.08$ V .

Also note that $V_C > V_{BB}$ which assures that the BC junction is reverse–biased and therefore confirms twice over that the BJT is in the active regime.

The operating point (I_B,I_C, V_{CE}) is the source of the equilibrium information needed to determine small-signal parameters g_m, r_π and r_0 as follows:

From equations (10.4-3), (10.5-1) and (10.5-2) and $I_C \cong 0.5$mA

$$g_m = \frac{I_C}{V_T} \qquad \cong \frac{I_C}{.025} \qquad = 40 I_C \qquad = \underline{\textbf{20mA/V}} \qquad \text{from} \quad (10.4\text{-}3)$$

$$g_\pi = \frac{g_m}{\beta_F} \qquad = \frac{20}{100} \qquad = 0.2\text{mA/V} \quad \text{or} \quad r_\pi = 1/g_\pi \ = \underline{\textbf{5.0kΩ}}$$

$$g_0 = \frac{I_C}{V_A} \qquad = \frac{0.5}{100} \qquad = 0.005\text{mA/V} \quad \text{or} \quad r_0 = 1/g_0 \ = \underline{\textbf{200kΩ}}$$

For the assessment of the two-port characteristics, start by determining R_{iB}, using either equation (10.6-1) or equation (10.6-8):

R_{iB} = 5.0 + (100+1) × 0.5 $\qquad$ = 55.5kΩ

from which (equation (10.6-2)),

R_{in} = 360||120||55.5 $\qquad$ = <u>**34.3 kΩ**</u>

We also can find r_{out}, using equation (10.6-3), for which

$$r_{out} = r_0\left(\frac{r_\pi + (\beta_F + 1)R_4}{r_\pi + R_4}\right) = 200\times\left(\frac{5 + (101)\times 0.5}{5 + 0.5}\right) \qquad = 2018\ \text{k}\Omega$$

The output resistance is then

$$R_{out} = R_3 \,||\, r_{out} \qquad = 12 \,||\, 2018 \qquad = \underline{\textbf{11.93 k}\Omega}$$

This value confirms that the approximation $R_{out} = R_3 = 12\text{k}\Omega$ would have been very legitimate as well as much less overhead (i.e. forget about the labor of determining r_{out}).

In that respect a comparison between equations (10.6-5) and (10.6-7) is also in order. If we use equation (10.6-5) then

$$A_V = \frac{v_L}{v_I} = -\frac{\beta_F R_3 \,||\, R_L}{r_\pi + (\beta_F + 1)R_4} \qquad = -\frac{100\times 12\,||\,24}{55.5} \qquad = \underline{\textbf{14.4V/V}}$$

Note that the denominator is the same as $R_{iB.}$.

If we use equation (10.6–7) to find A_V, we get

$$\frac{v_L}{v_I} = \frac{-R_3 \,||\, R_L}{1/g_m + R_4} = \frac{-12\,||\,24}{1/20 + 0.5} \qquad = \underline{\textbf{14.5V/V}}$$

which is hardly a nickel's worth of difference, and so we might as well use the simpler option.

Most of this analysis is of sufficient simplicity to be achieved by inspection. And otherwise let any refinements be passed along to the circuit simulation utility.

Example 10.6-1 expended much overhead in evaluating the operating point. Much of this overhead can be omitted by the use of a current source to replace R_5 as represented by figure 10.6-2.

The operational advantage to use of a current source for bias of the transistor is that the operating current is independent of any bias shift of the operating point due to the signal swing. Consequently the circuit will be less afflicted by the non-linear characteristics of the transistor and produce a signal output with less bias-frame distortion.

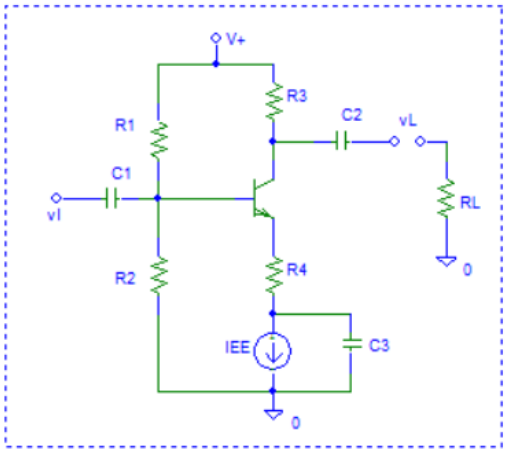


Figure 10.6-2 Common–emitter topology using a current–source.

Bias current $I_{EE} \cong I_C$ is also sufficient to define transconductance g_m and the other small-signal conductances for the transistor. The action of the capacitances is the same as for figure 10.6-1, and therefore this circuit has the same small–signal equivalent circuit and the same equation set.

10.7 SINGLE-TRANSISTOR BJT TOPOLOGIES: THE COMMON-COLLECTOR (VOLTAGE-FOLLOWER) CONFIGURATION

Although the evidence has yet to be presented, the configuration topology is the key to the transfer characteristics. The CE topology has one character and its topology cousins will have another.

The next-nearest cousin is the one in which the output is taken off the emitter (E) node instead of the collector (C) node. This topology is represented by figure 10.7-1. It gets the name common collector since the base node is committed to the input and the emitter is committed to the output. The collector is shared.

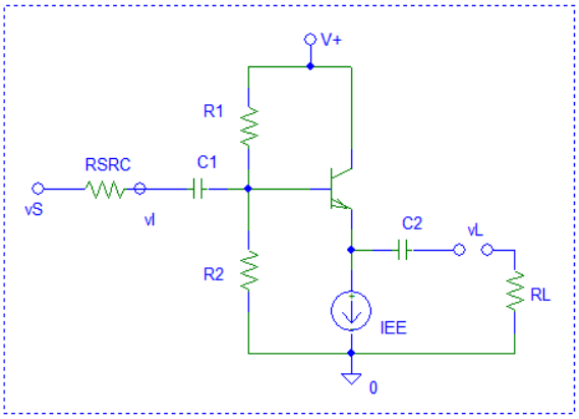


Figure 10.7-1 Common-collector topology (a.k.a. emitter-follower topology)

Because the emitter has no choice but to follow the base (since V_{BE} is approximately = 0.7V) the topology is more commonly called the emitter-follower (EF) topology or more correctly a voltage–follower.

Figure 10.7-1 elects to use a current-source bias. A resistance R_E could have been inserted in place of the fixed current source if so elected.

Take note of the fact that resistance $R_3 = 0$. This assures that the transistor will always be in the active mode regime since the collector is pinned to the voltage rail. And that forces the BC junction to always be in reverse bias.

In like manner to the analysis of the CE topology we can realize a small-signal model of the EF as shown by figure 10.7-2.

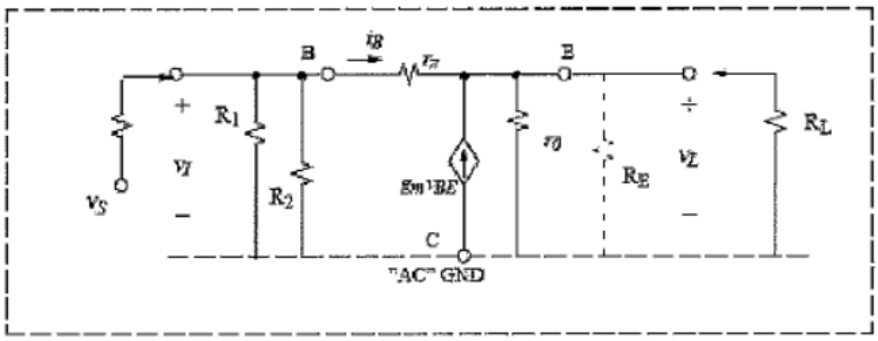


Figure 10.7-2. Two–port small-signal equivalent circuit for that of figure 10.7-1. If the current source is replaced by resistance R_E it would exist in the location denoted by the dashed lines.

Take note that there is nothing sacred about the orientation or the rigidity of the small-signal hybrid-pi transistor model. We know that the signal v_I inputs directly to the base (B). We know that signal v_L is taken directly off the emitter (E). And we know that the collector (C) is connected directly to AC GND. That is the topology represented by figure 10.7-1. Then we bend the transistor small-signal model to fit.

And in like manner to the CE topology an input to the base will see a resistance R_{iB} 'looking into' the base of identical context as the CE topology except that a different resistance is at the emitter node. In this case it is R_L and so the R_{iB} will be

$$R_{iB} = r_\pi + (\beta_F + 1)R_L \qquad (10.7\text{-}1a)$$

The emitter multiplication context is pinned to the relationship between i_B and i_E which is always the factor ($\beta_F + 1$) and if we happen to have the R_E included in the emitter leg it falls in parallel with R_L, so that

$$R_{iB} = r_\pi + (\beta_F + 1)R_E \| R_L \qquad (10.7\text{-}1b)$$

The input resistance R_{in} is then

$$R_{in} = R_1 || R_2 || R_{iB} \qquad (10.7\text{-}2)$$

Now, if we look at the output node (= node E) and apply a nodal analysis

$$v_E(g_0 + g_\pi + G_L) - g_\pi v_B - g_m v_{BE} = 0$$

Since $v_{BE} = v_B - v_E$, and since $v_E = v_L$ and $v_B = v_I$ then

$$v_L(g_0 + g_\pi + G_L + g_m) - g_\pi v_I - g_m v_I = 0$$

Solving in terms of v_L and v_I the voltage transfer ratio is then

$$\frac{v_L}{v_I} = \frac{g_m + g_\pi}{g_m + g_\pi + g_0 + G_L} \tag{10.7-3}$$

Relaxing the accuracy (which is a somewhat superfluous quantity anyway) and recognizing that both g_0 and $g_\pi << g_m$ then

$$\frac{v_L}{v_I} \cong \frac{g_m}{g_m + G_L} \tag{10.7-4}$$

If we do include a resistance R_E in the emitter leg, then the load on the emitter signal is $R_E||R_L = R_L$' and equation (10.7-4) is modified accordingly:

$$\frac{v_L}{v_I} \cong \frac{g_m}{g_m + G_L'} \tag{10.7-5}$$

Since this ratio is of positive sign and since g_m is typically large then $v_L/v_I \cong 1$, which confirms the context of E 'following' B. In this respect the nomenclature *emitter-follower* or a *voltage- follower* topology should be acknowledged as a performance description as well as a context name.

The output resistance is obtained by assessing the current at the output node of the transistor when there is zero applied signal, i.e. $v_S = 0$. Then the small–signal circuit will be of the form shown by figure 10.7-3

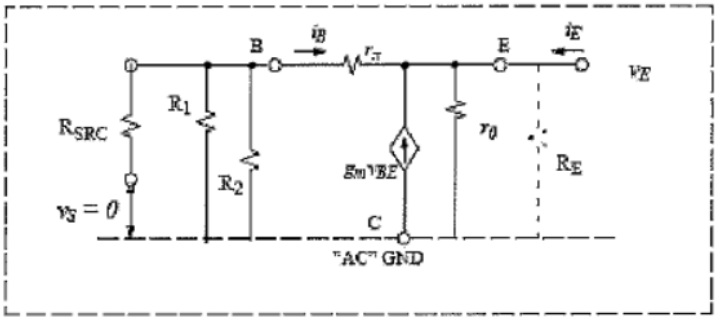


Figure 10.7-3 Assessment of output resistance requires that $v_S = 0$, consistent with Thevenin's theorem.

This circuits can be condensed to a more negotiable form by use of

$$R_{BS} = R_1||R_2||R_{SRC} \tag{10.7-6}$$

and figure 10.7-3 simplifies to figure 10.7-4

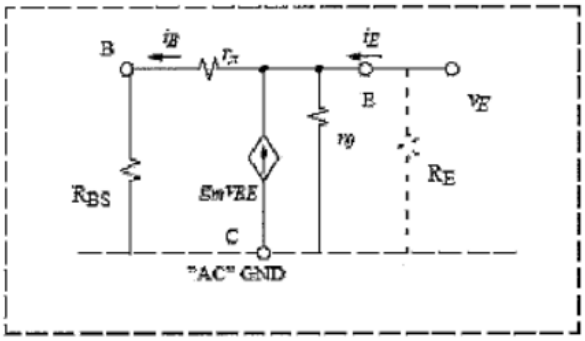


Figure 10.7-4. Assessment of output resistance, simplified topology.

Using figure 10.7-4 the resistance into the emitter is

$$R_{iE} = \frac{v_E}{i_E} \qquad \cong \frac{i_B \times (r_\pi + R_{BS})}{i_E} \qquad = \frac{i_B}{i_E} \times (r_\pi + R_{BS}) = \frac{1}{\beta_F + 1} \times (r_\pi + R_{BS})$$

And since β_F = large then

$$R_{iE} = \frac{v_E}{i_E} \cong \frac{1}{\beta_F} \times (r_\pi + R_{BS}) = \frac{r_\pi}{\beta_F} + \frac{R_{BS}}{\beta_F}$$

Which, using $r_\pi/\beta_F = 1/g_m$ gives (simplest)

$$R_{iE} \cong \frac{1}{g_m} + \frac{R_{BS}}{\beta_F} \tag{10.7-7}$$

This result also neglects the tiny contribution to the current due to r_0. Equation (10.7-7) is the resistance 'looking into' node E which is also the output resistance R_{out} unless we happen to have an emitter resistance R_E in the bias leg of the circuit. Then

$$R_{out} = R_{iE} \,||R_E \tag{10.7-8}$$

Taking an overlook of the transfer characteristics of the emitter-follower as defined by equations (10.7-2), (10.7-4) and (10.7-8) we should expect the input resistance $R_{in} \cong$ moderate–to–high, output resistance $R_{out} \cong$ low, and the voltage transfer $\cong$ unity and of the same phase as the input signal.

These characteristics are those of a 'buffer' stage, for which the voltage follower transfers the signal to a low impedance output, one that can easily drive a next stage, most likely of the form of the CE configuration. If the load to the EF = R_{in} for the next stage, the input resistance to the EF becomes a factor $\beta_F + 1$ higher according to equation (10.7-4).

10.8 SINGLE-TRANSISTOR BJT TOPOLOGIES: THE COMMON-BASE (CURRENT–FOLLOWER) CONFIGURATION

As indicated by the small-signal model (figure 10.5-4) of the BJT signal current i_C through the BJT is controlled by the signal bias v_{BE}. We can therefore apply an input signal either to the base (B) or to the emitter (E) to accomplish signal control of the BJT. Another topology option is therefore one of the form shown by figure 10.8-1 in which the input signal is to the emitter and the output is at the collector. The base may be shunted to AC ground by means of a capacitance, as shown. This configuration is called the *common-base* configuration, or the *current-follower* configuration.

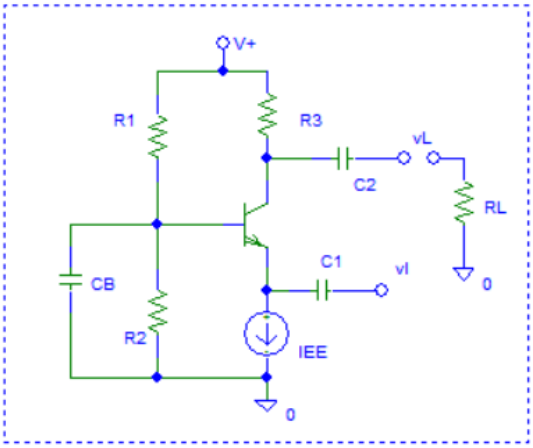


Figure 10.8-1 Common–base topology using a current-source bias.

A resistance R_E could be set in place of the current source I_{EE} much like that suggested for the other topologies. Taking the same approach as before with a small-signal equivalent to figure 10.8-1 the equivalent circuit will be of the form of figure 10.8-2.

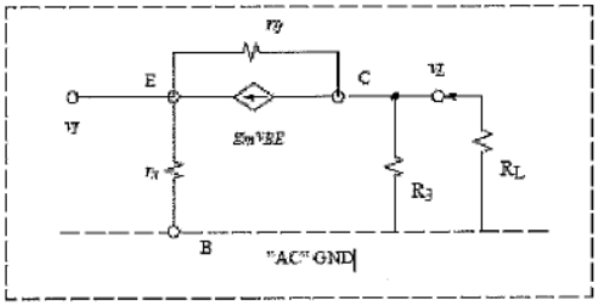


Figure 10.8-2 Small–signal equivalent model of the common-base configuration. Note that the bias resistances R_1 and R_2 are shunted by capacitance C_B and so do not appear in the small–signal circuit.

The input resistance is the resistance that we would see 'looking into' the emitter not unlike that of equation (10.7-7) except that $R_{BS} = 0$ since all bias resistances at the base node are shunted to AC ground by the capacitance C_B. Therefore the input resistance is

$$R_{in} = R_{iE} \cong \frac{1}{g_m} \qquad (10.8\text{-}1)$$

If we undertake a nodal analysis at node C then we will get

$$v_C(G_L + G_C + g_0) - g_0 v_E + g_m v_{BE} = 0$$

And since $v_{BE} = v_B - v_E = -v_E$, (since v_B is shunted to AC ground)

$$v_C(G_L + G_C + g_0) - (g_m + g_0)v_E = 0$$

for which we get the voltage transfer gain

$$\frac{v_C}{v_E} = \frac{v_L}{v_I} = \frac{g_m + g_0}{G_C + G_L + g_0}$$

Or, neglecting the small conductance g_0, the voltage transfer gain is

$$\frac{v_L}{v_I} = \frac{g_m}{G_C + G_L} \qquad = +g_m R_C || R_L \qquad (10.8\text{-}2)$$

The output resistance will be just the resistances r_0 and R_3 in parallel, since with $v_I = v_E = 0$ the current source is turned off. Then

$$R_{out} = r_0 || R_C \qquad \cong R_C \qquad (10.8\text{-}3)$$

If we elect to determine the current transfer ratio i_L/i_I . Using the chain rule

$$\frac{i_L}{i_I} = \frac{i_L}{v_L} \times \frac{v_L}{v_I} \times \frac{v_I}{i_I} \qquad = G_L \times \frac{g_m}{G_C + G_L} \times \frac{1}{g_m}$$

where equation (10.8-1) is $R_{in} = \frac{v_I}{i_I} = \frac{1}{g_m}$. Otherwise this analysis reduces to

$$\frac{i_L}{i_I} = \frac{G_L}{G_C + G_L} \qquad (10.8\text{-}4)$$

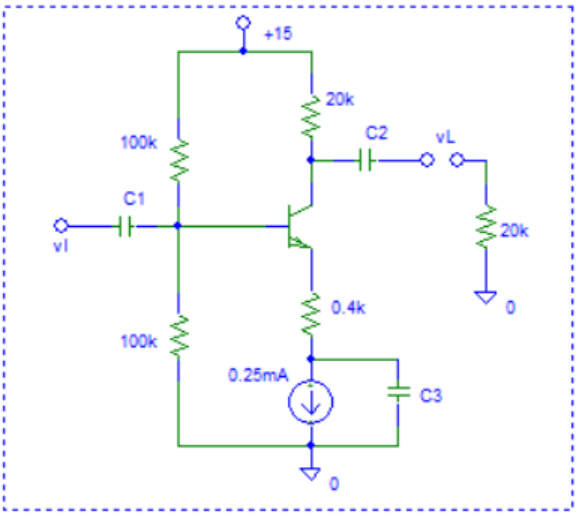
which is the equation for a current divider and tells us is that the common-base topology is of the form of a current follower.

10.9 SINGLE-TRANSISTOR BJT AMPLIFIERS: OVERVIEW AND APPROXIMATIONS

The three topologies analyzed in the three previous sections are the only three accepted circuit options. We may choose to make some variation in the bias networks or add feedback resistances, but as far as amplifier building blocks are concerned, these three is all there is. Naturally we can assess each of them using the two-port formulae as derived. But they are *not* precise and should not be treated as if they are. They are design guides only. With normal variation in component parameters we should not expect back-of-the-envelope results any more accurate than two significant figures.

Given the simplicity of the approximations and the fact that accuracy is not expected many of these topologies can be analyzed by inspection. Consider the following example.

EXAMPLE 10.9-1: CE Amplifier topology. Determine its two–port transfer characteristics (R_{in}, R_{out}, v_L/v_I)



Defaults:

Capacitances large

Resistances in kΩ. Currents in mA

Assuming default $\beta_F = 100$

SOLUTION:

The small-signal conductance parameters are

$g_m = 40 \times 0.25 \quad = 10\text{mA/V}$ $\qquad$ $r_\pi = 100/g_m \quad = 10\text{k}\Omega$

Note that we assume that I_C is approximately the same as that of the current source. The minor difference between I_E and I_C falls outside of the accuracy context of any and all characteristics of the BJT and the circuit components.

Also note: We seldom know the working value of β_F and so we assume $\beta_F = 100$ unless otherwise defined.

Then input resistance R_{iB} to the base of the BJT is

$R_{iB} \cong r_\pi + 100 \times 0.4 \quad = 50\text{k}\Omega$

Then the input resistance is (approximately)

$$R_{in} \cong 100||100||50 \qquad = \underline{\textbf{25 kΩ}}$$

The output resistance R_{out} is (approximately)

$$R_{out} \cong R_3 \qquad = \underline{\textbf{20 kΩ}}$$

and the voltage transfer gain is (approximately)

$$\frac{v_L}{v_I} \cong -\frac{20||20}{1/10+0.4} \qquad = \underline{\textbf{- 20 V/V}}$$

Note that we did not need to make so much as a sideways glance at a calculator to realize these performance metrics.. Even if the numbers had been a little less convenient, the imprecise nature of the results accommodates an educated estimate. For example, consider the following example

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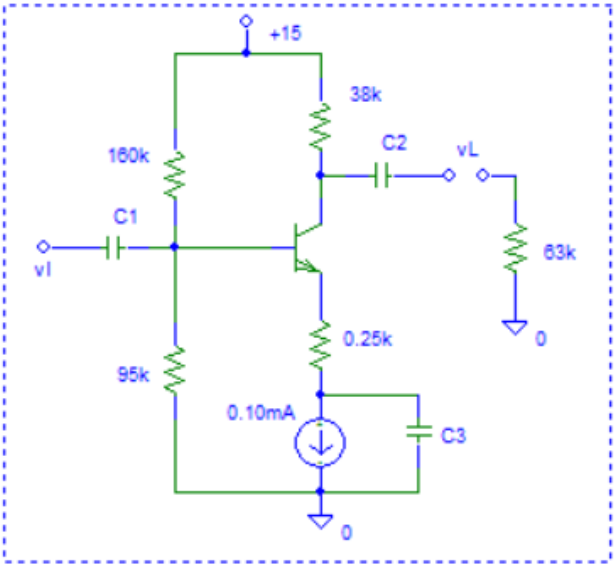
EXAMPLE 10.9-2: CE Amplifier topology. Determine its two-port transfer characteristics (R_{in}, R_{out}, v_L/v_I)



SOLUTION: The transistor parameters are

$$g_m = 4\text{mA/V} \quad r_\pi = 100/g_m = 25\text{k}\Omega$$

$$R_{iB} = 25 + 100 \times 0.25 = 50\ \text{k}\Omega.$$

Input resistance is then

$$R_{in} = 160||95||50 \cong 150||100||50 = \underline{\textbf{27kΩ}}$$

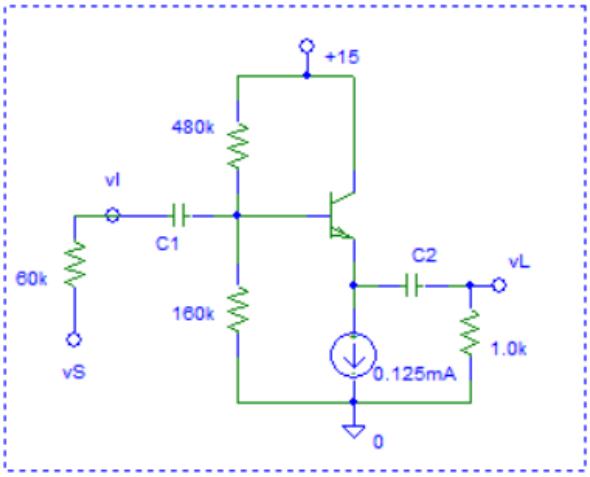
The output resistance is $R_{out} \cong \underline{\textbf{38kΩ}}$

and the voltage transfer gain is $\frac{v_L}{v_I} \cong -\frac{40||60}{1/4+0.25} = -\frac{24}{0.5} \cong \underline{\textbf{-48V/V}}$

As long as there is no need to make a high accuracy calculation, then the quick, rough approximations made in example 10.9-2 are adequate. Usually estimates within 10% are sufficient. Any more precise assessments are b obtained by simulation analysis using SPICE.

This estimate process can also be applied to the other topologies. Consider the following example:

EXAMPLE 10.9-3: Voltage–follower topology. Determine its two–port transfer characteristics (R_{in}, R_{out}, v_L/v_I) and v_L/v_S .



Defaults:

Capacitances large
Resistances in kΩ. Currents in mA

SOLUTION: Assuming default $\beta_F = 100$ the transistor parameters are then

$g_m = 40 \times 0.125 = 5\text{mA/V}$ $\qquad$ $r_\pi = 100/5 = 20\text{k}\Omega$

Then the resistance Ri_B into the base of the BJT is

$R_{iB} = r_\pi + 100 \times 1.0 = 120\text{k}\Omega$

And input resistance is (approximately)

$R_{in} = 480||160||120 = \underline{\mathbf{60k\Omega}}$

The output resistance *Rout* is (approximately)

$$R_{out} = \frac{1}{g_m} + \frac{R_{BS}}{\beta_F} = \frac{1}{5} + \frac{160||480||60}{100} = 0.2 + \frac{40}{100} \cong \underline{\mathbf{0.6k\Omega}}$$

and the voltage transfer gain is (approximately)

$$\frac{v_L}{v_I} = \frac{5}{5+1} = \underline{\mathbf{0.83V/V}}$$

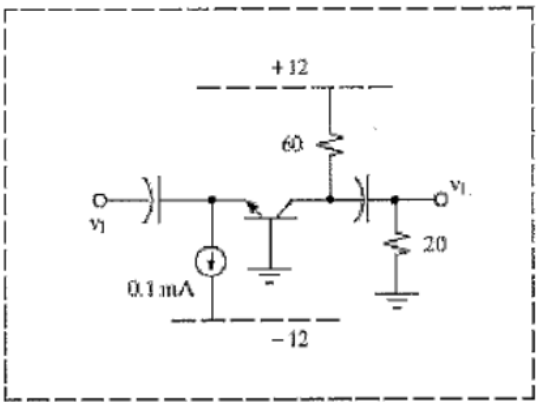
Note that this transfer gain is always less than unity. The source–to–load transfer gain can also be determined

$$\frac{v_L}{v_S} = \frac{R_{in}}{R_{SRC} + R_{in}} \times \frac{v_L}{v_I} = \frac{60}{60+60} \times 0.83 = \underline{\mathbf{0.42V/V}}$$

More precise analysis is probably not all that necessary. But if so, it would be a task for SPICE.

As a final example, consider the current–follower topology. In this case we will choose to use a bipolar power supply, so that base bias by means of the R_1, R_2 voltage divider is unnecessary.

EXAMPLE 10.9-4: Current–follower topology. Determine its two–port transfer characteristics (R_{in}, R_{out}, v_L/v_I)



SOLUTION:

Assuming β_F = 100, (default) the transistor parameters are

$$g_m = 40 \times 0.1 = 4 \text{ mA/V}$$

$$r_\pi = 100/4 = 25 \text{ k}\Omega$$

Then input resistance is

$$R_{in} \cong \frac{1}{g_m} = \frac{1}{4} \qquad \cong \underline{\mathbf{0.25k\Omega}}$$

The output resistance is approximately

$$R_{out} \cong R_3 \qquad = \underline{\mathbf{60\ k\Omega}}$$

and the current transfer ratio, for the current divider shown, is approximately

$$\frac{i_L}{i_I} = \frac{1/20}{1/20 + 1/60} \qquad = \underline{\mathbf{0.75\ A/A}}$$

If we want to find the voltage transfer ratio then

$$\frac{v_L}{v_I} = +4 \times 20 \,||\, 60 \qquad = \underline{\mathbf{60V/V}}$$

Like the other topologies the analysis can be done without need for a calculator provided that a little slop is acceptable.

10.10 CURRENT SOURCES AND TOPOLOGIES

It should be evident from the process of the series of explanations that the transistor is a device that controls current levels and is defined by the current level at which it operates. And that is why the circuit topologies reduce to such a simple context when they include a current source fixture. It therefore makes a great deal of sense to acquire the topology for current sources and realize the circuit form of the current source fixture. A current source is also a very simple construct, which makes it a ready appendage to the collection of circuit topologies.

As has been referenced in the exposition on the BJT the characteristics reveal that the collector node is also identified as the 'stiff' current node, which is another way of saying that the current is relatively fixed for a wide range of voltage differences across the transistor.

The stiffness context is also characteristic of a current source. Comparison is shown by figure 10.10-1.

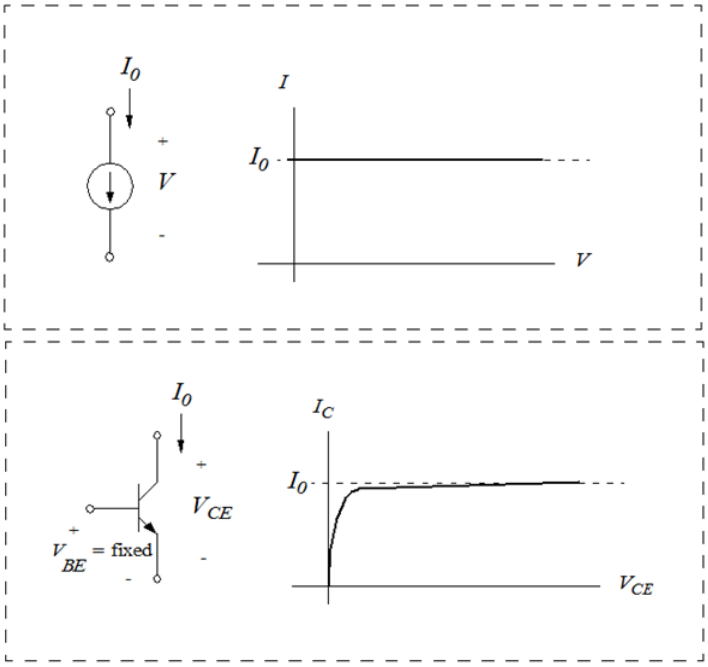


Figure 10.10-1. Ideal current source and comparison to transistor current I_C: Electrical characteristics.

Since current sources are a construct rather than a component, we have just uncovered the basis of the construct. And whereas the stiff node of the transistor realizes a very good current source, the rest of the story is the control of the source to achieve a fixed level of current. This control is accomplished by the current-mirror topology shown by figure 10.10-2.

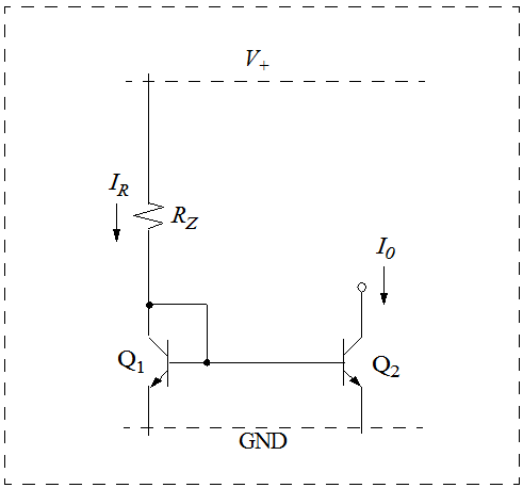


Figure 10.10-2. Simple current mirror. With fixed current $I_0 \cong I_R$

Figure 10.10-2 identifies that the output current I_O is a reflection of the current in the reference side. Transistor Q_1 is connected in a 'diode configuration', for which the voltage drop between C and E will be equivalent to that of a junction diode ≅ 0.7V.

Resistance R_Z then defines the current by

$$I_0 \cong I_R \cong \frac{V_+ - 0.7}{R_Z} \qquad (10.10\text{-}1)$$

And this assessment can also be accomplished by inspection. Consider the following example.

EXAMPLE 10.10-1: CE topology biased by current mirror. Determine R_Z needed for g_m = 4mA/V and determine the transfer characteristics (R_{in}, R_{out}, and v_L/v_I).

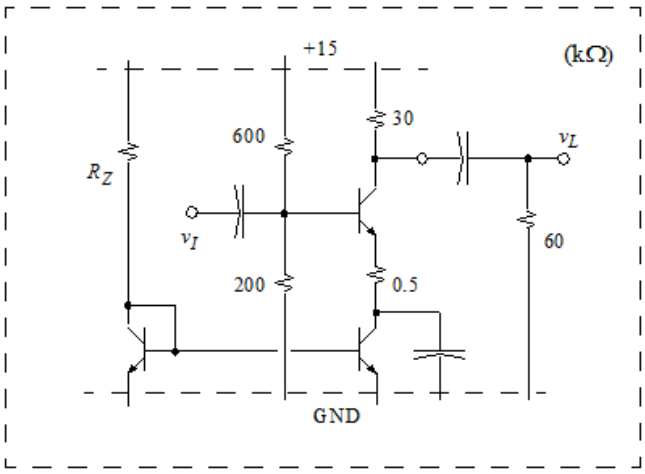


Figure E10.10-1. CE topology with current mirror source.

SOLUTION: Since $g_m = 4\text{mA/V} = 40 \times I$ then $I = 4/40 = 0.1$ mA $\cong I_R$

and from equation 10.10-1 $R_Z \cong \dfrac{V_+ - 0.7}{I_R} = \dfrac{15 - 0.7}{0.1}$ = **143kΩ**

By inspection and (assumption) default $\beta_F = 100$ $R_{iB} \cong 100 \times (1/4 + 0.5)$ $\cong 75\text{k}\Omega$

$R_{in} = 600 \| 200 \| 75$ $\cong$ **50kΩ** $R_{out} \cong R_3$ = **30kΩ**

$$\frac{v_L}{v_I} \cong -\frac{30 \| 60}{1/4 + 0.5} = -\frac{20}{0.75} \cong \textbf{27 V/V}$$

There is one other consideration which needs to be identified since the use of current source have passed over most of the context of operating point slip. It relates primarily to the fact that transfer gain relies on the magnitude for R_3. But there is an upper limit to R_3 courtesy of the fact that the BC junction must remain in reverse-bias. The maximum value of R_3 is

$$R_3(max) = \frac{V_+ - V_C(\text{min})}{I} \qquad (10.10\text{-}2)$$

If we estimate the node voltage at V_B to be approximately that defined by the R_1, R_2 voltage divider, this is sufficient to identify a lower limit on V_C. Applying this criterion to Example 10.10-1 we find that R_3(max) will be

$$R_3(max) = \frac{15 - 3.75}{0.1} = \textbf{112 kΩ}$$

This analysis should be included in the menu for the CE topology.

EXAMPLE 10.10-2: EF topology with current mirror. Determine R_Z needed for g_m = 20mA/V and evaluate the transfer characteristics (R_{in}, R_{out}, and v_L/v_I).

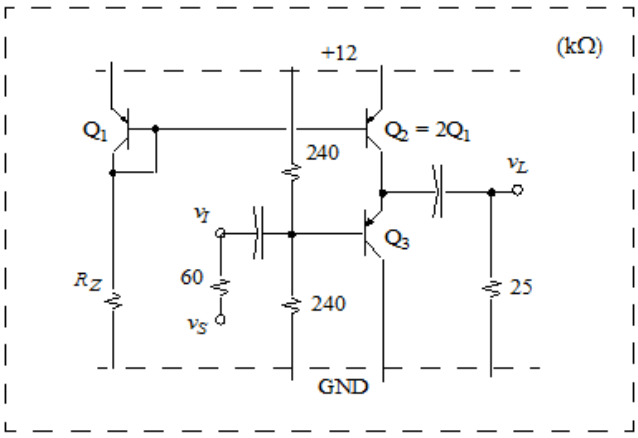


Figure E10.10-2. EF topology with current mirror source.

SOLUTION: Since g_m = 20mA/V = 40 × I then I = 20/40 = 0.5 mA $\cong 2I_R$

Take note that the simple current mirror can be sized. It is not uncommon to render either Q1 or Q2 to be a pair of transistors in parallel, which would show up as a factor of two as shown.

From equation 10.10-1 $$R_Z \cong \frac{V_+ - 0.7}{I_R/2} = \frac{12-0.7}{0.25} = \underline{\mathbf{45k\Omega}}$$

By inspection and (assumption) default β_F = 100 $R_{iB} \cong 100 \times (1/20 + 25) \cong 2500\ k\Omega$

$$R_{in} = 240||240||2500 \cong \underline{\mathbf{120k\Omega}}$$

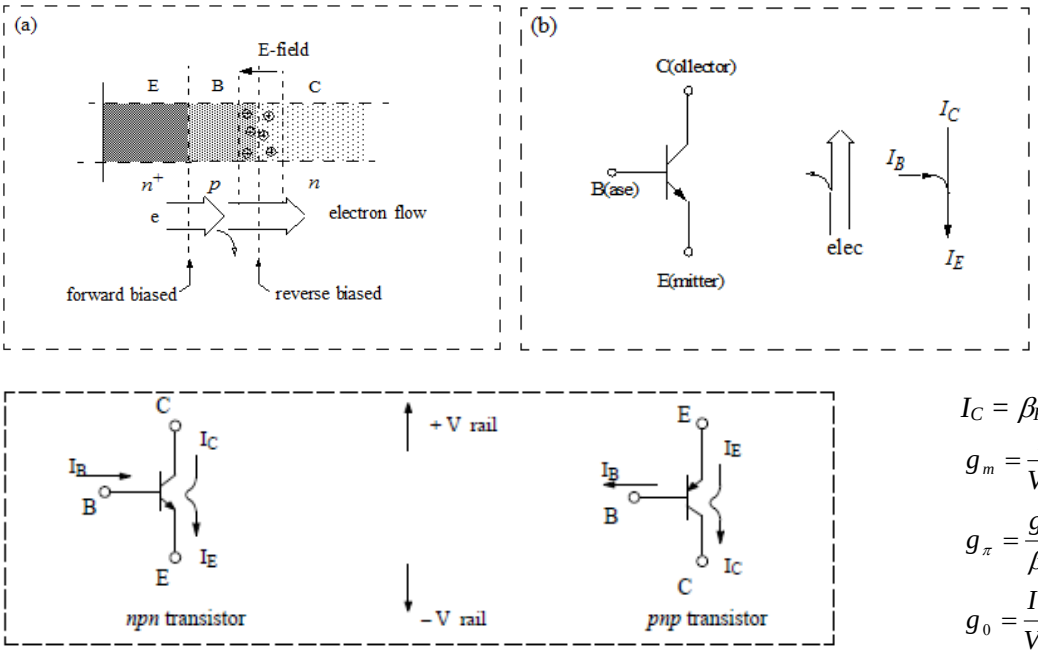
$$R_{out} = \frac{1}{g_m} + \frac{R_{BS}}{\beta_F} = \frac{1}{20} + \frac{60\,||\,240\,||\,240}{100} = 0.05 + \frac{40}{100} \cong \underline{\mathbf{0.45k\Omega}}$$

$$\frac{v_L}{v_I} = \frac{20}{20 + 1/25} \cong \underline{\mathbf{1.0V/V}}$$

Note that the approximations expressed by these examples allow considerable latitude. As has been emphasized, electronic circuit analysis is not a craft in which analytical precision is either expected or needed. Component manufacture is not a precise process. The analysis accomplished by these examples is only first-order. If a more comprehensive analysis is desired these first-order assessments serve as a touchstone for that which can be provided by a circuit simulation utility.

PORTFOLIO and SUMMARY

(a) bipolar-junction transistor (BJT)



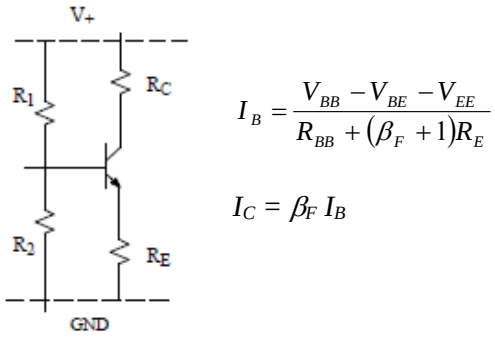
$$I_C = \beta_F I_B$$

$$g_m = \frac{I}{V_T} \cong 40 I_C$$

$$g_\pi = \frac{g_m}{\beta_F}$$

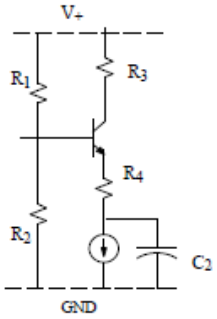
$$g_0 = \frac{I_C}{V_A}$$

(b) 4-resistance bias frame



$$I_B = \frac{V_{BB} - V_{BE} - V_{EE}}{R_{BB} + (\beta_F + 1) R_E}$$

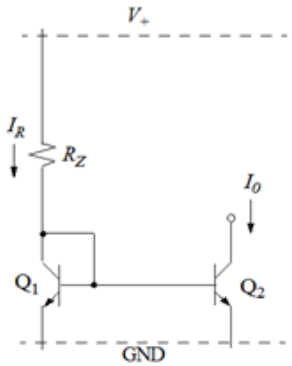
$$I_C = \beta_F I_B$$



$$I_B = \frac{I_{EE}}{\beta_F + 1}$$

$$I_C = \beta_F I_B$$

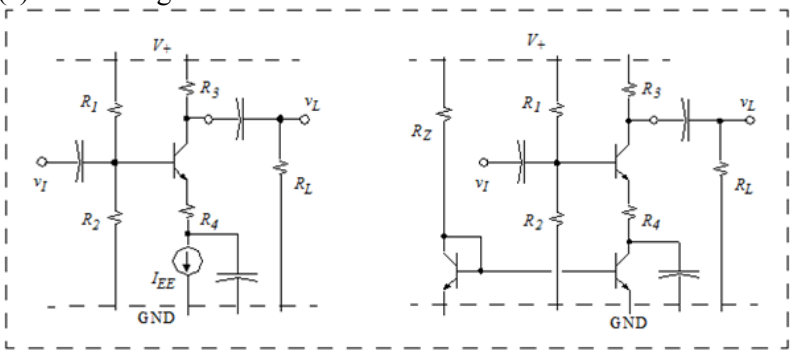
(c) Current mirror



$$I_0 \cong I_R \cong \frac{V_+ - 0.7}{R_Z}$$

Single-transistor topologies

(a) CE configuration



$$R_{iB} = r_\pi + (\beta_F + 1)\, R_4 \cong \beta_F \times (1/g_m + R_4)$$

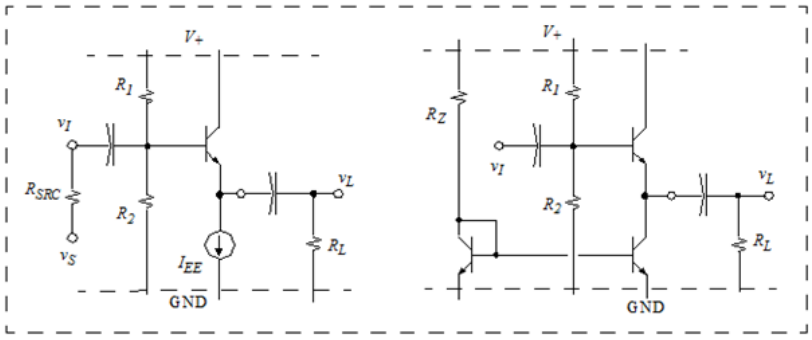
$$R_{in} = R_1 || R_2 || R_{iB}$$

$$R_{out} \cong R_3$$

$$\frac{v_L}{v_I} = \frac{-R_3 \,||\, R_L}{1/g_m + R_4}$$

$$R_3(max) = \frac{V_+ - V_C(\min)}{I}$$

(b) EF configuration



$$R_{iB} = r_\pi + (\beta_F + 1)\, R_L \cong \beta_F \times (1/g_m + R_L)$$

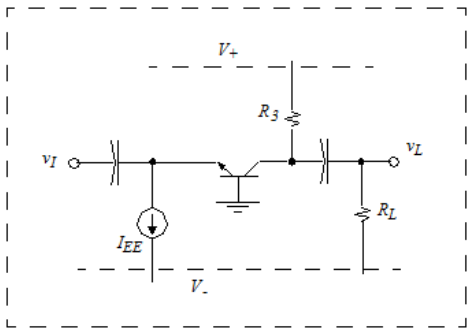
$$R_{in} = R_1 || R_2 || R_{iB}$$

$$R_{iE} \cong \frac{1}{g_m} + \frac{R_{BS}}{\beta_F}$$

$$R_{out} \cong R_{iE}$$

$$\frac{v_L}{v_I} \cong \frac{g_m}{g_m + G_L}$$

(c) Common-base configuration



$$R_{iE} \cong \frac{1}{g_m} \qquad R_{in} \cong R_{iE}$$

$$R_{out} \cong R_3$$

$$\frac{v_L}{v_I} = g_M \times R_3 \,||\, R_L$$