Chapter Three

PARALLELING TECHNIQUES

Paralleling of converter power modules is a well-known technique that is often used in high-power applications to achieve the desired output power with smaller size power transformers and inductors [B1]. Since magnetics are critical components in power converters because generally they are the size-limiting factors in achieving high-density and/or low-profile power supplies, the design of magnetics becomes even more challenging for high-power applications that call for high power-density and low-profile packaging. Instead of designing large-size centralized magnetics that handle the entire power, low-power distributed high-density/low-profile magnetics can be utilized to handle the high processing power, while only partial load power flow through each individual magnetics [B1, B2].

In addition to physically distributing the magnetics and their power losses and thermal stresses, paralleling also distributes power losses and thermal stresses of the semiconductors due to a smaller power processed through the individual paralleled power stages. As a result,

paralleling is a popular approach to eliminating "hot spots" in power supplies. In addition, the switching frequencies of paralleled, lower-power power stages may be higher than the switching frequencies of the corresponding single, high-power processing stages because lower-power, faster semiconductor switches can be used in implementing the paralleled power stages. Consequently, paralleling offers an opportunity to reduce the size of the magnetic components and to achieve a low-profile design for high power applications.

Without increasing the number of power stages and control-circuit components, the transformer magnetics can be distributed by direct transformer paralleling. Not only that transformer paralleling distributes the processed power in each magnetics components, but also their power losses and thermal stresses are distributed at the same time. However, current sharing among the paralleled transformers needs to be maintained to ensure power balance.

In its basic form, the interleaving technique can be viewed as a variation of the paralleling technique, where the switching instants are phase-shifted within a switching period [B7]. By introducing an equal phase shift between the paralleled power stages, the total inductor current ripple of the power stage seen by the output filter capacitor is lowered due to the ripple cancellation effect [B7].

This chapter discusses the paralleling techniques to achieve high-density, low-profile designs for relative high power applications. It analyzes and compares the current sharing in various implementations of transformer paralleling. Also different approaches in interleaving techniques are presented, compared, and experimentally evaluated.

3.1. Transformer Paralleling

3.1.1. Direct Paralleling

In the forward converter shown in Fig. 3.1, T_1 and T_2 are two low-profile transformers connected directly in parallel and have the same secondary circuitry. The same techniques can be used in flyback converter to increase power handling capability. The following analysis uses forward converters for illustration, while the general conclusions are applicable to flyback converters.

For proper operation of the circuit, the transformers need to share the load current. However, the mismatched elements in the two paralleled transformers will cause an uneven distribution of the load current between the two transformers. The equivalent circuit and the key waveforms of the two transformers in parallel are shown in Fig. 3.2. Assuming $i_{m1} = i_{m2} \approx 0$, it can be derived that (detailed in Appendix I.(i)):

$$\frac{I_{s1}}{I_{s2}} = \frac{R_2}{R_1} \tag{3-1}$$

where R_1 and R_2 are the winding resistances of the two transformers. Therefore, the current sharing depends on the parasitics of the transformers and this approach works only with well-

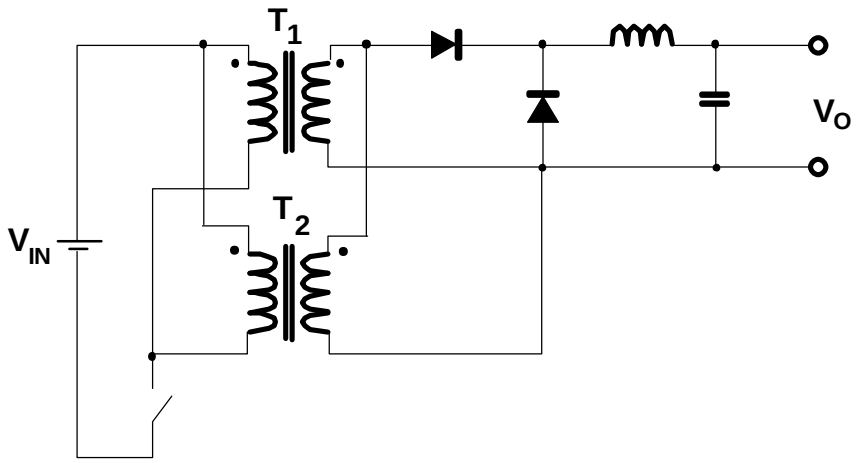


Figure 3.1. Direct transformer paralleling.

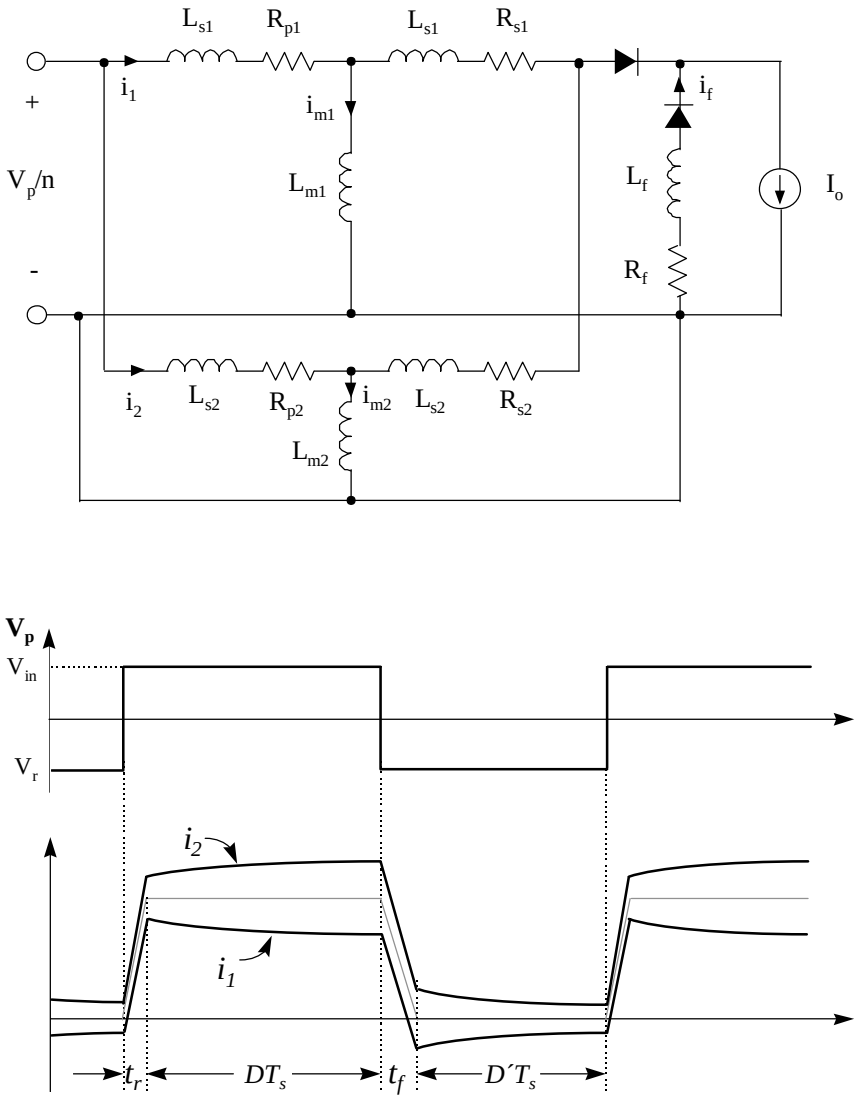


Figure 3.2. Equivalent circuit and key waveforms of direct transformer paralleling. R_p, L_p and Lm are the reflected primary winding resistance, leakage inductance, and magnetizing inductance of the transformers, respectively. L_s and R_s are secondary leakage inductance and winding resistance. R_f and L_f are the parasitic resistance and parasitic inductance on the freewheeling path.

matched transformers. It can also be observed from Fig. 3.2 that current oscillation can occur between paralleled modules due to parameter mismatch and cause additional circulating energy.

The transformer parasitic resistance is usually comparable with trace resistance. To take into account effect of the trace resistance mismatch, R_1 and R_2 in Eq. (3-1) should also include the trace resistance. At the connecting ends of the transformers, the trace layout of the transformer connection should be symmetrical in order not to introduce any unbalanced trace resistance.

3.1.2. Paralleling With Separate Forward Diodes

A modification can be made by using separate forward diodes to reduce the parasitic effect, as shown in Fig. 3.3, where the equivalent circuit and the key waveforms are shown in Fig. 3.4. With a configuration like this, the current sharing is governed by (detailed in Appendix I.(ii))

$$\frac{I_{s1}}{I_{s2}} = \frac{R_2 + R_{D2}}{R_1 + R_{D1}} \tag{3-2}$$

where R_{D1} and R_{D2} are the diode on-resistances. It can be seen from Fig. 3.4 that the unidirectional current conduction of the separate diodes eliminates the oscillation between modules during the off-time. Furthermore, because diode on-resistance is much larger than parasitic resistance, i.e., $R_D \gg R_1, R_2$, current sharing can be simplified to

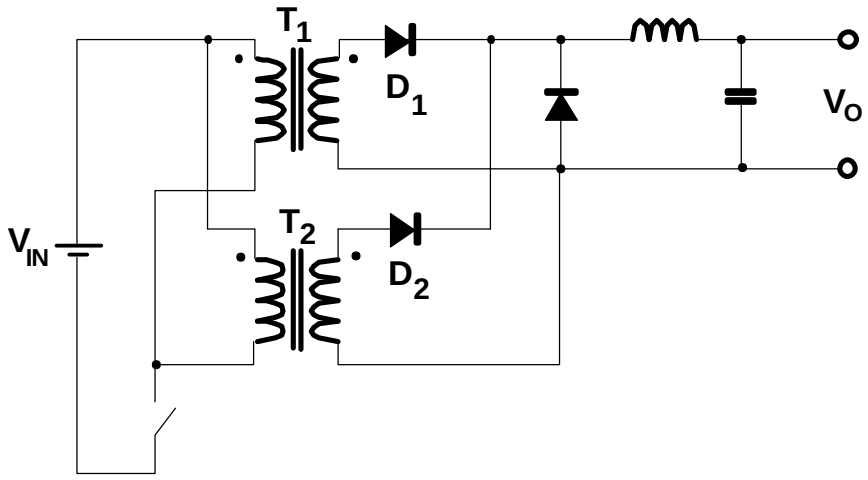


Figure 3.3. Transformer paralleling using separate forward diodes.

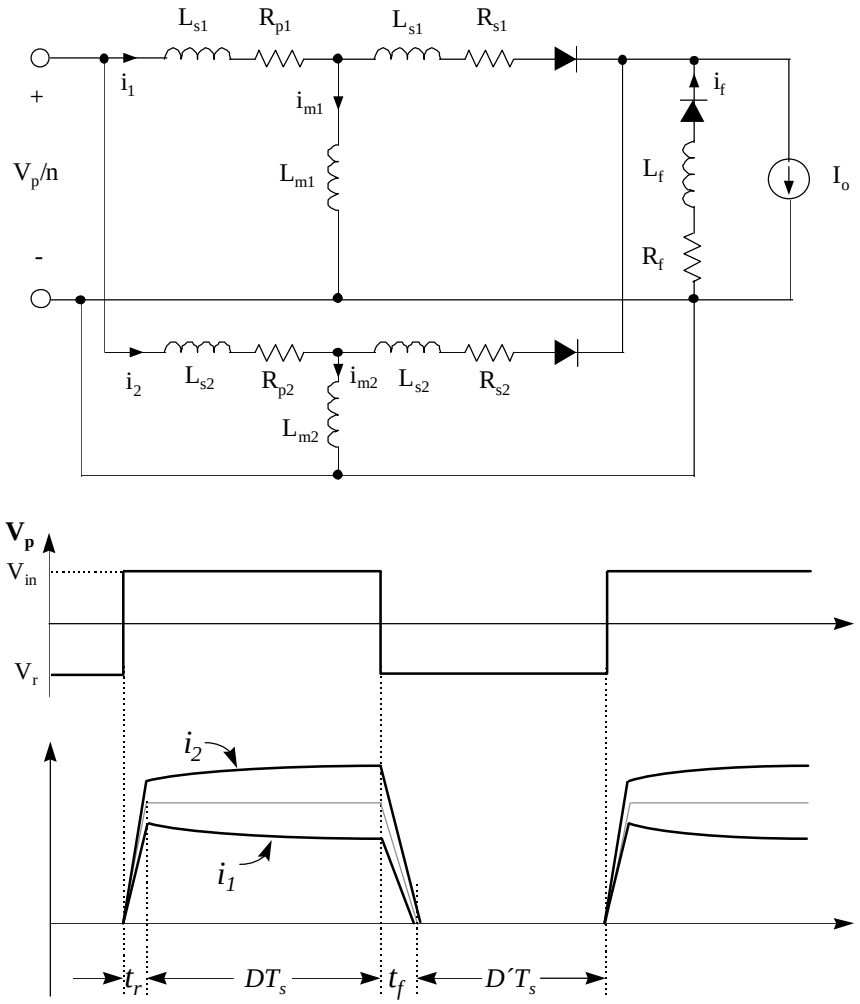


Figure 3.4. Equivalent circuit and key waveforms of transformer paralleling with separate forward diodes.

$$\frac{I_{s1}}{I_{s2}} = \frac{R_{D2}}{R_{D1}}. \tag{3-3}$$

Thus, current sharing depends on the diode on-resistance instead of the parasitics. Since the diode on-resistance is manufactured more uniformly, using separate forward diodes is a better solution for current sharing.

3.1.3. Paralleling with Common Heat Sink

On-resistance of diodes has negative temperature coefficient, i.e., on-resistance decreases as temperature rises. This results in a potential problem for current sharing: if one diode starts with higher current due to a slight mismatch between the diode on-resistance, its on-resistance will become smaller because of higher temperature by larger power dissipation. This makes the heated diode draw even more current by Eq. (3-3). Proper thermal design needs to be taken to prevent current hogging. Under steady state, the electro-thermal current unbalance can be quantified as

$$I_{s1} = \frac{I_o}{2} + DI, \quad I_{s2} = \frac{I_o}{2} - DI, \tag{3-4}$$

where I_o is the output current and DI is the current deviation caused by the deviation of the forward-voltage drop between the two paralleled diodes:

$$V_{F1} = V_F - dV_F, \quad V_{F2} = V_F + dV_F. \tag{3-5}$$

Using the electro-thermal equivalent circuit model, shown in Fig. 3.5, Appendix II shows that the current sharing depending the thermal coupling resistance as

$$D = \frac{DI}{I_o} = \left[\frac{1 + \frac{KV_F I_o (R_a + R_b)}{2}}{1 + \frac{KV_F I_o R_b}{2 + \frac{R_c}{R_b}}} \right] \frac{d}{2}, \tag{3-6}$$

where K is the temperature coefficient of the diode forward-voltage drop and $d = dV_F / V_F$. Without the negative temperature coefficient K, i.e., $K = 0$, the current unbalance is determined solely by the diode parameter mismatch, d, as

$$D = \frac{d}{2}. \tag{3-7}$$

If the two paralleled diodes are mounted on separate heatsinks, the thermal coupling resistance is practically infinite ($R_c = \infty$). On the other hand, R_c, can be theoretically null if the two devices are mounted very closely on the same heatsink ($R_c = 0$). The results of these two extreme cases are:

$$\begin{cases} D = \left[1 + 0.5KV_F I_o (R_a + R_b)\right] \frac{d}{2}, & R_c = \infty \text{ (insulated)}; \\ D = \left[\frac{1 + 0.5KV_F I_o (R_a + R_b)}{1 + 0.5KV_F I_o R_b} \right] \frac{d}{2}, & R_c = 0 \text{ (perfect coupling)}. \end{cases} \tag{3-8}$$

As an example, the current unbalance, D, of two paralleled transformers with separate IR 82CNQ30 Schottky diodes is plotted in Fig. 3.6 as a function of the device deviation d and the

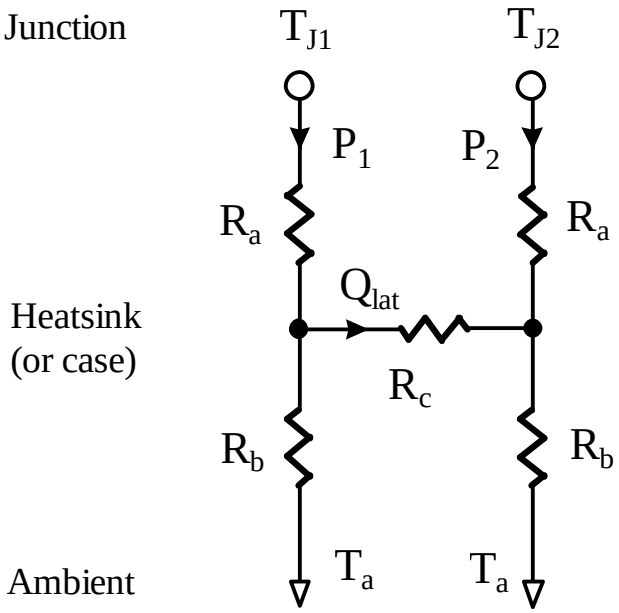


Figure 3.5. Thermal equivalent circuit for two diodes in parallel. R_a and R_b are thermal resistance from the junction to the thermal coupling interface (either the case for in-chip paralleling or the heatsink for external paralleling). R_c represents the thermal coupling between the paralleled diodes.

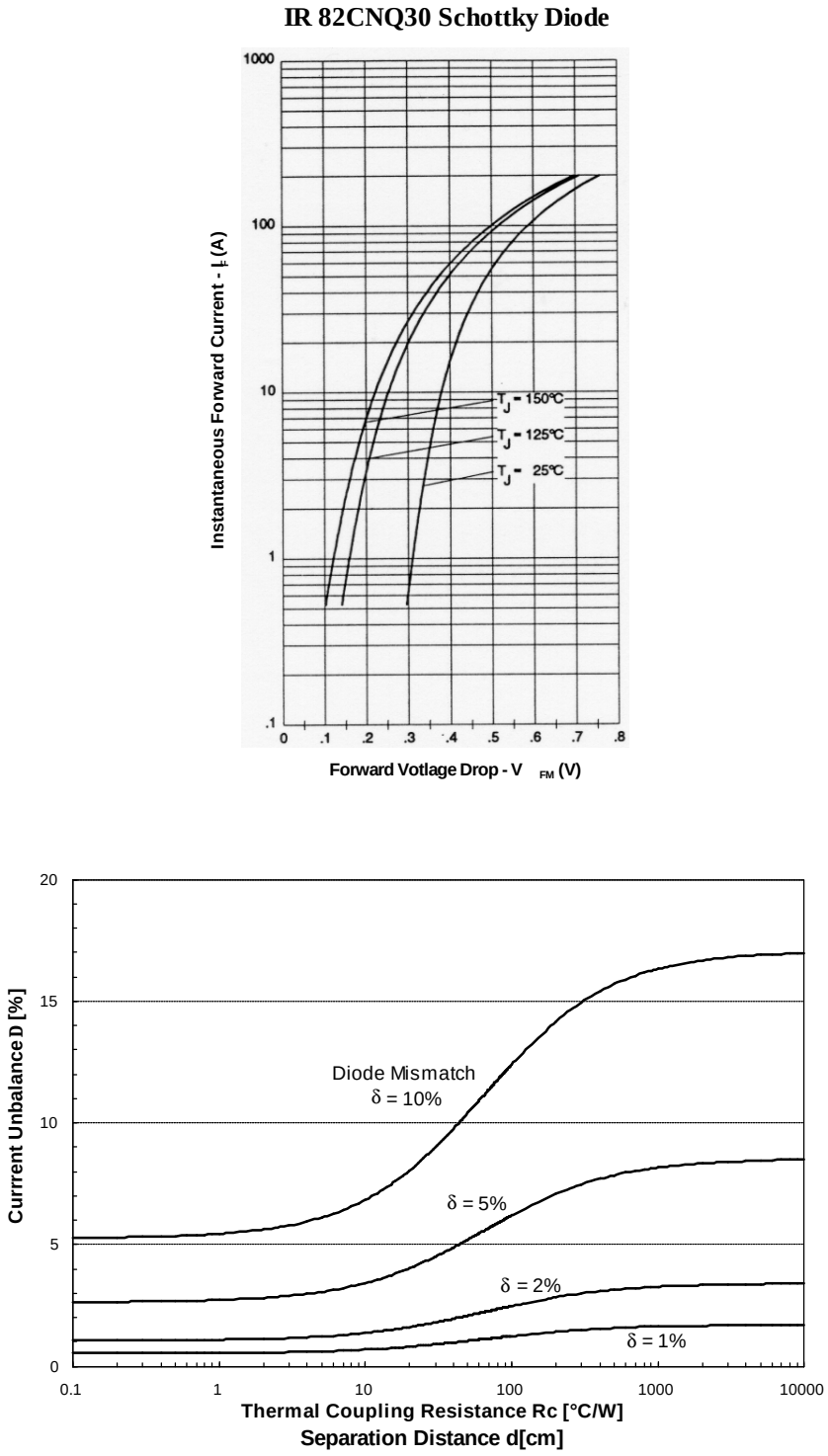


Figure 3.6. Current unbalance as a function of device deviation *d* and thermal coupling resistance R_c (and spacing, *d*, between two diodes).

lateral thermal coupling resistance R_c (and the spacing, d, between the two diodes). It can be seen that without thermal coupling ($R_c = \infty$), the temperature coefficient hogs current deviation from the initial $d/2$ to a higher level. However, equilibrium can be achieved if temperature dependence is not a strong function, i.e., no thermal runaway. As can be seen from Fig. 3.6, two diodes spaced 1 cm apart on a 0.5-cm thick, 2-cm wide aluminum heatsink will have $D \approx 0.55\ d$, which is already pretty close to $0.5d$, the result with $K = 0$. The correction of the current distribution using thermal coupling is to offset the effect of the temperature coefficient.

If $R_a \ll R_b$, complete offset can be achieved with perfect coupling ($R_c = 0$). Namely, the current distribution deviation can be reduced back to the initial value $d/2$, i.e., Eq. (3-8) for $R_c = 0$ is reduced to $D = d/2$. The diode paralleling can be done either internally (in-chip paralleling) or externally. For these two cases,

$$\begin{cases} R_a = R_{JC} + R_{CH}, \ \ R_b = R_{CA}, & \text{external paralleling with a common heatsink;} \\ R_a = R_{JC}, \ \ R_b = R_{CH} + R_{CA}, & \text{in-chip paralleling.} \end{cases} \tag{3-9}$$

R_a can be reduced using the in-chip paralleling. But the reduction is significant only when R_{CA} is close to R_{JC} and R_{CH} (usually R_{JC} is of the same order of R_{JC}). Therefore, in-chip paralleling or external paralleling with a common heat sink can provide good thermal coupling between the paralleled diodes and consequently can reduce the current hogging caused by the negative temperature coefficient of the diode forward-voltage drop.

Using the positive temperature coefficient characteristic of MOSFET on-resistance, replacing the diodes with synchronous rectifier [B15] can solve the electro-thermal unbalance problem inherently. Synchronous rectifiers always exhibit good current sharing; thus no current

hogging is possible. However, the complexity of the circuit increases, which may defeat the simplicity of transformer paralleling.

3.1.4. Experimental Evaluations

A forward converter was implemented with two transformers in parallel. Four cases were measured to investigate the current distribution dependence on the circuit configurations and layout parasitics, as shown in Fig. 3.7. In case ①, a symmetrical layout is designed for the two paralleled transformers, and a single forward diode is shared by the two transformers. An asymmetrical layout is used for the two transformers in case ②, which increases the parameter mismatch in the two paralleled channels. Case ③ replaces the shared forward diode with two separate diodes, each in series with one of the two paralleled transformers. Finally, in case ④ the two forward diodes are mounted on the same heatsink with 1-cm spacing to reinforce current sharing by electro-thermal coupling. The measured parameter mismatches are tabulated in Table 3-I. The analytical calculations using Eqs. (3-1), (3-3) and , (3-6), PSpice simulation results, and measurement data of current sharing in the four tested configurations are also listed in Table 3-I. As can be seen from Table 3-I, as the parameter mismatch increases from case ① to case ②, the current unbalance increases correspondingly. Using separate forward diodes (case ③) corrects the effects of layout parasitics to some extent. The most desirable current sharing solution is provided by case ④, which further balances the negative temperature coefficient in diodes. Overall, the analytical, simulated and measured results agree very well.

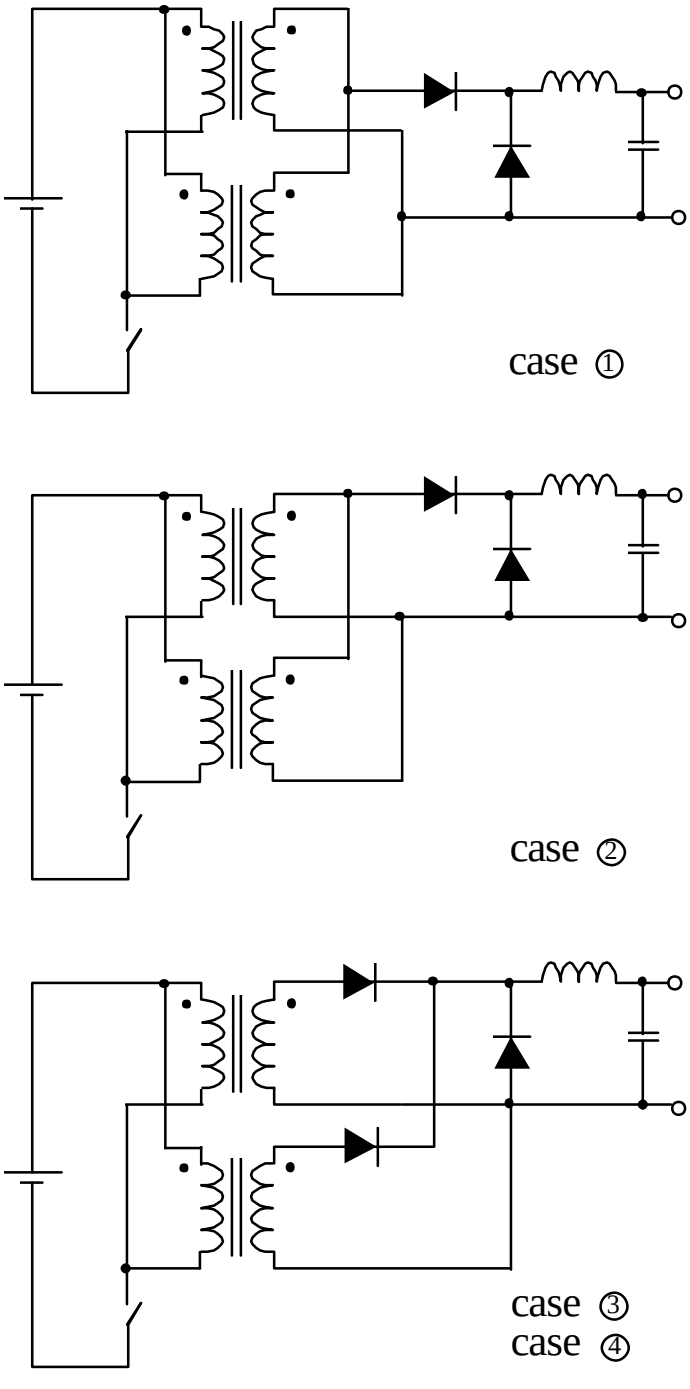


Figure 3.7. Four experimented configurations for current sharing measurement: (a) single forward diode with symmetrical layout; (b) single forward diode with asymmetrical layout; (c) separate forward diodes with asymmetrical layout (case ③ uses separate heatsinks and case ④ uses a common heatsink).

TABLE 3-I

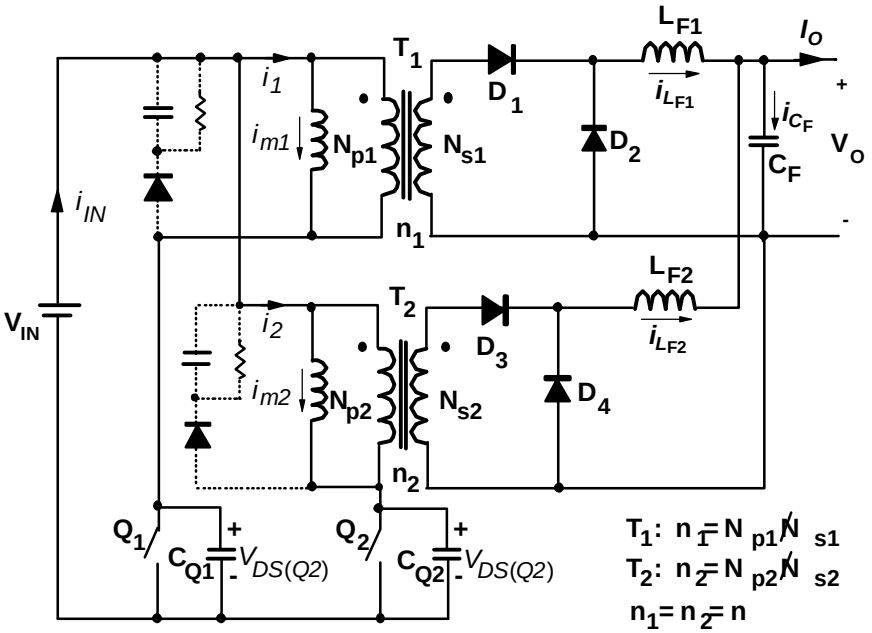
PARAMETERS AND CURRENT SHARING IN FOUR TESTED CONFIGURATIONS.

Configuration	Case ①	Case ②	Case ③	Case ④
	Parameter Mismatches			
R_1 [mΩ]	4.48	4.48		
R_2 [mΩ]	5.43	8.93		
R [mΩ]	4.96	6.71		
DR [mΩ]	0.48	2.23		
L_1 [nH]	18.86			
L_2 [nH]	20.56			
L [nH]	19.72			
DL [nH]	0.84			
	Current Sharing			
Analysis	1.21 : 1	1.99 : 1	1.16 : 1	1.10 : 1
Simulation	1.20 : 1	1.96 : 1	1.16 : 1	—
Measurement	1.2 : 1	2.0 : 1	1.2 : 1	1.1 : 1

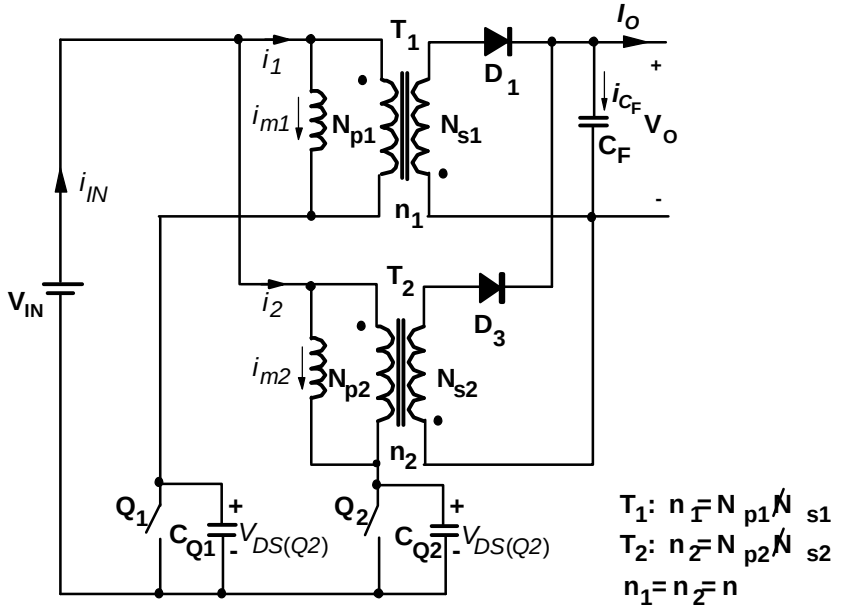
3.2. Interleaved Converters

The interleaving technique can be viewed as a variation of the paralleling technique, where the switching instants are phase-shifted over a switching period [B7]. Figures 3.8(a) and 3.8(b) show the typical interleaving implementations for forward and flyback converters. By introducing an equal phase shift between the paralleled power stages, the output-filter-capacitor ripple is lowered due to the ripple cancellation effect [B7]. At the same time, the effective ripple frequencies of the output-filter-capacitor current and the input current are increased by the number of interleaved modules. As a result, the size of the output filter capacitance can be minimized.

Generally, the interleaving in topologies with inductive output filters (forward-type) can be implemented in two ways. One interleaving approach is to directly parallel the outputs of the individual power stages so that they share a common output filter capacitor (the two-choke approach) [B11]. The other approach is to parallel the power stages at the input of a common LC output filter (the one-choke approach). The former approach distributes the transformer and output filter magnetics, while the latter approach distributes only the transformer magnetics [B11, B12]. Due to its distributed-magnetics structure and minimum-size output filter, the interleaving approach is especially attractive in high-power applications that call for high power-density and low-profile packaging, for example, distributed power modules (both front-end and load converters).



(a)



(b)

Figure 3.8. Interleaving implementations: (a) two-choke interleaved forward converter; (b) interleaved flyback converter.

3.2.1. Analysis of Operation of Interleaved Forward Converters

A. Two-Choke Approach

Two interleaved forward converters that utilize two complete forward converter modules (two-choke approach) are shown in Fig. 3.8(a), while the key waveforms are given in Fig. 3.9. In the implementation in Fig. 3.8(a), the reset of the transformers is done by the resonance between the magnetizing inductance of the transformers and the output capacitance of the MOSFETs (including external capacitance) [B13], or by an RCD-clamp reset circuit [B14], shown in dotted lines in Fig. 3.8(a). Since the two modules operate in anti-phase with duty cycles less than 50%, the current-sharing among the modules is ensured by employing the current-mode control. The operation principle of the interleaved converters in Fig. 3.8(a). is identical to that of the single resonant-reset or RCD-clamp reset forward converter. As can be seen from Fig. 3.9, the interleaving reduces the ripple current through the common output-filter capacitor.

B. One-Choke Approach

The one-choke approach, shown in Fig. 3.10, uses only one output inductor for the purpose of saving a magnetic component. Because in the one-choke interleaved forward converter the two modules share the same freewheeling diode and output filter, these two modules do not work independently. In fact, the operation of two interleaved forward converters with one choke is quite different from that of the two-choke interleaved converters. To facilitate the analysis of operation of the circuit in Fig. 3.10, the key waveforms of the one-choke interleaved forward converters with resonant reset are shown in Fig. 3.11.

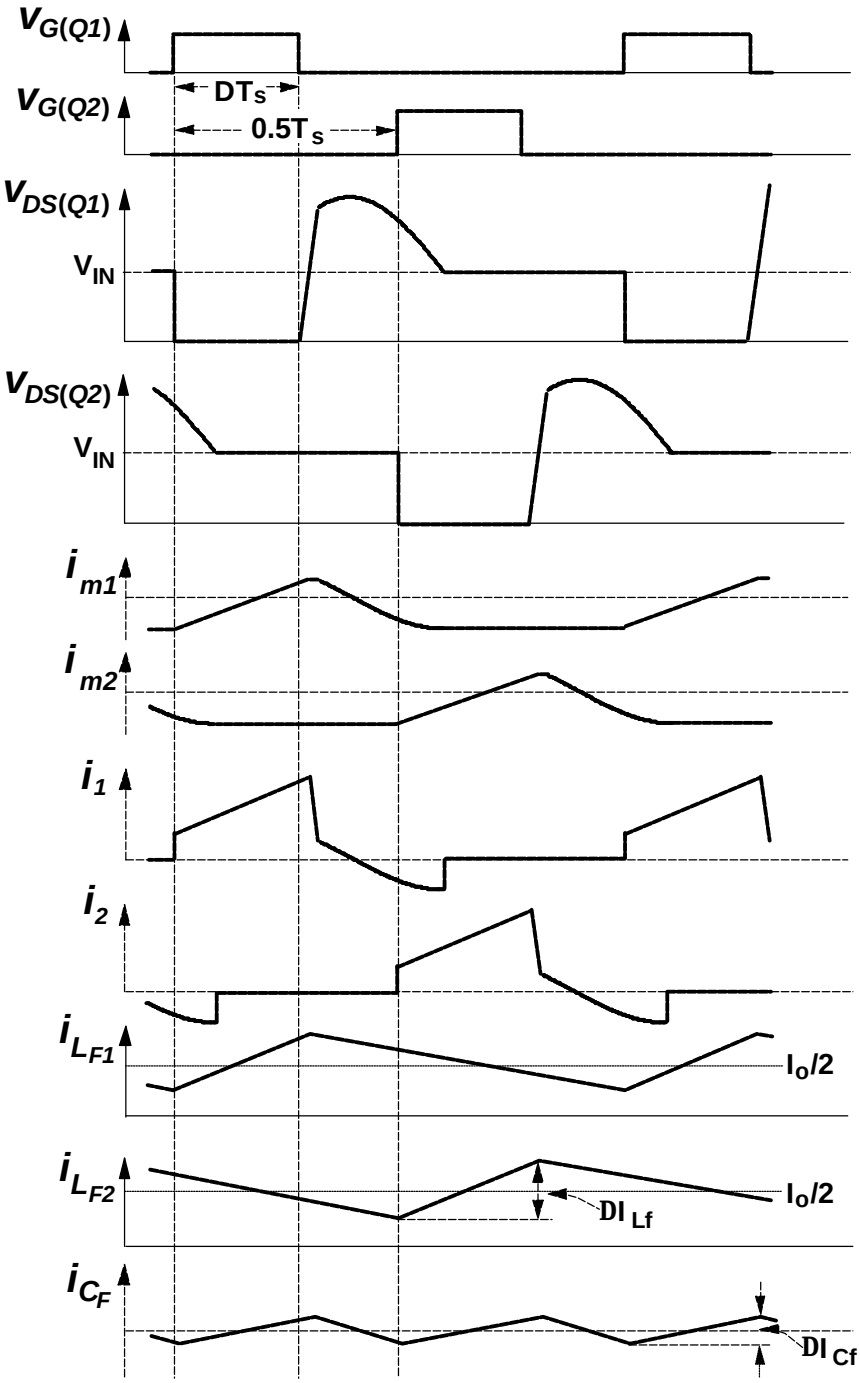


Figure 3.9. Key waveforms of two-choke interleaved forward converter.

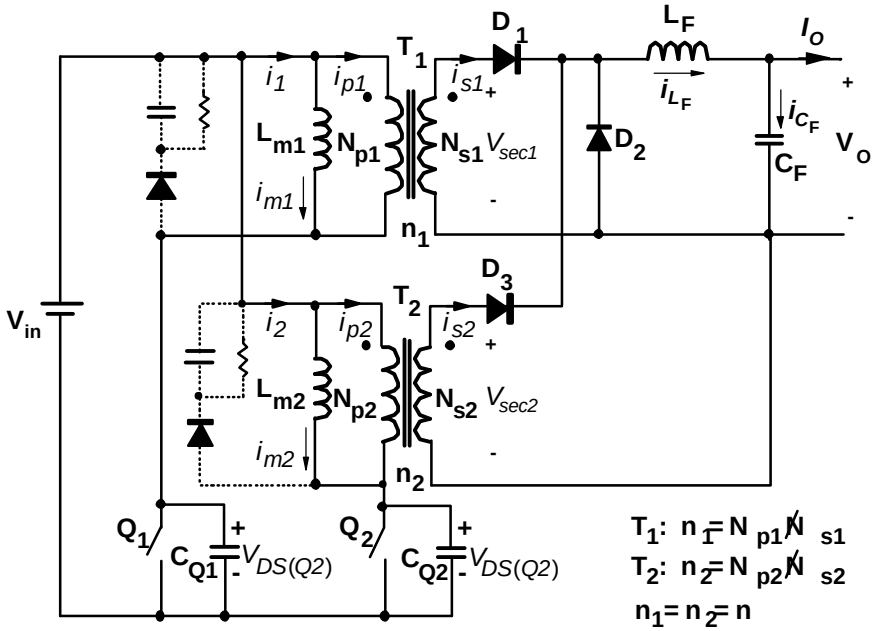


Figure 3.10. One-choke interleaved forward converter.

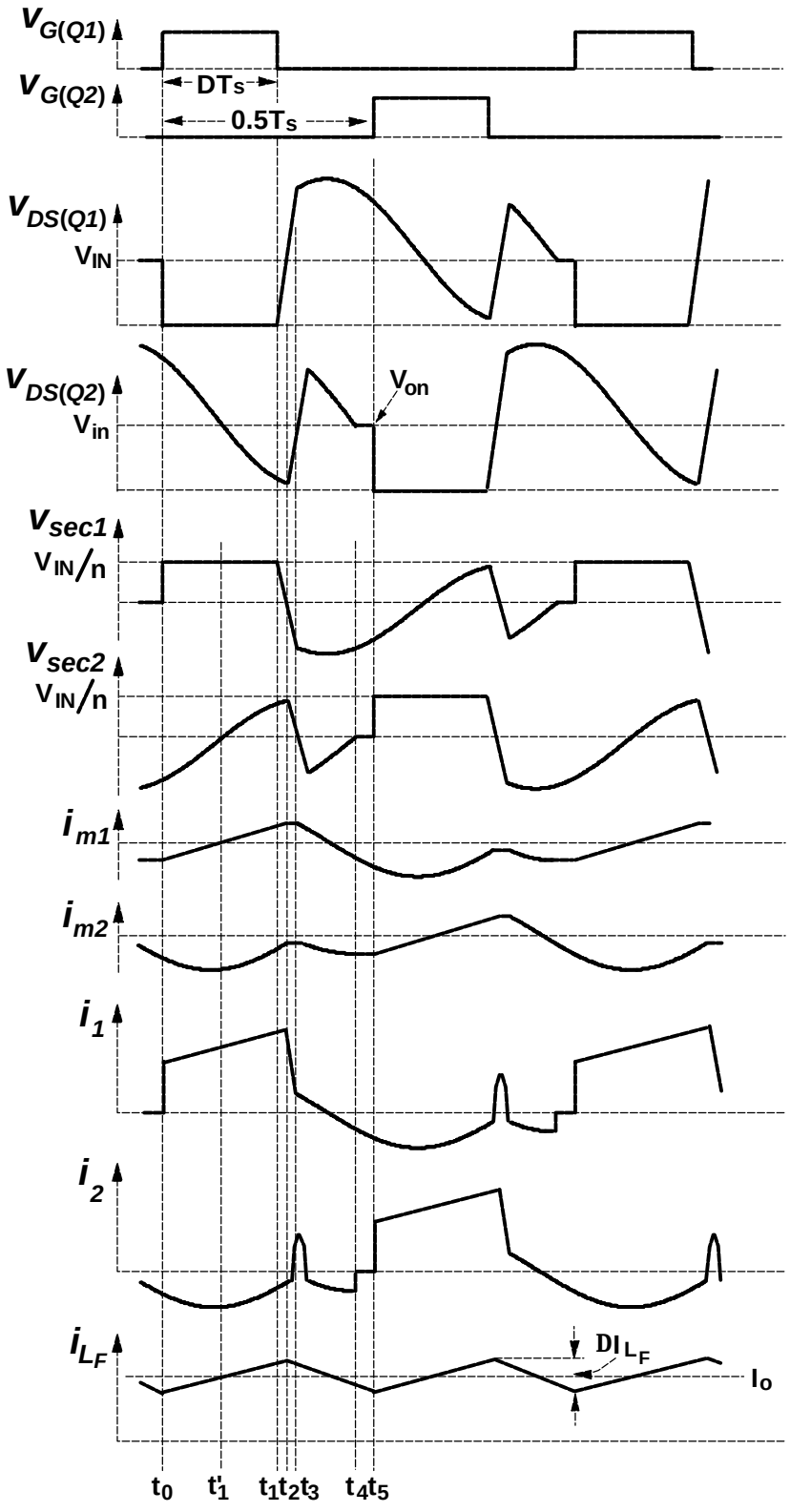


Figure 3.11. Key waveforms of one-choke interleaved forward converter.

To simplify the analysis, it is assumed that all semiconductor devices are ideal, i.e., they represent short circuits in their on states and open circuits in their off states. In addition, the transformers are modeled as ideal transformers with added magnetizing and leakage inductances. Finally, capacitors C_{Q1} and C_{Q2} shown in parallel with switches Q_1 and Q_2 represent the total capacitance connected between the drain-to-source terminals of the switches. Generally, C_{Q1} and C_{Q2} consist of a sum of the switch output capacitance (C_{oss}) and the externally added capacitance, if any.

In steady state, during a switching cycle, the circuit in Fig. 3.10 goes through five topological stages shown in Figs. 3.12(a)- 3.12(e). Immediately before switch Q_1 is turned on at $t = t_0$, filter inductor current i_{Lf} flows through freewheeling diode D_2. At the same time, diode D_3 is reverse-biased because the core of transformer T_2 is being reset and, consequently, V_{sec2} is negative.

Topological Stage A [t_0-t_1]

When switch Q_1 turns on at $t = t_0$, filter inductor current i_{Lf} commutates from freewheeling diode D_2 to forward diode D_1, as shown in Fig. 3.12(a). The commutation of i_{Lf} from D_2 to D_1 does not affect the conduction state of forward diode D_3, i.e., D_3 stays off. However, when D_1 starts conducting at $t = t_0$, the potential of the cathode of D_3 increases from 0 V (which is set by conducting D_2 prior to $t = t_0$) to $V_{sec1} = V_{IN} / n$. As a result, to turn D_3, on it is necessary that the potential of the D_3 anode reaches $V_{sec2} \geq V_{IN} / n$.

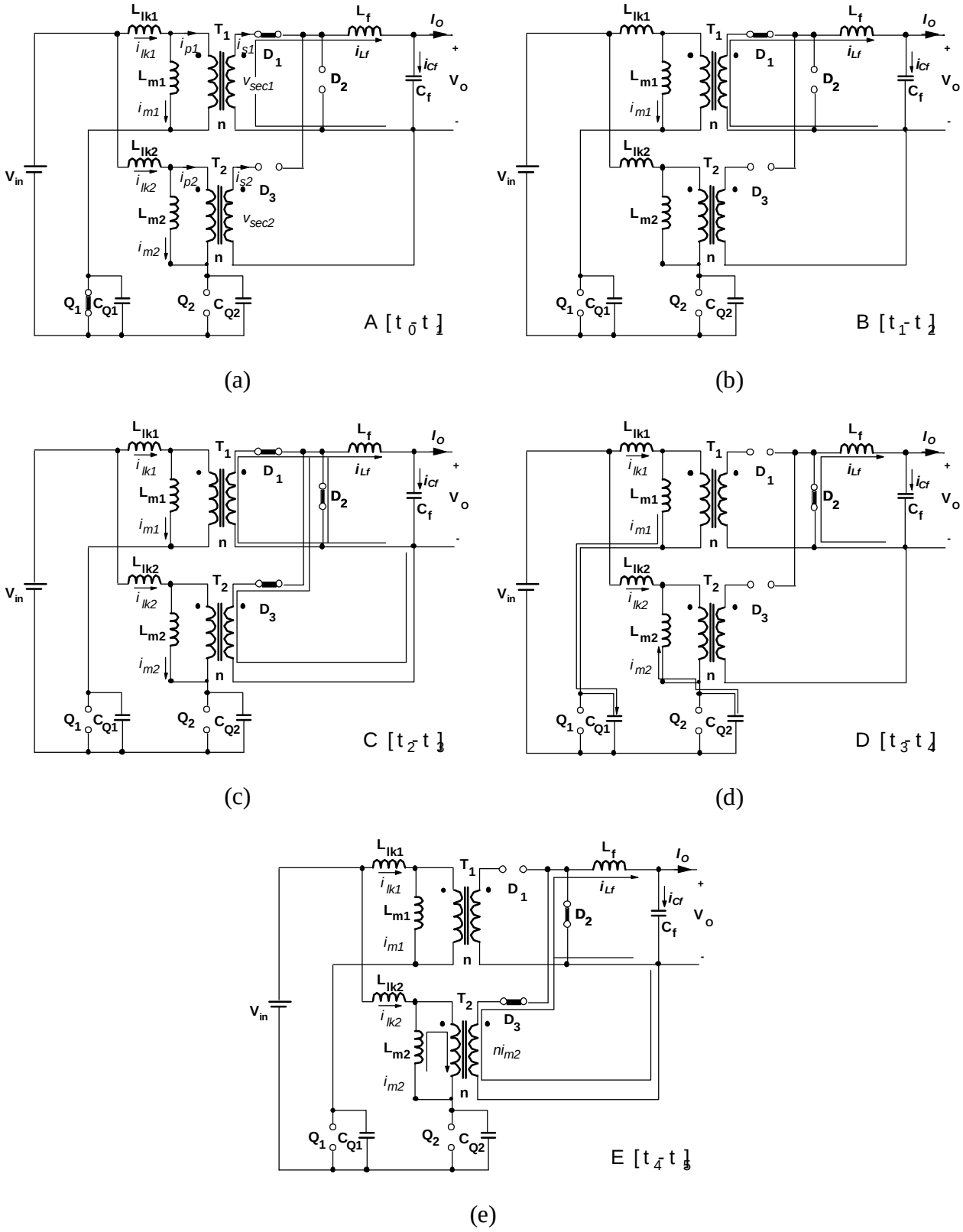


Figure 3.12. Equivalent topological stages (TS): (a) A [t_0-t_1]; (b) B [t_1-t_2]; (c) C [t_2-t_3]; (d) D [t_3-t_4]; (e) E [t_4-t_5].

Due to anti-phase operation, prior to switch Q_1 turn on at $t = t_0$, transformer T_2 is in its reset phase, i.e., a negative voltage is applied to the primary of the transformer because $V_{DS(Q2)} > V_{IN}$. The reset of the core of transformer T_2 continues after switch Q_1 is turned on and $V_{DS(Q2)}$ continues to decrease in a resonant fashion (determined by L_{m2} and C_{Q2} resonance) towards V_{IN}. In a single resonant-reset forward converter, or in interleaved forward converters with multiple chokes as in Fig. 3.9, the drain-to-source voltage of the switch, $V_{DS(Q)}$, cannot fall below the level of input voltage V_{IN} because of the clamping action of the forward diode [B14]. Namely, when $V_{DS(Q)}$ reaches V_{IN}, the forward diode becomes forward-biased and starts conducting the secondary-side reflected magnetizing current. Due to the simultaneous conduction of the forward diode and freewheeling diode (which carries the load current), the secondary winding is shorted and $V_{DS(Q)}$ is clamped to V_{IN}. However, in the circuit in Fig. 3.12(a), switch voltage $V_{DS(Q2)}$ during the transformer reset period can decrease below V_{IN} because the potential of the cathode of D_3 is raised to $V_{sec1} = V_{IN} / n$ by the conduction of D_1 so that D_3 is reverse-biased even when $V_{DS(Q2)} < V_{IN}$. As can be seen from Fig. 3.12, after reaching V_{IN} at $t = t_1'$ in Fig. 3.11, switch voltage $V_{DS(Q2)}$ continues to decrease below V_{IN} until topological state A ends at $t = t_1$, when switch Q_1 is turned off.

Topological Stage B [t_1-t_2]

After switch Q_1 is turned off at $t = t_1$, voltage $V_{DS(Q1)}$ starts resonating because capacitor C_{Q1} is charged by the sum of the magnetizing current and the reflected output-filter inductor current, i.e., $i_1 = i_{m1} + i_{Lf} / n$, as shown in Fig. 3.12(b). At the same time, $V_{DS(Q2)}$ continues to decrease below V_{IN} because transformer T_2 is still in the reset phase. This topological stage ends at $t = t_2$ when $V_{DS(Q1)}$ ramps up to V_{IN}.

Topological Stage C [t_2-t_3]

When $V_{DS(Q1)}$ reaches V_{IN} at $t = t_2$, freewheeling diode D_2 becomes forward-biased, and it starts conducting a part of the output-filter-inductor current i_{Lf}. Since during this interval both diodes D_1 and D_2 conduct simultaneously, as shown in Fig. 3.12(c), the secondary of transformer T_1 is shorted. As a result, leakage inductance L_{lk1} and capacitance C_{Q1} start resonating, which increases voltage $V_{DS(Q1)}$ above V_{IN}, as shown in Fig. 3.11. At the same time, the conduction of D_2 makes D_3 forward-biased because it lowers the potential of the cathode of D_3 to 0 V, while secondary voltage $V_{sec2} = [V_{IN} - V_{DS(Q2)}] / n$ is positive because at $t = t_2$, $V_{DS(Q2)} > V_{IN}$. Due to the conduction of D_3, the secondary of transformer T_2 is also shorted, and voltage $V_{DS(Q2)}$ increases at a fast rate because of the resonance between L_{lk2} and C_{Q2}, as shown in Fig. 3.11. This topological stage terminates at $t = t_3$, when the leakage-inductance current of T_1 becomes equal to the magnetizing current, i.e., $i_{lk1} = i_1 = i_{m1}$, causing diode D_1 to turn off.

Topological Stage D [t_3-t_4]

During this stage, both forward diodes D_1 and D_3 are off, and i_{Lf} is carried by freewheeling diode D_2, as shown in Fig. 3.12(d). As a result, transformer T_1 starts to reset through the L_{m1} - C_{Q1} resonance, while the L_{m2} - C_{Q2} resonance discharges C_{Q2}, forcing $V_{DS(Q2)}$ to decrease towards V_{IN}. This topological stage ends naturally at $t = t_4$ when $V_{DS(Q2)}$ decreases to V_{IN}. However, it should be noted that this stage may also end before $V_{DS(Q2)}$ reaches V_{IN} by the turn-on of switch Q_2, as illustrated in Fig. 3.12(b). In this case, a half-cycle operation is completed without the existence of topological stage E.

Topological Stage E [t_4-t_5]

When $V_{DS(Q2)}$ becomes equal to V_{IN} at $t = t_4$, diode D_3 becomes forward-biased, and magnetizing current $n \cdot i_{m2}$ starts flowing through D_3, as shown in Fig. 3.12(e). Due to the shorted secondary of T_2, i_{m2} stays constant during the entire duration of topological stage E. Also, during this stage, the core of transformer T_1 continues to reset. Topological stage E terminates at $t = t_5$, when Q_2 is turned on, and the other half of the switching cycle is initiated. During this half-cycle, the operation is identical to the above-described operation, except that the roles of switches Q_1 and Q_2 are exchanged.

The above analysis of the operation of the single-choke interleaved forward converter with the resonant resets can be directly extended to the single-choke interleaved forward converters with the RCD-clamp reset. In fact, the only difference between the two reset schemes is seen during the initial phase of the transformer core reset, after the primary switch is turned off. Specifically, with the RCD-clamp reset, primary switch voltage waveforms, $V_{DS(Q)}$, immediately after the switch is turned off (e.g. $t = t_4$ in Fig. 3.11), have a flat top (because of the clamping action of the RCD-clamp circuit) instead of a resonating waveform, as shown in Fig. 3.12. The clamping action lasts until the magnetizing current of the transformer falls to zero. After that instant, the RCD-clamp-reset circuit completes the core reset in the same fashion as the resonant-reset circuit.

Finally, it should be noted that the operation of the single-choke interleaved converter with the active-clamp reset is identical to the operation of a single converter, because for the active-clamp-reset forward converter the reset voltage is present during the entire off period. As a result, during the transformer reset period, the primary switch voltage is never lower than V_{IN},

which eliminates topological stage C, shown in Fig. 3.12(c), that makes the operation of one- and two-choke approaches very much different.

3.2.2. Component Size and Loss Comparisons

A. Magnetic Component Size Comparisons

From the preceding analysis of operation and key waveforms shown in Fig. 3.12, it can be seen that during the on-time of the primary switch, the output-filter inductor current (whose average is load current I_o) of two interleaved forward converters with one choke flows through the module with the conducting switch. On the other hand, in the two-choke interleaved circuit, only one-half of the load current flows through each module. Nevertheless, the primary-switch current in both implementations are the same, because the turns ratio of the transformers in the one-choke implementation can be twice as high as that in the two-choke implementation. Namely, in the one-choke implementation, the input of the output filter "sees" the voltage waveform which has the frequency that is twice the switching frequency. As a result of doubled volt-second product at the input of the output filter, the turns ratio of the transformers in the one-choke implementation can be doubled compared to that of the two-choke implementation with the same duty cycle.

Finally, it should be noted that the transformer flux excitation is different in the one- and two-choke approaches. Specifically, as can be seen from V_{sec1} and V_{sec2} waveforms in Fig. 3.12, the transformer in the one-choke implementation exhibits two periods with positive volt-second

product during a switching cycle. Therefore, the operating point of the transformer core goes through two minor B-H loops, which create a small additional core loss.

To compare the sizes of the output inductors in the two interleaved approaches, the inductor current ripples need to be determined first. For the two-choke approach, the current ripple in each inductor shown in Fig. 3.9 is

$$DI_{Lf(2L)} = \frac{V_o(1-D)}{L_{f(2L)} \cdot f_s}, \tag{3-10}$$

where V_o is the output voltage, $L_{f(2L)}$ is the output-filter inductance, and f_s is the switching frequency. With the inductor current ripple cancellation, the ripple current of the output-filter capacitor becomes

$$DI_{Cf(2L)} = \frac{V_o(1-2D)}{L_{f(2L)} \cdot f_s}, \tag{3-11}$$

which is lower than that in Eq. (3-10).

Since the size of an inductor is proportional to its stored energy, the combined volume of the two output-filter inductors is proportional to the total stored energy:

$$E_{(2L)} = 2\left[\frac{1}{2} L_{f(2L)} (\frac{I_o}{2})^2\right], \tag{3-12}$$

where I_o is the output current. Calculating $L_{f(2L)}$ from Eq. (3-11) and substituting it in Eq. (3-12) yield

$$E_{(2L)} = \frac{V_o I_o^2}{4DI_{Cf(2L)} f_s}(1-2D). \tag{3-13}$$

Since in the one-choke approach, the effective frequency "seen" by the output LC filter is twice the switching frequency, the output-filter-inductor current ripple, shown in Fig. 3.11, is

$$DI_{Lf(1L)} = \frac{V_o(1/2-D)}{L_{f(1L)} \cdot f_s}. \tag{3-14}$$

Because no ripple-cancellation effect is present in the one-choke approach, the output-filter capacitor current is also given by Eq. (3-14), i.e.,

$$DI_{Lf(1L)} = DI_{Cf(1L)} = \frac{V_o(1-2D)}{2L_{f(1L)} \cdot f_s}. \tag{3-15}$$

Finally, the filter-inductor size of the one-choke implementation is proportional to

$$E_{(1L)} = \frac{V_o I_o^2}{4DI_{Cf(1L)} f_s}(1-2D). \tag{3-16}$$

Comparing Eqs (3-13) and (3-16), it can be seen that with the same specifications and the same duty-cycle, the two implementations will have the output inductors of the same size, provided that both implementations are designed to have the same capacitor ripple currents DI_C.

As explained earlier, the turns-ratio of the transformers in the one-choke implementation is double that in the two-choke approach ($n_{(1L)} = 2 \cdot n_{(2L)}$), while the primary currents in both implementations are the same. As a result, if the same size core and the same number of

secondary turns are used in both implementations, the one-choke implementation has flux excursion which is only one-half of that in the two-choke approach. Consequently, the core loss of the one-choke approach is lower. Also, the smaller flux excursion in the one-choke approach creates an opportunity to reduce the size of the transformer by having a trade-off between the size and core loss. However, the size reduction of the transformer in the one-choke approach is limited by the available winding area to fit the increased number of primary turns.

B. Loss Comparisons

Because the output power in the two-choke approach is evenly distributed between the two interleaved modules, the total conduction losses of the transformers, the primary switches, and the rectifiers are

$$P_{(2L)}^{cond} = 2\left\{\left[\left(\frac{I_o}{2n_{(2L)}}\right)^2 R_{pri(2L)} + \left(\frac{I_o}{2}\right)^2 R_{sec(2L)} + \left(\frac{I_o}{2n_{(2L)}}\right)^2 R_{DS(on)}\right]D + V_F\,\frac{I_o}{2}\right\}. \quad (3\text{-}17)$$

where $R_{pri(2L)}$ and $R_{sec(2L)}$ are the primary- and secondary-winding resistances of the transformers, respectively, $R_{DS(on)}$ is the on-resistance of the primary switches, and V_F is the forward-voltage drop of the rectifiers.

Similarly, because the output current in the one-choke implementation flows through only one module during the on-time, the conduction losses are given by

$$P_{(1L)}^{cond} = 2\left[\left(\frac{I_o}{n_{(1L)}}\right)^2 R_{pri(1L)} + I_o^2 R_{sec(1L)} + \left(\frac{I_o}{n_{(1L)}}\right)^2 R_{DS(on)}\right]D + V_F I_o\,, \quad (3\text{-}18)$$

where $R_{pri(1L)}$ and $R_{sec(1L)}$ are the primary- and secondary-winding resistances of the transformers, respectively. If the two converters are designed to have the same duty cycles and $n_{(1L)} = 2 \cdot n_{(2L)}$, the conduction losses on the primary side, i.e., the primary-switch and primary winding losses, are the same. Assuming that rectifier-loss difference between the one- and two-choke implementations is small, the conduction loss difference for $n_{(1L)} = 2 \cdot n_{(2L)}$ can be calculated from Eqs. (3-17) and (3-18) as

$$DP^{cond} = (2R_{sec(1L)} - \frac{1}{2} R_{sec(2L)}) I_o^2 D \,. \tag{3-19}$$

Generally, the difference between the switching losses of the primary switches in the one-choke and two-choke implementations is caused by the differences in the capacitive turn-on switching losses. Namely, the turn-on and turn-off switching losses due to the overlapping primary-switch voltages and currents are the same in both implementations because in both implementations the primary switches conduct the same current and block the same voltages if $n_{(1L)} = 2 \cdot n_{(2L)}$. However, the capacitive turn-on switching losses may be different because the primary switches in the two implementations may be turned on while having different voltages across them.

In fact, according to Fig. 3.9, the primary switches in the two-choke implementation always turn on with the voltage across the switch equal to input voltage V_{IN}. As a result, the total capacitive turn-on switching loss of two interleaved modules is given by

$$P_{(2L)}^{sw} = 2(\frac{1}{2} C_Q V_{IN}^2) f_s \,. \tag{3-20}$$

In the one-choke implementation, the primary switches may turn on when their voltages are larger than V_{IN}, generating the capacitive turn-on switching loss:

$$P_{(1L)}^{sw} = 2(\frac{1}{2} C_Q V_{on}^2) f_s, \qquad V_{on} \geq V_{IN}, \tag{3-21}$$

where V_{on} is the voltage across the switches at the moment of turn-on. Therefore, the difference in the switching losses of the two interleaving implementations is

$$DP^{sw} = (C_{Q(1L)} V_{on}^2 - C_{Q(2L)} V_{in}^2) f_s, \qquad V_{on} \geq V_{IN}. \tag{3-22}$$

From Eq. (3-22), it can be seen that if $C_{Q(1L)} = C_{Q(2L)}$ the capacitive turn-on switching loss of the one-choke implementation is higher than or equal to that of the two-choke implementation because $V_{on} \geq V_{IN.}$

3.3. Experimental Evaluations

Evaluations of the discussed one-choke and two-choke interleaved forward converters were performed on 300 kHz, 5-V/40-A power stages designed to operate in the 40-60 Vdc input voltage range. The components used in the implementations of the power stages of the two-choke implementation, shown in Fig. 3.8(a), and the one-choke implementation, shown in Fig. 3.10 are summarized in Table 3-II. As can be seen from Table I, due to a larger number of primary turns, the leakage inductances of the transformers in the one-choke implementation are

TABLE 3-II

COMPONENT LIST OF POWER STAGES OF TWO-CHOKE AND ONE-CHOKE IMPLEMENTATIONS

		Two-Choke Implementation	One-Choke Implementation
Q_1, Q_2		IRF640 (International Rectifier)	
D_1, D_2		82CNQ30 (International Rectifier)	
T_1, T_2	core:	TDK PC30LP23/8Z-12	
	primary	9 turns of 4 stands of #26 wire	12 turns of 3 stands of #26 wire
	secondary	3 turns of 3 mils Cu foil	2 turns of 3 mils Cu foil
	Lm	108 µH	214 µH
	L_{lk}	200 nH	325 nH
	R_{sec}	6.7 mΩ	3.4 mΩ
C_{Q1}, C_{Q2}		1 nH ceramic	3.3 nH ceramic
L_{F1}, L_{F2}	core	Magnetics MPP55304	Magnetics Kool Mµ^{TR} 77310
	winding	10 turns of 2 stands of #17 wire	4 turns of 5 stands of #17 wire
	inductance	10.5 µH	3.85 µH
C_F		4400 µF electrolytic	

larger than those of the two-choke approach. As a result, to keep the same voltage stress on the primary switches in both implementations, larger resonant capacitances C_{Q1} and C_{Q2} are selected in the one-choke implementation.

Figure 3.13 shows the oscillogram of the primary-switch voltages of the two-choke interleaved forward converters. As can be seen from Fig. 3.13, the switches always turn on when the voltage across them is equal to the input voltage, i.e., $V_{on} = V_{IN}$.

Figure 3.14 shows the oscillograms of the primary-switch voltages of the one-choke implementation at full load and 50% of the full load. As can be seen from Fig. 3.14(a), at full load the primary switches turn on when the voltage across them is higher than V_{IN}. Specifically, the switches turn on with $V_{on} \approx 122$ V, although $V_{IN} = 50$ V. However, at the half of full load, the switches turn on with $V_{on} \approx V_{IN}$, as shown in Fig. 3.14(b). In addition, at half load, the resonance between L_m and C_Q never takes switch voltage $V_{DS(Q)}$ significantly below V_{IN} because of insufficient energy stored in the L_{lk}, as seen in Fig. 3.14(a). On the other hand, at full load, the energy stored in L_{lk} is more than sufficient to resonate $V_{DS(Q)}$ all the way down to 10-20 V, as shown in Fig. 3.14(b).

The measured full-load efficiencies of the one- and two-choke implementations as functions of the input voltage are shown in Fig. 3.15. As can be seen, the efficiency of the two-choke implementation is higher than the efficiency of the one-choke implementation in the entire input-voltage range. Moreover, the efficiency of the one-choke implementation is a strong function of the input voltage, while the efficiency of the two-choke implementation is almost independent of the input voltage. In fact, according to Fig. 3.15, the two-choke circuit is around

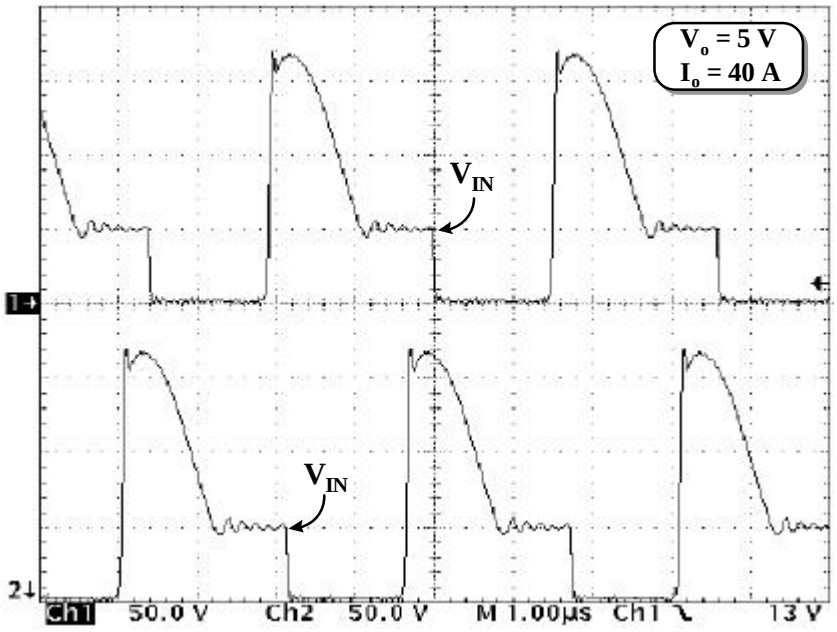
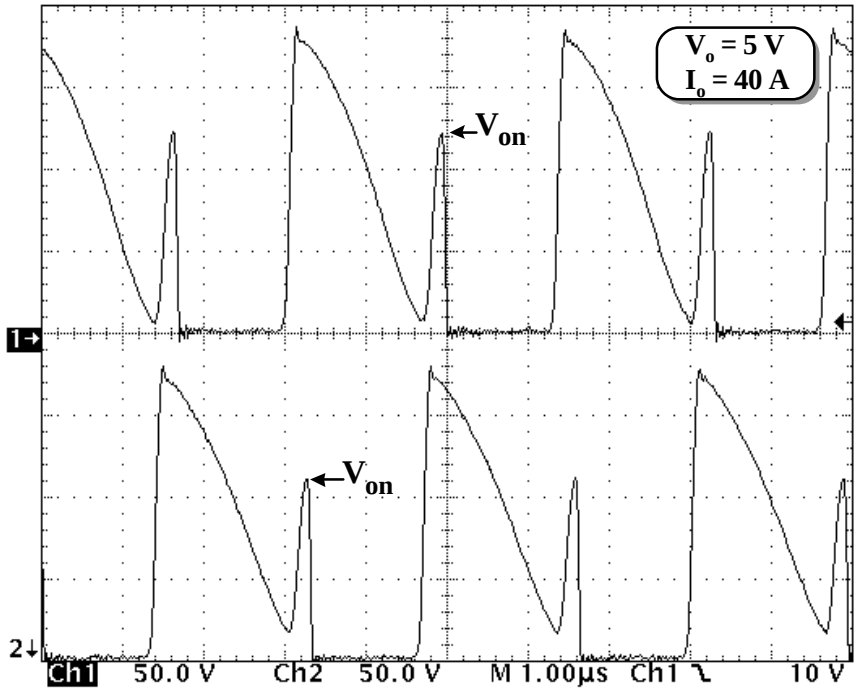
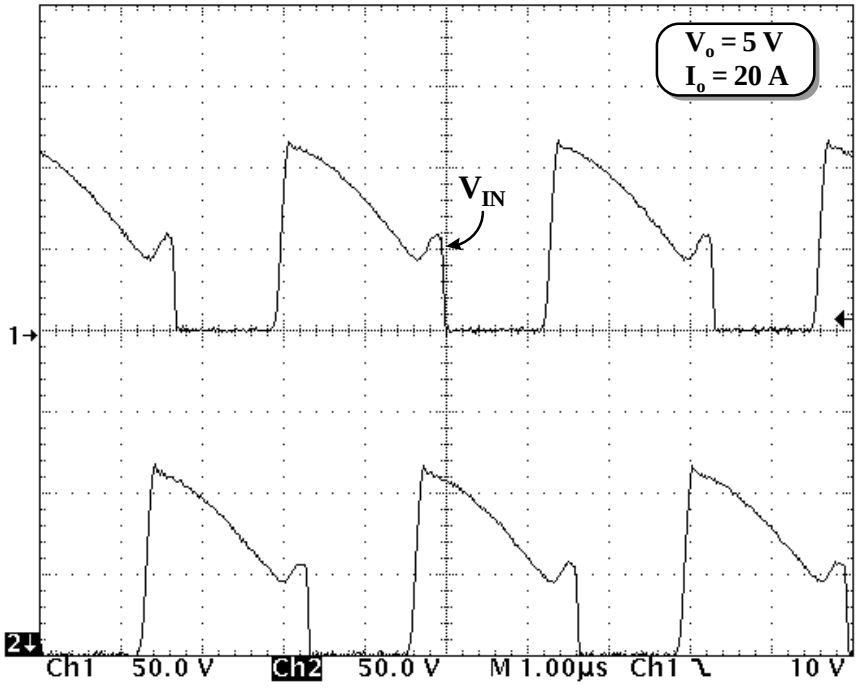


Figure 3.13. Experimental $V_{DS(Q1)}$ and $V_{DS(Q2)}$ waveforms of two-choke implementation for V_{IN} = 50 V. Scales: $V_{DS(Q1)}$ = 50 V/div.; $V_{DS(Q2)}$ = 50 V/div.; time = 1 µs /div.



(a)



(b)

Figure 3.14. Experimental $V_{DS(Q1)}$ and $V_{DS(Q2)}$ waveforms of one-choke implementation for V_{IN} = 50 V: (a) at full load I_o = 40 A; (b) at 50% of full load I_o = 20 A. Scales: $V_{DS(Q1)}$ = 50 V/div.; $V_{DS(Q2)}$ = 50 V/div.; time = 1 µs /div.

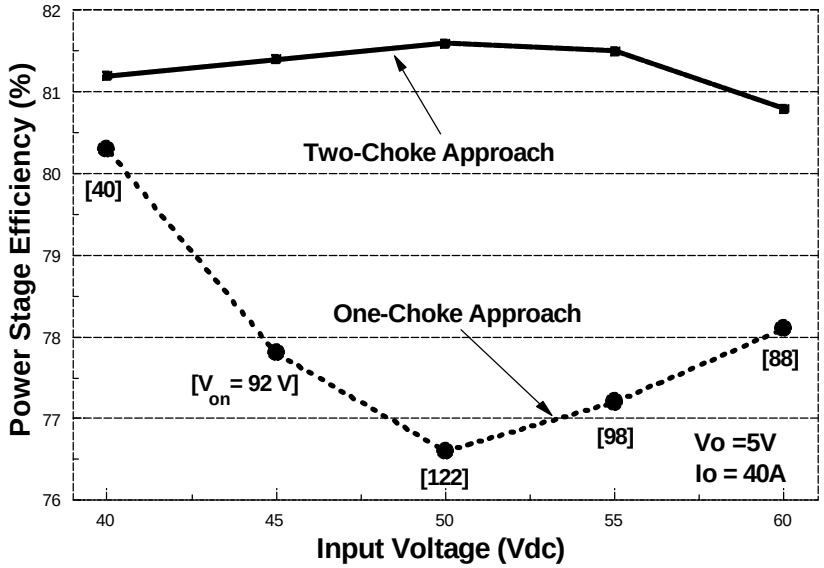


Figure 3.15. Measured full-load efficiencies of one-choke and two-choke implementations as functions of input voltage. For one-choke implementation V_{on} values for each measured point are indicated. For two-choke implementation $V_{on} = V_{IN}$.

1% more efficient than the one-choke circuit at V_{IN} = 40 V, and approximately 5% more efficient at V_{IN} = 50 V. The input-voltage dependence of the efficiency of the one-choke implementation is caused by increased conduction and particularly switching losses compared to the corresponding losses in the two-choke circuit. The conduction loss difference is brought about by the secondary winding resistance difference between the transformers in the two implementations, while the switching loss difference is caused by the difference in the switch voltage at the turn on. For example, by using component values from Table I, the duty cycles of the primary switches (which are the same in both implementations) at V_{IN} = 50 V can be calculated from

$$D = \frac{n_{(2L)}V_o}{V_{IN}} = \frac{2n_{1-L}V_o}{V_{IN}} = \frac{3 \cdot 5}{50} = 30\% . \tag{3-23}$$

According to Eq. (3-19), the conduction loss increase of the one-choke implementation over the two-choke implementation at full load of 40 A can be calculated as

$$DP^{cond} = (2 \cdot 3.4 \cdot 10^{-3} - \frac{1}{2} \cdot 6.7 \cdot 10^{-3}) 40^2 \cdot 0.3 = 1.7 \ W . \tag{3-24}$$

To calculate the capacitive turn-on switching loss difference of the two implementations, Fig. 3.15 also shows measured primary-switch voltages at turn-on, V_{on}, for each measured point of the one-choke circuit. For example, for V_{IN} = 40 V, V_{on} = 40 V, i.e., $V_{IN} = V_{on}$. However, for V_{IN} = 50 V, V_{on} = 122 V » V_{IN}. In fact, by applying Eq. (3-22), the increased switching loss of the one-choke approach is

$$DP^{sw} = (3.3 \cdot 10^{-9} \cdot 122^2 - 1 \cdot 10^{-9} \cdot 50^2) \cdot 300 \cdot 10^3 \approx 14.0 \ W , \tag{3-25}$$

at V_{IN} = 50 V and I_o = 40 A. Therefore, the one-choke implementation dissipates approximately 15.7 W more than the two-choke implementation. The calculated power dissipation is in a very good agreement with the experiment data, because at V_{IN} = 50 V, the measured efficiencies are 81.5% and 76.8% for the one- and two-choke implementations, respectively. This efficiency difference corresponds to a 15.5-W power dissipation difference.

In addition to the fact that the one-choke interleaved forward converter with resonant reset or RCD-clamp reset has a lower conversion efficiency compared with the two-choke interleaved forward converter, the achievable power-density of the one-choke approach is thermally limited by the lower efficiency. The relationship between power conversion efficiency and achievable power-density is shown in Figs. 4.3(a) and 4.3(b), which reveals that power density is severely penalized by a poor efficiency. Therefore, although one-choke approach has the same filter-inductor size and low-profile transformers, the overall power-density will be not as high as that of the two-choke approach.

3.4. Summary

Paralleling techniques can be used to design high-power, low-profile converters by using a number of low-power, low-profile transformers. For good current sharing, the resistance of the paralleled transformers (including trace resistance) should be matched. Using a common heat sink and/or synchronous rectifiers can ensure good current sharing. Interleaving provides the

additional advantage of ripple current cancellation and ripple frequency doubling for further filter size reduction. Analysis, design, and performance evaluations of two interleaved forward converters with common output-filter inductor (one-choke approach) and separate output-filter inductors (two-choke approach) are presented. It was shown that the operation of the one-choke implementation of the two interleaved forward converters with the resonant or RCD-clamp resets is quite different from that of the corresponding one-choke implementation. In addition, the two interleaved approaches were compared with respect to their output filter sizes and power losses. It was shown that the one-choke approach is less efficient than the two-choke approach.