Chapter 3
Spacecraft Design Guidelines

Section 3.1 describes processes involved in immunizing a spacecraft against spacecraft charging problems. Section 3.2 lists design guidelines. If the reader wishes to make a requirements document, the basic requirements include:

a. Determine whether or not the mission passes through or stays in regions with a charging threat.

b. If in a charging threat region, determine the threat that is applicable to that environment.

c. Implement measures to mitigate the threat to an acceptable level.

Sections 3.2.1 (General ESD Design Guidelines), 3.2.2 (Surface ESD Design Guidelines, Excluding Solar Arrays), 3.2.3 (Internal ESD Design Guidelines), 3.2.4 (Solar Array ESD Design Guidelines), and 3.2.5 (Special Situations ESD Design Guidelines) can be used as aids.

3.1 Processes

The system developer should demonstrate through design practices, test, and analysis that spacecraft charging effects will not cause a failure to meet mission objectives. This section briefly discusses those processes.

3.1.1 Introduction

The classic approach to avoiding or eliminating electromagnetic problems is to look at the source of the problem, the victim, and the coupling between them. In the case of space charging, excess electrons deposit on surface or external spacecraft areas or penetrate directly to victim circuit areas, the charge being

buried in a circuit board immediately adjacent to the victim. As a result, the three elements (source, coupling, and victim) are not always clearly distinguishable. For that reason, this book has disregarded these categories; however, this approach may sometimes be fruitful and is described below for completeness.

3.1.1.1 Source

The basic source of in-space charging problems is the charged particle environment (CPE). If that environment cannot be avoided, the next sources of ESD threats are items that can store and accumulate charge and/or energy. Ungrounded (isolated) metals are hazardous because they can accumulate charge and energy. Excellent dielectrics can accumulate charge and energy as well. Limiting the charge storing material or charging capacity is a useful method for reducing the internal charging threat. This can be accomplished by providing a bleed path so that all plasma-caused charges can equalize throughout the spacecraft or by having only small quantities of charge-storing materials.

3.1.1.2 Coupling

Coupling energy from a source via a spark (ESD) is very configuration-dependent and a function of the radiated and directly coupled signals. An ESD can occur in a variety of ways, such as from metal-to-metal, metal-to-space, metal-to-dielectric, dielectric-to-dielectric, dielectric breakdown, etc. The configuration of the charges determines the type of breakdown and hence the form of coupling. An isolated conductor can discharge directly into an IC lead causing serious physical damage at the site, or the arc can induce an attenuated signal into a nearby wire causing little damage but inducing a spurious signal. As these examples illustrate, the coupling must thus be estimated uniquely for each situation. Eliminating coupling paths from a spark source to a victim will significantly lower the ESD threat. Coupling paths could be eliminated by separation, shielding, or filtering.

3.1.1.3 Victim

A victim is any part, component, subsystem, or element of a spacecraft that can be adversely affected by an arc discharge (or field effects, in the case of some science instruments). Given the different effects of ESDs, the types and forms of victims can be highly variable. ESD and electromagnetic compatibility (EMC)-induced parts failures, while major problems, are not the only ones. Effects can range from the so-called soft errors; e.g., a memory element may be reset, to actual mechanical damage where an arc physically destroys material. Thus, the victims can range from individual parts to whole systems, from electronic components to optical parts. (Discharging in glass has long been

known to cause fracturing and damage to optical windows or dielectrics, but empirical data suggests that optical lenses have apparently had a largely successful usage in space.) The major victims and design sources will be either individual electronic components or cables that can couple the transient voltage into a subsystem. Shielding or filtering at the victim will limit the adverse effects of ESDs.

3.1.2 Design

The designer should be aware of design guidelines to avoid surface and internal charging problems (Sections 3.2.2 and 3.2.3). All guidelines should be considered in the spacecraft design and applied appropriately to the given mission.

3.1.3 Analysis

Analysis should be used to evaluate a design for charging in the specified orbital environment. There are two major approaches to such analysis: a simple analysis and a detailed analysis, perhaps with a computer code. A very simple analysis of internal electrostatic charging is illustrated in Appendix D. Several appropriate computer transport codes are listed in Appendix C.2. An example of a simple surface charging analysis is described in Appendix G.

3.1.4 Test and Measurement

Testing usually ranks high among the choices to verify and validate the survivability of spacecraft hardware in a given environment. For spacecraft charging environments, it is difficult to replicate the actual energetic plasma and total threat in all respects. The real electron environment can envelop the whole of the spacecraft and has a spectrum of energies. There is no test facility that can replicate all the features of that environment. As a consequence, verification and validation of charging protection are done with lower level hardware tests and with less realistic test environments. This does not reduce the value of the tests, but additional analyses must be done to provide design validation where testing alone is inadequate. Several tests that can be performed to validate different aspects of charging are briefly described below.

3.1.4.1 Material Testing

Material electrical properties should be known before they are used. The key material properties needed are the ability to accumulate charge, i.e., resistivity or conductivity, and the pulse threat, e.g., stored voltage, energy. Secondary but important parameters include resistivity changes with time in space, temperature (cold is more resistive), and, to a lesser extent, radiation-induced and E-field-induced conductivity. Other properties are secondary electron

emission, backscatter emission, and photoelectron emission properties. Surface contamination of materials in space also changes their charging behavior.

Information about these parameters can be obtained from reference texts or by electron beam tests or conventional electrical tests. (Section 6.1 contains a sample dielectric materials list.) Analysis or tests can be used to determine the threat for particular sizes and shapes of these materials. Some test methods are described in Appendix E.

3.1.4.2 Circuit/Component Testing

The susceptibility threshold of components (transistors, ICs, etc.) is useful in understanding the threat from ESD events. The susceptibility can be a disruption threshold or a damage threshold. A Vzap test (Appendix Section E.8) can be used to determine an electronic device's capability to withstand the effects of an electrical transient.

3.1.4.3 Assembly Testing

Potentially susceptible assemblies should be tested for sensitivity to ESD. The assembly to be tested is to be mounted on a baseplate and tested while operating. Pulses are to be injected through the box of the assembly or injected into the pins of the connector while the performance of the assembly is monitored for upsets. The pulses used are to cover the expected range of current amplitudes, voltages, and pulse durations. It is very important that the pulse injection device be isolated electrically from the assembly being tested and the monitoring equipment. It is also important to ensure the transient is not disturbing the support equipment.

3.1.4.4 System Testing

System-level testing is often the final proof that a system can survive a given environment. For IESD environments, system testing is not feasible. Materials, circuit, and assembly testing, together with analysis, must provide the system-level verification for internal charging concerns.

3.1.5 Inspection

Inspection is an important means for recognizing and minimizing the possibility of spacecraft charging discharge-induced anomalies. This inspection should be conducted as the spacecraft is being assembled by a person experienced in recognizing likely areas of concern from environmentally induced interactions. A list of acceptable values of resistance for joints and connections within the spacecraft should be generated ahead of the inspection, but the inspection should take a broader view and look for other possible areas of concern.

3.2 Design Guidelines

This section contains general guidelines and quantitative recommendations on design guidelines/techniques that should be followed in hardening spacecraft systems to spacecraft charging effects. This section contains design guidelines divided into subsections for General (Section 3.2.1), Surface Charging (Section 3.2.2), Internal Charging (Section 3.2.3), Solar Arrays (Section 3.2.4), and Special Situations (Section 3.2.5).

3.2.1 General ESD Design Guidelines

3.2.1.1 Orbit Avoidance

If possible, avoid orbits and altitudes where charging is an issue. Usually, this is not an option (Fig. 1-1 and Fig. 1-2 show hazardous environments near Earth).

3.2.1.2 Shielding

Shield all electronic elements with sufficient aluminum-equivalent thickness so that the internal charging rate is benign. Experience has shown that for GEO orbits and today's hardware, an adequate shielding level has been on the order of 110 mil of aluminum-equivalent shielding, but 200 mil is more conservative and may be necessary for certain situations (Section 3.2.3.2.2). For some ESD-immune hardware, the amount needed may be less; it almost certainly will exceed 33 mil but may be as low as 70 mil. This is the total shielding, accounting for geometry. A more accurate determination can be done by ray tracing using radiation shielding codes capable of handling detailed geometric and spacecraft material descriptions, and comparing results to the sensitivity of possible victims.

Shield all electronic elements in a Faraday cage construction. The primary spacecraft structure, electronic component enclosures, and electrical cable shields should provide a physically and electrically continuous shielded surface around all electronics and wiring (Faraday cage). The primary spacecraft structure should be designed as an electromagnetic-interference- (EMI-) tight shielding enclosure (Faraday cage). The purposes of the shielding are to prevent entry of charged particles into the spacecraft interior and to shield the interior electronics from the radiated and conducted noise of an electrical discharge on the exterior of the spacecraft. All shielding should provide at least 40-decibel (dB) attenuation of radiated electromagnetic fields associated with surface discharges. An approximately 40-mil thickness of aluminum or magnesium will easily provide the desired attenuation if made electromagnetically tight. This enclosure should be as free from holes and penetrations as possible. Many penetrations can be closed by use of well-grounded metallic meshes and plates.

All openings, apertures, and slits should be eliminated to maintain the integrity of the Faraday cage.

The vacuum deposited aluminum (VDA) metallization on multilayer insulation (MLI) thermal blankets is insufficient to provide adequate shielding for both EMC and internal charging. Layers of aluminum foil mounted to the interior surface and properly grounded can be used to increase the shielding effectiveness of blankets or films. Aluminum honeycomb structures and aluminum face sheets can also provide significant attenuation. Electronic enclosures and electrical cables exterior to the main Faraday cage region should also be shielded to extend the coverage of the shielded region to 100 percent of the electronics. Unless all seams, penetrations, gaps, etc., are shielded with a totally connected conductive skin, the Faraday cage implementation is incomplete and cannot be counted as proper protection to the interior electronics. For example, a viewing aperture of a star tracker is a penetration. Another example is a "mouse hole" for cable penetrations. All must be given careful attention as to the effects of the violation of the Faraday-Cage principle.

Cable shields exterior to the Faraday cage are used to maintain and extend the cage region from their exit/entrance of the main body of the spacecraft. Cable shields should be fabricated from aluminum or copper foil, sheet, or tape. Standard coaxial shielding or metalized plastic tape wraps on wires do not provide adequate shielding protection for internal charging protection and should not be used. Shields should be terminated when they enter the spacecraft structure from the outside and carefully grounded at the entry point with a 360-deg EMC connector. Braid shields on wires should be soldered to any overall shield wrap and grounded at the entrances to the spacecraft. Conventional shield grounding through a connector pin to a spacecraft interior location cannot be used without violating the total shielding integrity.

Electrical terminators, connectors, feedthroughs, and externally mounted components (such as diodes) should be electrically shielded, and all shielded connector covers must be bonded to the common structural ground of the space vehicle.

3.2.1.3 Bonding

Bond all structural elements. Identify isolated conducting elements and provide bonding to chassis for those areas. Make a separate bond strap for conductive items mounted at the end of dielectric booms. Every conductive internal part should be connected by a deliberate or leakage impedance to chassis as measured with an ohmmeter; 10^{12} Ω in a vacuum is adequate. A design with leakage resistance less than 10^{8} Ω permits construction verification with a good

hand-held ohmmeter. Conductive fittings on dielectric structural parts should also comply.

All conducting elements, surface and interior, should be related to a common electrical ground reference, either directly, through a charge bleed-off resistor, or via a controlled voltage on the conductor as in electrical/electronic circuitry (nothing electrically floating).

All structural and mechanical parts, electronics boxes, enclosures, etc., of the spacecraft should be electrically bonded to each other. All principal structural elements should be bonded by methods that assure a direct-current (dc) resistance of less than 2.5 milliohm (mΩ) at each joint if required for EMC or electrical ground referencing reasons; otherwise, a high value bleed resistance is permissible. The collection of electrically bonded structural elements is referred to as structure or structure ground. The objective is to provide a low-impedance path for any ESD-caused currents that may occur and to provide an excellent ground for all other parts of the spacecraft needing grounding. If structure ground reference must be carried across an articulating joint or hinge, a ground strap, as short as possible, should carry the ground across the joint. Relying on bearings for a ground path is unacceptable. If structural ground must be carried across slip rings on a rotating joint, at least two (preferably more) slip rings should be dedicated to the structural ground path, some at each end of the slip ring set. The bond to structure should be achieved within 15 cm of the slip ring on each end of the rotating joint. Slip rings chosen for grounding should be remote from any slip rings carrying sensitive signals.

3.2.1.3.1 Surface Materials and Their Bonding. All spacecraft surface (visible, exterior) materials should be conductive in an ESD sense (Section 3.2.1.5). All such conductive surface materials should be electrically bonded (grounded) to the spacecraft structure. Because they are intended to drain space-charging currents only, the bonding requirements are less stringent than those for structural bonding. The dc impedance to structure should be compatible with the surface resistivity requirements; that is, less than about 10^9 Ω from a surface to structure. The dc impedance must remain less than 10^9 Ω over the service life of the bond in vacuum, under temperature, under mechanical stress, etc.

3.2.1.3.2 Wiring and Cable Shields and Their Bonding. All wiring and cabling entering or exiting the shielded Faraday cage portion of the spacecraft (Section 3.2.1.2) must be shielded. Those cable shields and any other cable shields used for ESD purposes must be bonded (grounded) to the Faraday cage at the entry to the shielded region as follows:

a. The shield must be terminated 360 deg around a metal shielded backshell, which in turn must be terminated to the chassis 360 deg around the cabling.

b. The shield bond (ground) should not be terminated by using a connector pin that penetrates the Faraday cage and receives its ground inside the shielded region.

c. A mechanism should be devised that automatically bonds the shield to the enclosure/structure ground at the connector location, or a ground lug that uses less than 15 cm of ground wire should be provided for the shield, and procedures that verify that the shield is grounded at each connector mating should be established.

d. The other end of the cable shield should be terminated in the same manner. The goal is to maintain shielding integrity even when some electronics units must be located outside the basic shielded region of the spacecraft.

3.2.1.3.3 Electrical and Electronic Grounds. Signal and power grounds (zero-volt reference points) require special attention in the way they are connected to the spacecraft structure ground. NASA-HDBK-4001, *Electrical Grounding Architecture for Unmanned Spacecraft* [1], is a good reference. For ESD purposes, a direct wiring of electrical/electronics units to structure is most desirable. In particular, do not use separate ground wires daisy-chained from unit to unit or from each unit to a distant single point (star ground) on the structure.

3.2.1.4 Conductive Path

Have a conductive path to the structure for all circuitry. A simple and direct ground path is preferred without outside wiring to the ground point. Note areas where circuits or wires may be isolated for any reason. Place bleed resistors on all circuit elements that may become unreferenced (floating) during mission events, such as switching or connector demating. Use NASA-HDBK-4001 [1] as a guide to eliminate ground loops if necessary.

3.2.1.5 Material Selection

Limit usage of excellent dielectrics. Metals are conductive, and protecting them from internal charging is a relatively simple matter of ensuring a charge-leakage path. Therefore, the materials of concern in controlling internal charging are dielectrics. Prominent dielectrics in modern satellites include, but are not limited to, Teflon®, Kapton®, and FR4 circuit boards. These are

excellent charge-storing materials. Their use should be avoided if possible, especially in large blocks. Usages such as wire insulation or thin films (5 mil, for example) seem to contribute less or no problems on the interior of spacecraft. Circuit board materials may be a problem, but densely populated boards are less of a problem; short paths through the dielectric to nearby circuit traces permit easy electron bleed-off. Validate material performances with electron beam tests in accordance with Appendix E.1. Brunson and Dennison [2] have measured dielectric resistivity at lower temperatures and quantified the known increase in resistivity with decreasing temperature.

Make all interior dielectrics electrically leaky. Internal dielectrics should be static-dissipative or leaky. This applies specifically to circuit boards but would be desirable for all dielectrics, including cable wiring and conformal coatings. The degree of leakiness or conductivity does not need to be great enough to interfere with circuit performance. It can be on the order of 10^4 to 10^{11} Ω-cm or of 10^5 to 10^{12} Ω/square (see Appendix E.3 for a discussion of Ω/square) and still provide a bleed path to electrons for internal charging purposes. Verify that the conductivity remains adequate over the mission life. Meeting this requirement and also providing the other necessary properties (mechanical, workable, etc.) might be a challenge.

Make all spacecraft exterior surfaces at least partially conductive. The best way to avoid differential charging of spacecraft surfaces is to make all surfaces conductive and bonded to the spacecraft structure. However, typical spacecraft surface materials often include insulating materials such as Mylar®, Kapton®, Teflon®, fiberglass, glass, quartz, or other excellent dielectrics. It should be recognized in the design phase that there may be areas for which use of dielectric surfaces is particularly crucial, such as areas adjacent to receivers/antennas operating at less than 1 gigahertz (GHz), sensitive detectors (Sun and Earth detectors, etc.), or areas where material contamination or thermal control is critical. For these applications use of (grounded) indium tin oxide (ITO) coatings is recommended.

This section first defines the conductivity requirements for spacecraft surface materials. Materials that are typically used are then evaluated, and their usage is discussed. Analysis is suggested to estimate the effects of any dielectric surfaces that may remain on the spacecraft. At the conclusion of this section, use of materials with a high secondary electron yield is discussed.

3.2.1.5.1 Surface Material Selection Advice. By the proper choice of available materials, the differential charging of spacecraft surfaces can be minimized. At

present, the only proven way to eliminate spacecraft potential variations is by making all surfaces conductive and connecting them to a common ground.

Surface coatings in use for this purpose include conductive conversion coatings on metals, conductive paints, and transparent, partially metallic vacuum-deposited films, such as ITO. Table 3-1 describes some of the more common acceptable surface coatings and materials with a successful use history. Table 3-2 describes other common surface coatings and materials that should be avoided if possible.

The following materials have been used to provide conducting surfaces on the spacecraft (remember, these conductive surfaces must be grounded or at least not floating):

a. Vacuum-metalized dielectric materials in the form of sheets, strips, or tiles. The metal-on-substrate combinations include aluminum, gold, silver, and Inconel® on Kapton®, Teflon®, Mylar®, and fused silica.

b. Thin, conductive front-surface coatings, especially ITO on fused silica, Kapton®, Teflon®, or dielectric stacks.

c. Conductive paints, fog (thin paint coating), carbon-filled Teflon®, or carbon-filled polyester on Kapton® (Sheldahl black Kapton®).

d. Conductive adhesives.

e. Exposed conductive facesheet materials (graphite/epoxy - scuffed with fine sandpaper to expose conductive graphite fibers - or metal).

f. Etched metal grids or bonded (or heat embedded) metal meshes on nonconductive substrates.

g. Aluminum foil or metalized plastic film tapes.

Because of the variety in the configuration and properties of these materials, there is a corresponding variety in the applicable grounding techniques and specific concerns that must be addressed to ensure reliable in-flight performance.

Table 3-1. Surface coatings and materials acceptable for spacecraft use (Note: Must be grounded to chassis).

Material	Comments
Paint (carbon black)	Work with manufacturer to obtain paint that satisfies ESD conductivity requirements of Section 3.2.2 and thermal, adhesion, radiation tolerance, and other needs.
GSFC NS43 paint (yellow)	Has been used in some applications where surface potentials are not a problem; apparently will not discharge.
ITO (250 nm)	Can be used where some degree of transparency is needed; must be properly grounded. For use on solar cells, optical solar reflectors, and Kapton® film, use sputtered method of application and not vapor deposited.
Zinc orthotitanate paint (white ZOT)	Possibly the most conductive white paint; adhesion difficult without careful attention to application procedures, and then difficult to remove.
Alodyne	Conductive conversion coatings for magnesium, aluminum, etc., are acceptable.
DuPont Kapton® XC family	Carbon-filled polyimide films; 100XC10E7 with nominal resistivity of 2.5×10^4 Ω-cm; not good in atomic oxygen environment without protective layer (ITO, for example).
Deposited conductors	Examples: aluminum, gold, silver, Inconel® on Kapton®, Teflon®, Mylar®, and fused silica.
Conductive paints	Over dielectric surfaces, with some means to assure bleed-off of charge.
Carbon-filled Teflon® or Kapton®	Carbon filler helps make the material conductive.
Conductive adhesives	Especially if needed for bridging between a conductor and ground.
Conductive surface materials	Graphite epoxy (scuffed to expose carbon fibers) or metal.
Etched metal grids	Etched or bonded to dielectric surfaces, frequent enough to have surface appear to be grounded.
Aluminum foil or metalized plastic film tapes	If they can be tolerated for other reasons such as thermal behavior.

Table 3-2. Surface coatings and materials to be avoided for spacecraft use.

MATERIAL	COMMENTS
Anodyze	Anodyzing produces a high-resistivity surface to be avoided for ESD applications. The coating can be made quite thin and might be acceptable if analysis shows stored energy is small.
Fiberglass material	Resistivity is too high and is worse at low temperatures.
Paint (white)	In general, unless a white paint is measured to be acceptable, it is unacceptable.
Mylar® (uncoated)	Resistivity is too high.
Teflon® (uncoated)	Resistivity is too high. Teflon® has demonstrated long-time charge storage ability and causes catastrophic discharges.
Kapton® (uncoated)	Generally unacceptable because of high resistivity; however, in continuous sunlight applications if less than 0.13 mm (5 mil) thick, Kapton® is sufficiently photoconductive for use.
Silica cloth	Has been used for antenna radomes. It is a dielectric, but because of numerous fibers or if used with embedded conductive materials, ESD sparks may be individually small. It has particulate issues, however.
Quartz and glass surfaces	It is recognized that solar cell cover slides and second-surface mirrors have no substitutes that are ESD acceptable; they can be ITO coated with minor performance degradation, and the ITO must be grounded to chassis. Their use must be analyzed and ESD tests performed to determine their effect on neighboring electronics. Be aware that low temperatures significantly increase the resistivity of glasses [3].

The following practices have been found useful for grounding/bonding surface materials:

a. Conductive adhesives should be used to bond fused silica, Kapton®, and Teflon® second-surface mirrors to conductive substrates that are grounded to structure. If the substrate is not conductive, metal foil or wire ground links should be laminated in the adhesive and bolted to structure. Only optical solar reflectors (OSRs) with conductive back surfaces (example: Inconel®) should be used.

b. When conductive adhesives are used, the long-term stability of the materials system must be verified, particularly conductivity in vacuum after thermal cycling, compatibility of the materials (especially for epoxy adhesive) in differential thermal expansion, and long-term resistance to galvanic corrosion.

c. Metalized Teflon® is particularly susceptible to ESD degradation, even when grounded. Avoid using it. If there is no substitute for a specific application, the effects of EMI, contamination, and optical and mechanical degradation must be evaluated.

d. Paints (ESD-conductive/leaky) should be applied to grounded, conductive substrates; the primer must be conductive, too. If painting over a grounded surface is not possible, paint coverage should be extended to overlap grounded conductors around the paint's perimeter.

e. Ground tabs must be provided for free-standing (not bonded down) dielectric films with conductive surfaces.

f. Meshes that are simply stretched over dielectric surfaces are not effective; they must be bonded or heat-sealed in a manner that will not degrade or contaminate the surface.

g. There are several techniques for grounding thin, conductive front-surface coatings such as ITO. At least one commercial manufacturer has found the added cost of a reliable ITO coating and grounding/referencing method on OSRs and coverglasses has provided excellent in-orbit performance and thus is worth that cost. The methods include welding of ground wires to front-surface metal welding contacts, front-surface bonding of coiled ground wires (to allow for differential thermal expansion) by using a conductive adhesive, and chamfering the edges of OSRs before ITO coating to permit contact between the coating and the conductive adhesive used to bond the OSR to its substrate.

h. For MLI, extending the aluminum foil tab to the front surface is suitable.

3.2.1.5.2 Nonconductive Surfaces. If the spacecraft surface cannot be made 100% conductive, an analysis must be performed to show that the design is acceptable from an ESD standpoint. Note that not all dielectric materials have the same charging or ESD characteristics. The choice of dielectric materials can affect surface voltage profiles significantly. For example, it has been shown [3,4] that different cover slide materials have differing resistivities and that all are affected by temperature. Cover slide material can noticeably affect spacecraft charging.

An adequate analysis preceding the selection of materials must include a spacecraft charging analysis to determine surface potentials and voltage gradients, spark-discharge parameters (amplitude, duration, frequency content), and EMI coupling. The cost and weight involved in providing adequate protection (by shielding and electrical redesign) could tilt the balance of the trade-off to favor the selection of less optically transmissive cover slides that

are more reliable from spacecraft charging, discharging, and EMI points of view.

The proven materials have their own cost, weight, availability, variability, and fabrication effects. In addition, uncertainties relating to spacecraft charging effects must be given adequate consideration. Flight data have shown apparent optical degradation of standard, stable thermal control materials, e.g., OSRs and Teflon® second-surface mirrors, that is in excess of ground test predictions, part of which could be the result of charge-enhanced attraction of charged contaminants. In addition, certain spacecraft anomalies and failures may have been reduced or avoided by using charge-control materials.

When the spacecraft design is completed, the remaining dielectric materials on the surface of the spacecraft must be evaluated for their ESD hazard. Evaluate potential stored energy and nearby potential victims to see if a spacecraft threat exists.

A spacecraft with larger portions of dielectric may have retarding electric fields because the dielectric diminishes the effects of the photoemission process [5]. As a result, the spacecraft structure potential may go more negative and thus reduce the differential voltage between the dielectric and the spacecraft.

The lesson to be learned is that all surface dielectrics must be examined for their differential charging. Each dielectric region must be assessed for its breakdown voltage, its ability to store energy, and the effects it can have on neighboring electronics (disruption or damage) and surfaces (erosion or contamination).

3.2.1.5.3 Surface Secondary Emission Ratios. Other means to reduce surface charging exist, but they are not well developed and are not in common usage. One suggestion for metallic surfaces is an oxide coating with a high secondary electron yield. This concept, in a 3-D surface charging simulation, reduced charging of a spacecraft dramatically and reduced differential charging of shaded Kapton® slightly. Any selected materials should be carefully analyzed to ensure they do not create problems of their own and will work as intended over their service lives.

3.2.1.6 Radiation Spot Shields and Other Floating Metals

Grounding radiation spot shields is essential, i.e., radiation spot shields must be grounded. Bodeau [6,7] in particular emphasizes this rule. Grounding can be done in a number of ways. If a Solithane or other conformal coating has adequate resistivity (on the order of 10^{10} Ω-cm or less), a separate ground wire

is unnecessary. It must be determined that any solution, such as partially conductive Solithane, will not degrade (increase resistivity) in the expected radiation and long-term vacuum environments. (This relatively large resistivity, $<10^{10}$ Ω-cm, is generally acceptable on an interior surface since charging fluxes are lower on the interior of a spacecraft. Check actual charging fluxes if uncertain about a particular application.)

3.2.1.7 Filter Circuits with Lumped Elements or Circuit Choices

Use low pass filters on interface circuits. Use low-speed, noise-immune logic, if possible. Use complementary metal-oxide-semiconductor (CMOS) circuits that have higher interface noise immunity. Beware, however, of the latch-up sensitivity of CMOS. For IESD purposes, the filter or protection network must be applied so that it is physically at the device terminals.

Electrical filtering should be used to protect circuits from discharge-induced upsets. All circuits routed into the Faraday cage region, even though their wiring is in shielded cabling, run a greater risk of having ESD-caused transient voltages on them. Initial design planning should include ESD protection for these circuits. It is recommended that filtering be applied to these circuits unless analysis shows that it is not needed.

The usual criterion suggested for filtering is to eliminate noise shorter than a specific time duration, i.e., above a specific frequency. On the Communications Technology Spacecraft (CTS), in-line transmitters and receivers effectively eliminated noise pulses of less than 5-μs duration, which were suitable to its circuitry. Similar filtering concepts might include a voltage threshold or energy threshold. Filtering is believed to be an effective means of preventing circuit disruption and should be included in system designs. Any chosen filtering method should have analyses and tests to validate the selected criteria. Filters should be rated to withstand the peak transient voltages over the mission life. Today's circuitry with smaller feature sizes and lower operating voltages may need even more stringent filtering for ESD protection.

3.2.1.8 Isolate Transformer Primary-to-Secondary Windings

Isolate the primary and secondary windings of all transformers. Reduce primary-to-secondary winding capacitance to reduce common mode noise coupling. This is an EMC solution to reduce coupling of ESD-induced noise.

3.2.1.9 Bleed Paths for Forgotten Floating Conductors

Provide a conductive bleed path for all conductors (including structural elements), including but not to be limited to the following items:

a. Signal and power transformer cores.

b. Capacitor cans.

c. Metallic IC and hybrid device cases.

d. Unused connector pins and unused wires in cables, including those isolated by switching.

e. Relay cans.

These items may be protected by stray leakage by deliberate resistors to ground, through their conformal coating, normal bleed paths, or small charge/energy storage areas. Ensure that the presumed bleed path really works or that the ungrounded items are not an ESD threat before depending on stray leakage for ESD protection.

3.2.1.10 Interior Paints and Conformal Coatings

Most paints and conformal coatings are dielectrics and can be charged by energetic particles. This must be considered in evaluating the likelihood of interior charging of a design. If conductive coatings are used, these must be grounded to the structure to allow charge to bleed off. For conductive coatings, conductive primers must be used. If nonconductive primers are used, the conductive coating will be isolated from ground and will charge. Other grounding means must be provided if the primer or substrate is non-conductive.

3.2.1.11 Cable Harness Layout

Route cable harnesses away from apertures. Care should be taken in the layout of the internal electrical harnesses to minimize exposure to the environment's energetic particles. The harness should not be close to the edges of apertures.

3.2.1.12 External Wiring

Provide additional protection for external cabling. Cables external to the spacecraft structure should be given adequate protection. The dielectric coatings can charge to a point where discharge can occur. At present, there are no simple design rules for the degree of shielding needed. Cables should be tightly wrapped to minimize gaps where discharges can propagate.

3.2.1.13 Slip Ring Grounding Paths

Carry bonds and grounds across all articulated and rotating joints. For a rotating joint with slip rings, the chassis or frame ground (bond) must be carried through the slip ring also and then grounded. Note that for the case of the solar array and other situations that may involve transfer of ESD current, a series resistance in the path from spacecraft frame to solar array frame will be

required to limit the amount of current that can carry this ESD current into the satellite (Section 3.2.4.3, Paragraph t).

3.2.1.14 Wire Separation

Segregate cabling from outside the spacecraft after it enters the Faraday cage. Wires coming from outside the spacecraft should be filtered, preferably at the entry point but certainly before being routed with other interior cabling. This is based on an assumption of external ESD noises and is to prevent coupling to the interior. It is a poor design practice to route the filtered and unfiltered wires together in the same bundle because noise can be coupled between them.

3.2.1.15 ESD-Sensitive Parts

Pay special attention to ESD-sensitive parts. In the parts list, flag all parts that are Class 1 ESD-sensitive in accordance with MIL-STD-883G, Test Method Standard for Microcircuits [8] (Method 3015.7, Electrostatic Discharge Sensitivity Classification (Human Body Model)). Do a charging analysis after completion of the spacecraft design. Evaluate the charging rates with respect to Section 3.2.2 parameters. Protect the devices if they might be damaged by an expected threat.

3.2.1.16 Procedures

Institute proper handling, assembly, inspection, and test procedures to ensure the electrical continuity of the space vehicle grounding system. The continuity of the space vehicle electrical grounding and bonding system is of great importance to the overall design susceptibility to spacecraft charging effects. In addition, it will strongly affect the integrity of the space vehicle EMC design. Proper handling and assembly procedures must be followed during fabrication of the electrical grounding system. All ground ties should be carefully inspected, and dc resistance levels should be tested during fabrication and again before delivery of the space vehicle. A final check of the ground system continuity during preparation for space vehicle launch is desirable.

A related reference is NASA-HDBK-4001 [1], which describes how to establish an electrical grounding architecture system for power and signals. This design book is complementary to the ESD effort.

3.2.2 Surface ESD Design Guidelines, Excluding Solar Arrays

3.2.2.1 Qualitative Surface ESD Guidelines

Refer to General ESD Design Guidelines, Section 3.2.1.

3.2.2.2 Quantitative Surface ESD Guidelines

These detailed surface conductivity design guidelines are equation-based to assist designers accounting for differing geometries and material conductivities. Since these are general, projects may formulate their own rules.

To discharge surfaces that are being charged by space plasmas, a high resistivity to ground can be tolerated because the plasma charging currents are small. The following guidelines are suggested:

a. Conductive materials (e.g., metals) must be grounded to structure with resistance, expressed in Ω:

$$R < 10^9/A \tag{3.2-1}$$

where:

A = exposed surface area of the conductor in square centimeters.

b. Partially conductive surfaces, e.g., paints, applied over a grounded conductive surface must have a resistivity-thickness product, expressed in Ω-cm^2

$$rt < 2 \times 10^9 \tag{3.2-2}$$

where:

r = material resistivity in Ω-cm

t = material thickness in cm.

c. Partially conductive surfaces applied over a dielectric and grounded at the edges must have material resistivity, expressed in Ω-cm, such that

$$rh^2/\mathrm{t} < 4 \times 10^9 \tag{3.2-3}$$

where:

r = material resistivity in Ω-cm

t = material thickness in cm.

h = greatest distance on a surface to a ground point in cm.

The above guidelines depend on the particular geometry and application. A simplified set of guidelines is supplied for early design activities as follows:

a. Isolated conductors must be grounded with less than 10^6 Ω to structure. This is the same value recommended in ECSS-E-ST-20-06C [9].
b. Materials applied over a conductive substrate must have bulk resistivities of less than 10^{11} Ω-cm.
c. Materials applied over a dielectric area must be grounded at the edges and must have a resistivity less than 10^9 Ω per square.

The term Ω per square is defined as the resistance of a flat sheet of the material, measured from one edge of a square section to the opposite edge. (Appendix E.3 describes this more fully.)

These requirements are more strict than the preceding relations, which include effects of spacecraft geometry.

In all cases, the usage or application process must be verified by measuring resistance from any point on the material surface to structure. Problems can occur. For example, one case was observed where a non-conductive primer was applied underneath a conductive paint; the paint's conductivity was useless over the insulating primer.

All grounding methods must be demonstrated to be acceptable over the service life of the spacecraft. It is recommended that all joint resistances and surface resistivities be measured to verify compliance with these guidelines. Test voltages to measure resistivity of dielectric samples should be at least 500 V. See Appendix E.4 for measurement examples.

Grounding methods must be able to handle current bleed-off from ESD events, vacuum exposure, thermal expansion and contraction, etc. As an example, painting around a zero-radius edge or at a seam between two dissimilar materials could lead to cracking and a loss of electrical continuity at that location.

3.2.3 Internal ESD Design Guidelines

Guidelines for internal hardware are often the same as for the guidelines for surfaces.

3.2.3.1 Qualitative Internal ESD Guidelines

Refer to General ESD Design Guidelines, Section 3.2.1.

Internal regions also have surfaces, and surface rules apply.

3.2.3.2 Quantitative Internal ESD Guidelines

Quantitative guidelines are recommended in the following sections.

3.2.3.2.1 Grounding Conductive Elements. Unused spacecraft cables, circuit traces, and other non-circuit conductive elements greater than 3 cm^2 in surface area (0.3 cm^2 for conductive elements on circuit boards) or longer than 25 cm in length must be ground referenced; be sure to provide a deliberate or known bleed path for all radiation spot shields. For other wires and metal, being in a circuit is usually adequate. It is best not to have any deliberate ungrounded metals including unused connector pins as an example. Exceptions are allowed in situations in which one of the following conditions is true:

a. Discharges will not occur in the expected charging environment.

b. The discharges expected to occur will not damage or disrupt the most sensitive circuits in the vicinity nor cause EMI that exceeds the EMC requirements, assuming separate EMC requirements exist.

These historic quantitative guidelines may need reconsideration for newer spacecraft. For example, ECSS-E-ST-20-06C [9] recommends a maximum of 1 cm^2 ungrounded metal on the surface of a spacecraft.

3.2.3.2.2 Shielding to Limit Internal Electron Fluxes. Determine electron fluxes at all part locations using a worst-case electron spectrum (Fig. 2-6 for GEO) and shield all electronic circuitry to the following levels (Fig. 2-5 basis with no margin; projects may wish to consider margins).

GEO orbit approximate rule of thumb to limit IESD: If there are 110 mils of aluminum equivalent shielding, it was previously stated that there is no need to shield further and there is no need to do an electron transport analysis unless there is a desire to save weight (GEO orbit approximate rule only). Bodeau's [6,7] recommendations for lower flux limits have the effect of raising this to 200+ mils of aluminum shielding in Earth GEO orbits.

If the computed flux at the location is less than 0.1 pA/cm^2, the circuit needs no additional shielding (any electron environment). (Basis: less than 10^{10} e/cm^2 deposited in 10 hours—using only the incident fluence is more conservative.) Note, however, that Bodeau [6,7] and Balcewicz et al. [10] recommend one-tenth of this (0.01 pA/cm^2) which begins to present difficulties in implementation. Note also that this recommendation depends on the assumed room temperature bulk resistivities of commonly used dielectric materials. For applications which are constantly at cryogenic temperatures, the flux limit must

be adjusted downward to account for the increased cryogenic bulk material resistivities (see in particular Bodeau [7]). Also note that ECSS-E-ST-20-06C [9] and Bodeau [7] recommend longer flux integration times to account for dielectric materials with time constants greater than 10 hours.

If the incident flux is between 0.1 pA/cm^2 and 0.3 pA/cm^2, shield to a level of 0.1 pA/cm^2 if the circuitry is Class 1 ESD-sensitive (MIL-STD-88G3 [8], Method 3015.7); or if this type of circuitry has had a known on-orbit anomaly. (Again, remember that Bodeau indicates that less flux/more shielding may be appropriate for very sensitive circuits.)

If the incident flux is between 0.3 pA/cm^2 and 1 pA/cm^2 and Class 2 ESD-sensitive or greater circuitry is present, then shield to < 0.3 pA/cm^2.

If the incident flux is greater than 1 pA/cm^2, IESD problems may exist.

3.2.3.2.3 Filter Circuits. For wiring protected less than the levels of Section 3.2.3.2.2 protect attached circuits by filtering. To protect the interior sensing circuit for temperature transducers that are located outside the main box of the spacecraft, resistor-capacitor (RC) filters or diode protection can be used to suppress any ESD effects. Another reason for filtering is if the shielding levels of Section 3.2.3.2.2 cannot be achieved. The filter should anticipate a pulse on the order of 20 ns wide. As a rough example, filtering should protect against a 20-pF capacitance charged with 100 nC (about 5 kV stress, 250 μJ). The real estimated threat should be used, if possible.

3.2.3.2.4 Voltage Stress. Keep the electric field stress in dielectrics below 100 V/mil (~4 × 10^4 V/cm or 4 × 10^6 V/m; see [11, 12]). When designing high-voltage systems, keep the electric field below 100 V/mil in any material or gap. This voltage stress could be in circuit board dielectrics being charged by the incident electron flux while the adjacent metals remain at a low voltage. Other sites of concern are ungrounded metal radiation shields on insulating surfaces charged by the electron flux while the adjacent surfaces remain at low voltages or insulated surfaces being charged while internal wires remain at low voltage. Power supplies can sustain a discharge after an arc has been initiated, so power wiring should never be bare (exposed). All such possible sources must be eliminated where possible.

3.2.3.2.5 Coat Circuit Boards with Leaky Dielectric. Use leaky/conductive conformal coating on circuit boards. Leung and Mikkelson [13] use a 10^{10} Ω-cm clear coating, resulting in an automatic bleed path of resistance (R), such that 10^9 Ω < R < 10^{13} Ω. This shunt leakage will not affect circuit

operation but can bleed off most levels of internal charging. The coating has been space qualified (temperature cycle, vacuum, etc.). It has demonstrated dramatic reduction in discharge voltages on its victims in laboratory tests and does not involve circuit or board layout changes. At present, the specific formulation is a proprietary product, but the concept could be adapted.

3.2.3.2.6 Fill Circuit Board Material with Grounded/Referenced Metal. Limit the regions where charge can accumulate. Place grounded (best) or referenced traces in open (unused) areas. This is a new idea in this book (based on NASA-HDBK-4002A) to minimize the size of any ESD arc inside of a circuit board by reducing the dielectric volume that might contain a discrete lump of ESD energy. It was not developed in response to a specifically identified failure in space and *has not been validated*. The derivation is shown in Appendix H.

Circuit boards should be designed so that any metal area greater than 0.3 cm^2 should also have a bleed path with the same ESD grounding limits of 0 to 10 MΩ resistance to ground. Circuit boards should be designed so that there will be no open (unused) surface areas greater than 0.3 cm^2. Otherwise, place a metal land that is ESD grounded with 0 to 10 MΩ resistance to ground in the unused dielectric area.

This effect is shown in Fig. 3-1, which also proposes a new rule for circuit board exposed dielectric areas. (The term “ground” in Fig. 3-1 means (a) not floating or (b) referenced within the circuit.) The design rule assumes a standard FR4 circuit board material of 80-mil thickness. The term “depth to ground plane” means the distance from any dielectric to a ground-referenced plane. For example, if the board is 80 mil thick with a ground plane on one external surface, the depth to ground plane is 80 mil; if both exterior surfaces are ground (or power) planes, the depth to ground plane is 40 mil.

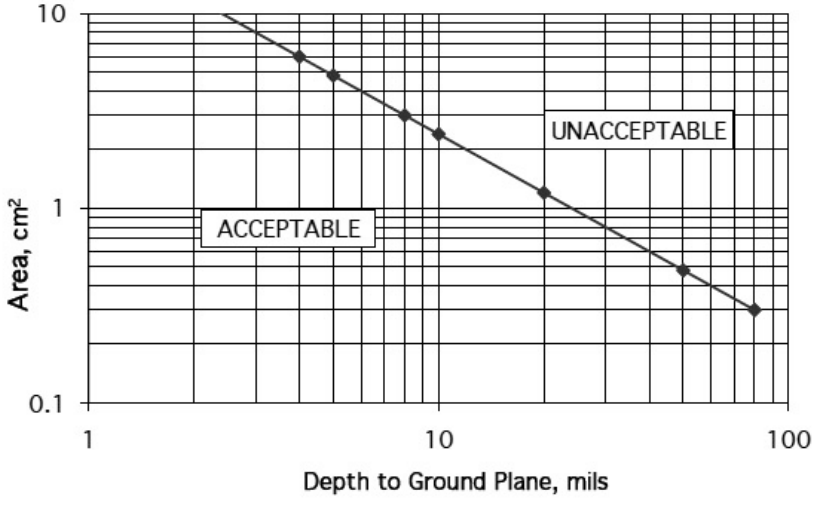


Fig. 3-1. Permissible area versus depth-to-ground plane.

3.2.4 Solar Array ESD Design Guidelines

This section contains guidelines to protect solar arrays from ESD charging problems.

3.2.4.1 Solar Array Possible ESD Problem Areas

Solar arrays, with their possibly high operating voltages and their available power, can cause the following spacecraft charging effects:

a. Arcing with loss of power and permanent damage to the solar arrays if the arcing is sustained by power from the array itself or by power from the spacecraft internal stored energy.

b. Arcing with momentary loss of power and degradation of solar arrays (similar to that listed in paragraph 3.2.4.1.a, but without sustained arc).

c. Charging of spacecraft structures with respect to the plasma and resultant problems (contamination by attraction of charged surfaces and/or possible erosion of surfaces as species are attracted to the surface). This is very noticeable in LEO environments [14].

d. Disruption of science (electric fields from the surface potentials of solar arrays will alter the path of electrons and ions so that plasma measuring instruments will not record the proper directionality of electrons and ions entering their field of view).

e. Loss of power related to current leakage at exposed conductors in the array. A dramatic rise in power loss can occur at string potentials of ~200 to 1000 V positive with respect to plasma potential related to the phenomenon of snap-over. At a geometry- and material-dependent voltage, the current in the array's current/voltage (I/V) curve makes a dramatic change to increasingly larger currents because of enhanced secondary emission and greater plasma contact area.

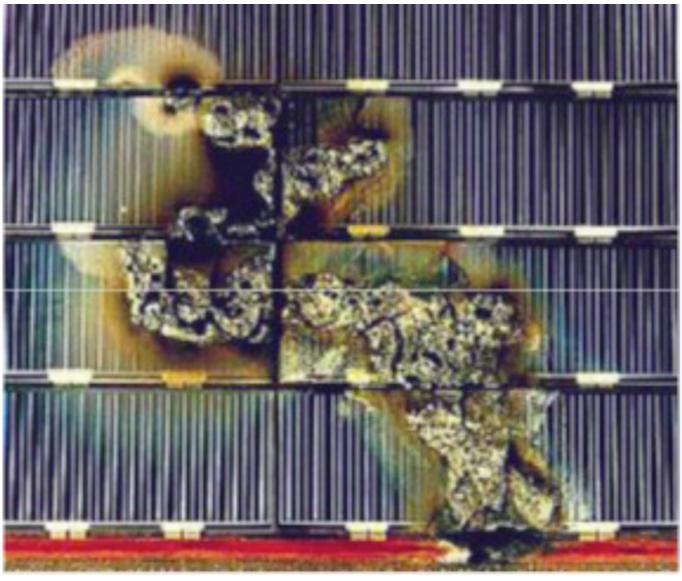
3.2.4.2 Background

The following are basic rules to avoid spacecraft charging issues related to solar arrays that can cause surface damage, upset science instruments on the spacecraft, or may result in power loss to the space plasma, and resultant ESDs and damage. The rules are gleaned from several sources. Good references for this subject include references [3, 14–17] and references therein.

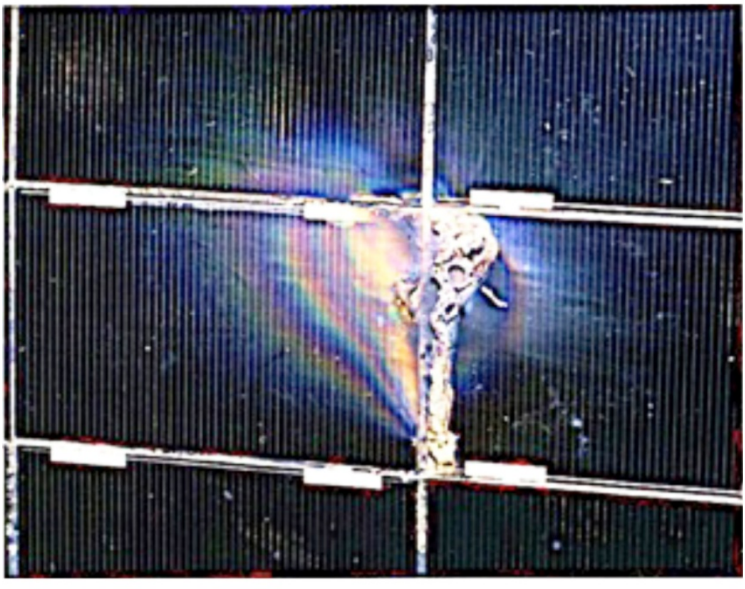
Note that there has not been enough flight experience with higher voltage solar arrays (operating voltages greater than 28 V) at the time of this writing (2011) to generate guaranteed and optimal design rules for any space plasma environment situation, so the following should only be considered as guidelines. (Exception: the ISS uses higher voltage and massive arrays. Their impact has been investigated in several papers [18].) The principle rule still must be: test any new design in the anticipated environment. There has been considerable focus on solar arrays [19], and there will be more in the next few years. Progress, especially in the design of test protocols that expand on the existing ideas and rules contained herein, is anticipated in the near future.

It is not necessary to use all the design ideas listed herein because that would cause excess mass, excess cost, reduced efficiency, etc. Trade-offs are needed to achieve an adequate design. The point is that after the design has been optimized by engineering and analysis, the final design must be verified by test with as realistic test conditions as possible. The test considerations are described in the following material with a shopping list of design features. To illustrate the severity of the problem, Fig. 3-2 shows the type of damage that may occur to solar arrays if the design is inadequate in a space plasma environment.

Figure 3-2a is a photograph [15] of a solar array recovered from the European Space Agency (ESA) European Retrievable Carrier (EURECA) mission by the Space Shuttle. As space failures typically are not retrieved, ground tests have to be performed for failure analysis. These, however, do not represent an actual product that failed in space as Fig. 3-2a shows. As an example of the corresponding ground simulation, Fig. 3-2b shows a solar array that failed in a plasma environment during ground test [20, 27].



(a) Failure caused by in-flight ESD arcing.



(b) Failure caused by ground ESD arcing.

Fig. 3-2. Examples of solar-array failures caused by (a) in-flight ESD arcing and (b) ground ESD arcing.

3.2.4.3 Solar Array Design Guidelines to Protect Against Space Charging and ESDs

a. Build solar arrays so they do not arc. This is a difficult requirement with the present trend toward higher power solar arrays with higher voltages (to minimize wiring size and weight).

b. Test any new design in a representative plasma and energetic particle environment; test with a voltage margin on the solar array to assure that the design is adequate.

c. Arrays with 40-V or less maximum cell-to-cell potential difference are assumed not to be a hazard with margin. This has been measured to be a reasonable guideline. Potentials on the order of 80-V cell-to-cell potential difference can, however, initiate arcs on unprotected solar array designs. Note that string voltages might be ~20 percent higher than nominal if they are not carrying current/open-circuited.

d. Place diodes in series with each string so that an arc on a single string will not be sustained by energy/current from the other strings on the array or the main bus stored energy. Available currents on the order of 2 A can sustain an arc with unprotected solar array designs. Size the diodes to tolerate the maximum anticipated ESD arc or short circuits to chassis.

   Figures 3-3 and 3-4 [3] illustrate rules 3.2.4.3.c and 3.2.4.3.d.

e. Especially for LEO, consider building arrays so that they are not negatively grounded to the spacecraft frame/chassis ground. A “floating array,” if the power converter can provide isolation, is one option. With this design, the array voltage with respect to the plasma will adjust to minimize power loss currents from the array through the plasma potential (assuming a conventionally built array, with exposed cell potentials on the edges). This results in a (soft) virtual ground such that about 5 percent of the array area is higher than the plasma potential, and 95 percent of the array is lower than the plasma potential. The authors generally oppose any totally floating conductor system.

   An alternate option to floating that addresses the same issue is to ground the solar array at the positive end. This has less effect on the overall spacecraft potential and less current/energy losses to space. The best fixed grounding solution to keep the spacecraft frame at plasma potential is to ground the solar array strings to frame at about 5 to 10 percent of the distance (potential) from the positive end of the solar array. The objectives are to reduce the power loss of leakage current through the plasma and to reduce the voltage of any one part of the array with respect to local plasma below potentials that could trigger an arc.

The two objectives do not have the same solution, so a compromise may be necessary. Analyses of the applicable charging currents, power loss, and resulting voltage balance should be done before adopting this design approach [15]. The reason that this design might be more useful at LEO is that the greater plasma density has a greater impact on the space charging concerns listed in these paragraphs. A similar situation may exist if an electric thruster effluent impacts the solar array or if some other higher density plasma surrounds the arrays.

f. Design the solar arrays to avoid excessive power loss, e.g., keep the positive voltage with respect to frame less than ~100 V. The remedy here if high voltages must be used is to insulate the high-voltage metal regions (interconnects and wiring) with insulating grout (space-qualified room-temperature vulcanized (RTV) silicone). Avoid any air pockets/voids in the grouting. This latter instruction is very important because entrained air can assist in creating a Paschen discharge, meaning that it takes less voltage to trigger an arc. The fabrication processes must be well thought out, the assembly personnel must be well-trained, and fabrication inspections (quality assurance (QA)) must be part of the process.

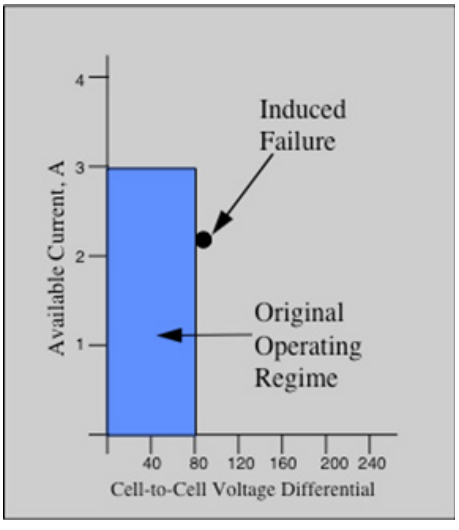


Fig. 3-3. Measured gallium arsenide (GaAs) coupon I/V failure threshold.

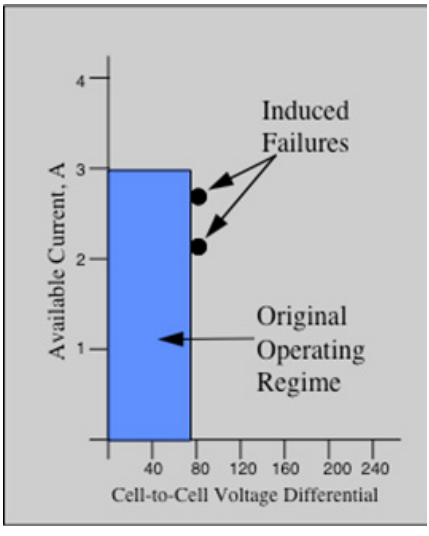


Fig. 3-4. Measured silicon (Si) coupon I/V failure threshold.

g. Do not vent any gas onto or in the vicinity of exposed solar array potentials. A discharge can be triggered at lower voltages in the presence of the resultant partial pressure regimes. Most typically, the gas would be attitude control gas venting but could also be cryogenic cooler gas venting (again, a possible Paschen discharge).

h. Insulate the solar arrays so that there is no potential-carrying conductor exposed to space. The simplest concept is to grout all the spaces between solar cells as in (f) in this Section, 3.2.4.3. Figures 3-5 and 3-6 [3] illustrate the configuration being discussed. Figure 3-6 illustrates a shortcut that may be permissible if testing demonstrates its adequacy. Figure 3-6 assumes that cells 1 and 3 are connected in a string and that the potential between them is small, so no grouting is placed between them. Cells 1 and 2 and 3 and 4, by contrast, are adjacent strings with different potentials and need insulation the full distance of their shared edge. At the regions labeled RTV Barrier, the RTV is extended out a bit at the corner as an extra insulation where higher electric fields may be present. In Fig. 3-6, b is grout width; in Fig. 3-5, b, r, g, and x are variables used in equations from reference [3]. A full RTV barrier would be the most robust design.

   Figures 3-7 and 3-8 [3], when compared to the original operating regime illustrated in Figs. 3-3 and 3-4, show the improvement when grouting is used.

i. Use slightly conductive cover slides to limit electric fields at potential arc sites.

j. Use cover slides with large overhang to limit electric fields in the plasma region.

k. Limit the differential potential between adjacent cells in the array to reduce arc likelihood. As a limit, 40 V is suggested, but test the array design.

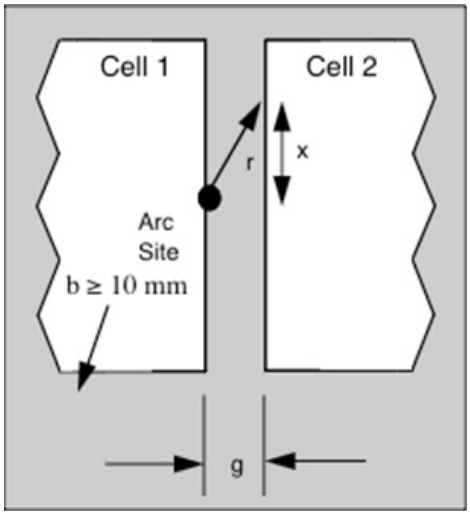


Fig. 3-5. An intercell gap.

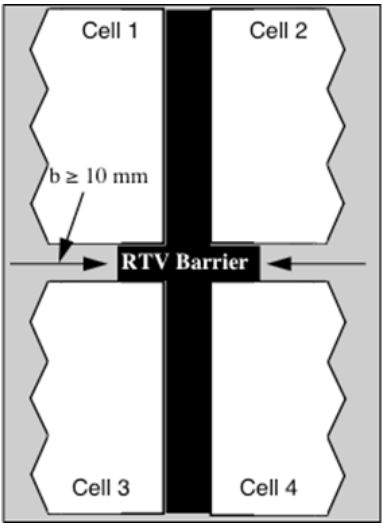


Fig. 3-6. Grouting barrier to stop arcs.

Fig. 3-7. GaAs coupon with RTV barrier installed.

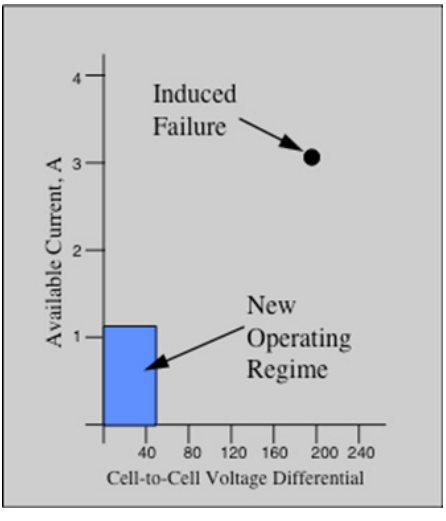


Fig. 3-8. Si coupon with RTV Barrier installed.

l. Make the cell inter-gap spacing wide enough so that there will be no arcing. Testing in plasma must be performed for the chosen candidate designs. This design solution is less likely, because it reduces cell density and thus results in less power density (W/m^2 and/or W/kg).

m. Verify that solar array materials will not outgas in space or decay at high temperatures.

n. Make all insulating materials thick enough to withstand the anticipated electric fields so that they are below the breakdown voltage of that material. Do not make the materials so thick that they accumulate charge to the degree that they cause problems. Make this part of the ESD analysis/test process.

o. Use a plasma contactor (neutral plasma beam) on the spacecraft as a means to keep the spacecraft at plasma potential. This is useful in LEO or for performing low-energy plasma measurements or to reduce erosion of surfaces caused by impact of attracted charged particles. Any such active device carries reliability concerns in addition to weight, complexity, power consumption, and consumables, but the ISS contactors are working well.

p. Use thin dielectrics with resistivities such that a charge will not build up in the anticipated environment. Examples include wire insulation, substrates, and structures. The idea is to make the resistivity/thickness combination so that charge can bleed off through the material to ground faster than hazardous potentials can arise on the material surface or in its volume.

q. Do not put ESD-sensitive electronics near where a solar array discharge may occur. An example would be a thermistor or its wiring placed near the solar cells so that ESD energy can be carried back to an ESD-sensitive telemetry data multiplexing unit.

r. Filter solar array wiring, preferably at the entry to the spacecraft Faraday cage, but definitely before it enters the power supply. If solar array wiring is not filtered at the entry point to the Faraday cage, shield the wiring from that point to the power supply.

s. Filter temperature sensors and other data signals from the solar array as they enter the spacecraft or at least at the entry point into their electronic sensing box.

t. Isolate the solar array substrate ground from spacecraft chassis ground. Place a ~2 to 250 kΩ isolation resistance between the solar array substrate/frame and spacecraft chassis. This will limit currents from the solar array to its substrate and returning through the spacecraft structure. The resistance should be calculated for all the parameters of the solar array and environment. This is a new rule compared to NASA TP-2361 [5], which had recommended that the solar array structure be carefully grounded to the spacecraft structure. Extra mechanical complexity will

be required to provide the necessary insulation between the main spacecraft and the solar array structure. See Bogus et al. [21] for example.

The resistor lower bound size should be a value that limits any fault currents to a small value that will interrupt any holding currents caused by a triggering ESD event from the array to the structure. Assuming 1 mA as a maximum permissible sustained fault current (very conservative) on a 100 V array, the calculation would be 100 V/1 mA or 100 kΩ as the minimum solar array structure isolation from the spacecraft chassis.

The resistor upper bound sizing relates to controlling the differential potential of the array with respect to chassis. For example, if space plasma charging currents are expected to be 1 nA/cm^2 (GEO), the maximum value of collected current would be calculated as array area times 1 nA/cm^2. If we assume that the maximum array support structure potential with respect to the spacecraft bus is desired to be less than ~10 V and the array area is 4 m^2, this gives 250 kΩ as the maximum solar array isolation from the spacecraft chassis.

u. Consider possibilities. For example, in LEO regimes, the plasma can initiate an arc for 75 V arrays, and the arc can be sustained by the power of the solar array. At GEO and other locations, the arc initiator could be charging of the dielectric surfaces (this environment requires perhaps as much as a 400 V differential to the array wiring) in the vicinity of a conductor with the same result. The design should accommodate any situation that occurs, with focus on the anticipated environment, if known. Extreme temperatures, solar illumination, cell-to-cell potentials, and plasma density and temperatures are some of the environmental parameters.

v. Consider Si cells versus GaAs cells. It may be that Si or GaAs cells are inherently less likely to have ESDs. To date, the data have too many variables to say which is better, but future research may determine that there is an advantage to one or the other.

w. Insulate the solar array connector wires leading into the spacecraft as much as possible. Solar array drive assembly details include isolating wiper arms and slip ring spacer insulator height [22].

x. Consider use of the stretched lens array as advocated by Brandhorst [23]. This is a concentrator technology that may eliminate many space charging problems with solar arrays and has been space qualified.

3.2.4.4 *Solar Array Testing Rules for Space Charging Characterization*

Figure 3-9 [3] shows the typical elements of a solar array ESD charging threat test. Figure 3-9 is intended to provide a simple introduction to test needs. Many solar array test plans become increasingly complex with attempts to add better simulation of reality but in a limited test space and with sample coupons rather than the real full-size article. The test layout in Fig. 3-9 may be modified to reflect a more specific knowledge of solar array equivalent schematics or changed if newer applicable requirements documents become available. Additional details involve capacitances to simulate stored energy in the capacitance of the cells that can cause an initial high current pulse, inductances in wiring that can cause ringing and resonances, and a grounded substrate that may provide a ground return for an arc. A well-thought out test has a number of details needed to simulate the space situation as closely as possible.

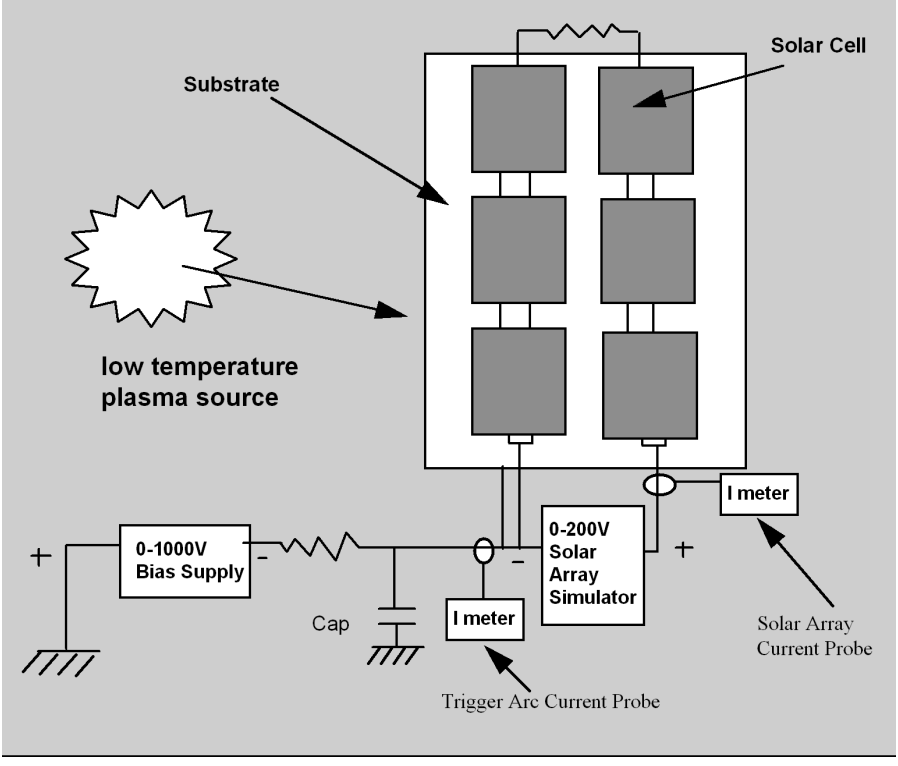


Fig. 3-9. NASA Lewis Research Center (LeRC) (now Glenn Research Center (GRC)) solar array space charging and ESD test setup.

Test parameters that add to the complexity include:

a. Actual spacing and construction of the solar array.
b. Simulation of the plasma environment.
c. Simulation of the higher energy electron environment.
d. Simulation of the Sun.
e. Temperature of the array/cover glass, including occultation (no solar simulation).
f. Energy storage of a string (capacitance to ground, if a partial array is used).
g. Simulation of the solar array dynamics, including transient voltage slew rate and capacitance to ground.
h. Simulation of the wiring (capacitance and inductance effects).
i. Presence of grounded or isolated cell substrate.

Amorim [24] is an excellent paper showing solar array arcing current as measured in the laboratory, with discussion and interpretations for space needs.

3.2.5 Special Situations ESD Design Guidelines

The guidelines in this section are special situations that are easier treated separately. General ESD design guidelines are provided in Section 3.2.1.

3.2.5.1 Thermal Blankets

All metalized surfaces in MLI blankets must be electrically grounded to the structure. The metalized multilayer surfaces in each separate blanket should be electrically grounded to each other by ground tabs at the blanket edges. Each tab should be made from a 2.5 cm-wide strip of 0.005 cm-thick aluminum foil. The strip should be accordion folded and interleaved between the blanket layers to give a 2.5 × 2.5 cm contact area with all metalized surfaces and the blanket front and back surfaces. Nonconductive spacer or mesh material must be removed from the vicinity of the interleaved tab; or it must be verified that all conductive layers are grounded, if spacer/mesh material is not removed. The assembly should be held in place with a metallic nut and bolt that penetrates all blanket layers and captures 2.0 cm-diameter metallic washers positioned on the blanket front and back surfaces and centered in the 2.5 cm × 2.5 cm tab area. The washers may have different diameters, with the inner surface of the smaller washer recessed to ensure maximum peripheral contact area between the interleaved foil strip and each metalized blanket surface. The tab should be

grounded to structure by a proven technique such as a wire that is as short as possible (15 cm maximum) or conductive Velcro®.

Redundant grounding tabs on all blankets should be implemented as a minimum. Tabs should be located on blanket edges and spaced to minimize the maximum distance from any point on the blanket to the nearest tab. Extra tabs may be needed on odd-shaped blankets to meet the condition that any point on a blanket should be within 1 m of a ground tab.

The following practices should be observed during blanket design, fabrication, handling, installation, and inspection:

a. Verify layer-to-layer blanket grounding during fabrication with an ohmmeter.

b. After installation, verify less than 10-Ω dc resistance between blanket and structure with an ohmmeter. (Verification details in test procedures.)

c. Close blanket edges (cover, fold in, or tape) to prevent direct irradiation of inner layers.

d. Do not use crinkled, wrinkled, or creased metalized film material.

e. Handle blankets carefully to avoid creasing of the film or possible degradation of the ground tabs.

f. If the blanket exterior is conductive (paint, ITO, fog), make sure that it is grounded. Verify with an ohmmeter.

3.2.5.2 Thermal Control Louvers

Bond/ground the thermal control louver blades and axles. The easiest way to bond the blades to chassis is to have the bimetal spring electrically bonded at both the blade/axle and the spacecraft structure. Alternatively, place a thin wiper wire from spacecraft chassis to the axle.

3.2.5.3 Antenna Grounding

Antenna elements usually should be electrically grounded to the structure. Implementation of antenna grounding will require careful consideration in the initial design phase. All metal surfaces, booms, covers, and feeds should be grounded to the structure by wires and metallic screws (dc short design). All waveguide elements should be electrically bonded together with spot-welded connectors and grounded to the spacecraft structure. These elements must be grounded to the Faraday cage at their entry points. Conductive epoxy can be

used where necessary, but dc resistance of about 1 Ω should be verified by measurements.

3.2.5.4 Antenna Apertures

Spacecraft radio frequency (RF) antenna aperture covers usually should be ESD conductive and grounded. Charging and arcing of dielectric antenna dish surfaces and radomes can be prevented by covering them with grounded ESD-conductive material. Antenna performance should be verified with the ESD covering installed.

For a dielectric radome, there have been problems of damage to nearby electronics. Sometimes the radome may be spaced very near low-noise amplifiers (LNAs). If the radome surface charges, electrostatic attraction may draw its surface near the LNAs, and a spark could destroy them; this is a suspected culprit for some on-orbit failures. In such a case, the radome must be spaced far enough away that it cannot damage any LNA or similar nearby electronic devices.

A similar problem exists if there are metal antenna elements in a dielectric matrix, all exposed on the surface. An ESD arc from the dielectric to the antenna element, carried down a coaxial cable to the receiver front end (or transmitter output), can do the same sort of damage. Situations such as this (ESD events caused by surface metals near dielectrics that are carried down to delicate electronics) must be handled with care; filtering or diode protection must be applied to protect the electronics from damage.

Coverings on antenna feeds and parabolas should be considered. Isolated dielectric materials on an antenna system, especially near feed lines, can store excess charge or energy. For example, if there is an isolated dielectric mounted on top of a fiberglass separator that is adjacent to the feed electrical path, there can be discharges directly into the receiver. These dielectrics are special problems because they are on the outside of the spacecraft and have less shielding. Assess each of the region's hazards, and compare to the receiver or LNA ESD sensitivity.

3.2.5.5 Antenna Reflector Surfaces Visible to Space

Grounded, conductive spacecraft charge-control materials should be used on antenna reflector rear surfaces visible to space. Appropriate surface covering techniques must be selected. Such methods include conductive meshes bonded to dielectric materials, silica cloth, conductive paints, or non-conductive (but charge bleeding) paints overlapping grounded conductors. Properly constructed thermal blankets may also accomplish this need to prevent surface charging.

Ungrounded array elements, such as for special antenna surfaces, may include ungrounded conductors as a necessary part of their design, e.g., tuned reflector array elements. These may be left ungrounded if analysis shows that the stored energy available from space charging will not affect any possible victims.

3.2.5.6 Transmitters and Receivers

Spacecraft transmitters and receivers should be immune to transients produced by ESDs, including those from dielectrics in the antenna (surface charging) and feed system (internal charging). Transmitter and receiver electrical design must be compatible with the results of spacecraft charging effects. The EMI environment produced by spacecraft ESD should be addressed early in the design phase to permit effective electrical design for immunity to this environment. The transmitter, receiver, and antenna system should be tested for immunity to ESDs near the antenna feed. Consider the possibility of an arc from a dielectric that sparks to the center conductor of a coaxial cable to a delicate receiver or transmitter device at the other end of that coaxial cable. Change the design if necessary. Verification tests should be established by an experienced ESD engineer.

3.2.5.7 Attitude Control Packages

Attitude control electronics packages should be made insensitive to ESD transients. Attitude control systems often require sensors that are remote from electronics packages for Faraday cage shielding. This presents the risk that ESD transients will be picked up and conducted into electronics, especially via the cabling if shielded inadequately. Particular care must be taken to ensure immunity of interface circuits to ESD upset in such cases.

3.2.5.8 Deployed Packages

Deployed packages should be grounded by using a flat ground strap extending the length of the boom to the vehicle structure. Several spacecraft designs incorporate dielectric booms to deploy payloads. The payload electrical system may still require a common ground reference, or the experiment may require a link to some electric potential reference. In these cases, it is recommended that a flat ground strap be used to carry this ground tie to the vehicle structure. Electrical wiring extending from the deployed payload to the spacecraft interior must be carried inside or along the dielectric booms. This wiring should be shielded and the shield grounded at the package end and at the Faraday cage entrance.

3.2.5.9 Ungrounded Materials

Specific items that cannot be grounded because of system requirements should undergo analysis to assure specified performance in the charging environment.

Certain space vehicles may contain specific items or materials that must not be grounded. For example, a particular experiment may have a metallic grid or conducting plate that must be left ungrounded. If small, these items may present no unusual spacecraft charging problems; however, this should be verified through analysis.

3.2.5.10 Honeycomb Structures

Honeycomb structures need special grounding methods. Be aware that the aluminum honeycomb interior may be isolated from conductive and grounded face sheets by felt pre-preg adhesive-impregnated material. A small ground wire running across the aluminum honeycomb and pressed against the edge can provide a ground. The conductive face sheets may lose their grounding when they are butted against each other. Develop processes that assure that all metal parts of the honeycomb structure and face sheets will be grounded. After assembly, the inner parts cannot be checked to see if they are grounded.

3.2.5.11 Deliberate or Known Surface Potentials

If a surface on the spacecraft must be charged (e.g., detectors on a science instrument), it should be recessed or shielded so that the perturbation in the surface electrostatic potential is less than 10 V. Scientific instruments that have exposed surface voltages for measurement purposes, such as Faraday cups, require special attention to ensure that the electrostatic fields they create will not disrupt adjacent surface potentials or cause discharges by their operation. They can be recessed so that their fields at the spacecraft surface are minimal or shielded with grounded grids. These detector apertures should have a conductive grounded surface around them and in their field of view. An analysis may be necessary to ensure that their presence is acceptable from a charging standpoint and that surrounding surfaces do not affect the measurements.

Figure 3-10 [25] presents an analytic result showing the disturbances in electron paths in the presence of electric fields from spacecraft surface charging, in this case from dielectric surfaces charged by space plasma. Figure 3-10 shows a calculation of particle trajectories distorted by electric fields on parts of the Galileo spacecraft. The 10 curves represent paths of 1 to 50 eV electrons, with lines at logarithmically equally spaced energies. The distorted paths of the lower energy electrons show clearly in this simulation. The design was changed to permit undistorted science measurements.

3.2.5.12 Spacecraft-Generated Plasma Environment

The total plasma environment includes plasma generated by spacecraft electric propulsion (arc jets, Hall thrusters, and ion thrusters) and possibly other

sources. This was shown to be a critical consideration because when thrusters are fired they can surround GEO spacecraft with LEO-type plasma. That plasma can have a major impact on, as a minimum, GEO solar array designs. It is especially important if thrusters are fired during the time a spacecraft is negatively charged by GEO plasma. It can result in unexpected synergistic effects that can lead to ESD events and damage of solar arrays [26].

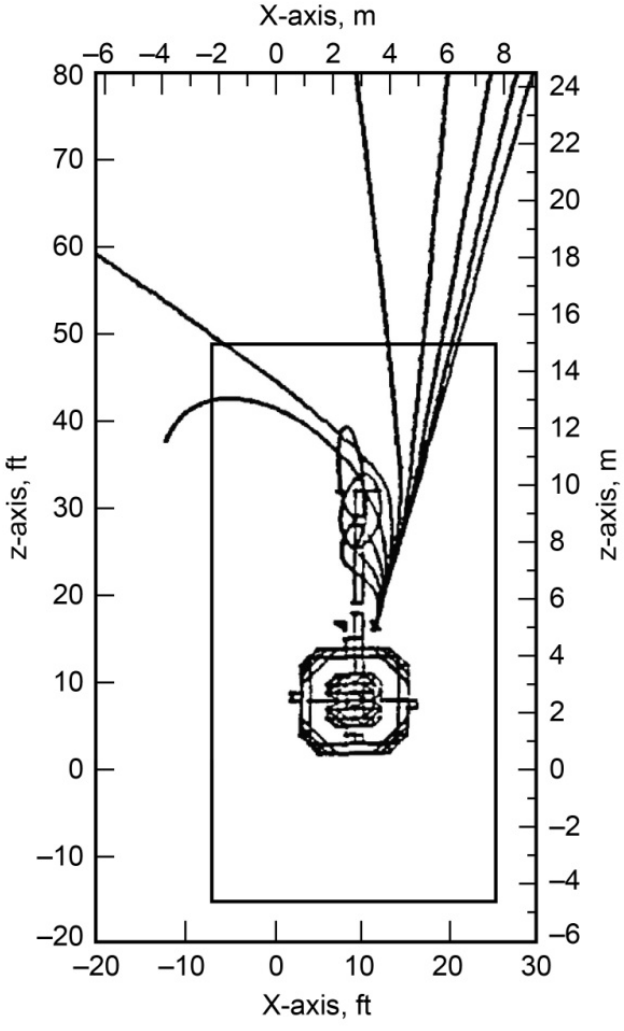


Fig. 3-10. Electron trajectories for Galileo [25].

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