Chapter 4: Programmable Logic Devices

4.1 Chapter Overview

This Chapter provides an overview on Programmable Logic Devices (PLDs) form the history of programmable logic devices to the device types. PLDs come in two forms, Complex Programmable Logic Devices (CPLDs) and Field Programmable Gate Arrays (FPGAs) both having their advantages and disadvantages with respect to the specific application or design they are to be used in. The PLD used for our design, which was a CPLD from Lattice Semiconductor is discussed. There is a need for design of smaller more dense electronic designs requiring less board space as well as less power in the space and military industries there are very few PLD vendors that provide Radiation Hardened components. Unfortunately intellectual Property Cores will be discussed which is the latest trend for vendors to provide system-on-a-chip capability for their FPGA's.

4.2 Introduction

4.2.1 Background of Programmable Logic Devices

A programmable Logic device refers to any type of integrated circuit that a logic design can be implemented and reconfigured in the field by the end user. Since these logic devices can be programmed in the field they are also called Field Programmable Logic Devices (FPLDs). The PLD provides flexibility for designers to implement many different designs in varying complexities for many different applications. One of the most common PLDs is the one time Programmable Read-only Memory (PROM). This comes in two different types: (a) mask programmable devices programmed by the vendor using a custom mask and interconnects and (b) field programmable devices that are

configured by the user. One of the great advantages of PLDs is that they are very inexpensive at low quantities.

A device that was a follow on from the PROM technology that can be used for logic designs was the Programmable Logic Array (PLA). The PLA using the PROM structure turned out to be the first Field Programmable Logic Array (FPLA). The first FPLA was introduced in the mid-1970s. The FPLA had a fixed number of inputs, outputs and product terms that consisted of AND and OR arrays that contained programmable inputs. The FPLA did not have great success because they were very slow and complicated to use. The designer had to design to a fuse map instead of conventional boolean equations or schematic capture.

In the late 1970s the Programmable Array Logic (PAL) architecture was introduced that increased the use of programmable logic. The PAL architecture consisted of a programmable AND array and a fixed OR array so that each output is the sum of a specific set of product terms. The design entry tool for the earlier PAL was in the form of Boolean equations making it very easy to learn and implement. PAL devices are now available in different varieties from different vendors providing flexibility inputs/outputs, size of the OR-gate, and flip-flops. Some PALs are even provided in either NAND/NAND or NOR/NOR structure to increase design flexibility instead of the AND/OR structure.

PLDs can be divided into two groups, Simple Programmable Logic Devices (SPLDs) and High-Density Programmable Logic Devices (HDPLDs). SPLDs come in the PAL and PLA architecture, while HDPLDs include CPLDs and FPGAs. Figure 4.1

contains a hierarchical block diagram of the PLD architectures, subfamilies and programming technologies.

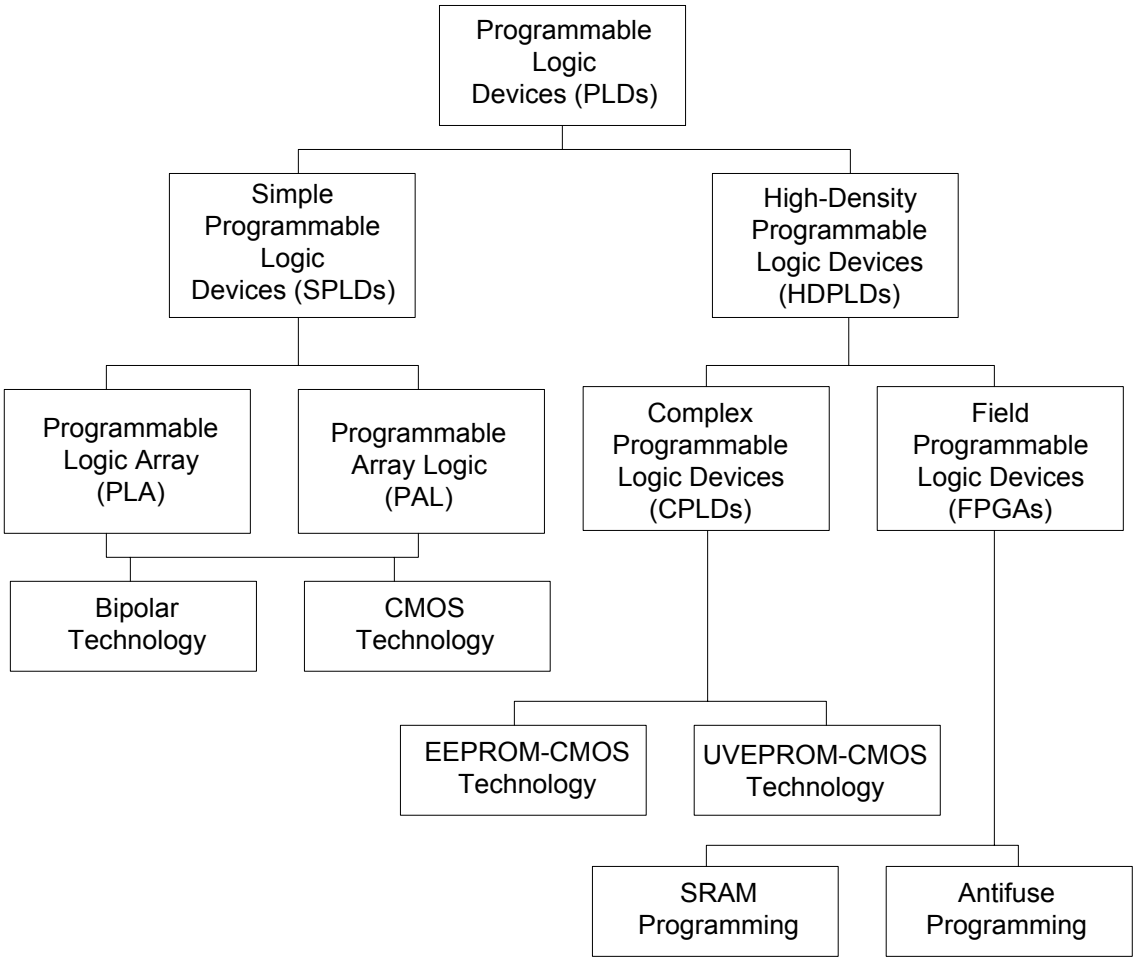

Figure 4.1 PLD Hierarchical Architecture

4.2.2 Simple Programmable Logic Devices

The simple PAL architecture has become an industry standard. PLAs and PALs that have pin packages of 20 – 44 pins and density ranging from 100 to several hundred gates are considered SPLDs. The Basic AND/OR architecture PALs are flexible devices that can implement logic equations in Boolean sum-of-product (SOP) form. Some enhancements to SPLDs have been programmable input/outputs (I/Os), bidirectional I/Os, programmable output polarity, flexible register configurations and chip clocks.

One important advantage for PLDs is that they can replace small to medium-scale integrated (SSI/MSI) circuits for higher packaging density. One PLD could replace tens of integrated circuits with 200 – 500 gate equivalent. Other benefits for SPLD is that they reduce power, have faster turn-around time, faster performance because they reduce interconnects between chips and higher reliability. SPLDs are available in bipolar and Complementary Metal Oxide Semiconductor (CMOS) technology. In CMOS technology, they come in Erasable PROM (EPROM) based which are Ultraviolet Erasable (UVEPROM) and Electronically Erasable (EEPROM).

Due to the simple architecture of an SPLD they offer very high performance. The SPLD devices are at 0.5 um CMOS process with logic delays down to 3.5 ns and frequencies as high as 200 MHz. Higher density devices are coming on the market in the area of Complex Programmable Logic Devices (CPLD) with high performance, but SPLDs still have the best performance, easier to use and design with because they are an industry standard. Computer networking components and other telecommunication equipment still demand the need for SPLD devices due their high performance. Because of the trend to migrate to higher densities SPLDs have been driven to specialty markets such as cellular phones, video games and hand held web browsers. Table 4.1 shows a comparison of SPLDs and CPLDs over a broad range of criteria.

New innovative advancements in SPLD include programmable output logic, macrocells that can be configured as combinatorial or register operation and active low or active high polarity. SPLDs are also available in lower-voltage and low power offering 5 volt and 3.3 volt devices. This allows more flexibility for design applications that require trade-offs between low power, high frequency and low voltage.

Criteria	SPLD	CPLD
Propagation Delay	High Speed - Typically 3.5 ns	High Speed - Typically 10 ns
Density	100 to Several Hundred	Several Hundred to several Thousand (25,000 Gates)
Technology	Bipolar and CMOS	CMOS
Ease of Designing	Very Easy	Medium Ease
Complexity	Simple Architecture	Medium to Difficult Architecture
Frequency	200 MHz	100 MHz
Programmable I/Os	Yes	Yes

Table 4.1 SPLD and CPLD Comparison

4.2.3 High Density Programmable Logic Devices

The main disadvantage for the SPLD is an architectural limitation. SPLDs have a limited amount of logic structures that can be allocated in a design in a fixed way. High-density or high-capacity PLDs (HDPLDs/HCPLDs), which are also called complex PLDs (CPLDs) and Field Programmable Gate Arrays (FPGAs), try to solve the silicon limitation by adding more flexible block structures and interconnects. Programmable Logic Devices include simple as well as high-density PLDs.

In 1985 Xilinx Corporation came out with the first FPGA. It introduced the Logic Cell Array (LCA) and was the building block for all FPGAs to follow. It contained a pool of independent logic cells and multiple routing resources that allowed any logic cell to be connected to any other logic cell. This provided routing flexibility. The first LCA consisted of a combinatorial logic function and a flip-flop. The I/Os could be programmed as input, output and bi-directional and the routing resources allowed for distributed clock through the chip, high speed and low-skew signals and local routing from LCA to LCA.

The two major elements of CPLDs and FPGAs are the logic elements and the interconnect structure. The logic elements are also known as macrocells, logic cells and/or logic blocks. The interconnect structure is how those elements are connected together to perform the design for a specific application. As mentioned there are two high-density programmable logic devices. Those are complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs). It is hard to determine the difference between the two but usually in CPLDS there is fixed routing resources on-chip and routing is done via a switching matrix, which leads to predictable delays. In the SPLD architecture, each macrocell contains its own product term. However, in the CPLD architecture the vendor takes advantage of the complex macrocells and employs product term steering or product term sharing between the macrocells. The term complex in CPLD refers to pin count and the amount of internal macrocells. The vendors try to provide an output pin for each input set, which increases the complexity.

One of the main performance criteria for PLDs is Total propagation delay (Tpd), which is the delay from the input to the output pin through a specific function. On SPLDs of 44 pins this value is fixed and predictable due to less complex designs and is averaged to be about 5 ns. When there is a larger and more complex design the Tpd can be as high as 7.5 ns on devices that have 100 pins and 128 macrocells.

In the past, there has not been a clear distinction between the roles of CPLDs and FPGAs until recently. A CPLD used to be higher priced and as mentioned have predictable timing specifications making them ideal for high-speed applications. FPGAs where more reasonably priced and satisfied the requirements for low to medium end performance applications. FPGAs have found a niche for space and military applications

due to the availability of radiation Hardened devices. This will be discussed later in the chapter. Recently, CPLDs have been reduced in cost and have added additional features such as in-circuit programmability and higher gate count. They tend to lend themselves toward high-speed applications; real time video processing and Digital Signal Processing (DSP). The CPLDs used for this design cost $50.00 a unit making them attractive for a tight budget. Both CPLDs and FPGAs are available in SRAM based programming configuration but only CPLDs can be EPROM or EEPROM programmed. This means that CPLDs can be up and running when power is applied and are nonvolatile. Some FPGAs are antifuse-based allowing them to only be one time programmable devices (OTPs) and SRAM based, which can be programmed as many times as required.

High-density PLDs come in two basic architectures. Figure 4.2 shows the connectivity differences between the two architectures. They are segmented-block based and channel-array-based. Segmented-block architecture consists of a series of logic arrays and I/O macrocells that are connected together with an interconnect matrix. CPLD Examples of these are Advanced Micro Devices/Vantis MACH family and Altera Corporation's MAX family of devices. Segmented-block FPGAs have different means of implementing logic functions. One way is through the use of SRAM based Look-up tables (LUTs) and the other is through multiplexer-based logic elements that are typically in antifused-based devices like Actel Corporation's ACT1, ACT2 and ACT3. Antifuse-based FPGAs have less resistance than SRAM based, which decreases delay times, but are non-reprogrammable. Nonsegmented-block or channel-array-based contain input pins connected to logic array elements that have interconnect paths to macrocells which in-turn are connected to the I/O pins. Some examples of channel-array-based FPGAs are

Xilinx Corporation Logic Cell Array (LCA), Atmel's 6000 series and Lucent technologies' ORCA series. Channel-array-based devices are register rich, have many I/Os and have programmable interconnects between the logic elements and the I/O blocks. The SRAM based devices are more resistive than the antifuse-based and are typically slower.

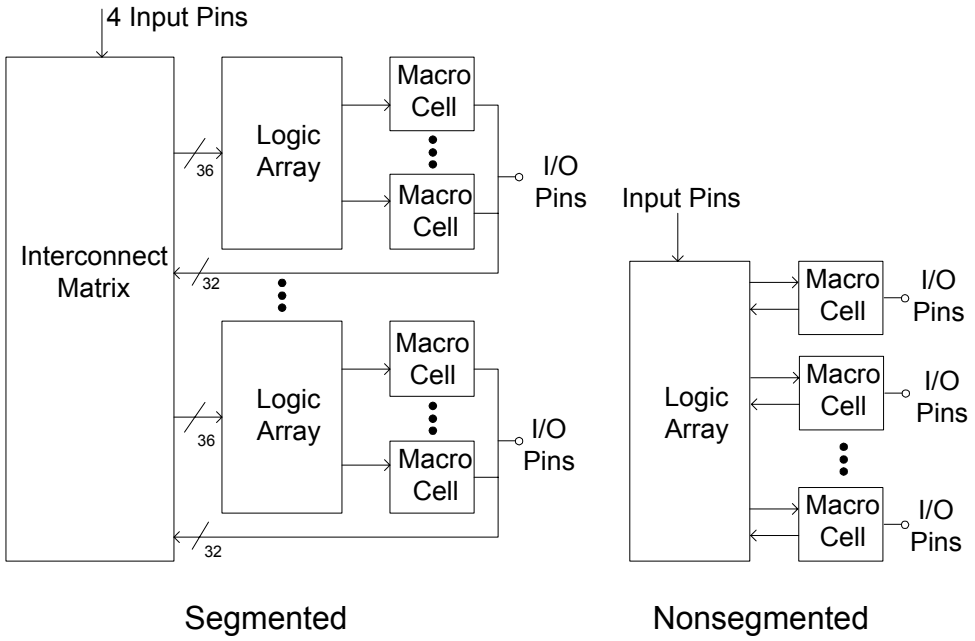

Figure 4.2 Architectural Comparison Between Segmented and Nonsegmented

There has always been a debate over when to use a FPGA and when to use a CPLD. CPLDs are ideal for control circuits and state-machine based control logic. They have fast, predictable timing. It is very difficult to predict the data path delays in a FPGA. The greatest advantage to FPGAs is having finer logic blocks and a very flexible architecture for implementation in control logic designs, data path designs, arithmetic and logic functions as well as register rich designs.

4.3 Simple and Complex Programmable Logic Devices

4.3.1 Detailed Architecture

Low density PLDs consist of PAL or PLA structures. These structures can be in the form of AND-OR, NAND-NAND or NOR-NOR in multi levels of logic with I/O macrocells and I/O pins. Figure 4.3 shows a portion of a simple PAL architecture. The four most important elements of the PAL structure are as follows:

1. The AND-plane provides the connections between the inputs and the AND gates or the product terms that implement the logic functions or control logic.
2. The OR-plane makes the connections between the AND-plane and the outputs. The OR-plane defines the number of ORed outputs, the number of product terms per output, how the product terms are distributed over the outputs and the connections of the Ored outputs with the storage elements.
3. The storage elements determine the structure of the outputs. The storage elements are flip-flops that can provide clocking or feedback into the logic. The outputs can be configured to be sequential or combinatorial and have active high or low pull up resistors. The storage elements can be configured as edge-triggered D-type, J-K, R-S or T flip-flops, or transparent latches.
4. The I/O pins can be configured as an input, output or bidirectional.

SPLDs of today are ten times faster then the original PALs. The propagation delay of PLDs is down to 3.5 ns and even faster for state-of-the-art versions. The delay is slow due to the oxide-isolated submicron 0.35 um processes and the UVEPROM and EEPROM storage cells.

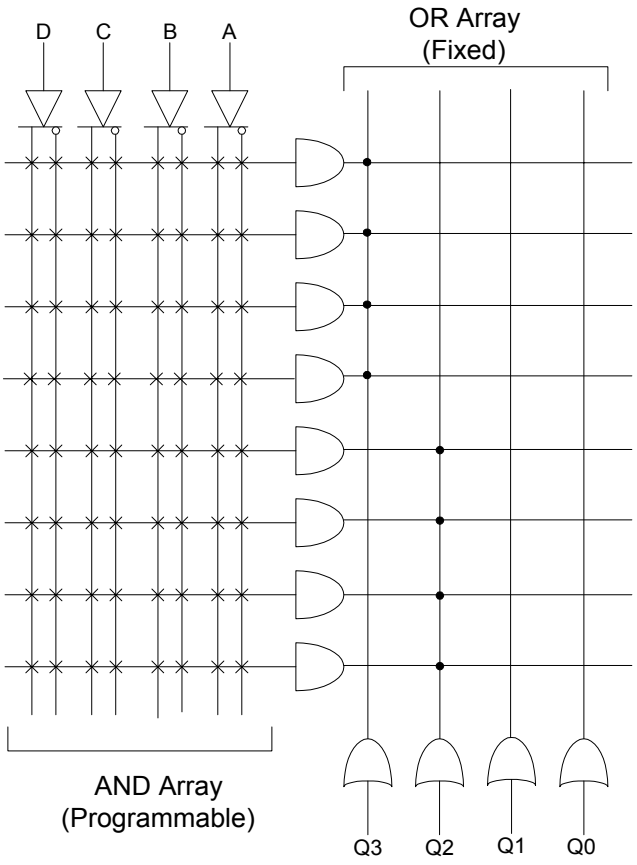

Figure 4.3 Simple PAL Architecture

CPLDs consist of logic blocks, programmable interconnects, and I/O cells. Each logic block in the CPLD contains inputs, logic arrays and the array allocators, macrocells, and I/O cells. Figure 4.4 contains a generic block diagram of the CPLD architecture and functional description. The logic blocks perform sum of product logic function and store the results in registers in the macrocells. The interconnections route signals to and from the logic and I/O cells to implement the desired logic design.

The resources that are available in a CPLD are as follows:

1. The number of macrocells is the amount of registers available to implement the logic function or the design to be implemented. The number of macrocells determines the complexity of the design.

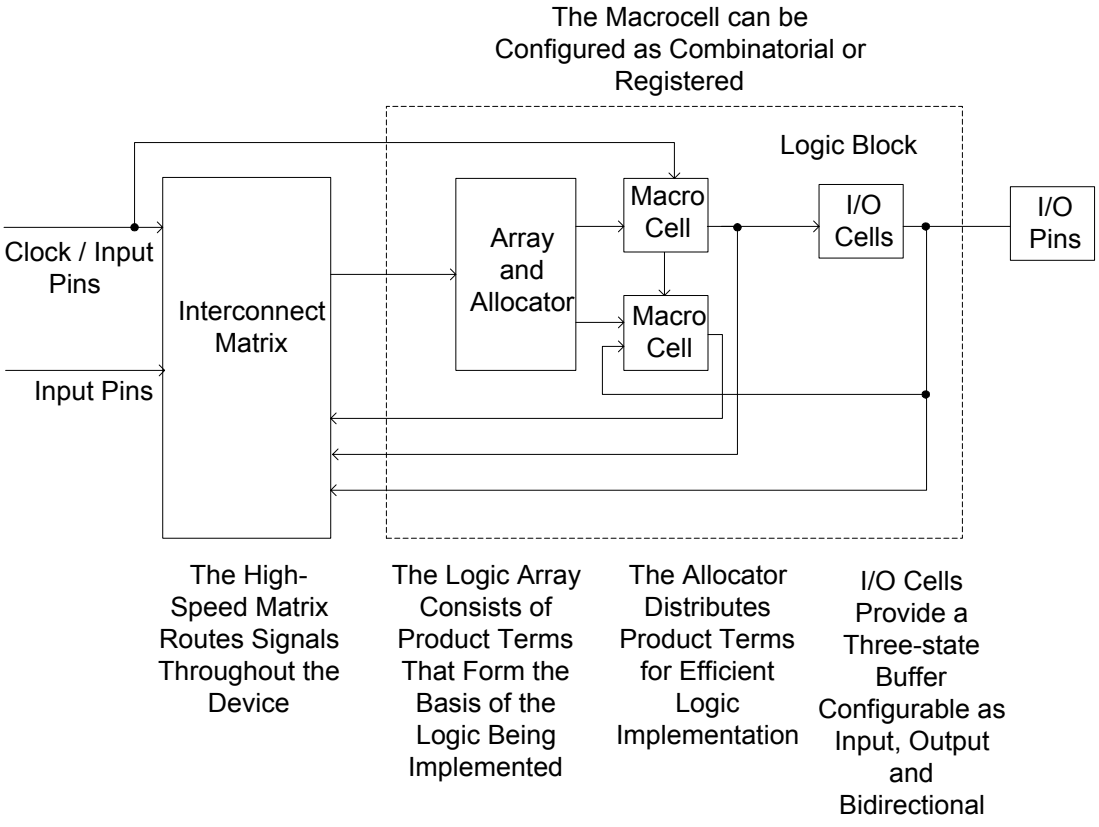

Figure 4.4 CPLD Architectural Block Diagram

2. The number of inputs to individual logic blocks is another important resource. If the design requires more inputs to a specific set of logic blocks than are available, then multiple logic blocks can be used to account for the lack of available inputs.
3. The final resource is the total number and allocation of product terms. The total number of product terms that the device can OR together defines the upper limit for the amount of logic that can fit into the CPLD. Product term allocation is sometimes more important than the total number of product terms. Some times the allocation function needs to feedback through multiple logic cells to implement the logic function at the expense of increased delay. Sometimes the allocation function requires that product terms be assigned to individual macrocells or product terms to be assigned to multiple macrocells for product term steering and sharing respectively.

The CPLD performance is dependent upon the interconnections between logic cells for which there are two different aspects as follows:

1. The number of signals that the global interconnect provides to each logic cell determine how well the CPLD will perform on a specific logic design. If the amount of input signal to the logic cells is smaller than the number that is required for the logic function then it will have to be slit between multiple logic cells to account for the lack of input signals.
2. The second performance aspect is routability efficiency or how well the interconnect signals get routed between the logic cells in the most efficient manner. When the number of signals that need to be routed reaches a maximum for the specific design and chip architecture, it becomes more difficult to route the signals.

CPLDs consist of two types of interconnect structures.

1. The first type is called the crosspoint switch architecture. This architecture is completely routable because any combination of signals can be routed from any logic block via the global interconnect. The only problem with this architecture is that the vast amount of routing capability decreases the overall speed and increases the die size.
2. The multiplexer approach is used instead of the crosspoint switch to increase the overall speed and to reduce the size of the chip. Figure 4.5 contains a block diagram of the multiplexer-based interconnect structure. Many vendors have different approaches to try to optimize the routability efficiency.

CPLDs have a wide input structure and large sum of product arrays. They are ideal for implementing fast state machine designs, high speed control logic and fast decode

applications. Many vendors have implemented the in-system programmability function that reduces on the chip handling and makes it flexible to change designs while the chip is mounted on the board.

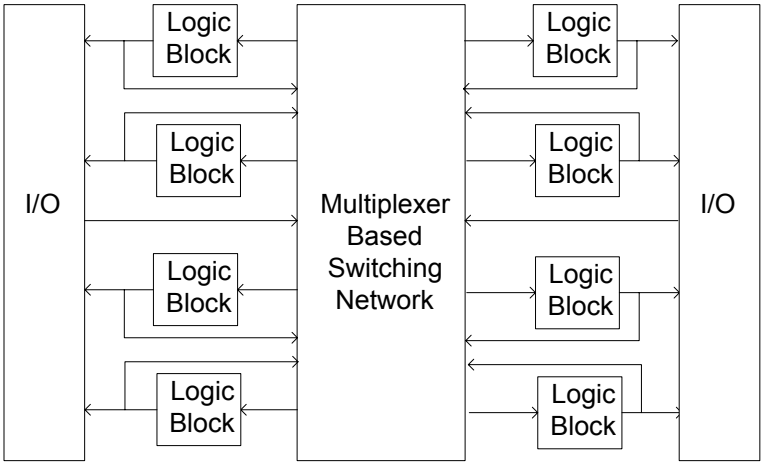

Figure 4.5 CPLD Multiplexer-Based Interconnect Structure

4.3.2 Programming Technologies

The programming technology of earlier PLDs was based on bipolar processes, which came from PROM technologies. The PROM structure contained lateral fuses and vertical fuses. The lateral fuses, or metal alloy, would interconnect two wires. When the lateral fuses are blown due to the current through a bipolar transistor, the two wires are not connected. The vertical fuses did not have the metal alloy but they did have the bipolar transistors in series with back-to-back diodes. The diodes would isolate the two wires in the not blown state. Enough current through the transistor would cause an "avalanche effect" that would short one of the diodes connecting the two wires. The fuses are made out of different materials like nichrome, titanium-tungsten and platinum silicide. The fusible-link PLDs have different programming requirements that are specified by the vendor in the data sheets.

The programming technologies for CPLDs are UVEPROM and EEPROM. In the EEPROM and UVPROM CPLDs transistors are used as switches to make interconnects just as the fuses in the SPLDs. The programming technology is an important element when selecting devices. The selection of a particular device also depends on volatility, nonvolatility, reprogrammability, in-system programmability (ISP), program time, erase time and testability.

The electrically erasable CMOS technology is based on a stored charge on a transistor with a "floating gate" or a gate that has no connection. There are actually two transistors, one that has the floating gate and another that is the control gate. In the programmed state the transistor is turned on due to a positive charge caused by a deficit of electrons in the floating gate. Figure 4.6 shows the schematic for the electrically erasable programming cell.

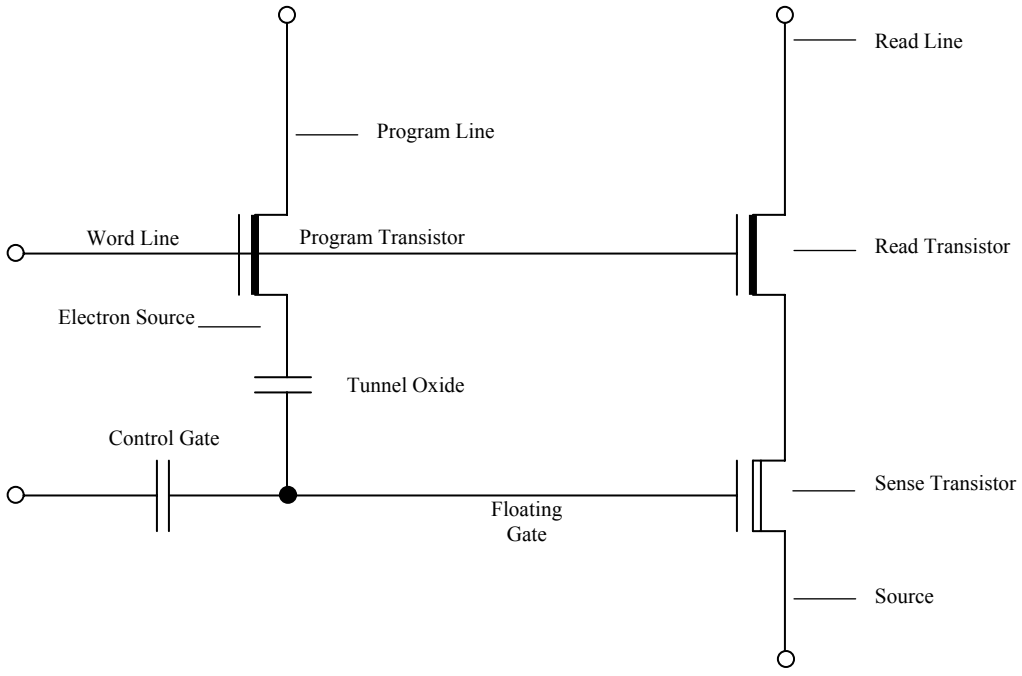

Figure 4.6 Schematic of Electrically Erasable Programming Cell

Hot electron injection and tunneling are the two ways of transferring a charge on to the floating gate. UVEPROM uses hot electron injection and EEPROM uses tunneling. In hot electron injection a bias is set between the source and the drain of the transistor of the control gate and the substrate. A strong current is present causing the channel to be pinched off. A field is formed in the diagonal direction by two applied electrical fields. The electrons can not pass in that direction due to the oxide barrier. Some electrons have enough energy to cross the barrier at the shortest point over into the floating gate where they are trapped. The term hot electron injection refers to the high electron fields. During programming large electron fields are established to get a large amount of electrons over the oxide barrier and over to the floating gate. Exposing the device to UV light will erase the device because it causes the electrons to cross back over the barrier. The UVEPROM devices need a window to allow the UV light to enter the device. The special packaging of the device increases the cost and results in about 30 to 45 minutes to erase the device. Figure 2.7 shows a schematic of hot-electron injection in UV-erasable devices.

Electrically erasable devices use Fowler-Nordheim tunneling to get the electron over the barrier onto the floating gate. The electrons tunnel through the barrier when a field is applied. For electrically erasable parts the oxide barrier is about one-third the thickness as it is for UV parts, making the field much less to get the electrons across. EEPROM based devices are more cost effective than UVEPROM based devices.

To improve the performance of electrically erasable PLDs, the programming cell has been divided into two parts. One is the programming portion and the other is the data path portion. The programming portion requires transistors that can handle high

electrical fields and the data path portion requires transistors that are fast. A cell is programmed if it generated a negative voltage as a result of no charge on the floating gate. Large amounts of charge on a floating gate caused by applying a negative voltage will erase a cell. When a voltage is applied between the program and control gate nodes, the direction of that voltage determines if the device is getting programmed or erased. If the control gate is given a positive voltage and the program node is grounded the device is being erased. The positive voltage draws electrons across the tunnel oxide form the program transistor to the floating gate, which turns the read transistor OFF. For programming, the program node voltage is higher and the control gate is grounded causing electrons to flow from the gate leaving behind a positive charge that turns the transistor on.

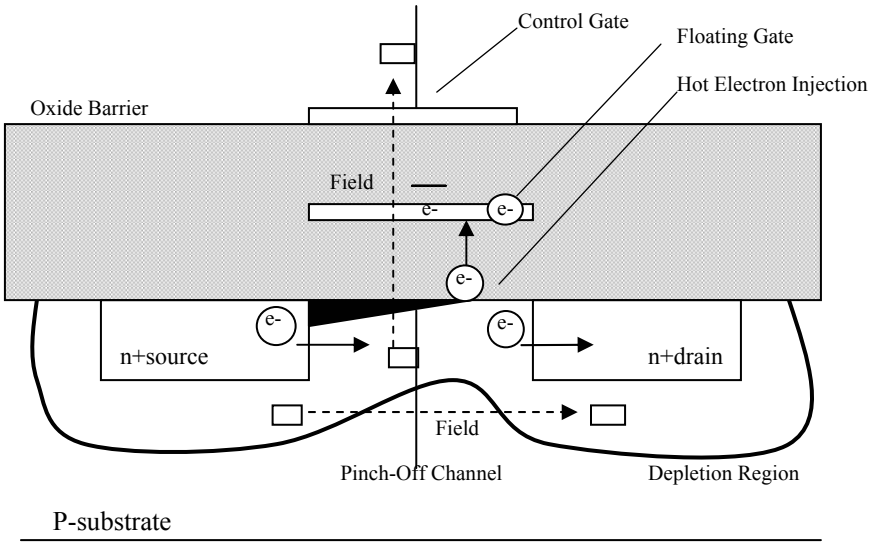

Figure 4.7 Schematic of Hot-Electron Injection

4.3.3 Simple and Complex Programmable Logic Devices Summary

There are many different SPLD/CPLD vendor and their device families and architectures. The major SPLD/CPLD vendors and device families are AMD/Vantis with PAL and MACH families, Altera with MAX and FLEX families, Cypress Semiconductor EPLD/CPLD families, ICT Peel arrays family, Phillips Semiconductors' CPLD families and Xilinx FastFlash CPLD family, just to name a few. Depending on the design requirements and specifications, there are tradeoffs on selecting FPGA architectures over CPLD architectures. There are also tradeoffs in selecting a specific CPLD architecture to meet the system requirements. The next section will cover the CPLD vendor and architecture chosen to implement the design. Lattice Semiconductor is the CPLD vendor with high-density in-system programmable Large Scale Integrated (ispLSI) CPLDs. The Lattice CPLD architecture provides very flexible architecture with high-density logic. The Camera design implemented is for a research and development project with general requirements. The in-system programmable feature allowed for ease in design modifications and debugging capability. The cost of the devices and the Electronic Design Automation tools to implement the design was reasonable for the budget available. A very important feature is the predictable timing of a CPLD. The interface design was a complex design done in VHDL. The predictable timing allowed for learning the design and the code rather than the device architecture and timing issues. The Lattice devices also have a wide range of speed options, which meet the requirements of the design. The VHDL implementation of the design will be discussed in Chapter 6, VHDL Design Entities.

4.3.4 Lattice Semiconductor Overview

Lattice Semiconductor CPLDs are nonvolatile EECMOS technology. There are six families and they are 1000/1000E, 2000/2000V, 3000 and 6000. The densities range from 1000 to 25,000 PLD gates. A very important feature of this architecture is the Global Routing Pool, which connects all the internal structures and I/O's with predictable timing. Another key element is the Generic Logic Blocks (GLB). They provide a high input to output ratio for design optimization. The architecture also allows for a Product-Term-Sharing Array (PTSA) and two types of clocking signals. The two clocks are an external globally distributed snychronous clock and an internal globally distributed asynchronous product term clock. The Output Routing Pool (ORP) allows for flexible interconnections between the GLBs and the I/O modules.

4.3.4.1 Lattice Semiconductor ispLSI 1000/E

The GLBs for the 1000/E contain 18 inputs, programmable AND/OR/XOR array and four outputs. The four outputs can be configured as combinatorial and registered. The difference in the 1000E is that it has two more global output enable pins and a programmable output slew rate control.

The Global Routing Pool (GRP) is the internal routing structure that connects the GLBs to the I/Os and the I/Os to the GLBs. The output of any GLB is available for input into any other GLB. The I/O pins are also available to interconnect to any GLB input. The ORP is the routing structure in the architecture that allows the GLBs to be connected to the I/Os. This allows flexibility when assigning I/O pins. A megablock consists of eight GLBs and 16 I/O cells. The 1000E has two dedicated input signals that are common to all GLBs and the product term OE which is common to all 16 I/Os. The densities in

the 1000/E family range form 16 GLBs to 48 GLBs. Figure 4.8 contains a functional block diagram of one of the ispLSI 1000 devices.

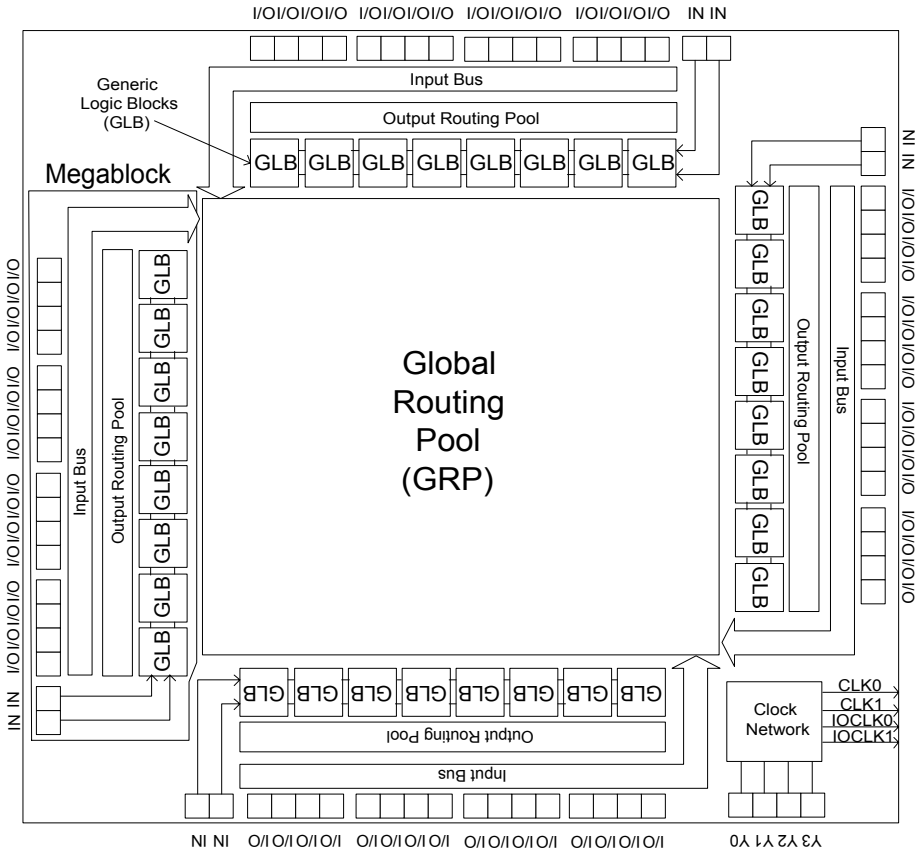

Figure4.8: isp LSI Functional Block Diagram

A GLB is divided into four sections. The four sections are the AND array, Product-Term-Sharing Array (PTSA), reconfigurable registers and the control functions. The AND array in the PTSA consists of 20 product terms that has 18 inputs available to produce a logic sum. 16 of the 18 inputs are from the GLP that can be connected to I/Os or any other GLB. The other two inputs are the dedicated inputs. The PTSA routes the 20 product terms to the 4 GLB outputs. The OR gates have four, five, or seven product term inputs to them. The OR gates can be routed to any GLB output. The PTSA allows

for product term sharing or combining. The reconfigurable registers are XOR gate inputs to D-type flip-flops. The XOR gate can be used as a logic element or to configure the register as a JK or T-type flip-flop. The registers can be bipassed if the design requires combinatorial logic and is brought out to the GRP. The I/O signals are routed to the GRP. The I/O cell is used to route input, output and bidirectional signals connected to the I/O. There are five global clocks for the devices. CLK0, CLK1 and CLK2 are for GLB clocking and IOCLK0 and IOCLK1 are for clocking the I/O cells.

4.3.4.2 Lattice Semiconductor ispLSI 2000/V

The ispLSI 2000 family has densities ranging from 32 macrocells up to 128 macrocells, which is equivalent to 1000 PLD gates and 6000 PLD gates respectively. The 2000V device is a low voltage version of the 2000 at 3.3 V. The global logic block (GLB) for the 2000 family is essentially the same as for the 1000 family. Figure 2.9 is the schematic of the generic logic block for the 2000 family. The general architecture has the following modifications and enhancements:

- GLB and clock multiplexer scheme is different on the 2000 series. There are three dedicated clocks CLK0, CLK1 and CLK2. These clocks are used to clock all the GLBs that are configured as registers. The clocks are used inside the GLBs and are selected by a multiplexor. The internal clock signals are connected to the I/O pins Y0 through Y2.
- The 2000/V family made a simplified I/O register. The I/O cell can be configured as an input, output and bidirectional with tri-state control. The I/O clocks were removed and the outputs can be configured as totem pole or open-drain.

- The Output Routing Pool (ORP) was enhanced for further routing capability. The 2000 series devices have two sets of ORPs per megablock allowing all 32 outputs of the GLBs to have access to the 32 I/O cells. This architecture doubles the routability of this family.

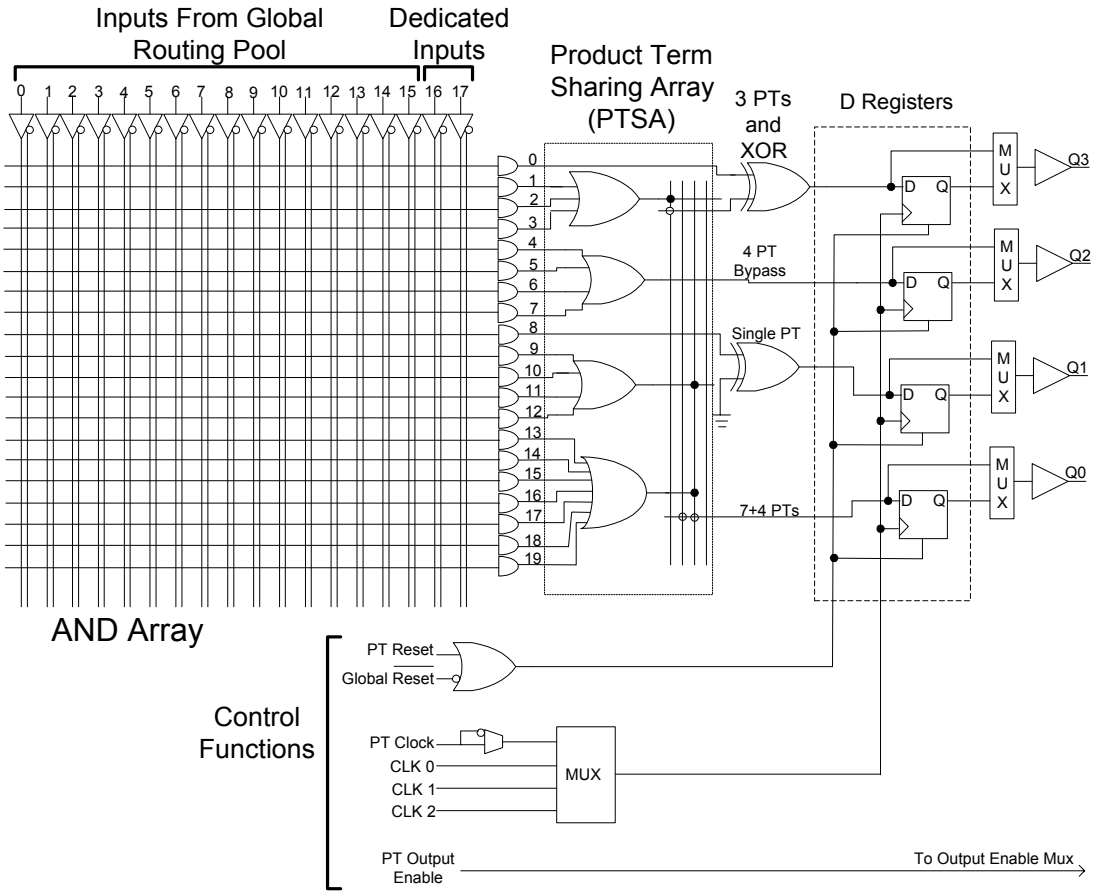

Figure 4.9 ispLSI 2000/V Generic Logic Block

4.3.4.3 Lattice Semiconductor ispLSI 3000/V

The ispLSI 3000 family of devices range from 7000 PLD gates / 192 macrocells to 14,000 PLD gates / 320 macrocells. The basic architecture of the device is similar to the 1000 series with the following exceptions:

- The generic logic blocks of the 3000 series devices are called twin GLBs. A twin GLB contains 24 inputs and 8 outputs. The GLB is divided into four sections and they are the AND array, PTSA, reconfigurable registers and the control section. The AND array consists of 20 PTSA's that can accept all 24 twin GLB inputs. The GLB inputs come from the I/Os or other GLBs. There are two sets of PTSAs in the twin generic logic block. There are 4 OR gates in the PTSA that have 4, 5 and 7 inputs from the AND array. The output of the four OR gates can be routed to any of the four outputs on the twin GLBs if more product terms are needed.
- A megablock in the 3000 devices consists of four twin GLBs with 24 inputs per twin GLB. There are no dedicated inputs. There are single-I/O devices and double-I/O devices. In the single-I/O structure, the 32 I/Os from the 4 twin GLBs get routed to only 16 I/Os through the ORP. There is only one I/O pin for every two GLBs. If your design contains many I/Os, this could cause a problem. The double-I/O structure allows for 32 I/O pins for all 32 GLB output pins. Figure 2.10 is the Lattice ispLSI 3000 family megablock layout for double-I/O devices.
- The global clock structure was changed form the 1000 family. There are now a total of 5 clocks that are networked to each GLB. Three clocks are for register clocking and the remaining two are for I/O clocking.
- The I/O cells are the same as the 1000/E families with the exception of the added boundary scan capability. There are added boundary scan registers that allow for JTAG IEEE 1149.1 on-chip test capability during the PCB testing. There are also added global OE pins for static testing.

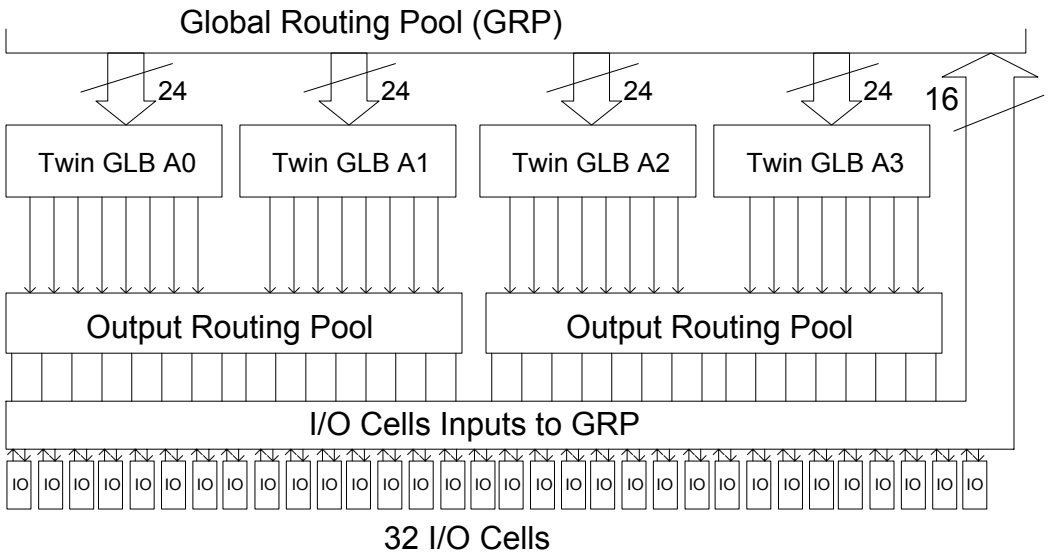

Figure 4.10 ispLSI 3000 Megablock Layout

4.3.4.4 Lattice Semiconductor ispLSI 6000

The ispLSI 6000 family of devices contains high-density cell-based programmable logic, dedicated memory module, a dedicated register / counter module and an 8000-gate area for general purpose logic. There are three devices in the family, which contain different types of memory modules. The ispLSI 6192FF contain FIFO, the ispLSI 6192SM contain single-port RAM and the ispLSI 6192DM contain duel port RAM. The basic architectural elements of the 6000 family are as follows:

- The twin Generic Logic Block (GLB) is the basic structure for the 6000 family. In the ispLSI 6192 there are 24 twin GLBs each containing 24 inputs, programmable AND, 2 OR / exclusive-OR arrays and 8 output blocks. The outputs can be configured as combinatorial or registered.
- The memory module can be configured as a dual-port FIFO, single-port RAM or dual-port RAM. The FIFO has dedicated input signals, its own control flags and can

be programmed as a 256 x 18 or a 512 x 9. The single-port RAM can be configured as a single 256 x 18 or 512 x 9 or two smaller 128 x 8 or 256 x 8 memories. The duel port can be configured as a 256 x 18 or 512 x 9 and can read and write concurrently.

- Eight 16-bit blocks can be configured as registers or shift registers. Four of them can be programmed as loadable up/down counters.
- The ispLSI 6000 devices also include boundary scan capability.

4.3.4.5 Lattice Semiconductor Summary

Lattice Semiconductor has recently introduced two new families into the high-density CPLD profile and they are the 5000 and 8000 family. Both these families have wider input capability into the GLBs and higher density of gates. The 8000 family has up to 45,000 PLD gates. The ispLSI 3320 70LM 208 was the device chosen for the design. It contains 320 macrocells, 14,000 PLD gates, 162 I/Os and supports a maximum frequency of 100 MHz. It allowed for high-density designs, flexible partitioning of the design and flexible development and debugging using the in-system programmable feature. This device was available in a 208-pin Metal Quad Flat Pack (MQFP), which made it ideal for prototyping the electronics without getting into Ball Grid Array (BGA) packaging issues. BGA Packaged devices have the I/O pins very close together and do not interface with standard Pin Grid Array (PGA) carriers. BGA are very small packages, ideal for Printed Circuit Board (PCB) applications.

4.4 Field Programmable Gate Arrays

4.4.1 Introduction

When considering an FPGA architecture, one must look at two main concerns; size / flexibility of the logic cell and the routing architecture. The logic cell can be as

simple as a transistor or as complex as a microprocessor. The logic blocks can be built from transistor pairs, small gates, multipelxers, look-up tables or wide fan-in AND-OR structures.

FPGA logic blocks differ in size and capabilities. Some FPGA vendors employ the sea-of-tiles architecture, which are small configurable units as logic cells and other vendors like Xilinx use the lookup table architecture which is relatively large. The logic cells can be defined by their granularity. Granularity is defined as the number of boolean functions, number of two-input NAND gates, total number of transistors or the number of I/Os. Granularity is broken down as follows:

1. Fine-Grain Logic Cells – Fine grain logic cells consist of a few transistors. The advantage of fine grain logic cells is it is easier and more efficient to implement complex designs in transistor level logic cells. The disadvantage, is that fine grain logic cells require a more complex and larger programmable interconnect structure increasing the size of the chip as well as internal chip delays.
2. Course-Grain Logic Cells – An example of a course-grain logic cell is the multiplexer architecture. The advantage of course-grain logic cells is that they can implement complex functions with very few transistors internal to the logic cell. The disadvantage it that a large number of inputs will be required for complex logic functions which stresses the influence of routing resources. Course-grain logic cells are associated with antifuse programming technology.

The routing architecture of an FPGA is the internal interconnection for the logic cells implementing a logic function. The interconnection resources consist of the connection block and the switch block. The connection block provides the interconnection between

the horizontal and vertical paths and the logic cells and the switch block provide the connections in the horizontal and vertical paths. The routing architecture affects density and performance of the FPGA. The routing architecture must meet two criteria: routability and speed. Routability is the ability of the FPGA to provide all the interconnections for a particular design. The speed of the FPGA is closely related to the propagation delay through the routing. This delay is 40% - 60% of the total delay. The programmable switch also introduces a RC delay to the total delay.

FPGAs are divided into three different architectural groups: (1) row-based (2) symmetrical and (3) fine-grain cellular. Row-based FPGAs are usually course-grain logic cells, organized in a row and divided horizontally by interconnect signals. The symmetrical architecture for FPGAs consists of rows and columns of large grain blocks called configurable logic blocks (CLBs) with horizontal and vertical routing channels. The fine-grain or cellular architecture can be described as the "sea-of-gates" approach in which the logic cells are very small or "fine". The next section will describe these in detail.

4.4.2 FPGA Architectural Groups

4.4.2.1 Row-based Architecture

Row-based FPGAs contain rows of logic cells that are separated by programmable interconnect structure or routing channels. Actel is a perfect example of a row-based FPGA. Figure 4.11 shows a very simple schematic for row-based FPGA architecture. Row-based FPGAs contain different lengths of wire segments that are connected together using antifuses.

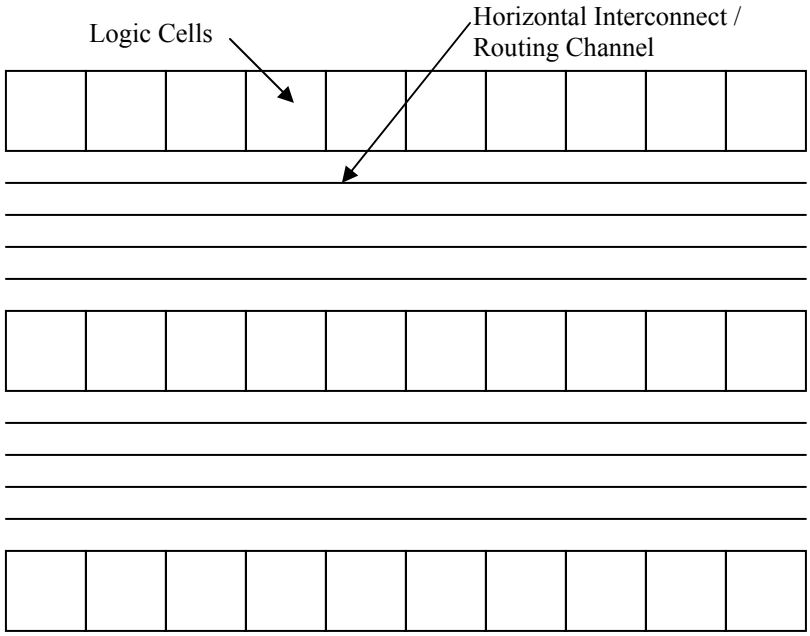

Figure 4.11 Schematic of Row-based FPGA

A critical design issue with respect to row-based FPGAs is having an accurate estimate of the number of tracks required to implement the design with respect to the number of tracks available in the chip. Typical designs could have tracks that run the length and the width of the chip consisting of many wire segments of varying length. Minimizing the number of fuses for any given net to increase the performance and timing characteristics is another critical issue with respect to row based FPGAs. There have been routability analysis and routing algorithms developed for the optimization of the routing channels in row-based FPGAs. The segmentation of the routing channels can be handled as unconstrained routing channel, fully segmented block channeling, non-segmented channeling, 1-segment channeling and 2-segment channeling. A detailed

description of each channel architecture will not be discussed but the results of the analysis are as follows:

- The wire segment length that connects the logic cells affects the performance of the design.
- It is critical to reduce the amount of switches or fuses to reduce the RC delay factor.
- It is important to understand the use of the routing design tools with respect to vendor devices. The tools take into account speed and performance as well as the area of routing channels available for specific chip architectures. It is important for user interaction to define critical nets to reduce the amount of tracks to meet performance requirements.

4.4.2.2 Symmetrical (SRAM-based) FPGA Architecture

Symmetrical or SRAM-based FPGAs contain memory cells as the logic blocks to implement the logic functions to create a design. There is no RAM area in the FPGA so it is distributed among the logic cells. SRAM FPGAs are built for density and stability and not necessarily for speed. The main disadvantage of SRAM-based is that they are volatile and need to be reprogrammed once power is reapplied. Xilinx is an excellent example of an SRAM-based FPGA with its architecture based on Logic Cell Arrays (LCAs) which contain functions as Look-Up Tables (LUTs). Figure 4.12 contains a simple schematic of an SRAM-based FPGA.

The RC delay introduced by each Programmable Interconnect Point (PIP) adds up over the routing path. The fewer PIPs used in SRAM based FPGAs will decrease the loading in the interconnect segments but reduce the routability. The more PIPs improve

routability but increase loading because with each PIP there is a memory cell that can increase the die size of the FPGA.

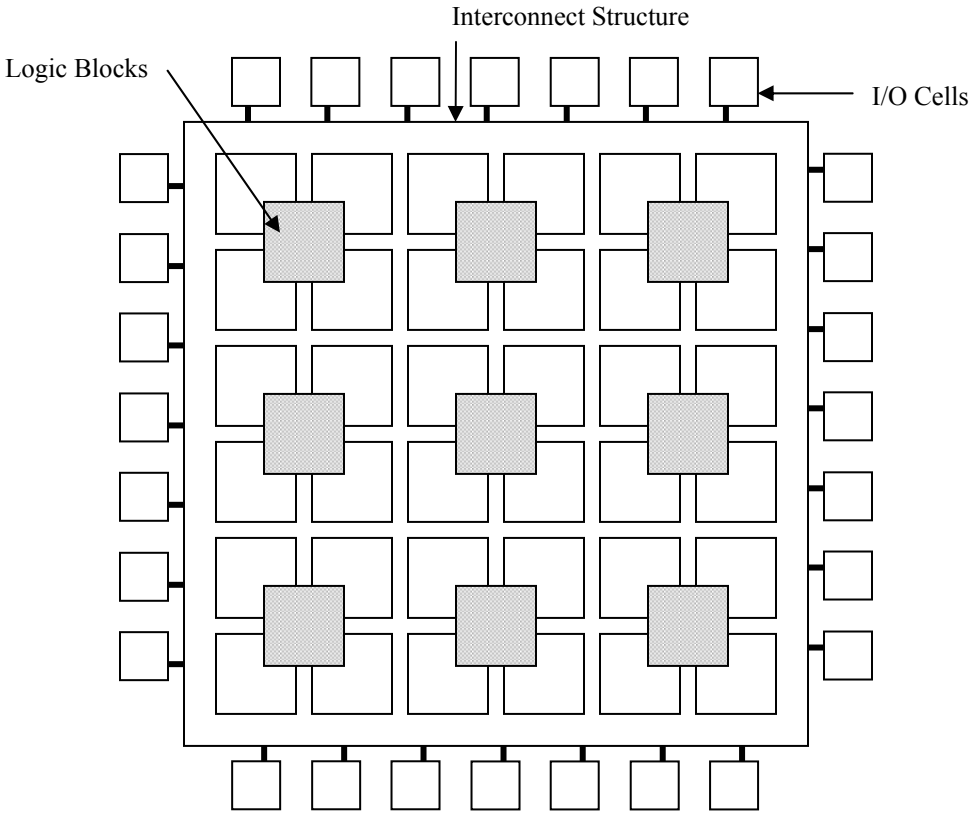

Figure 4.12 Schematic of Symmetrical / SRAM-based FPGA

SRAM-based FPGAs consist of three building blocks. The first is the memory cells that implement the logic function. The second is the Programmable Interconnect Point (PIP) and the third is the multiplexer controlled by the memory cell. The PIP is a pass transistor that is on or off depending upon the value in the memory cell. The pass transistor introduces a RC delay. The multiplexer is a uni-directional routing structure that can be as wide as necessary to implement the function.

In an FPGA architecture there are trade-offs between the size of the logic block and the speed and performance at which the design is implemented. Small logic blocks

have their advantage but may lead to slower performance due to the many interconnects that are required to implement a function. Large logic blocks may be able to handle complex designs while decreasing the amount of interconnects but have poor logic efficiency. The capacity and performance are dependent upon the architecture of the FPGA and the software tools that provide placement, routing and partitioning of the logic functions.

Recently FPGA vendors such as Actel, Altera and Xilinx have incorperated medium-size logic blocks of memory such as single-port or multi-port SRAMs, FIFOs and buffers. The imbedded memory allows designers to simplify designs and have the design operate faster with access time to the memory modules ranging from 5 to 20 ns. Xilinx used the LUT configuration in small blocks of RAM that is distributed throughout the chip where Altera and Actel used dedicated blocks of RAM within the FPGA.

4.4.2.3 Fine-grain (or cellular) FPGAs

Fine-grain FPGA structure consists of small logic cells in a compact structure for direct interconnect to perform local logic functions. Motorola Programmable Array (MPA) is a perfect example of the fine-grain architecture. The interconnect structure is hierarchical consisting of fast connections, medium interconnect and global interconnect. The local connections are very fast and join cells at the lowest level to form the macrocells that can be used to implement small functions like counters and comparators. The medium interconnect combines the macrocells together and the global interconnect is for the complete routing and chip layout.

The functionality of a cell is different for fine-grain FPGAs than course-grained channel-array devices. A basic cell is an AND / XOR function or an AND / D-type flip-

flop set. If this logic cell was to be used in a channel arrayed device, the cell would be very inefficient due to the routing resources. The hierarchical routing and the basic logic cells combined into macrocells make fine-grain devices very efficient with very low routing overhead. There are two advantages to using fine-grained FPGAs and they are as follows:

1. The logic cells are small enough to implement simple logic functions without having wasted resources. This reduces redundancy when implementing simple logic functions.
2. Since there are few critical paths through the cell, the cell can be optimized.

4.4.3 FPGA Programming Technologies

4.4.3.1 Antifuse

An antifuse is a two terminal device that when unprogrammed has a very high resistance between the two terminals and when programmed, or "blown", creates a very low resistance or permanent connection. The application of a high voltage from 11 V to 21 V will create the low resistive permanent connection. Antifuse technologies come in two types. The first is oxide-nitride-oxide (ONO) dielectric based and the other is amorphous silicon or metal-to-metal antifuse structures.

Dielectric based antifuses consist of a dielectric material between N+ diffusion and polysilicon which breaks down when a high voltage is applied. Early dielectrics were a single-layered oxide dielectric until Actel came out with the programmable low impedance circuit element (PLICE), which is a multi-layer oxide-nitride-oxide (ONO) dielectric fuse. A high voltage across the PLICE melts the dielectric and creates polycrystalline silicon between the terminals. When the PLICE is blown, it adds three

layers rather than the double metal CMOS process. The layers are a thin layer of oxide an top off the N+ surface, Low-pressure Chemical Vapor Deposition (LPCVD) nitride and the reoxidized top oxide. The programming current has an important effect because the higher the current during programming, the lower the link resistance, resulting in smaller thickness for the antifuse material. Programming circuits for antifuses need to supply high currents (15 ma for Actel) to insure high reliability and performance.

Amorphous silicon antifuse technology is the alternative to dielectric antifuse. It consists of amorphous silicon between two layers of metal that changes phases when current is applied. When the antifuse is not programmed the amorphous silicon has a resistance of 1 Gohm. When a high current (about 20 mA) is applied to the anitfuse the amorphous silicon changes into a conductive polysilicon link. QuickLogic pASIC FPGA is a perfect example of an amorphous silicon antifuse technology.

4.4.3.2 SRAM-based

SRAM FPGA architecture was discussed in section 4.4.2.2 and consists of static RAM cells to control pass gates or multiplexers. The FPGA speed is determined by the delay introduced by the logic cells and the routing channels. Multiplexers, look-up tables and output drivers affect the speed of signals through the logic cells. An FPGA with more PIPs is easier to route but introducing more routing delay. The size of the look-up table plays an important role depending on the design. Smaller LUTs provide higher density but larger ones are preferred for high-speed applications.

4.4.3.3 SRAM vs. Antifuse

The following is a list of advantages and disadvantages for the two technologies:

1. Antifuse programming technology is faster than SRAM programming technology due to the RC delays introduced by the interconnect structure.
2. Antifuse technology has more silicon area per gate and is easier to route than SRAM technology.
3. A disadvantage of antifuse FPGA is that they require more process layers and mask steps and also contain high voltage programming transistors.
4. SRAM-based technology contains higher capacity than antifuse technologies.
5. SRAM based technology is very flexible with in-system programmability and the ability to reconfigure the design during the debugging stage while antifuse technology is one-time programmable (OTP). This ability reduces design and development, which reduces overall cost of the design. Another advantage to this is that SRAM technology can be programmed at the factory through complete verification test where the antifuse are tested as "blanks" and require programming by the user to verify design requirements and operation.
6. A disadvantage of SRAM technology is that it is volatile meaning it has to be reprogrammed every time power is turned off and on again. The SRAM usually require an extra memory element to program the chip which occupies board space

4.5 Programmable Logic devices for Space Applications

4.5.1 Introduction

Over the years programmable logic devices have been used more and more in space and military applications because of there design flexibility, chip density for large complex designs, chip cost and fast turn-around times. ASICs and gate arrays have been used in the past and are still being used due to high performance and greater radiation

tolerances but they have high nonrecurring engineering (NRE) costs and they have longer turn-around times for engineering model and flight units.

4.5.2 Space Environment

The space environment has radiation risks that affect electronic components and devices as well as programmable logic devices on earth orbiting spacecraft missions and deep space missions. The space environment consists of radiating particles like high-energy electrons, protons, alpha particles and cosmic rays. These irradiating particles in the space environment, can cause problems and latch-ups in the electronic circuits. Electronic components in space are not affected by high doses of radiation but over a period of many years, depending on the mission, electronic system can accumulate a significant amount.

Ionization is high energy creating electron-hole (h-e) pairs when passing through a material. Ionization is the dominant effect of charged particles in space. Radiation can break atomic bonds by displacing the crystal lattice structure in a material and cause trapping recombination centers. Both of these can lead to problems in the performance of the device.

The electromagnetic radiation types that cause ionization are X rays and gamma rays. Gamma rays affect the electronic component by the charge interacting with the material. Ionizing particulate radiation can be in the form of uncharged particles, light charged particles and heavy charged particles. Neutrons are uncharged particles. Uncharged particles like neutrons cause crystal lattice damage. Electrons, protons, alpha particles and beta particles are charged particles. Lightly charged particles interact with the material of the device just as gamma rays. Iron, bromine, krypton, and Xenon are

examples of heavy charged particles. Heavy charged particles are in cosmic rays. The sun and galactic sources cause cosmic rays. Heavy charged particles create "volume ionization" within the substrate of the electronic component. The charge form heavy charged particles in cosmic rays collect on circuit nodes and causes problems in data loss through single-event upsets (SEUs) and transient upsets. Table 4.2 lists radiation types and the related failures. Radiation damage caused by charged particles form space environments can be broken down into total ionizing dose (TID) and single-event phenomenon (SEP) or single-event effect.

4.5.3 Radiation Damage

4.5.3.1 Total Ionizing Dose (TID)

Bipolar technology devices are not as sensitive with respect to total ionizing dose effects as MOS technology devices. Major radiation damage is caused by charged particles built up in passive oxides surrounding silicon surfaces. Bipolar technology depends on transistor junction for operation where MOS technology depends on surface and interface signals.

PLD designers prefer MOS technology because of low noise and power. It is sensitive to total ionizing dose effects. Trapped charge in the oxide layer of the CMOS device is the radiation damage related to ionization effects. The silicon dioxide (SiO2) is the most sensitive to ionizing radiation. As the radiation passes through the silicon dioxide, it creates electron-hole pairs. The field in the silicon oxide allows the electrons-holes to drift apart. The electrons drift out of the oxide and are collected by the gate electrode. Some of the holes form oxide traps and others form interface traps. Oxide traps stay where they were generated having a positive charge and the interface traps are

energy levels in the SiO2/Si interface. Interface traps reduces the conductance of the channel of the MOS transistor. The oxide traps and interface traps accumulate over time. The total ionizing dose received by a programmable logic device is expressed in rads (Si) or rads (siO2) as follows:

1 rad (Si) = 100 ergs absorbed / gram of Si

As a reference, Table 4.3 shows various levels of radiation expressed in rad (Si) for specific application requiring qualified parts.

Type of Radiation	Type of Degradation Failure	
	Transistor Level	**Circuit Level**
Photons (X rays and gamma rays		
Total Dose (Low dose rate) (High total dose)	Threshold voltage shifts	Performance degradation
	Drive current shifts	I/O parametric shift
	Carrier mobility reduction	Lost functionality
	Parasitic leakage current	Data upset/loss
Transient (High dose rate) (Low total dose)	Collapse of depletion region	Latchup
	Burn-out of metal interconnects	Catastrophic failure
	Damage to junction region	I/O glitches
		High photocurrents
Charged particles and cosmic rays		
Electrons and Protons	Threshold voltage shifts	Performance degradation or improvement
	Drive current shifts	I/O parametric shifts
	Carrier mobility reduction	Lost functionality
	Parasitic leakage current	Data upset (single bit/node, protons only)
	Carrier recombination and trapping	
	Collapse of depletion region (photons only)	
Alpha particles	Collapse of depletion region	Data upset (single bit/node, protons only)
Heavy ions	Collapse of depletion region	Data upset (single or multibit/node)
		Hard oxide failures
		Latchup
Uncharged particles		
Neutrons	Junction leakage	No performance effects on CMOS
	Bipolar beta reduction	Improves latchup tolerance on CMOS circuits
	Carrier recombination and trapping	Performance degradation on bipolar circuits

Table 4.2 Types of Radiation and Related Failures

Total Dose, rads (Si)	100	1K	10K	100K	1M
Nuclear Explosion			xxxxxxxxx	xxxxxxxxx	xxxxxxxxx
Spacecraft		x	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx
Satellite		xxx	xxxxxxxxx	xxxxxxxxx	
Aircraft	xxxxxxxxx	xxxx			
Ground-based Systems	xxxxxxxxx	xx			
Human Exposure Consequence	Serious illness	Usually fatal			

Note: The "x's" in the table indicate a range within the total dose columns.

Table 4.3 Ranges of Total Dose Exposures for Various Environments

4.5.3.2 Single-event Phenomenon

Single-event phenomenon (SEP) refers to the effect of high-energy particles hitting the sensitive nodes in the electronic component. They can be in three forms and they are single-event upset (SEU), single-event latch-up (SEL) and transient radiation effects.

1. Single-event upset (SEU) is the affect of charged particles causing logic change in flip-flops and RAM configuration bits in programmable logic devices. An SEU is called a soft error because the charged particles collect on a sensitive bit node in a memory element cause it to change logic level. An SEU is temporary and will regain operation upon system reset.
2. Single-event latch-ups (SEL) are called hard errors because when they happen the device can not recover from them. They are either low impedance states or avalanching in the drain junction of MOS transistors in CMOS devices. The hard errors are caused by single charged particles that induce photocurrent that can be at high levels causing burnout in the junction of the transistor.

3. Transient Radiation effect deals with the rate of the ionizing dose rather than the total ionizing dose effect. A higher rate of ionizing radiation causes a greater number of e-h pairs to be caught in the insulating layer and silicon. Transient upset is caused by a burst of ionizing radiation rather than from one charged particle.

As there is an increase in the charged particles from ionizing radiation, there is a loss of energy. This loss of energy is a result of the amount of energy mass and the amount of charge from the ionizing particles. The Linear Energy Transfer (LET) is the rate of energy from the charged particles (dE/dX) and is measured in units of MeV/[cm^2/mg] or MeV/um. The lower the LET the more chance the device will have a SEU or SEL. Proton belts have energies above 30 MeV, which is the minimum energy that can penetrate a spacecraft. 8 MeV is the minimum level for proton induced upsets. LET is found experimentally by testing the device under ionizing radiation. The LET is directly related to the specific design or the technology used. The critical charge (Qc) is the minimum charge necessary to cause a single-event phenomenon and can be simulated in a design.

Earth orbiting satellites operate in low earth orbit or geosynchronous orbit, which are 150 to 600 km and 35,880 km respectively. The magnetosphere, which is 6,380 km contains the highest radiation around the earth. The magnetosphere contains heavy charged particles and gets hit by heavy ions from solar and galactic cosmic rays. The interplanetary spacecraft encounter heavy charged particles form other planet's magnetospheres and heavy ions from cosmic rays.

Electronic designs using PLD for space applications have to be concerned about the following items:

- Protons and electrons trapped in Van Allen radiation belts

  The Van Allen radiation belts are two concentric donut-shaped clouds that store and trap charged particles form solar wind. They are aligned with the magnetic axis of the earth. Satellites and spacecraft passing through this region are bombarded with protons and electrons. They are 200 km to 1200 km from the earth's surface.
- Heavy ions in the magnetosphere
- Cosmic ray protons and heavy ions
- Protons and heavy ions form solar flares

Altitudes of about 1 to 12 Earth radii (where Re = 6380 km) contain electrons with energy levels of about 7 MeV. Protons from the solar and galactic rays have energy levels ranging from 1 Mev to 800 MeV. The actual radiation experienced by a spacecraft depends on the orbit, mission launch time and duration of the mission. A second source of radiation is the charged particles found in radiation belts. Besides the energy from the radiation belts there is sets of radiation from solar flares and cosmic rays. The charged particles from solar flares can last from a few hours to several days. Solar flares contain protons, electrons, alpha particles and heavy ions. Cosmic rays have energy ranging from a few million electron volts to 10 GeV and are composed of mostly protons, some alpha particles and heavy ions. There is a geomagnetic field around the equator that shields spacecraft from charged particles when orbiting at low altitudes and low inclination. The U.S. space station is in that type of orbit. The higher the altitude and larger the inclination the more solar flares and cosmic rays. If the inclination of the orbit reaches the polar area of the earth there is no protection form solar flares or cosmic rays. The highly elliptical orbits (HEO) of spacecraft have an altitude of 30,000 km and pass through the Van Allen

belt and get hit with constant cosmic rays and solar flares. Spacecraft in geostationary orbits (GEOs) are exposed constantly to cosmic rays and solar flares. The total radiation effecting the electronic components is not only a factor of radiation but also a factor of the shielding of the electronics.

4.5.4 Radiation hard / Radiation Tolerant

An electronic component has to go through many test to determine it if can withstand specific radiation levels. A Radiation Hard (RadHard) device is designed to withstand levels of radiation that include and exceed 300 Krad. A device that is radiation tolerant has not been designed or tested for radiation hardness but to some level of radiation resistance. The hardness levels of a device that is radiation tolerant may not be guaranteed and the process is less expensive indicating there may be important parameters such as oxide thickness not properly monitored, specified or tested.

4.5.5 Radiation Hardness Assurance (RHA) Testing

In unhardened programmable logic devices the performance characteristics and fabrication process vary form lot to lot within vendor parts. Radiation response of programmable logic devices depends on technology, fabrication process and design to be implemented. Radiation testing is required on devices to verify that they are going to meet the mission requirements. Radiation testing done on earth is very difficult to perform because it is hard to predict the space environment, which depends on particle types, energies and time of the mission.

The best way to test radiation hardness of semiconductor devices is to perform the tests in space. This approach is very costly and is limited to technology demonstrations

and research type satellites. The only way to test programmable logic devices is through ground based testing. The objectives of ground based testing are as follows:

- Determine how the radiation effects a particular device and device material and what failure rate.
- Determine the response of the device from radiation effects based on technology and the type of device.
- Evaluate the performance of the device and verify if it has met mission requirements.

The radiation sources used for the testing are radioactive isotopes such as Co-60, X-ray tubes and particle accelerators. Radiation tests are required to be performed at worst case temperatures because it greatly affects the overall performance of the device. Ground based radiation testing is done to check total dose effects, SEU and SEL, transient response and neutrons.

4.5.6 Radiation Hard and Radiation Tolerant Devices

4.5.6.1 Actel

4.5.6.1.1 General Architecture

Actel has had the leading edge for RadHard and RadTolerant devices. The ACT 1, ACT 2, ACT 3 and SX architectures are available in RadHard or RadTolerant devices. The logic block architecture, the routing resources, the I/O structure and the radiation specifications will be discussed in the following sections.

4.5.6.1.1.1 ACT 1

ACT 1 architecture was the first done by Actel with a silicon structure and oxide barrier. The ACT 1 devices consist of rows of logic blocks with 22 tracks of horizontal routing separating the rows. The tracks are broken into segments that can be connected

together to have short wire segments or long wire segments. Short segments can be connected by an antifuse to make long segments and there are programmable interconnects between the horizontal and vertical tracks. The logic module in an ACT 1 device has 8 inputs and 1 output and can be configured into basic logic functions i.e. AND gates and NOR gates or more complex logic functions, such as, latches and multiplexors. ACT 1 contains a clocking network distributed throughout the chip to a large number of flip-flops. Each logic module connects to horizontal tracks by vertical connections to implement the functions for each logic module. The I/O ports can be configured as input, output and bidirectional and would have to be sent through a logic cell to get it registered. Figure 4.13 shows the ACT 1 logic block.

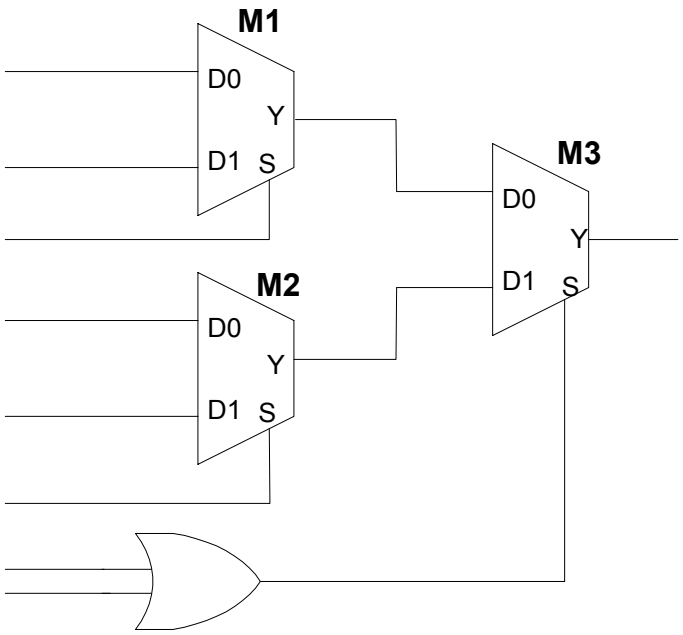

Figure 4.13 ACT 1 Logic Block, 8 Input and 1 Output

4.5.6.1.1.2 ACT 2

ACT 2 FPGAs have two types of logic blocks. The two tyes are C-module for combinatorial and S-module for sequential logic. The ACT 2 logic block consists of a 4 input multiplexor. This allows for wider fan in on logic functions. ACT 2 C-module is shown in Figure 2.14. An S-module is a C-module driving a flip-flop with an additional gate, which is the reset to the flip-flop. The row architecture consists of two C-modules adjacent to two S-modules and so on. Act 2 devices also contain horizontal routing channels that have segments that can be connected together by fuses. Vertical segments on inputs and outputs connect the logic block to the horizontal channels using antifuses. The input vertical segments on a logic module can be connected to the horizontal channel above or below the logic module. The output vertical segments can span two rows each direction. There are I/O modules at the end of each row and at the top and bottom of the device. The I/O modules at he end of the row can accept I/O form the rows above and below the module. The top and bottom I/O have a single source. ACT 2 supports tow dedicated clock inputs or two internal clock inputs that are distributed down each horizontal channel. ACT 2 has an improved internal layout allowing more routing capability. For this reason the ACT family range in speeds form 65 to 130 MHz.

4.5.6.1.1.3 ACT 3

ACT 3 devices contain the same C and S modules as the ACT 2 devices. The interconnection structure is the same as the ACT 2 devices except for additional vertical track per pair of C and S modules. The I/O modules were enhanced. The I/O module contains built-in flip-flops, dedicated clock and reset signals. Registered I/Os can be fed back to the internal logic as used as registers for the design. ACT 3 contains a general

clock network and a high-speed hard-wired clock network (HCLK). This allows for better speed performance with devices up to 150MHz clock frequencies with very low skews.

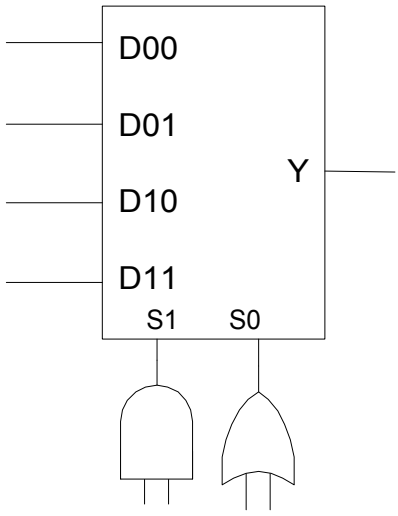

Figure 4.14 ACT 2 C-Module

4.5.6.1.1.4 Actel SX

The Actel SX is known for its "sea-of-modules" architecture instead of the row-based architecture. The grid of logic modules allows for very little chip area lost to routing resources. The SX family has two types of logic modules, the C-module and the R-module. The R-module or the register module contains a flip-flop with more control than previous Actel devices and architectures. It includes an asynchronous clear and preset with clock enable lines. The R-module allows for programmable clock polarity on a module by module basis. The clock for the R-module can be the hard-wired clock or the routed clock. The C-module, or the combinatorial module, can be configured as a wide range of logic function up to five inputs. The DB input and its inverter allow more

combinatorial logic functions than earlier Actel architectures increasing the options form 800 to 4000 logic functions. The Actel module organization in the SX devices is broken into clusters. There are two types of clusters. A type-1 cluster contains two C-modules and one R-module and the type-2 contains two R-modules and one C-module. The clusters are grouped into two types of superclusters. Figure 4.15 identifies the C and S-modules and the supercluster configuration. Supercluster-1 contains two sets of type-1 clusters and supercluster-2 contains one type-1 and one type-2 cluster. SX devices contain more supercluster-2 because most designs are more combinatorial in nature than register intensive. Actel has provided flexible routing resources in the SX architecture that reduces on the number of antifuses, which improves performance and allows them to be fast and predictable. There are local routing resources called "FastConnect" and "DirectConnect". DirectConnect is the hard-wired routing resources between the C-module and the R-module within the clusters. FastConnect is one programmable connection between the logic modules within and cluster. Global routing is throughout the chip providing interconnection within the superclusters and to the I/O pins. There are three clocks in the SX chip and they are HCLK, CLKA and CLKB. CLKA and CLKB are global clocks for internal logic and HCLK is a hard-wired clocking network for the R-module.

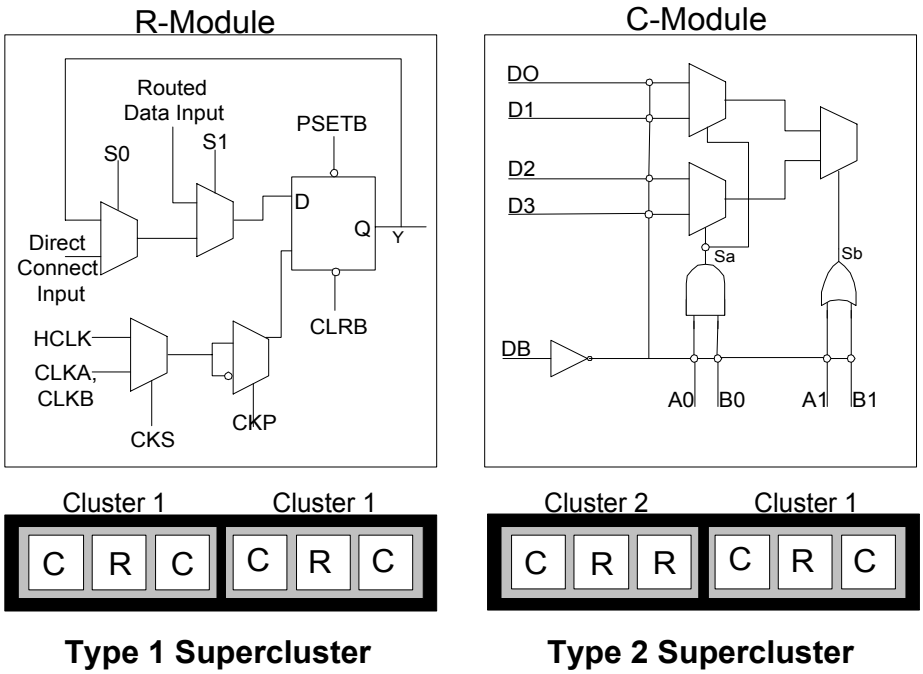

Figure 4.15 SX Module and Supercluster Architecture

4.5.6.1.2 Radiation Hard Actel Devices

4.5.6.1.2.1 RH1020 and RH1280

RH1020 and RH1280 have densities of 2,000 and 8,000 gates respectively and are the ACT 1 architecture with 50 MHz on-chip performance. They are processed in 0.8 micron, tow-level metal bulk CMOS technology. They have row-based architecture and Actel's PLICE antifuse technology. These devices are the only RadHard high density field programmable gate arrays on the market today with a total dose hardness of 300K rad(Si), latch-up immunity and a single-event upset tested at less than $1x10^{-6}$ errors/bit-day. Lockheed Martin Federal Systems in Manassas, Virginia has full Qualified Manufacturers List (QML) certification on these devices. QML indicates that the performance and quality of the device is built into the device rather than tested at the end. With the accumulated total dose effect at 300k rad (Si), these are ideal devices for deep

space spacecraft. They are ideal for high dose rate survivability from solar flares in earth orbiting applications. Table 4.4 and Table 4.5 shows the profile of the devices and the radiation specifications.

Device		RH1020	RH1280
Capacity	Gate Array Equivalent Gates	2,000	8,000
	PLD Equivalent Gates	6,000	20,000
	TTL Equivalent Packages	50	200
	20-Pin PAL Equivalent Packages	20	80
Logic Modules Flip-Flops	Total Logic Modules	547	1,232
	C-Modules	547	608
	S-Modules	0	624
	Maximum Flip-Flops	273	998
Routing Resources And I/O	Horizontal Tracks/Channel	22	35
	Vertical Tracks/Channel	13	15
	PLICE Antifuse Elements	186,000	750,000
	User I/O's	69	140

Table 4.4 RH1020 and RH1280 Device Profiles

Symbol	Characteristics	Conditions	Min.	Max.	Units
RTD	Total Dose			300K	Rad (Si)
SEL	Single Event Latch-Up	55°C≤T≤125°C		0	Fails/Device-Day
SEU1	Single Event Upset for S-modules	55°C≤T≤125°C		1E-6	Upsets/Bit-Day
SEU2	Single Event Upset for C-modules	55°C≤T≤125°C		1E-7	Upsets/Bit-Day
SEU3	Single Event Fuse Rupture	55°C≤T≤125°C		<1	FIT
RNF	Neutron Fluence		>1E+12		N/cm^2

Table 4.5 RH1020 and RH1280 Radiation Specifications

4.5.6.1.2.2 RAD-PAK

RAD-PAK® is a packaging technology from Space Electronics Inc. (SEI) that shield electronic components form total ionizing dose (TID) effects. This approach can be used on non-radiation hardened devices used in applications that require hardened devices. The RAD-PAK technology uses tungsten layer in the package lid to shield form electrons. High atomic number materials are useful in scattering electrons. The RAD-PAK technology is used on Actel A1020 and A1280 devices and flown on some NASA flight missions. RAD-PAK technology does not provide shielding form high-energy protons or heavy ions that cause SEU's and latch-up. The RAD-PAK technology used on Actel RP1280 and RP14100 introduce a higher density FPGA using ACT 1 and 2 architectures. This packaging technology eliminates the need for board and electronic assembly level shielding. The RAD-PAK devices can be used in a wide subset of earth orbiting and deep space missions. Table 4.6 shows the device profiles for Actel's Rad tolerant FPGA's with RAD-PAK packaging technology.

Device		**RH1020**	**RH1280**
Capacity	Gate Array Equivalent Gates	16,000	20,000
	PLD Equivalent Gates	8,000	10,000
	TTL Equivalent Packages	200	250
	20-Pin PAL Equivalent Packages	80	100
Logic Modules	Total Logic Modules	1,232	1,377
	C-Modules	608	680
	S-Modules	624	697
System Speed	Max. System Speed	40 MHz	60 MHz
I/O's	User I/O's	140	228

Table 4.6 Actel's RAD-PAK Devices

4.5.6.1.2.3 RadTolerant Devices

Actel has a wide range of devices that are RadTolerant. A device that is radiation tolerant has not been designed or tested for radiation hardness but to some level of radiation resistance. RadTolerant devices are available in ACT 1,2,3 and SX architecture. Radiation survivability for total dose results is summarized in two ways. The first is the amount of total dose that is reached when the device fails to meet the specification but still functions. The second is the total dose that is reached prior to failure. The ability for the RadTolerant devices to survive radiation effect is dependent upon the device and the lot. The 54SX family of devices have shown results form 60 – 100 Krad (Si) for not meeting the specification but still functioning and up to 240 Krad (Si) for functional failure. Table 4.7 contains the 54SX Actel RadTolerant device profile and Table 4.8 contains the radiation specifications.

Device	**RT54SX16**	**RT54SX32**
Gate Capacity	16,000	32,000
Logic Modules	1,452	2,880
Register Cells	528	1,080
Combinatorial Cells	924	1,800
Maximum User I/O's	177	224

Table 4.7 54SX Device Profile

Device	**Tech.**	**Bias Voltage**	**Tolerance Rad(Si)**	**Functional Rad(Si)**	**SEU LET_{th} $MeVcm^2/mg$**	**Latch-up LET_{th}**
RT54SX16 REV 0	0.6um	3.3/5.0	50-80K	>240K	17	>80
RT54SX16 REV 1	0.6um	3.3/5.0	100K		11	>82
RH54SX16	0.6um	3.3/5.0	>200K		19	>80

Table 4.8 54SX Radiation Specification

ACT 1, 2 and 3 RadTolerant devices have the capability of reach gate capacities of 20,000, on-chip frequencies of 85 MHz and up to 228 User I/O's. The RT1020 devices have results up to 100 Krads (Si) for ICC and >100 Krad (Si) for functional failure. The ACT 2 devices have results up to 10 Krad for ICC and 18 Krad for functional failure. The ACT 3 devices have typical results up to 28 Krad for ICC and 77 Krad for functional failure. Table 4.9 contains Actel's ACT 1, 2 and 3 RadTolerant device profile and Table 4.10 contains the radiation specifications.

Device		**RT1020**	**RT1280A**	**RT1425A**	**RT1460A**	**RT14100A**
Capacity	Gate Array Equivalent Gates	2,000	8,000	2,500	6,000	10,000
	PLD Equivalent Gates	5,000	20,000	6,250	15,000	25,000
	TTL Equivalent Packages	50	200	60	250	250
	20-Pin PAL Equivalent Packages	20	80	25	60	100
Logic Modules	Total Logic Modules	547	1,232	310	848	1,377
	C-Modules	547	608	150	416	680
	S-Modules	N/A	624	160	432	697
Tech.	Actel Technology	ACT 1	ACT 2	ACT 3	ACT 3	ACT 3
System Speed	Max. System Speed	20 MHz	40 MHz	60 MHz	60 MHz	60 MHz
I/O's	User I/O's	69	140	100	168	228

Table 4.9 ACT 1, 2 and 3 RadTolerant Device Profile

Device	**Tech.**	**Bias Voltage**	**Tolerance Rad(Si) Max.**	**Functional Rad(Si) Max.**	**SEU Max. LET_{th} $MeVcm^2/mg$**	**Latch-up LET_{th}**
RT1020	1.2um	5.0	>100K	>100K	25	>125
RT1280A	1.0um	5.0	5-10K	18K	26	>120
RT1425A	0.8um	5.0	20K	40K		
RT1460A	0.8um	5.0	28K	54-77K	32	>120
RT14100A	0.8um	5.0	20K	>50K	30	>120

Table 4.10 ACT 1, 2 and 3 Radiation Specification

4.5.6.2 Xilinx

4.5.6.2.1 General Architecture

As mentioned earlier, the first FPGAs introduced by Xilinx was in 1985 with the XC2000 family. Now there are four families of devices, which are the XC2000, XC3000, XC4000 and XC5000. The configurable logic blocks (CLBs), the I/O blocks and the routing resources of the XC4000 family will be discussed in this section. The XC4000 is a very flexible family of devices and has recently introduced the XQR4000XL radiation hardened FPGA for space and satellite applications. In general, Xilinx FPGAs are a relatively course-grained structure that contains logic cells form 64 to 1024 corresponding to gate ranges from 6,000 to 25,000.

4.5.6.2.2 XC4000 Family

The Xilinx logic cell arrays (LCAs) are called configurable logic blocks (CLBs). The CLB for the XC4000 family is more complex than the earlier families and are course in structure than the Actel devices. The CLB consists of two four input logic blocks that feed into a third logic block with a ninth input. A simple logic function or a combined function can be derived form the two combinatorial outputs driven by the logic blocks. The combinatorial outputs can feed the two flip-flops or they can be fed by an independent set of signals. There are four outputs from the CLB, two are from the flip-flops and two are from the combinatorial logic. Each flip-flop has a common control line, programmable set and reset common enable, individual override and common clock. The CLB architecture is ideal for fast arithmetic operations. For example each block can be configured as a two-bit adder with fast carry. The excellent carry network can be used as counters. 8 CLBs can be used to design a 16-bit up / down counter. The two large

function blocks inside a single CLB can be configured as a 32-bit RAM. The propagation delay and the access time are about 5.5 ns. Figure 4.16 shows a block diagram of the Xilinx XC4000 configurable logic block.

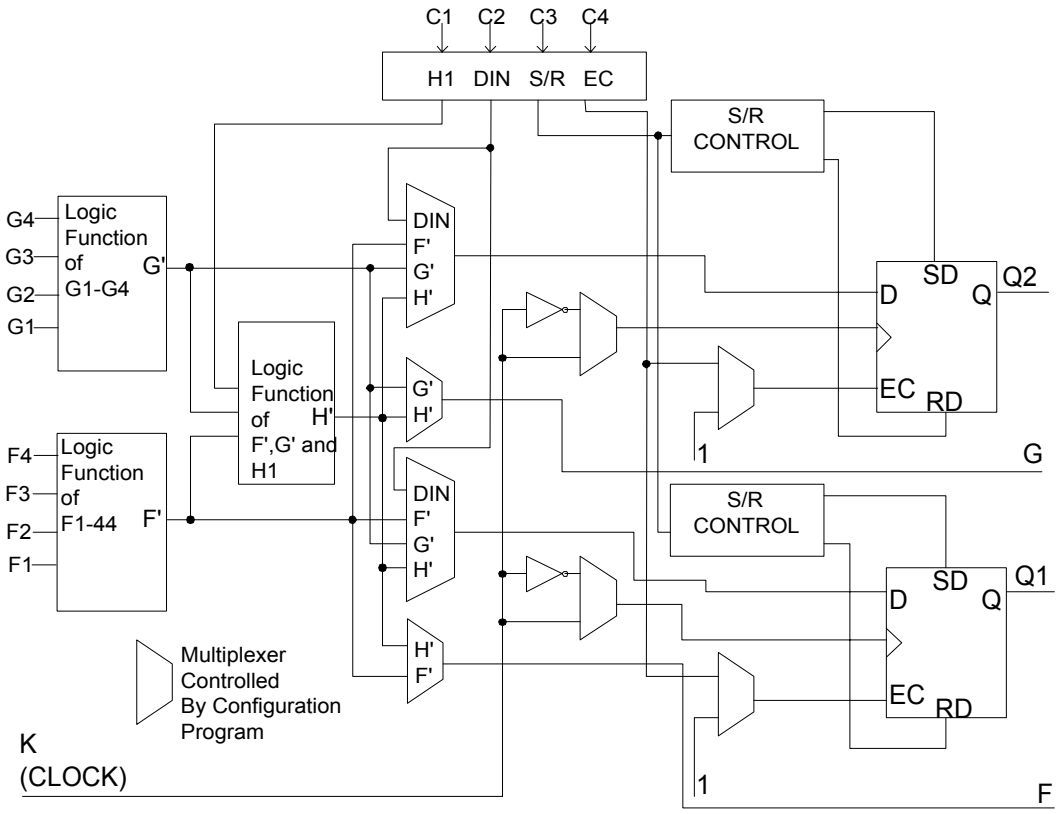

Figure 4.16 Xilinx XC4000 Configurable Logic Block (CLB)

The I/O blocks offer CMOS/TTL threshold selection, three-state control, slew rate controls and pull-up and pull-down resistors. The XC4000 device has flip-flop / latches for the I/O signals. The XC4000 family has a Wide Edge Decoder on the periphery of the chip. Depending on the specific device they range from 42 to 72 inputs and can be broken up into more narrow decoders. The advantage of this is to provide wide logic

functions just as the CPLDs. For example, it may take three to four levels of logic to decode a bus instead of just one using the wide decoder architecture.

The cell interconnect structure of Xilinx devices are short and long vertical and horizontal lines. The short lines make the interconnections between the switch matrices, the CLBs and the long lines. The long lines carry signals throughout the devices with high fan-out and low skew. The XC4000 cell interconnect structure contains symmetrical placement of the CLB I/Os, double length lines and a flexible simple switch matrix. There are three types of interconnects and they are single-length lines, double-length lines and long lines. The single length lines are the horizontal and vertical lines that intersect at each switch matrix. There are programmable n-channel pass transistors that connect the single-length lines in the switch matrix. The double-length lines are metal segments that are twice the size of single-length lines and pass two CLBs before they meet at a switch matrix. The long lines are metal interconnects that run the entire width of the device. They are connected to the single-length lines via programmable interconnect points. Long lines are used for high fan-out, low skew and time critical nets. The XC4000 family can reach frequencies of 60 to 70 MHz because of the flexible routing resources.

4.5.6.2.3 Radiation Hardened XC4000

Xilinx Corperation with Ericsson Saab Avionics conducted the first neutron radiation tests on the XC4000-series devices for applications in an atmospheric radiation environment. The test concluded, that SRAM FPGAs can be used in atmospheric radiation environment with results of one bit-error per 275,000 hours of operation at a 1000 km altitude at 60 degrees. Xilinx then proceeded to aim for demands for low earth

orbiting devices. The fabrication process was modified for the XQR series with 7 micron epitaxial layer and implant layers to meet the CMOS threshold levels and performance. The internal architecture and logic cells were not changed. Xilinx now offers radiation hardened devices with gate capacities of 62,000. The Devices can handle a total dose of 60K rad (Si) and are immune to latchup at 100 MeV. They have incorporated two methods to detect soft errors and hard errors caused by a single-event upset. These are the ability to readback all the configuration data and provide triple redundancy error detection. The readback function provides read-out capability of all the configuration data while allowing the device to normally operate. The triple redundancy method requires three FPGAs to detect an error, which will result in all the devices being configured form the original source or the faulty device to be configured via readback from the others. Table 4.11 and 4.12 contain the Xilinx radiation hardened device profile and the radiation specifications respectively.

Device	Logic Cells	Max. Logic gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)	CLB Matrix	Total CLBs	# of F-F	User I/O
XQR4013XL	1,368	13,000	18,432	10,000-30,000	24x24	576	1,536	192
XQR4036XL	3,078	36,000	41,472	22,000-65,000	36x36	1,296	3,168	288
XQR4062XL	5,472	62,000	73,728	40,000-130,000	48x48	2,304	5,376	384

Table 4.11 Xilinx XC4000 Radiation Hardened Devices

Symbol	Description	Max.	Units
TID	Total Ionizing Dose	60K	Rad (Si)
SEL	Single Event Latch-up >100MeV cm^2/mg +125°C	0	
SEU	Single Event Upset Galactic p+ 68km LEO	2.43E-8	
SEU	Single Event Upset Galactic Heavy Ion 68km LEO	9.54E-8	
SEU	Single Event Upset Trapped p+ 68km LEO	2.50E-7	
SEU	Single Event Upset Galactic p+ 35,000km GEO	5.62E-8	
SEU	Single Event Upset Galactic Heavy Ion 35,000km GEO	2.43E-7	

Table 4.12 Xilinx XC4000 Radiation Specification

4.6 Intellectual Property Cores for System-on-a-chip Applications

4.6.1 Intellectual Property Cores Introduction

Intellectual property (IP) cores are predesigned and preverifed logic functions for ASIC and PLD-based designs. IP cores were originally provided to designers by third party suppliers for ASIC system design and are now available for PLDs. PLD densities have increased rapidly allowing for IP cores to be integrated into the design and still allow plenty of room for interface logic. They have become high level building blocks for complex designs.

IP cores come in three different forms i.e. hard cores, soft cores and the mixture of the two, firm cores. Hard cores have been tested to have a proven layout and accurate timing specifications. Implementing a hard core into a PLD design is similar to integrating a packaged semiconductor onto a board for discrete functions. Hard cores have already been optimized and are ideal for timing critical applications. Hard cores cannot be changed and are typically the property of large semiconductor companies like Motorola and Texas Instruments.

Soft cores are more flexible than hard cores. A soft core is described at a behavioral or Register Transfer Level (RTL) and in VHDL or Verilog. The soft cores are

designed to meet minimum specifications over a large range of device technology. Many of the soft cores come with VHDL test benches. After synthesis the cores can be verified with the test benches for post synthesis simulation. It is critical to modify the test bench to include complete system level testing when the soft core is integrated with the interface logic. Soft cores are more flexible and can be targeted to various PLD vendors after post synthesis timing verification and simulation.

A firm core is a cross between a hard core and a soft core. A firm core is a synthesized gate-level description of a function. A firm core cannot be changed but can be simulated, placed and routed with the interface logic. Refer to Table 4.13 for the IP cores, their representation and characteristics.

IP Category	Representation	Characteristics
Soft	Microprocessor – targeted C code	Flexible, technology-independent mapping
	RTL HDL netlists	Slow system level simulation
		Describes hardware architecture function but not low level performance.
		High IP security risk
Firm	Assembly-code algorithms	Less flexibility
	Gate-level HDL netlists	Very slow system-level simulation
	Generic technology library	Reliably predicts hardware low level performance
	Timing models, floorplan	High IP security risk
Hard	Object code / machine code	Least flexible, technology-specific fab-process mapping
	Gate-level netlists	Very slow and/or difficult system-level simulation
	Technology-specific, process specific library	Predicts hardware performance most reliably
	Timing models, routing Polygon data	Low IP security risk

Table 4.13 IP Categories, Representation and Characteristics

System designers require the IP building blocks to be completely tested and verified prior to integration into a complete design. IP testing is very complicated and time consuming. The IP vendors are providing system-level evaluation models (SEMs) to the designers. The SEMS allow the designers to verify the system level performance of the design using algorithm/behavioral versions of the IP. Recently there has been two standards put through the industry on IP packaging and interfaces. The first standard is the Virtual Socket Interface (VSI). VSI standard outlines requirements for processor, bus functional and behavioral IP cores and defines the set of documentation required by the designers to integrate the IP blocks into their design. The Open Model Forum (OMF) Standard defines a standard for IP core simulators. Open Model Interface (OMI) will permit an OMF-compiled IP core to be simulated regardless of the developing language. These standards will play an important role in the design process using IPs. The overall design process can be broken down into three stages to make the design flow of complex designs more manageable. The first stage is the design and verification of the system at an individual block level. The second stage is to assemble the blocks into the system design for virtual prototyping. The third stage is creating a physical prototype through hardware emulation to reflect the functionality and the performance of the design in the targeted device technology.

IPs can be used for system-on-a-chip designs that would include third party IP processors, which can be integrated with peripheral devices, for example UARTs. There are many PLD vendors that are providing IP cores.

4.6.2 Intellectual Property Core Vendors

IP cores are available from various FPGA vendors, which include Actel, Xilinx, Altera, Lucent Technologies and Gatefield Corporation. Altera, Xilinx and Actel IP cores will be discussed in the following sections.

4.6.2.1 Altera Megafunctions

Altera's Flex 10K family contains an embedded array of logic cells with large blocks of RAM that can be integrated with other megafunctions. The Flex 10K architecture has the logic array blocks (LABs) with embedded array blocks (EABs). The FLEX 10K architecture lends itself to IP core integration rather than for single application designs. Altera's MegaCore function and Altera Megafunction Partners Program (AMPP) provide many different types of IP cores.

MegaCore functions are pre-optimized and tested logic blocks to perform a well-defined task in a system. The MegaCore functions can replace standard IC's or can replace new functions, for example, processors and bus controllers. The MegaCore functions come in VHDL, Verilog or Altera's Hardware Descriptive Language and can be used in schematics, EDIF netlist files or HDL code. The MegaCore functions are optimized for Altera's FLEX 8000 and FLEX 10K device families. The MegaCore functions library contains the following eight megafunctions:

- 8237 DMA controller
- 6502 8-bit processor
- 6402, 16450, and 8251 UART processors
- 6850 Asynchronous communications interface adapter
- 8259 Interrupt controller

- 8255 parallel I/O controller

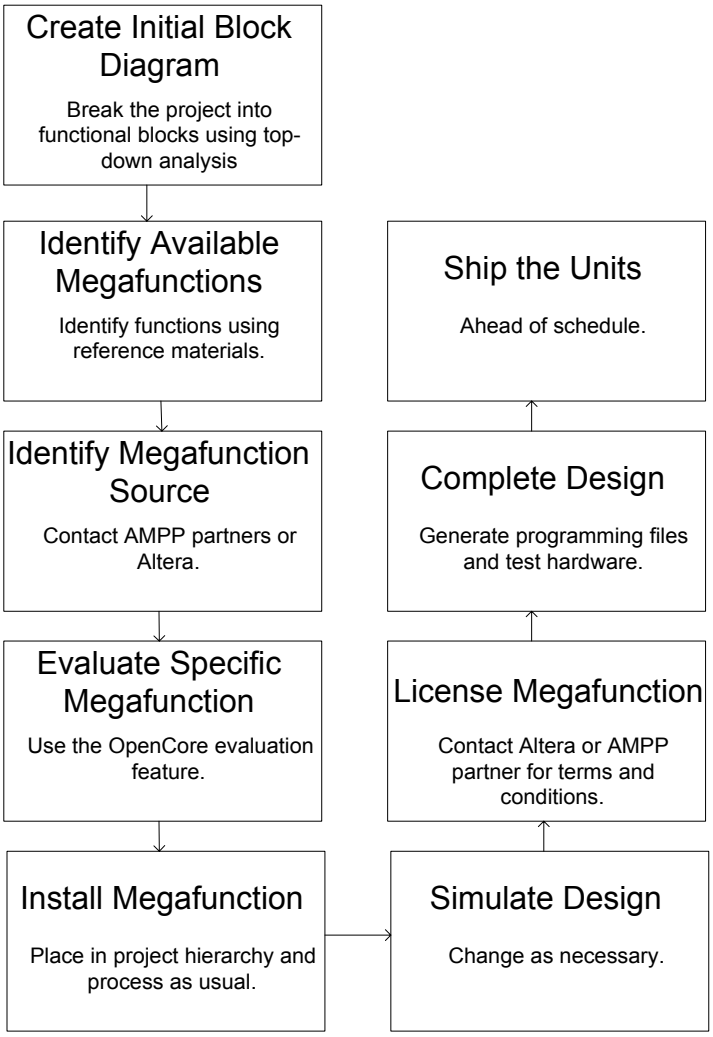

Figure 4.17 Altera Megafunction Top-Down Design Flow

The AMPP is an alliance between Altera and companies who specialize in specific megafunctions to increase the use of IP cores in PLDs. This alliance focuses on digital signal processing (DSP), bus interfaces such as PCI and USB and communications. DSP megafuctions will support fast Fourier transforms (FFTs) and adaptive impulse response (FIR) functions and have been provided by Silicon Systems Ltd. Who specialize in DSP ASICs and DSP megafunctions. PCI megafunctions are

coming form Eureka Technology and running at speeds of 33 MHz. In the area of communications AMPP joined with Nova engineering to provide parameterized complex multiplier/mixer and quadrature output NCO.

An important factor with using IPs in a complex system is the verification and validation that the core can meet the design requirements and specifications. Altera has introduced the OpenCore evaluation system, which allows the designer to try the core and see if it meets the specifications prior to licensing the megafunction. Figure 4.17 shows Altera's Megafunction top-down design flow.

4.6.2.2 Actel Intellectual Property Cores

Actel is partnered with industry to provide IP cores that are optimized for the specific architecture of Actel devices. The cores are avialable in hardware descriptive language (VHDL or Verilog) or in netlist format for a specific device family or technology. The documentation that is delivered with the core is the source code (HDL or netlist), testbench, synthesis script, user guide and data sheets. All the cores are designed, verified and tested in Actel FPGAs. Table 4.14 contains the Actel core application and description and the associated Actel target technology.

Application	Description	Target Technology
Processor	8-bit microprocessor	MX,SX
Telecon	All digital phase lock loop	MX,SX
	ISDN E1 framer/deframer	MX,SX
	High Level Data Link Controller	MX,SX
	ATM Forum Utopia level II interface	MX
Interfaces	Controller Area Network bus interface	MX,SX
	I2C Master and Slave interfaces	MX,SX
	Universal Asynchronous Receiver Transmitter Interface (UART)	MX,SX
	VME Slave Interface	MX,SX
	Serial Communication Controller	MX,SX

Table 4.14 Actel Core Applications and Description

4.6.2.3 Xilinx Intellectual Property Cores

The Xilinx XC4000 architecture is the key device for Xilinx CORE solutions. Xilinx next generation FPGAs will have gate density ranges form 20,000 to 500,000 and will soon be up to 1 million gates. The Xilinx Virtex family currently has 1500 to 32,000 logic cells, with on-chip frequencies of 100 MHz and an internal supply voltage of 2.5 V and 3.3 V I/O buffers. The Xilinx CORE solutions contain predefined logic functions that are optimized for Xilinx architecture to increase performance and assist in reducing the development time of the design. The Xilinx CORE solutions are broken into four groups supporting four applications areas, which are as follows:

- Xilinx CORE solutions applications
    1. Standard Bus Interfaces – such as PCI, PCMCIA, USB and IIC.
    2. DSP Functions – These range from small functions to large functions. The small functions include adders, registers and multipliers. The large functions include FIR filters and transforms.
    3. Communications and Networking – These functions include Asynchronous Transfer Mode (ATM) cores, Forward Error Detection cores and Telecommunication cores, such as HDLC Protocol and MT1F T1 Framer.
    4. Base-Level Functions - These include small cores, such as, decoders, multiplexers, integrators and parallel multipliers and large cores like UARTs and RISC processors.

- Xilinx CORE solutions groups
    1. LogiCORE Products – These are intellectual property cores that have been pre-implemented and verified logic functions sold and supported by Xilinx.
    2. AllianceCORE Program – This is the alliance between Xilinx and third-part IP vendors. This provides many more available IP products.
    3. Reference Designs – Reference designs allow designers to practice with IP cores in system level architecture and are free of charge.
    4. LogiBLOX Products – Graphical tool for creating simple modules and using generic modules in a logic implementation. LogiBLOX comes as part of the Xilinx standard set of software.

Through research the Xilinx CORE solutions was the largest set of Intellectual Property Cores available for FPGAs. The IP cores of interest for the implemented design covered by this thesis are the UART and certain DSP functions. The current design contains an external UART that could just as well been implemented using a Xilinx XC4000 device and an IP core. It is common practice for camera systems to have image preprocessing capability prior to data analysis. Common filters and transforms in DSP cores can easily be implemented into the system design for distribution of device overhead and data processing and is being considered for the next generation camera interface electronics. The detailed design of the APS camera system and the interface electronics is contained in chapters that follow.

4.7 Programmable Logic Devices Summary

Programmable Logic Devices (PLDs) come in two general categories. The categories are Simple Programmable Logic Devices (SPLDs) and High-Density

Programmable Logic Devices (HDPLDs). HDPLDs come in two architectures, which are Complex Programmable Logic Devices (CPLDs) and Field Programmable Gate Arrays (FPGAs). Both CPLDs and FPGAs are available in SRAM based programming configuration but only CPLDs can be EPROM or EEPROM programmed. This means that CPLDs can be up and running when power is applied and are nonvolatile. Some FPGAs are antifuse-based allowing them to only be one time programmable devices (OTPs) and SRAM based, which can be programmed as many times as required. The two major elements of CPLDs and FPGAs are the logic elements and the interconnect structure. Both FPGAs and CPLDs have their advantages and disadvantages. CPLDS are ideal for high-speed applications requiring critical timing and FPGAs are more flexible with the finer-grained architecture. Lattice semiconductor CPLDs were used for the design, specifically the ispLSI 3000 series. This CPLD architecture offered predictable timing, high densities, in-system programmability, flexible architecture for mixed combinatorial and register intensive designs and system partitioning. Some applications can not use CPLDs. Planetary Spacecraft and earth orbiting satellites and science instruments require Radiation Hardened PLDs. The mission length and orbit will determine the levels of radiation the device will have to withstand. Actel is the leading FPGA vendor for RadTolerant and RadHard devices with Xilinx just recently releasing its first RadHard family of devices, the XC4000 series. Intellectual property (IP) cores are the latest trend in the FPGA market. IP cores are predesigned and preverifed logic functions for ASIC and PLD-based designs. They range in complexity form larger processor and DSP cores to smaller multiplexer and UART cores. Three companies were outlined, and those were Actel, Xilinx and Altrea.