CHAPTER 5

COMPARISON BETWEEN SINGLE-STAGE AND TWO-STAGE PFC TECHNIQUES WITH UNIVERSAL-LINE INPUT

5.1 INTRODUCTION

As introduced in Chapter 1, the active PFC converters can be implemented using either the two-stage approach or the single-stage approach. The two-stage approach is the most commonly used approach. In this approach, an active PFC stage is employed as the front-end to force the line current to track the line voltage. Additionally, the PFC stage establishes a loosely regulated high-voltage dc bus at its output, which serves as the input voltage to a conventional dc/dc stage with a tightly regulated output voltage. While the two-stage approach is a cost-effective approach in high-power applications, its cost-effectiveness is diminished in low-power applications due to the additional PFC power stage and control circuit. A low cost alternative solution to this problem is to integrate the active PFC input-stage with the isolated dc/dc output stage. A number of active single-stage PFC (S^2PFC) techniques have been introduced in recent years [B1-B19]. In all of these approaches, the PFC switch and controller are saved. For the S^2PFC converters, generally, the CCM S^2PFC converters are more attractive than the DCM S^2PFC converters in many applications. The CS S^2PFC converter presented in the previous chapter is a good example of the CCM S^2PFC converter with good performance.

Naturally, it is expected that the S^2PFC converters have lower cost than the two-stage PFC converters. However, it really depends on the different applications. Unlike in the two-stage approach, the dc voltage on the energy-storage capacitor in a S^2PFC converter is not regulated.

As a result, in universal-line applications (90 – 265 Vac), the energy-storage-capacitor voltage varies with the load and line. In this chapter, a detailed comparison study between the CCM S^2PFC converter and the two-stage converter is given for universal line application with the hold-up time requirement. The analysis in this chapter shows that the wide bulk-capacitor voltage range increases the ratings, size, and cost of the components, and it also reduces the overall efficiency. The merits and limitations of the two-stage and single-stage approaches are also discussed.

5.2 THE EXAMLE CIRCUITS OF TWO ACTIVE PFC APPROACHES

5.2.1 Two-stage PFC approach and its example circuit

The conceptual structure of the two-stage PFC converters is re-drawn in Fig. 5.1. In this approach, there are two independent power stages. The front-end PFC stage is usually a boost or buck/boost converter. The boost converter front-end consists of a boost inductor, boost switch, and rectifier. The PFC controller senses the line voltage waveform and forces the input current to track the line voltage to achieve the unit input power factor. Since the voltage of energy-storage bulk capacitor C_B, V_B, is loosely regulated, V_B is a dc voltage which contains a small second order harmonic. This bus voltage is typically regulated at around 380 Vdc in the entire line input voltage range from 90 V_{ac} to 265 V_{ac}. The high bus voltage V_B minimizes the bulk capacitor value for a given hold-up time. In addition, the narrow-range-varying V_B improves the efficiency of an optimized dc/dc output stage. The dc/dc output stage is the isolated output stage that is implemented with at least one switch, which is controlled by an independent PWM controller to tightly regulate the output voltage. To minimize cost, R-C-D reset scheme is used.

Figure 5.2(a) shows the input current and voltage waveforms of a two-stage PFC converter, whereas Fig. 5.2(b) shows the duty-cycle variations of the front-end PFC stage and the dc/dc output stage during a rectified-line cycle. With a variable PFC duty-cycle d_{PFC} on the PFC switch, the input current can be shaped exactly in shape and phase of the input voltage to achieve unit input power factor. Since the input and output voltage of the dc/dc converter are constant, the duty cycle of the dc/dc converter, $d_{dc/dc}$, is also constant, as shown in Fig.5.2 (b).

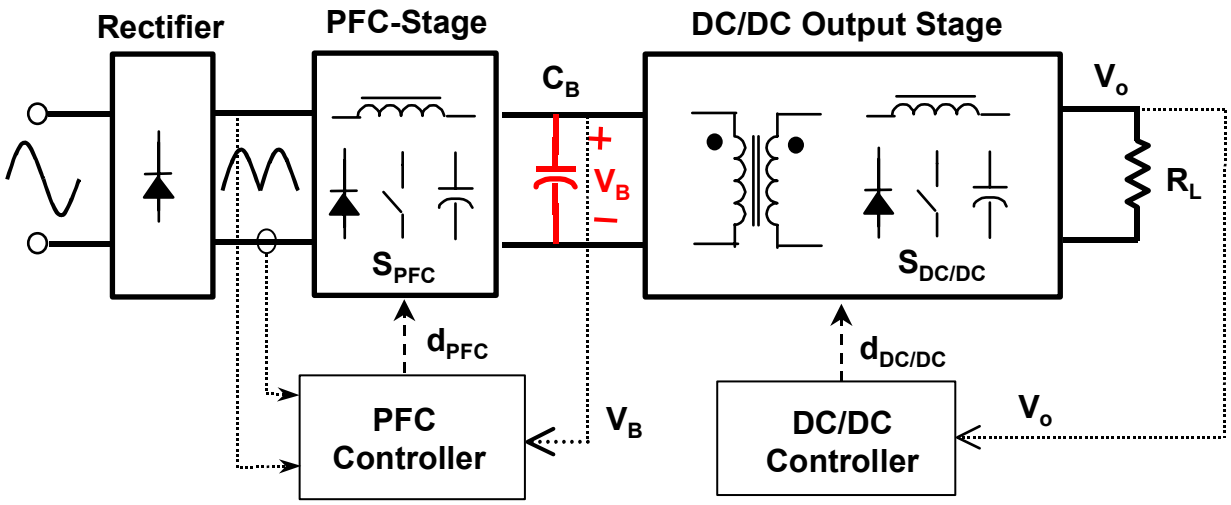


Figure 5.1 Conceptual structure of the two-stage PFC converters

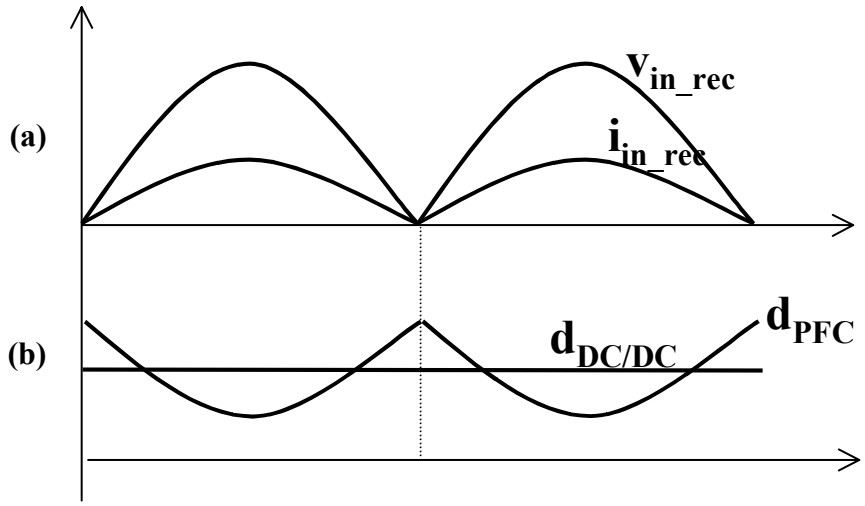


Figure 5.2 Ideal waveforms of the two-stage PFC converter:
(a) rectified input voltage and current;
(b) duty-cycle of the PFC and DC/DC switches.

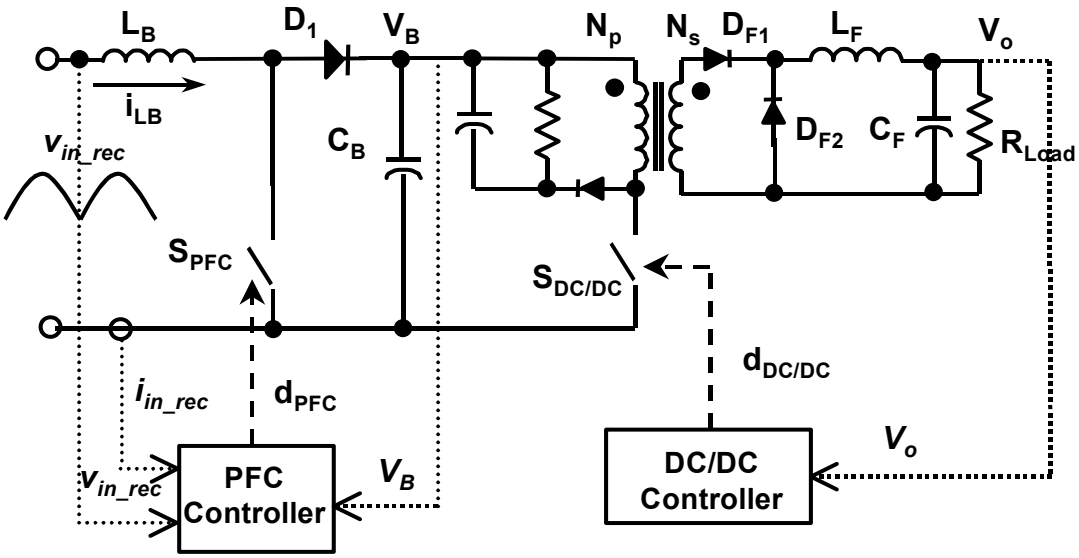


Figure 5.3 CCM boost PFC converter with RCD reset forward output stage

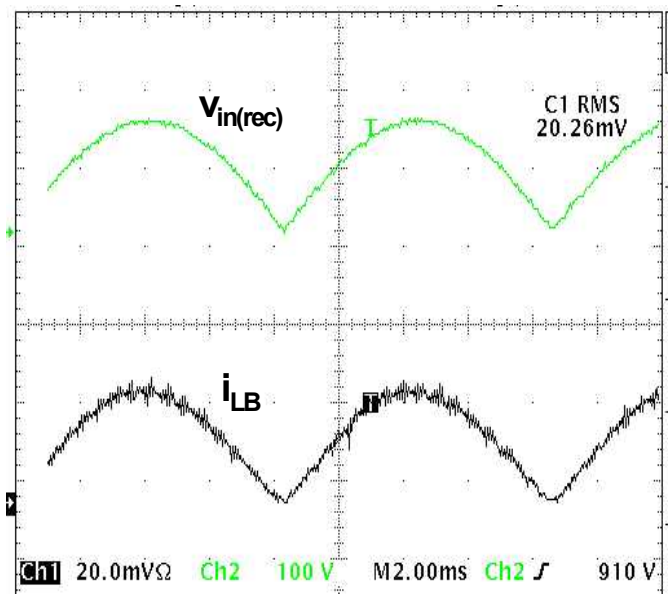


Figure 5.4 Tested rectified input voltage / current waveforms of the CCM boost PFC rectifier

Figure 5.3 shows the circuit diagram of the example two-stage PFC converter for comparison, which contain a CCM boost PFC front-end and a PWM forward DC/DC converter. Figure 5.4 shows the typical input inductor current waveforms of this converter.

5.2.2 Single-stage PFC approach and its example circuit

The generalized structure of the S^2PFC converter is re-drawn in Fig. 5.5. Compared to the two-stage approach, the single-stage approach uses only one switch and controller to shape the input current and to regulate the output voltage. The controller is used for a fast regulation of the output voltage. As a result, when the converter in Fig. 5.5 works in a steady state, the switch duty-cycle is almost constant during a line cycle. With a constant duty cycle $d_{DC/DC}$, the boost inductor provides a naturally shaped current with certain distortion. Although for a S^2PFC converter attenuation of input-current harmonics is not as good as for the two-stage approach, generally, it is good enough to meet the IEC 61000-3-2 class D requirements.

Generally, for any PFC converter, the instantaneous input power during a line cycle is pulsating, while the output power is constant. Therefore, in any PFC circuit, there must be an energy-storage capacitor to store the unbalanced energy. However, in a single-stage PFC converter, unlike in a two-stage PFC converter, energy-storage-capacitor voltage V_B is no longer loosely regulated at a constant value because the controller is used to regulate the output voltage V_o, not V_B. As a result, in the single-stage PFC converters, V_B varies with the line voltage. For universal line input (90 Vac – 265 Vac), V_B is typically around 130 V at the low line and higher than 400 V at the high line. The wide voltage range has detrimental effect on the conversion efficiency, and it requires an energy-storage capacitor with a large capacitance and high voltage

rating (>400 Vdc) to meet the hold-up time requirement. Since the cost and size of an electrolytic capacitor increase with its capacitance, there is a strong trade-off between the cost and size savings brought about by using a single switch and controller and the increased cost and size of a larger capacitor. As a result, in universal-line application with a hold-up time requirement, the S^2PFC approach may not be more cost effective than the conventional two-stage approach.

The comparisons carried out here have been performed on CCM CS S^2PFC converters. Figure 5.6 shows the circuit diagram of the CS S^2PFC converter with forward output [B6, B7]. This converter uses an additional inductor L_1 to achieve the CCM operation. In the circuit in Fig. 5.6, an active clamped (ACL) reset circuit [B9] is employed to achieve a maximum duty cycle of the switch so that energy-storage capacitance can be minimize in this circuit.

Figure 5.7 shows typical input voltage and current waveform of a S^2PFC circuit and the input current harmonics comparison. Although, the input current is not sinusoidal, as shown in Fig. 5.7(b), it meets the IEC 61000-3-2 Class D requirement. The duty cycle $d_{DC/DC}$ of the switch in the S^2PFC converter is constant during a line cycle.

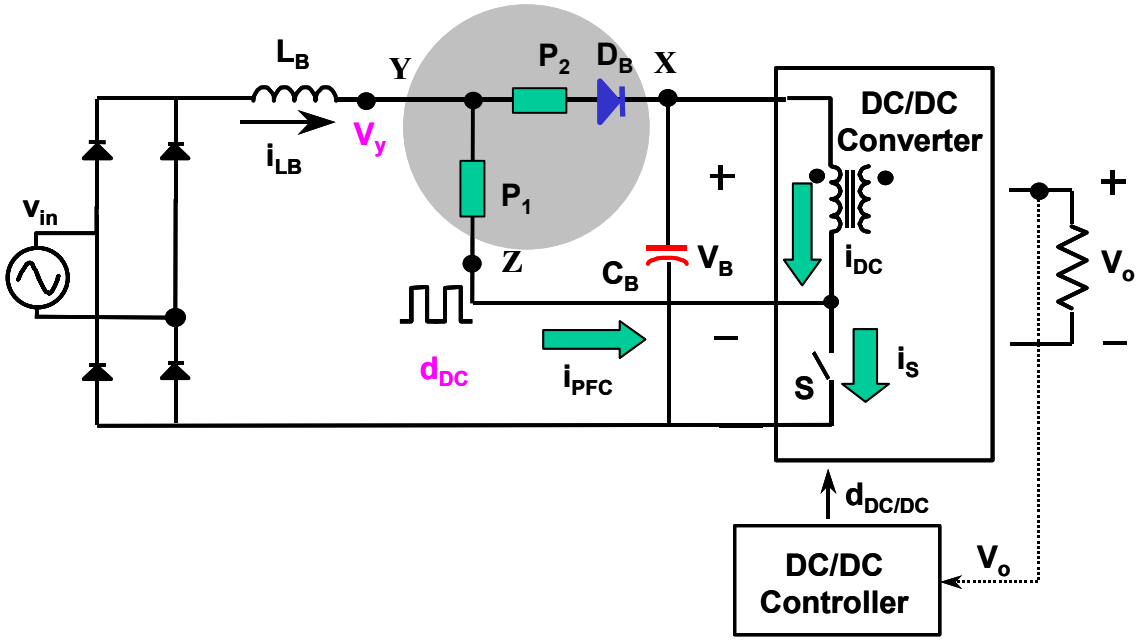


Figure 5.5 Generalized structure of the S^{2}PFC converter

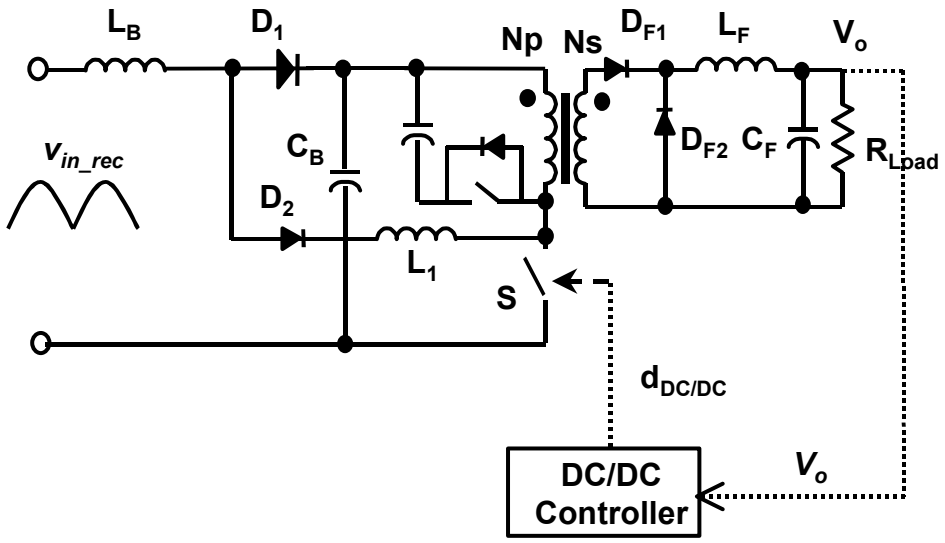
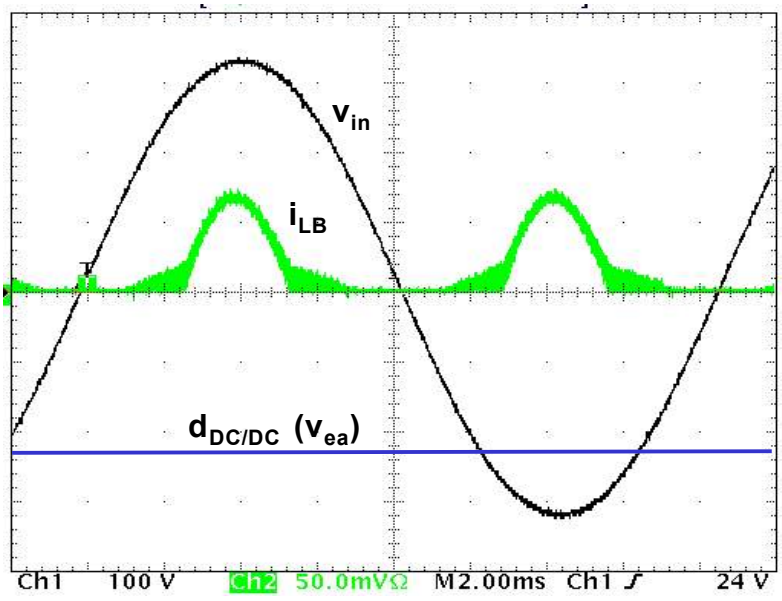
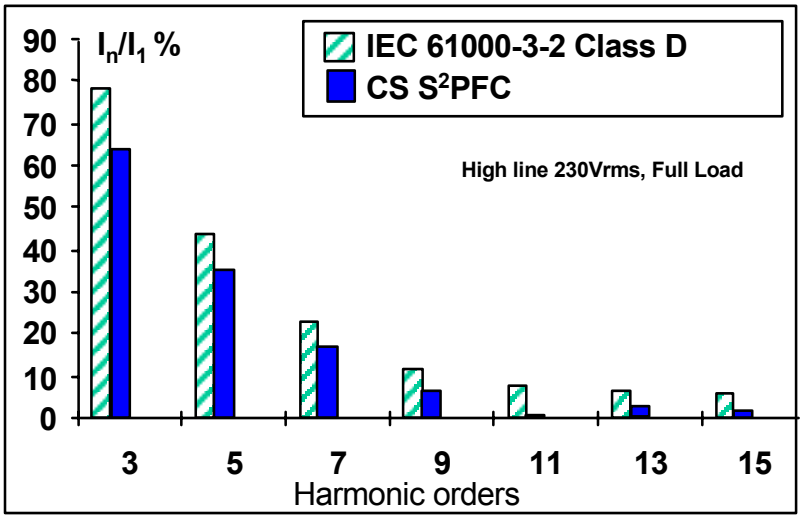


Figure 5.6 CCM CS S^{2}PFC converter with forward DC/DC output stage



(a)



(b)

Figure 5.7 Tested line-cycle waveform and input current harmonics of the CCM CS S^{2}PFC converter

5.3 COMPARISON BETWEEN THE TWO-STAGE AND SINGLE-STAGE PFC CONVERTERS

The comparison of the two-stage and single-stage PFC approaches was performed under the following assumptions:

- Input voltage is universal line voltage from 90 V_{ac} to 265 V_{ac}.
- Output voltage is 5 V_{dc}, and output power levels are 50 W, 100 W, 200 W, 300 W and 400 W, respectively.
- Hold-up time is also a requirement.
- The switching frequency was assumed to be 100 kHz for both the PFC switch and the switch in the dc/dc power stage. Also, it was assumed high frequency MOSFET devices were used for all the switches.
- In the two-stage PFC converter, the PFC stage efficiency η_{PFC} of 0.9 was assumed, whereas the dc/dc stage efficiency η_{DC} of 0.8 is assumed, for an overall efficiency η of around 0.72. For the S^2PFC converter, it was assumed that the overall efficiency η is about 0.7.

5.3.1. Comparison of the bulk-capacitors with hold-up time requirement

5.3.1.1) Difference of the bulk-capacitor voltage range

As discussed in previous sections, a fundamental difference between the two-stage and single-stage approach is the bulk-capacitor voltage V_B. In the two-stage PFC converter, V_B is loosely regulated to be around 400 V_{dc} regardless of the input voltage, which V_B in the S^2PFC converters is not regulated and changes with line and load change. Typically, the V_B of the CCM

S^2PFC converter varies from 130 V_{dc} to 400 V_{dc} at full load and universal-line input (90-265 V_{ac}). The following comparison will show that V_B range difference between the two-stage and single-stage approach will significantly impact the component rating and performance of these two converters.

5.3.1.2) Hold-up time and hold-up capacitance C_B

In a majority of computer-related applications a hold-up time is a very important requirement. Generally, the hold-up time is the time during which a power supply needs to maintain its output voltages within the specified range after a dropout of the line voltage. This time is used to orderly terminate the operation of a computer or to switch over to the UPS operation after a line failure. For example, the majority of today's desktop computers and computer peripherals require power supplies that are capable of operating in the 90-265 V_{ac} range and can provide a hold-up time of at least 10 ms. The required energy to support the output during the hold-up time is obtained from a properly sized energy-storage capacitor C_B. Figure 5.8 conceptual explains the hold-up time and the capacitor voltage V_B during the hold-up time. As shown in Fig. 5.8, when the line voltage fails at time instant t_0, to maintain the constant output V_o, the capacitor C_B has to provide the energy to the output until time instant t_1. The time interval t_1-t_0 is defined as the hold-up time.

The rating of the hold-up capacitor C_B significantly impacts the total size and cost of power supply. According to Fig. 5.8, the hold-up capacitance C_B is determined by Eq. (5.1), where $V_{B(90)}$ is the low line full-load capacitor voltage, and $V_{B(min)}$ is the minimum designed capacitor voltage. $P_{o(max)}$ is the maximum output power, t_{hold} is the hold-up time, and η_{dc} is the forward stage efficiency.

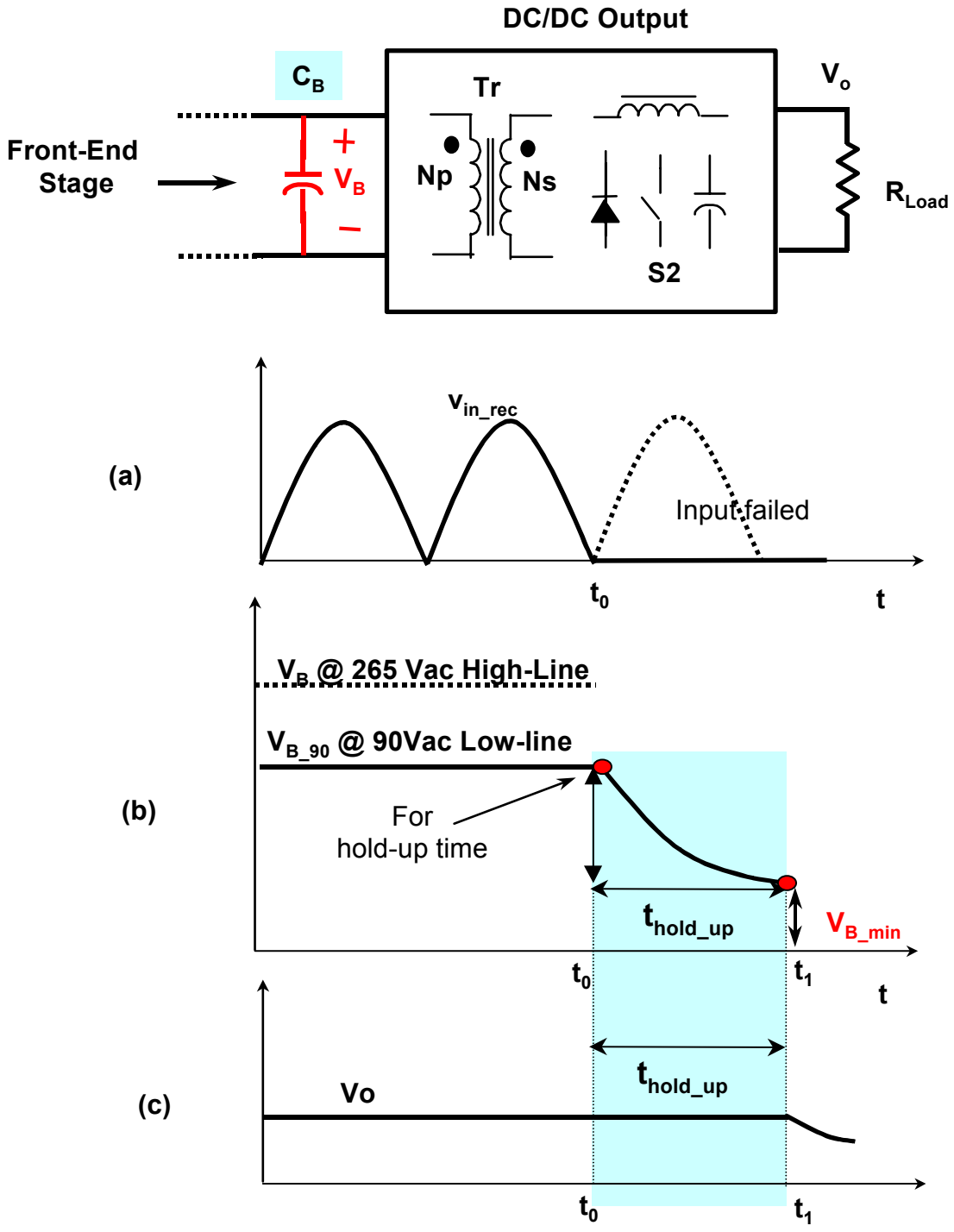


Figure 5.8 Definition of the hold-up time and hold-up capacitance
(a) Input voltage failure, (b) capacitor voltage V_B during hold-up time, (c) output voltage V_o

$$C_B = \frac{2 \cdot \frac{P_{o(\max)}}{\eta_{dc}} \cdot t_{hold}}{V_{B(90)}^2 - V_{B(\min)}^2} \tag{5.1}$$

5.3.1.3) Hold-up capacitance comparison between single-stage and two-stage PFC converters

If, for a two-stage PFC converter, the bus voltage $V_{B(90)}$ is regulated at 400 V and the minimum voltage $V_{B(min)}$ =300 V is selected, a relatively small bulk capacitor is required. For example, for t_{hold}=10 ms, $P_{o(max)}$=100 W, C_B is only 37.8 μF based on the Eq. (5.1). However, for a S^2PFC converter, the low line bus voltage is not regulated, but typically it is around 130 V when the input line voltage is 90 V_{ac}, which is the worst case for the S^2PFC converter. Therefore, if $V_{B(min)}$ is selected at 90 V_{ac}, C_B must be at least as high as 284 μF to maintain the same hold-up time. This capacitance value is seven times larger than the corresponding two-stage PFC capacitor value. Figure 5.9 shows the relationship between C_B and hold-up time t_{hold} for the output power of 100 W for two different PFC approaches. As can be seen in Fig. 5.9, the single-stage PFC converter requires much larger hold-up capacitance than the two-stage PFC converter does. In both cases, the capacitor voltage rating is 450 V_{dc}. Figures 5.10(a) and (b) show the dependence of C_B as a function of output power $P_{O(max)}$ for the two-stage and single-stage PFC converters, respectively. As can be seen in Fig. 5.10(a) and (b), the single-stage PFC requires a larger capacitance than the two-stage PFC converter for all power levels. In addition, for both converters, the capacitance always increases as the hold-up time increases.

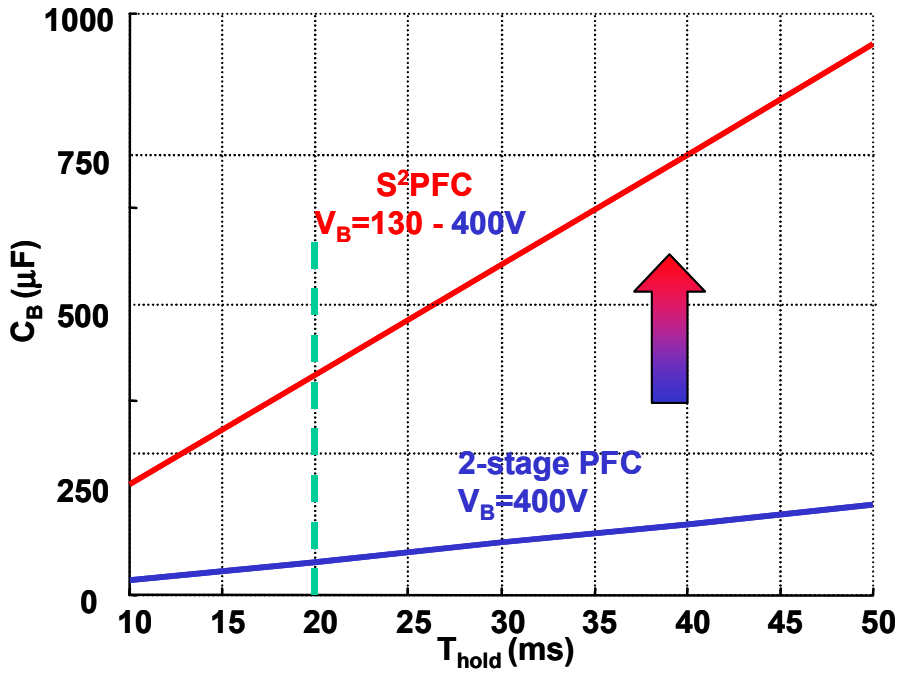


Figure 5.9 Energy-storage capacitance C_B vs. hold-up time (P_o=100W)

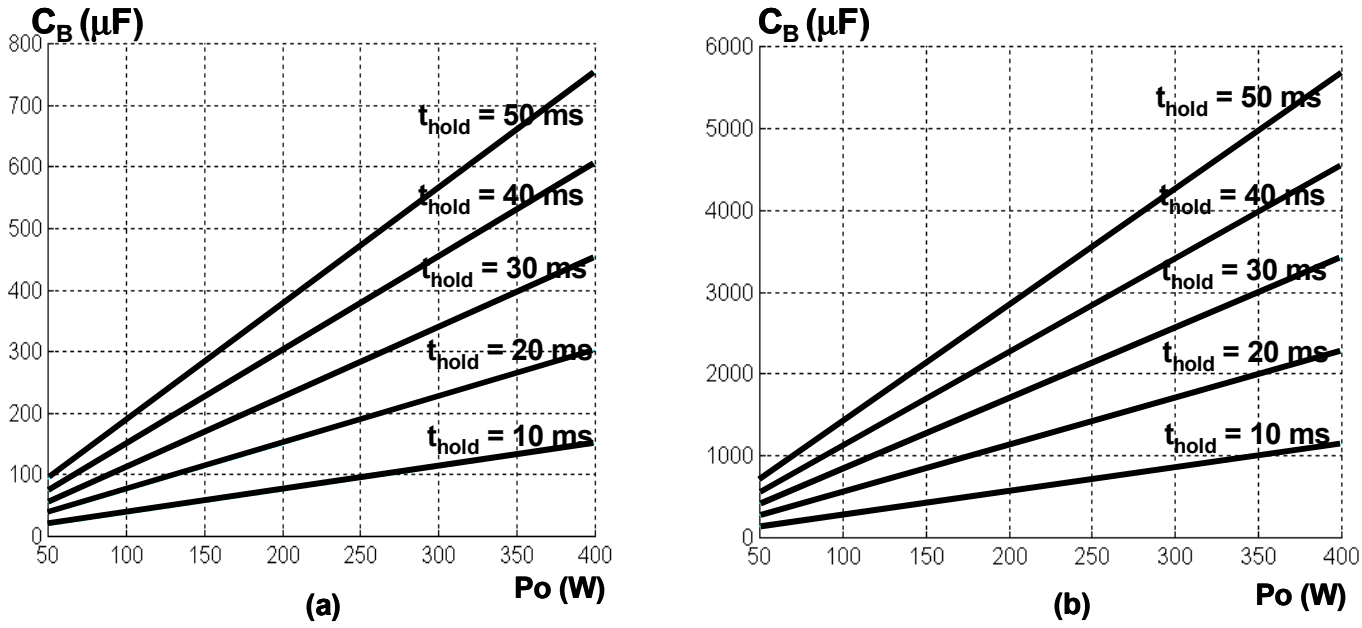


Figure 5.10 Energy-storage capacitance C_B vs. output power P_o for different hold-up time requirements: (a) two-stage PFC; (b) single-stage PFC

5.3.2 Comparison of the semiconductors

5.3.2.1) Switch(s) and their power loss

Although integrated S^2PFC eliminates the PFC switch S_{PFC}, the total input power still need to go through two power conversion steps to the output, if no feedback winding is used. In this case, the S^2PFC converter should not have significant efficiency improvement over the conventional two-stage PFC converter. In the two-stage PFC converter, the PFC switch handles the PFC current i_{PFC}, whereas the switch in dc/dc converter handles the dc/dc converter's current i_{DC}. The single-stage PFC converter combines these two switches into one. As a result, as shown in Fig. 5.5, the combined single switch handles both the PFC current and the dc/dc stage current so it is subjected to a higher current stress. The total switch current $i_S = i_{PFC}+i_{DC}$. In addition, since at low input line the energy-storage-capacitor voltage in a S^2PFC converter is much lower than the corresponding voltage in a two-stage PFC converter, the DC/DC current i_{DC} in the S^2PFC converter is much higher than the switch current in the two-stage PFC converter with the same output power. As to the forward transformer turns-ratio N, $N_{two\text{-}stage}$=36 and N_{S2PFC}=13. The current through the switch determines the loss on the switch. Generally, the rms current of the PFC switch in the two-stage PFC converter is given by Eq. (5.2) and (5.3):

$$I_{in\_pk} = \sqrt{2} \cdot \frac{P_{o\max}/\eta}{V_{in\_\min}} \tag{5.2}$$

$$I_{S\_PFC} = \frac{1}{\pi} \cdot \sqrt{\int_0^{\pi} (1 - \frac{\sqrt{2} \cdot V_{in\_\min}}{V_B} \cdot \sin(x)) \cdot I_{in\_pk}^2 \cdot \sin(x)^2 \, dx} \tag{5.3}$$

The switch current I_{S2} of the forward dc/dc converter can be calculated by Eq. (5.4):

$$I_{s\_DC/DC} = \frac{P_{o\max}/V_o}{N} \cdot \sqrt{D_{FWD}} \tag{5.4}$$

Where N is the turn-ratio of the forward transformer, and D_{FWD} is the duty-cycle of the forward converter.

For the CS S^2PFC converter, the input current cannot be expressed by a close-form equation because the input current has an irregular waveform. Therefore, the rms current of the switch in S^2PFC converter, $I_{S(rms)}$, has to be obtained by simulations.

Figure 5.11 shows the comparison of the current ratings between the two-stage PFC converter and the S^2PFC converter. It shows that the rms switch current in the S^2PFC is higher than the sum of the currents of both switches in the two-stage PFC converter. Therefore, the single-stage PFC implementation requires a larger switch compared to the switches in the two-stage PFC converters. The switch conduction loss equals to the rms current square times switch on resistance:

$$P_{CON} = I_S^{RMS} \cdot R_{ds(on)} \tag{5.5}$$

For example, for 100 W power supply, if use IXYS MOSFET IRPF450 (R_{ds}=0.8Ω @ T_j=100°C) for the S_{PFC} in two-stage PFC, IXTH5N100A (R_{ds}=3.1Ω @ T_j=100°C) for the $S_{DC/DC}$, and IXTH15N100 (R_{ds}=1.2Ω @ T_j=100°C) for the S^2PFC switch S, the switch conduction loss comparison is given in Fig. 5.12. It shows even the S^2PFC converter has larger switch, its switch conduction loss is still as high as twice of the total switch conduction losses in the two-stage PFC converter.

As to the switching loss, the CS S^2PFC converter may have advantage over the two-stage PFC converter because the CS inductor L_1 reduces the boost diode reverse-recovery loss. Even though, in general, the S^2PFC has a higher total loss than the two-stage PFC does. Or, to achieve the same efficiency, the S^2PFC approach requires more silicon than the two-stage PFC approach.

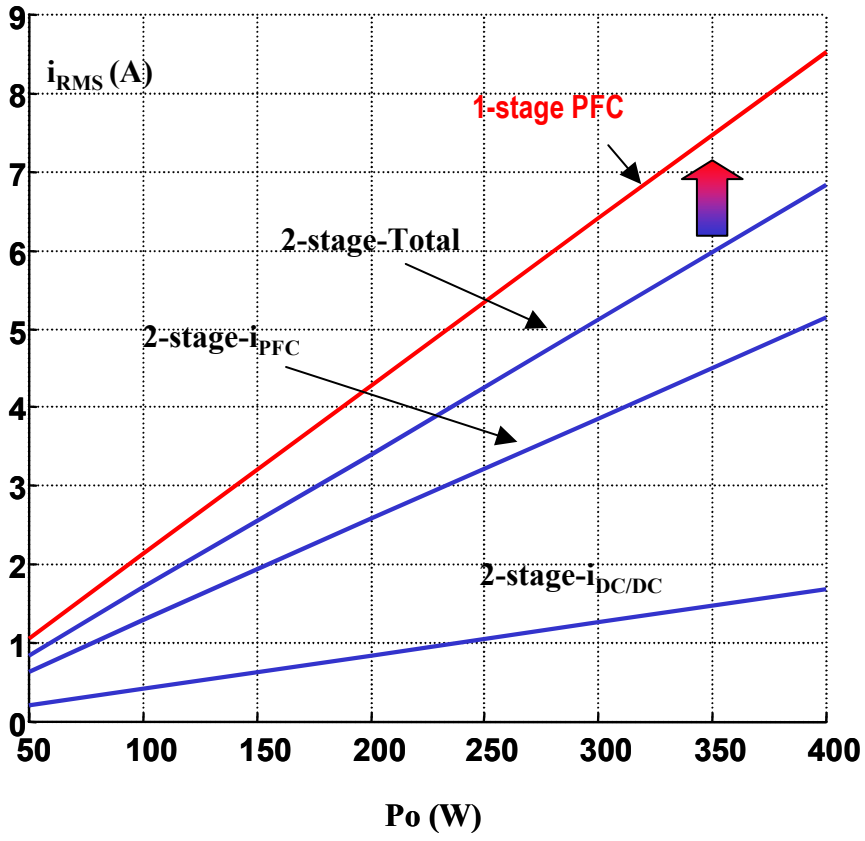


Figure 5.11 Switch RMS current comparison vs. the output power (V_{in}=90V)

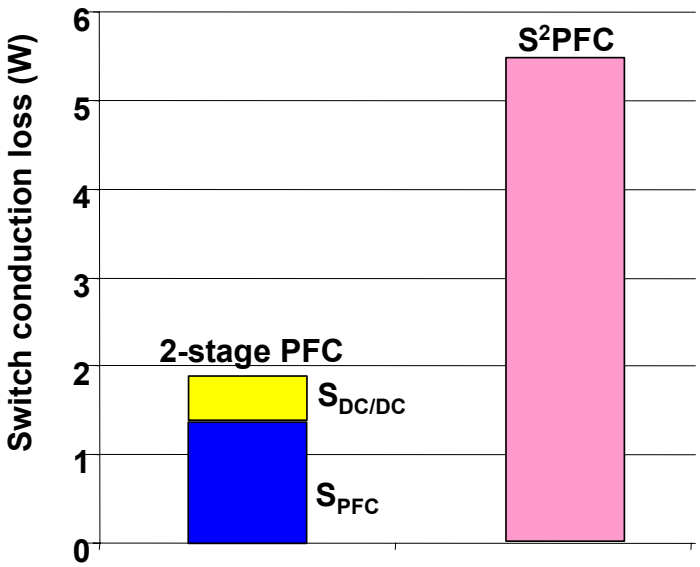


Figure 5.12 Switch conduction loss comparison between 2-stage and 1-stage PFC (V_{in}=90V, P_o=100W)

5.3.2.2) Current stress on the boost diode and output diode

When the conduction loss on the diode is concerned, the average diode current is used since the diode is like a voltage source. The average current through the boost diode and the output rectifier diodes are calculated for both the two-stage and single-stage PFC converters.

Figure 5.13 shows the comparison of the average current of the boost rectifiers. As can be seen, the S^2PFC converter has a higher rectifier current than the two-stage PFC converter at all power levels. The S^2PFC converter has a smaller effective boost duty-cycle d_{eff} and thus a larger diode conduction interval ($1-d_{eff}$). The rectifier voltage rating in both cases is 500 Vdc, *i.e.*, it is higher to the capacitor voltage V_B.

Finally, Fig. 5.14 shows the maximum average current of the forward output rectifiers as a function of the output power. As can be seen, the S^2PFC converter also has a higher current through the output rectifiers than the two-stage PFC converter. This is because the switch duty-cycle is very small in the S^2PFC converter at 265 V_{ac} input. Therefore, all the output inductor current goes through the bottom rectifier diode D_{F2} in Fig. 5.6. At the same time, with lower forward transformer turn-ratio, the voltage stress on the output rectifier in the S^2PFC converter is higher than the voltage stress in the two-stage circuit. For the 5 V output, the reverse voltage on the output (secondary side) rectifiers is 35 V in the S^2PFC converter, whereas the corresponding voltage in the two-stage PFC converter is only 12 V. Because of the higher reverse voltage on the output rectifiers, the power loss in the output rectifiers in the single-stage PFC converter is larger than in the two-stage PFC converter.

In summary, the S^2PFC converter has higher semiconductor losses than the two-stage PFC does. It means the S^2PFC converter surfers lower efficiency.

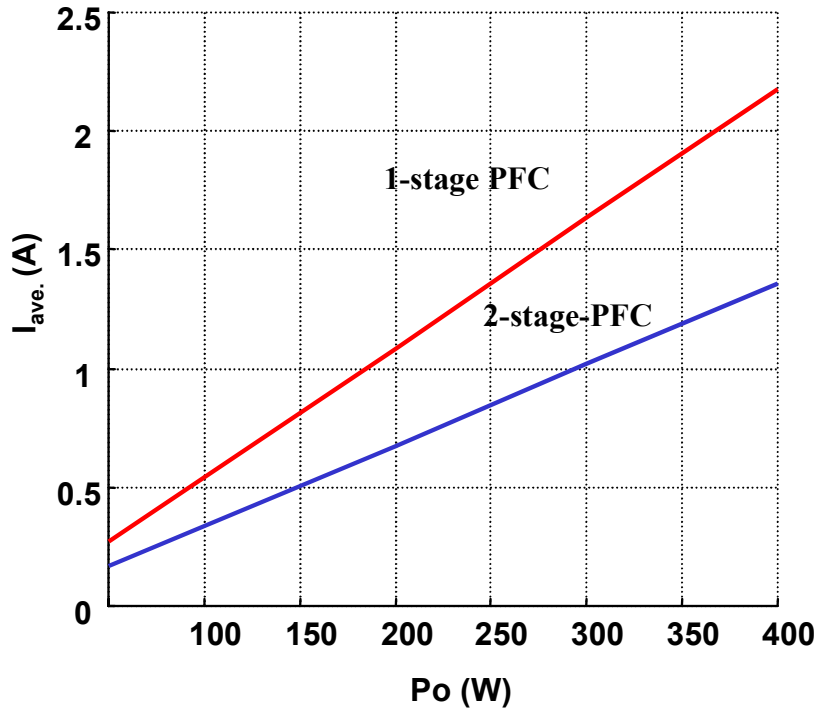


Figure 5.13 Boost diode maximum average current vs. output power (V_{in}=90V)

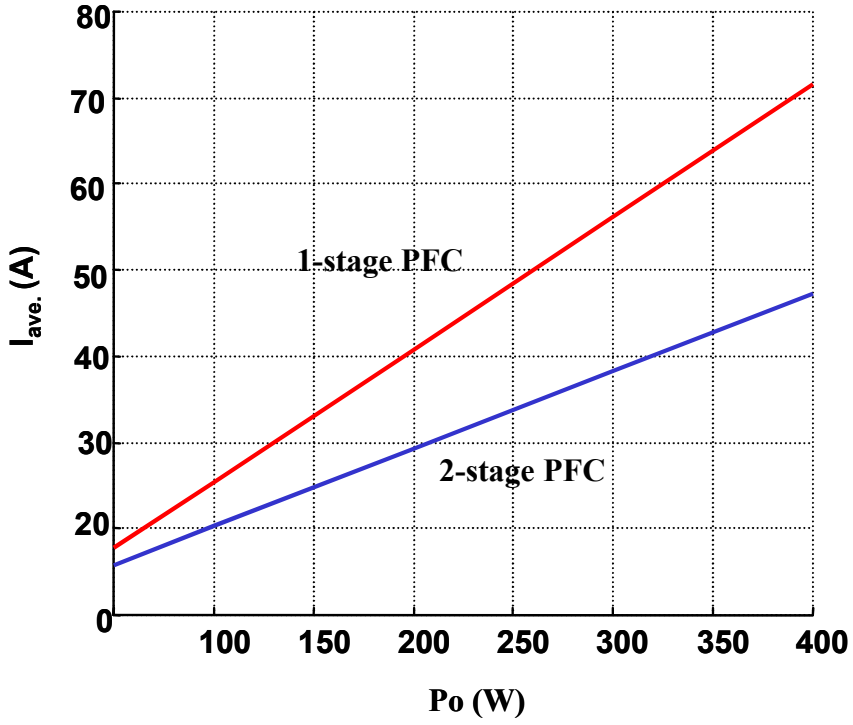


Figure 5.14 Maximum output Schottky rectifier average current vs. output power

5.3.3) Comparison of the inductors

5.3.3.1) PFC inductor(s)

In the two-stage PFC converter, the boost inductance L_B determines the magnitude of the switching-frequency input current ripple and the related DM-EMI filter size. In the CS S^2PFC converter, as discussed in Chapter 4, the total inductance $L_B + L_l$ determines the input current ripple. To do a fair comparison, the front-end inductors' values are compared under the condition that both circuits keep the same input current ripple at the switching frequency.

Since it is hard to mathematically calculate the high-frequency spectrum, circuit simulation is used as an approach to quantify the inductance in both converters. Figure 5.15 shows the simulated boost inductor current waveform i_{LB} and its high-frequency spectrum of the CS S^2PFC converter. As can be seen, when the input voltage is high, the boost inductor i_{LB} has larger DCM portion. As a result, the CS S^2PFC has high current ripple at high line. When the simulation circuit has switching frequency f_S=100kHz, output power P_o=100W, L_B=500μH and L_l=300 μH, the maximum switching-frequency current i_{fs}=1.28A, as shown in Fig. 5.15(d). Figure 5.16 shows the simulated i_{LB} waveform and its high-frequency spectrum of the CCM two-stage converter at $90V_{ac}$ input. Since the bulk-capacitor voltage is regulated around 400V, the input current ripple is maximized at low line while the switch duty-cycle is maximized. As can be seen, to maintain the same input current ripple at 100 kHz in Fig. 5.16(b) and Fig. 5.15(d), the two-stage PFC boost inductance is chosen as L_B = 1650 μH, which is much larger than the total inductance of L_B and L_l in the CS S^2PFC converter. It means the total front-end magnetic size of the CS S^2PFC converter may be smaller than that of the two-stage PFC, though the CS S^2PFC needs two inductors. Figure 5.17 conceptually explains why the CS S^2PFC converter needs small

inductance than the two-stage converter does. Every switching cycle, the PFC boost inductor current ripple is determined by:

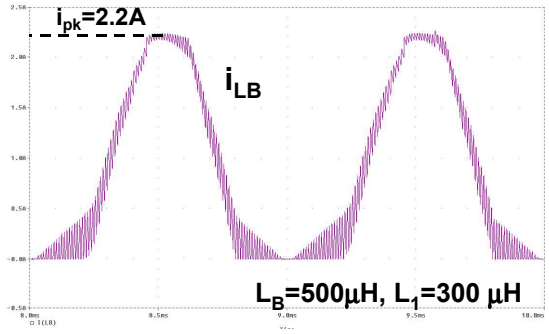
$$\Delta i_{LB} = \frac{v_{in} \cdot d_{PFC} \cdot T_S}{L_B} \tag{5.6}$$

In the two-stage PFC converter, the PFC duty-cycle d_{PFC} varies in the range from 1 to $(1\text{-}v_{in}/V_B)$ during every half line cycle. However, in the CCM S^2PFC converter, the boost inductor L_B sees the effective duty-cycle d_{eff}, which is limited by the maximum forward duty-cycle $d_{DC(max)}$. As shown in Fig. 5.17, d_{eff} in the CS S^2PFC converter is much smaller than the two-stage boost PFC duty-cycle d_{PFC}. Therefore, CS S^2PFC converter requires much smaller boost inductance to achieve same input current ripple as the two-stage PFC converter does. Figure 5.18 further shows the PFC inductance comparison between the two-stage and single-stage PFC vs. the output power. The CS S^2PFC converter has smaller total inductance.

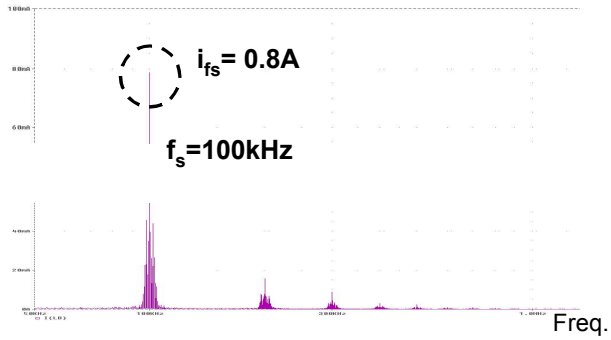
As a matter of fact, the actual inductor(s) size is a discrete number which is depends on the available commercial core size. Table 5.1 lists one designed example for comparison between the two-stage and single-stage PFC inductors' core size and weight. It shows that the CS S^2PFC converter has smaller total PFC inductor in terms of size and weight.

Table 5.1 PFC inductor designs and core size/weight comparison (P_o=100W, f_S=100kHz)

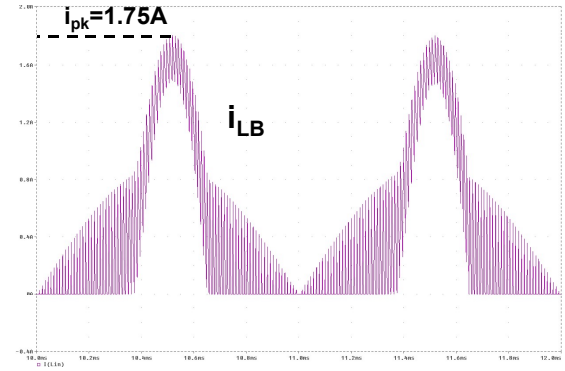
	2-stage PFC converter	1-stage PFC converter
Inductance (μH)	L_B = 1650	L_B = 500, L_1=300 (total 800)
Simulated peak current	2.1 A	2.2 A for both inductors
Simulated RMS winding current	$I_{LB(RMS)}$ = 1.15A	$I_{LB(RMS)}$=1.35A, $I_{L1(RMS)}$=0.7A
Core selection (Phillips – 3F3)	E34/14/9 – 5.15cm^3/13g	L_B: E25/16/6 – 2.84cm^3/7.1g L_1: E20/10/6 – 1.49cm^3/3.7g
Core volume (cm^3) / weight (g)	5.15cm^3/13g	Total: 4.3cm^3/10.8g



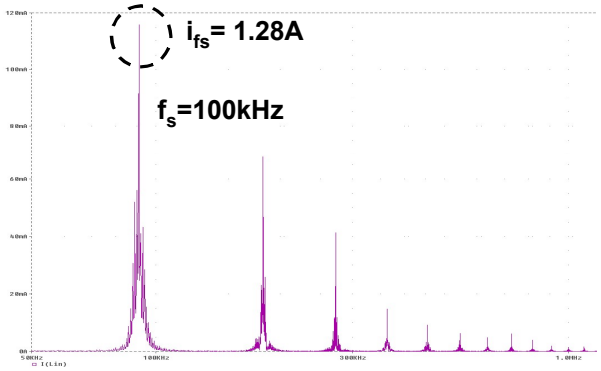
(a) i_{LB} waveform of CS S^2PFC @ v_{in}=90 V



(b) i_{LB} spectrum of CS S^2PFC @ v_{in}=90 V

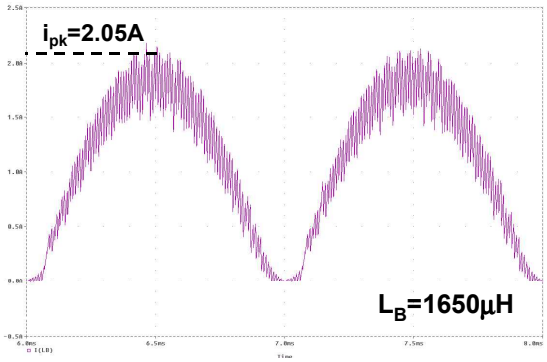


(c) i_{LB} waveform of CS S^2PFC @ v_{in}=265 V

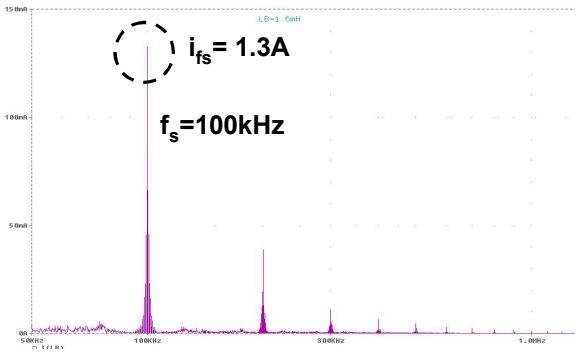


(d) i_{LB} spectrum of CS S^2PFC @ v_{in}=265 V

Figure 5.15 Boost inductor current waveforms and its spectrum of the CS S^2PFC (f_S=100kHz, P_o=100W)



(a) i_{LB} waveform of CCM Boost PFC (V_{in}=90V)



(d) i_{LB} spectrum of CCM boost PFC (v_{in}=90 V)

Figure 5.16 Boost inductor current waveform and its spectrum of the CCM boost PFC (f_S=100kHz, P_o=100W)

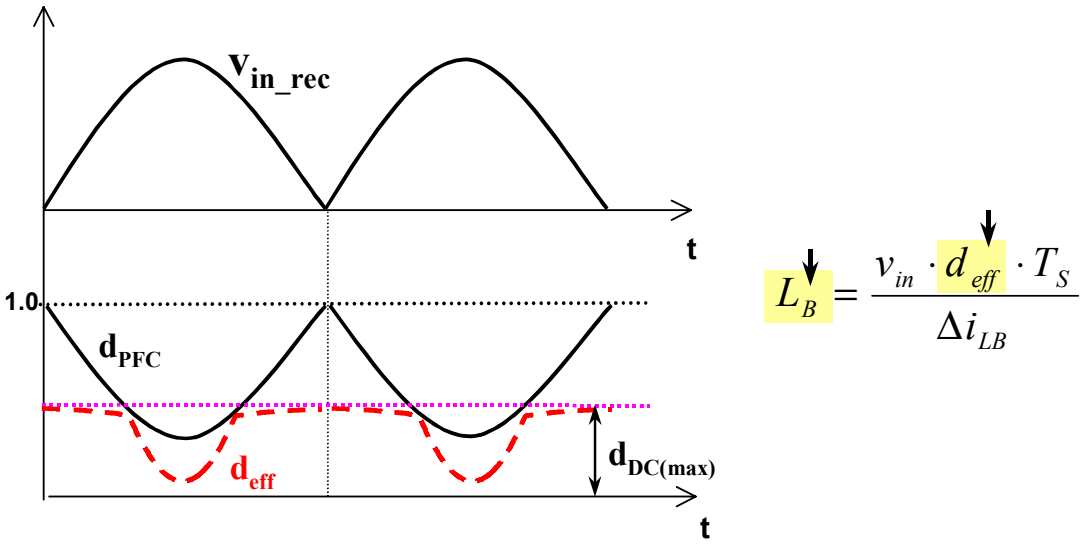


Figure 5.17 Conceptual duty-cycle waveforms show that the CS S^2PFC converter has smaller duty-cycle on the boost inductor L_B

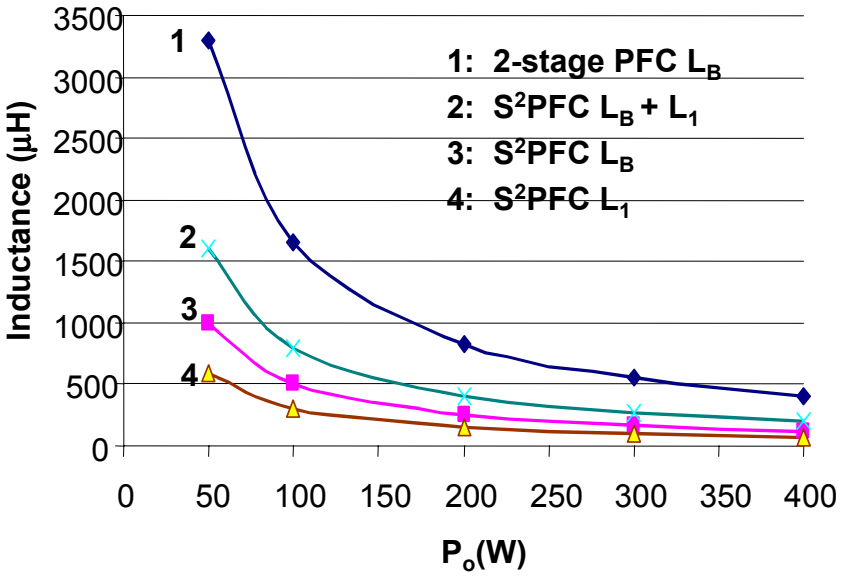


Figure 5.18 PFC inductance vs. output power (f_S=100kHz)

5.3.3.2) Output filter inductor

To compare the output inductors, it was assumed that the inductor-current ripples are the same; i.e., the peak currents through the output filter inductors in both cases are the same. However, because the energy-storage-capacitor voltage V_B varies in a wide range in the single-stage PFC converter, the switch duty cycle changes with the line changes. As a result, the single-stage PFC converter requires a larger output inductance than the two-stage PFC converter, as shown in Fig. 5.19.

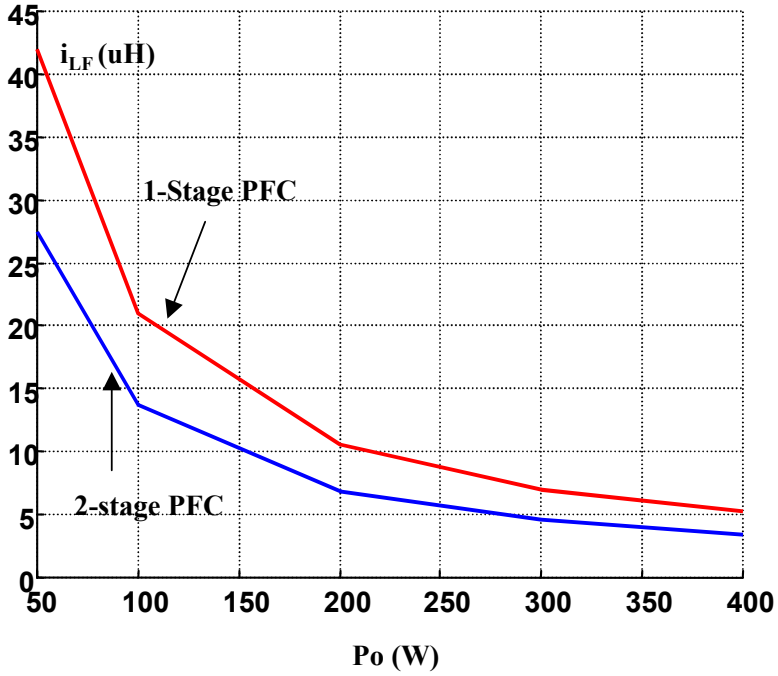


Figure 5.19 Output filter inductance vs. output power

5.3.4) Conclusions

Finally, Table 5.2 summarizes the comparison results between the single-stage and two-stage converter at P_O=100 W and t_{hold}= 10 ms.

Table 5.2. Comparison between two-stage and single-stage PFC converters at P_O=100 W (5V/20A) and for t_{hold}=10 ms.

	Two-Stage PFC	**1-Stage PFC**
Reset Circuit	RCD Clamp Reset	Active Clamp Reset
Forward Switch Duty Cycle	D_{oper} = 0.45, D_{max} =0.60	D_{90V} = 0.49 D_{265V} = 0.16, D_{max} = 0.7
PFC inductor(s) (assume use Phillips-3F3 core)	L_B=1650µH E34/14/9 5.15cm^3/13g	L_B=500µH, L_1=300µH L_B: E25/16/6, L_1: E20/10/6 Total: 4.3cm^3/10.8g
Bus voltage	V_{min} = 300 V, V_{oper} = 400 V	V_{min} = 90 V,V_{oper} = 130-400 V
Forward Transformer Turns-Ratio N	32.5	11.5
PFC Switch Rating	1.287 A / 400 V	NA
PFC Diode Rating	0.339 A / 400 V	0.544 A/ 400 V
Forward Switch Rating	0.42 A/ 727 V	2.134 A/ 574 V
Output diode rating	11.0 A / 12 V	16.8 A/ 34.9 V
Bus Capacitor	37.8 uF / 450 V	284 uF / 450 V
Output Inductor	13.7 uH / 22 A	21.0 uH / 22 A

According to the above comparisons, the following general conclusion can be obtained:

- Because, for universal-line applications, the S^{2}PFC converter exhibits a wide variation of the energy-storage-capacitor voltage, it requires higher rating components compared to the two-stage PFC converter.
- Although the CS S^{2}PFC converter needs two PFC inductors L_B and L_1, the total inductors' size and weight is lower than the PFC inductor in the two-stage PFC converter

- The total loss in the S^2PFC converter may be higher than in the two-stage PFC converter. Therefore, the efficiency of the single-stage PFC circuit may be lower than that of the two-stage PFC circuit.
- The S^2PFC converter reduces the number of components by eliminating a need for the PFC switch and control circuit. However, because the S^2PFC converter requires components with higher ratings, the single-stage approach may be attractive for applications at lower power levels (< 100 W) where the component rating difference is not very significant. At lower power levels, the overall cost of the S^2PFC converter still may be lower than that of the two-stage PFC converter. However, for higher power levels, the S^2PFC approach is more attractive.

5.4 SUMMARY

In this chapter, the two-stage PFC and single-stage PFC converters are reviewed, analyzed and compared. The comparison is done with different output power levels. The component values and their voltage and current stress are given in a number of plots to illustrate the difference between these two PFC approaches.

Generally, the S^2PFC converter has a simpler power stage and simpler control circuits. However, due to its wide bulk-capacitor voltage range at universal-line input, the S^2PFC converter requires higher-rated components, especially the energy-storage capacitor for hold-up time. Besides, the S^2PFC converter exhibits a high switch current stress and conduction loss compared with the two-stage PFC converter, which means low efficiency of the S^2PFC converter. The penalties of the S^2PFC converter significantly limit its power level for universal-line application, which is required by most low-power equipment.

In conclusion, only for lower-power, cost-sensitive applications, the single-stage approach may be more attractive. For higher-power applications, the two-stage approach is the best choice. To increase the power limit of the S^2PFC converters, it is very necessary to develop advanced S^2PFC techniques with improved performance for universal-line applications.