CHAPTER II

Process Development for Solder Joints on Power Chips

Solder-joint failure is a serious reliability concern in flip-chip and ball grid array packages. In current industrial practice, the solder joints take on the shape of a spherical segment. Mathematical calculations and finite element modeling have shown that hourglass-shaped solder joints would have the lowest plastic strain during a temperature cycle, thus the longest lifetime. In an effort to improve solder joint reliability, we have developed a stacked solder bumping technique for fabricating high standoff triple-stacked hourglass/column-shaped solder joints. This solder bumping technology can easily control the solder joint shape and height. The structure of triple-stacked solder joints consists of an inner cap, middle ball and outer cap. The triple-stacked solder joints are expected to have greater compliance than conventional solder joints and are able to relax the stresses caused by the coefficient of thermal expansion (CTE) mismatching between the silicon chips and substrates since it has a greater height. Furthermore, the hourglass-shaped solder joints are to have a much lower stress/strain concentration at the interface between the solder bump and the silicon die as well as at the interface between the solder bump and substrate than barrel-shaped solder joints, especially around the corners of the interfaces. In this chapter, solder joint structures and their corresponding fabrication processes are designed and described.

2.1 Introduction to Solder Bumping Process

The solder joint interconnection is a metallurgical system that consists of final chip metal pad, under bump metal and solder ball, as illustrated in Figure 2.1. It is very important to understand the solder joint interconnection structure and characteristics since this structure is the key to long-term reliability and shorter-term assembly considerations of a electronic assembly. Not all solder bumps are alike and the choice of bump material and construction can affect fabrication process as well as overall reliability. The metallurgy of the final metal which defines the circuit bond pad (aluminum or gold) and the chosen solder type for a given manufacturing process (i.e. eutectic Pb/Sn solder pastes) are typically distinct and not compatible. The under-bump-metallurgy (UBM) or ball limiting metallurgy (BLM) is the important element of solder

joint interconnection that reliably joins these two metallurgies. Therefore, a UBM should provide the following features or capabilities:

- Good adhesion to the wafer passivation,
- Good adhesion to the IC final metal pad,
- Protection of the IC final metal from the environment,
- Low resistance between IC final metal and solder bump,
- An effective solder diffusion barrier,
- Asolder wettable metal of appropriate thickness,
- Ability to be used on probed wafers.

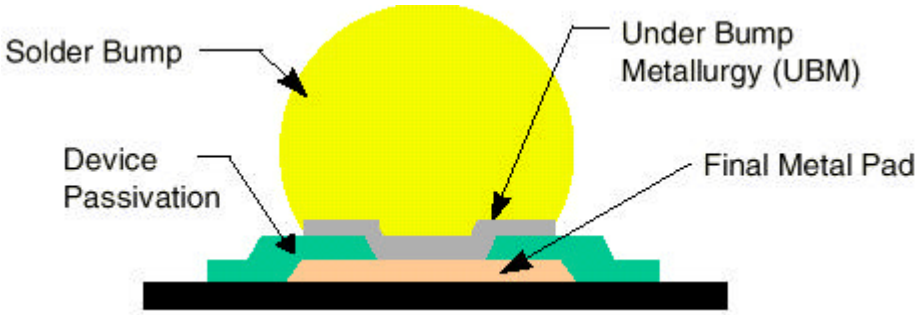


Figure 2.1. Schematic of a solder joint showing the final metal, under-bump-metallurgy and solder ball. These three metals must be joined, forming a single metallurgical system [1].

Solder ball is connected to a substrate and it is the path for the chip to communicate with the outside world. Figure 2.2 shows a scanning electron micrograph (SEM) of a eutectic Pb/Sn solder bump positioned on the aluminum bond pad. The ideal solder joint will provide a controlled collapse of the bump upon assembly. A collapsible bump increases the assembly process window by accommodating less than planar boards and by being able to self align on the circuit board pad even if it has not been completely centered.

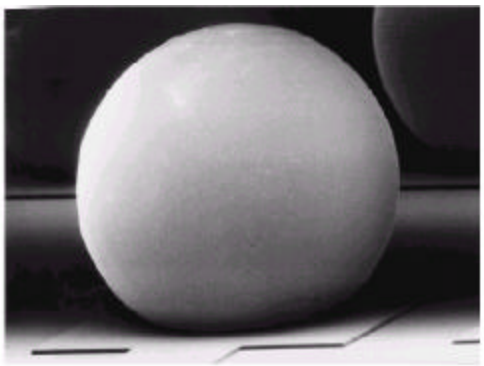


Figure 2.2. Scanning electron micrograph of a eutectic solder bump on a silicon IC [1].

Solder bumping is the heart of solder-bumped flip chip technology. There are many different ways to form solder joint on chip pads. Several popular solder bump deposition processes will be briefly reviewed in terms of their respective manufacturing processes. The deposition techniques are:

- Evaporated solder bump formation,
- Printed solder bump formation,
- Electroplated solder bump formation,
- Stud Bump Bonding,
- Electroless nickel under bump metallurgy paired with either printed solder bumps or conductive adhesives,
- Microball mounting,
- Tacky dots.

Some other less common methods, such as solder jet printing [2-3], fly-through solder jet printing [4], micropunching [5] were developed by some companies.

2.1.1 Evaporated Solder Bumping Technology

Evaporation of solder bump is quite mature. It can provide solder bumps with the best uniformity in composition and volume. The formation of the UBM and solder bump by evaporation, as practiced by IBM, is known as the "C4" process. C4 stands for Controlled Collapse Chip Connection. Utilizing a ductile material such as lead (95Pb/Sn or 97Pb/Sn), a compliant bump can be created for use on ceramic circuit boards. The collapsibility of the high lead bump allows for a compliant and reliable structure. The evaporation method also provides for excellent alloy control. This becomes important during the assembly process when all bumps must reflow during the same time and temperature window.

Process flow includes an in-situ sputter clean to remove oxides or photoresist prior to metal deposition. The cleaning also serves to roughen the wafer passivation and surface of the bond pad in order to promote better adhesion of the UBM. A metal mask is used to pattern the wafer for UBM and bump deposition. The metal mask is usually made of molybdenum, whose CTE is very close to that of silicon. Also molybdenum has excellent long-term dimensional stability at high temperatures. The assembly must be manually aligned and clamped to the wafer. The sequential evaporation of a chromium layer, a phased chromium/copper layer, a

copper layer and a Au layer are deposited to form a thin film UBM. Lead-tin solder is then evaporated on top of the UBM to form a thick layer. It should be noted that because the evaporation rate of Pb is higher than that of Sn, this method id usually applied to high Pb solder bumps such as Pb95Sn5, Pb97Sn3. The height of the bump is determined by the volume of the evaporated material that is deposited. This is also a function of the distance between the metal mask and the wafer, as well as the size of the mask opening. The deposited solder is conical in shape, due to the way that the solder is formed in the openings of the solder mask. The solder can be reflowed to form a sphere. Figure 2.3 shows the process steps described here. Evaporation bumping is a dry solder buildup process.

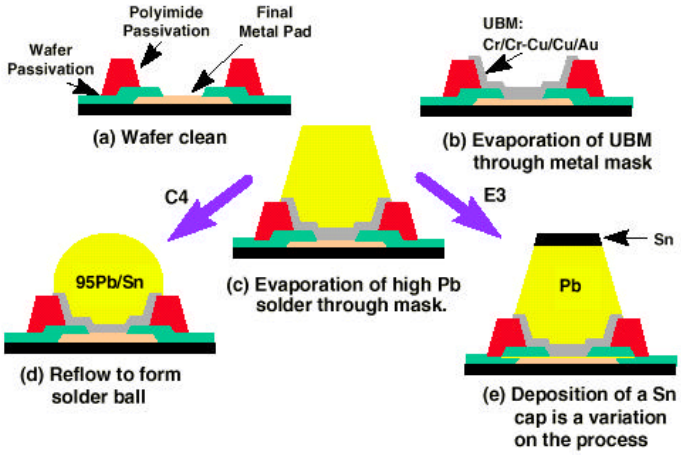


Figure 2.3. Evaporative Solder Bumping Process [1].

The high lead bump reflows at a temperature above 300°C and is, therefore, not suitable for use on those substrates which can not tolerate such high temperatures. This type of bump would act as a dry solder joint. It would be coupled with a eutectic solder which would be printed onto the circuit board. Figure 2.4 illustrates this concept. The drawback of this approach is that, because the high lead bump can not be fully reflowed, full bump collapsibility is lost. This will impact both solder joint reliability and placement tolerances.

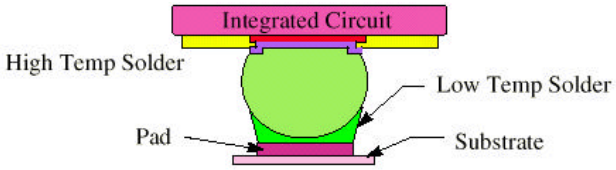


Figure 2.4. High temperature solder joined to non-ceramic substrate [1].

Note the extra layer of tin at the top of the lead bump shown in Figure 2.4. This process was introduced by Motorola and is called “Evaporated, Extended Eutectic”, abbreviated as “E3”.

E3 creates a bump with a mostly “pure” Pb column and a small amount of pure Sn at the top. This tin “cap” allows the device to be “attached to organic boards without the need for intermediate eutectic deposits on the board” [6]. The tin layer allows the assembler to heat the structure well below the melting point of the 95Pb/Sn solder. The goal of this procedure is to form a Pb/Sn eutectic at the tip of the solder ball, allowing the device to be placed on the board without incurring the added costs of applying eutectic solder onto the board itself.

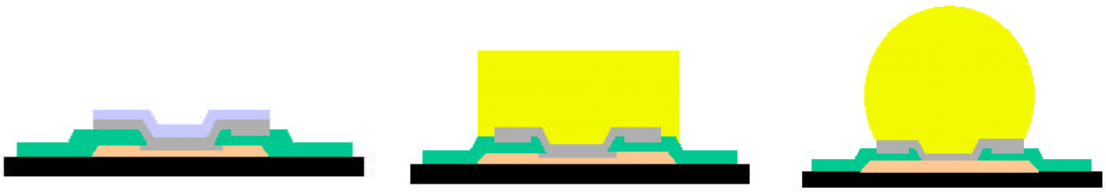
Although a tin cap can be deposited on a high lead bump in order to obtain a quasi-eutectic solder alloy at the top of the bump, this approach still presents several problems:

- The evaporative cost structure does not change significantly.
- Since most of the Pb bump will not be reflowed, the special “controlled collapse” feature of the bump is not taken advantage of. Therefore, the structure will be more sensitive to planarization issues. Similarly, the bump will not self-center, necessitating much more accurate placement tolerances.
- Ahigh contact pressure (9 -15 grams/bump) is needed during assembly of these devices.
- The Sn cap must wet to the board before the Sn goes into sol ution with the Pb. This represents a smaller process window for a successful operation.

2.1.2 Printed Solder Paste Bump Technology

The formation of the solder bump by either stencil or screen printing solder paste is practiced in many forms. Printing is less expensive than the evaporative wafer bumping processes and competitive with plated bumping costs and it is welcomed by system manufacturers since stencil printing of solder paste is one of their most important steps in surface mount technology.

First, UBM system can be sputtered or electroless plated on Al pads. Normally, Ni/Au or Ni/Cu is used as UBM system in printing method. The Ni layer serves two functions: it is an excellent solder diffusion barrier (especially for 63Sn/Pb solders) and it provides a solder wettable surface after the Au or Cu is consumed. Solder paste is then printed onto the UBM using either screen or stencil, and the bump is reflowed to form a sphere. Figure 2.5 illustrates this process. Figure 2.6 shows the SEM photos of printed solder bumping steps and Figure 2.7 shows reflowed solder bumps on wafer made by printing method.



(a) UBM formation; (b) Print solder paste; (c) Solder reflow.

Figure 2.5. Solder bumping by printing solder paste.

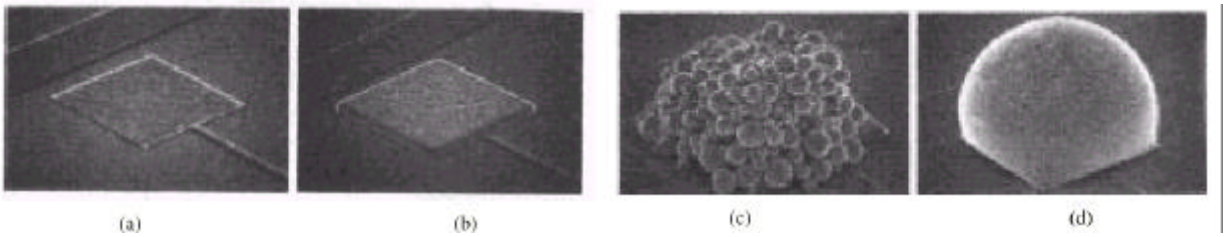


Figure 2.6. SEM photos of wafer bumping by stencil printing method. (a) Al pad; (b) Ni-Au UBM; (c) Solder paste; (d) reflowed bump [7].

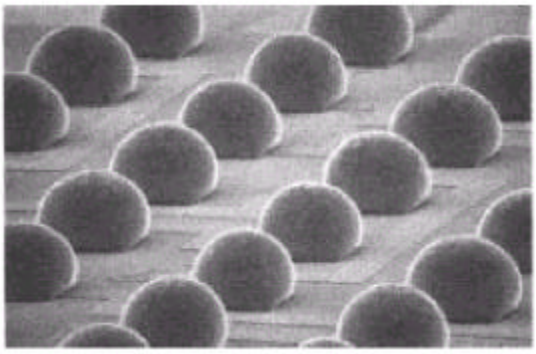


Figure 2.7. Solder bumps on wafer [7].

Several factors, such as operator, environment, printing parameter, printer, stencil, squeegee, and solder paste, influence the quality of solder paste printing on chip pads. The structure of the bump and the type of alloy used ensures a predictive amount of solder bump collapse. Depending upon solder alloy, size of bump, and substrate attachment geometry, the deposited solder bump can experience a 10-30% collapse upon assembly. This feature provides for robust assembly processes with high yields.

The solder paste processing allows for excellent metallurgical control. A direct result of this material control is that assembly reflow temperatures are always predictable and consistent. In addition, solder paste deposition allows for a variety of solder alloys to be used. Non-binary solders are a marked benefit to this type of wafer bumping process since they can be used to

generate lead free materials as well as solders with specific reflow temperatures that a customer may be require.

2.1.3 Electroplated Solder Bump Technology

Electroplating is another popular alternative to the evaporation process because of its lower equipment costs, facility and floor space requirements, and costs of processing.

There are several plating processes available. The traditional plating process for solder bump formation was adopted from the evaporated process and uses a Cr/Cr-Cu/Cu UBM with a high lead solder (only 3-5% Sn content). However, if a tin rich solder is required, such as with a eutectic 63Sn/Pb alloy, then the Sn will consume the Cu in the UBM, quickly degrading the integrity of the structure.

Therefore, one of the more accepted processes used for 63Sn/Pb solders involves the formation of a UBM by the deposition of an adhesion layer such as titanium/tungsten (TiW) followed by a thicker layer of copper (Cu). This thick copper layer is sometimes called a "minibump" or "stud". Because TiW is not a solder wettable metallurgy, the copper is used to allow the 63Sn/Pb alloy to wet to the UBM. However, since the solder has a high Sn content, one must be aware that the Sn will continue to consume the Cu, accelerating intermetallic formation over the life of the device.

The process flow follows: The wafer is cleaned to remove oxides or organic residue prior to metal deposition. As in the previous approaches, the cleaning roughens the wafer passivation and bond pad surface to promote better adhesion of the UBM. TiW, Cu and Au are sequentially sputtered or evaporated over the entire wafer. The UBM adheres to the wafer passivation as well as to the bond pads. Theoretically, the UBM layer will provide an even current distribution to facilitate uniform plating. For the creation of the minibump structure, the copper layer is plated over the bond pad to a height as determined by the patterned photoresist. Either a one mask process or a two mask process can be used. In a single mask process, the solder will then be electroplated on top of the copper minibump until it reaches the top of the mask. The two mask process is depicted in Figure 2.8. Electroplating is done by applying a static or pulsed current through the plating bath with the wafer as cathode. In order to plate enough solder to achieve a reasonable solder ball height, solder is plated over the photoresist coating to form a mushroom shape. The photoresist is stripped after the bump is formed, leaving

the UBM exposed on the wafer. The UBM is removed in one of two ways. In the first approach, a wet etch is used and the UBM is removed from the wafer with some undercutting around the bump. The solder is then reflowed into a sphere. In the second approach, the solder bumps are first reflowed, with the aim that any intermetallics formed within the bump structure will protect the bump by minimizing undercutting during the subsequent etching process.

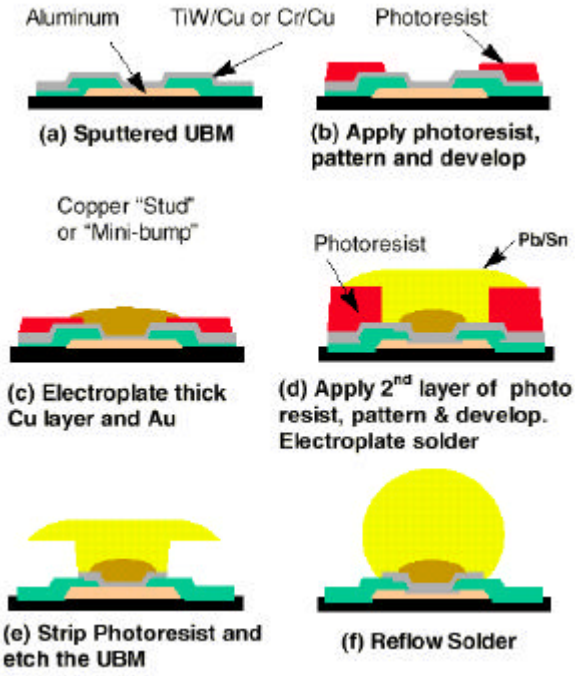


Figure 2.8. Electroplated UBM w/Mini Bump and Solder [8].

Electroplating is typically less expensive than evaporated wafer bumping. However, excessive variations in bump height uniformity and alloy control are the drawbacks of plating solder approach. Usually, due to the applied electrical current at the boundary of the wafer, i.e., current density variations across the wafer during the electroplating process, solder bumps near the edge of the wafer are taller then those near the center of the wafer. It is also non-trivial to scale this process to meet the requirements of larger wafer sizes. Additional issues involve solder voiding, which is more prevalent in plated bumping technologies. Higher solder voiding is due to the generation and entrapment of hydrogen gas as well as plating solutions within the deposited solder.

2.1.4 Stud Bump Bonding (SBB) Process

Stud bump bonding is a unique method to solder-bump the die without UBM is presented [9-11]. SBB has been used on microprocessors and memory devices. Much of this activity is

done in Japan by companies such as Matsushita and Fujitsu. Figure 2.9 (a) illustrates some of the fundamental motions of the solder bump formation. The movement for bonding is provided by the conventional stud bump bonding machine. After the solder wire is inserted into a ceramic capillary, a solder ball is formed at the tip of the wire by arc discharge in an Ar^+ 10%H2 gas flow introduced by means of two tubes positioned opposite each other. Figure 2.9 (b) shows the solder alloy ball formed by arc discharge. There are significant issues to understand when evaluating this technology. Although SBB can be performed at a rate of eight bumps per second, it is not a batch process and is, therefore, not appropriate for high I/O count devices where the lower throughput would not justify its cost savings. In addition, bumps can not be applied over active circuitry, limiting SBB to peripheral I/O configurations.

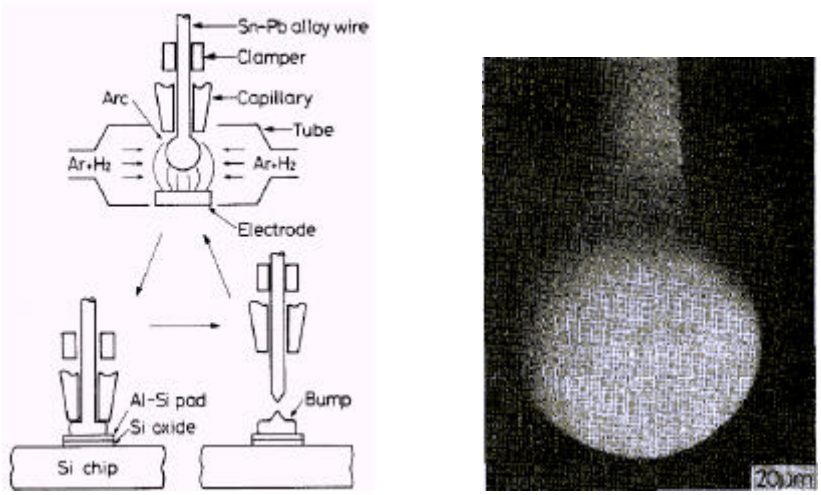
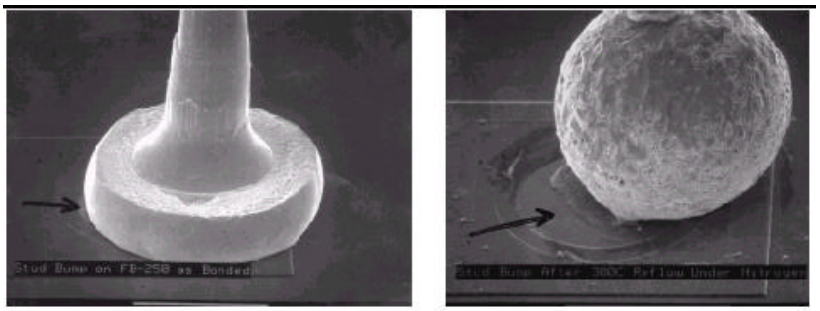


Figure 2.9. (a) Some funamental motions for solder bump formation and (b) SEM photo of the solder alloy ball formed by arc discharge [10].

When used in conjunction with conductive adhesives, stud bumping does not provide the same self-alignment properties found with solder bumps. For pitches of less than 150 μm, a placement accuracy of ≤5 μm is required. This necessitates the use of specialized flip chip assembly equipment rather than more conventional fine pitch SMT assembly equipment. This approach often requires heat and pressure to be applied which can considerably slow the assembly process.

A conventional solder SBB can have difficulty in sustaining a reliable joint during subsequent reflow operations. Figure 2.10 (a) illustrates the stud bump bonded to an aluminum IC pad, and Figure 2.10 (b) shows the solder dewetting from the pad after reflow. However, much research is being conducted in this area. Special solder based wires that can wet directly to

aluminum bond pads have been developed at Tanaka Denshi Kogyo [12] and Tohoku University. These alloys have had mixed success and are still limited in the reflow profiles and reliability results achieved to date.



(a) (b)

Figure 2.10. (a) SEM micrograph of a Sn/Pb SBB; (b) SEM micrograph of stud bump after 300°C reflow in a nitrogen. Solder has dewetted from the Al bond pad [1].

Corrosion of the aluminum bond pad is also a significant issue when using SBB techniques. In order to ensure that (a) the stud bump will not dewet from the Al, or (b) the Al bond pad will not corrode, a UBM can be applied over the Al bond pad. The addition of a UBM, however, will increase the cost of SBB to a point where it would offer neither a technological nor a cost advantage.

2.1.5 Electroless Nickel

Electroless nickel is an under-bump-metallurgy that can be used as a foundation for a solder bump, or as a stand alone minibump that can be used in conjunction with conductive adhesives. The process involves creating a UBM by building up nickel on the aluminum bond pad. The Al bond pad is partially etched and activated by treatment with an alkaline zincate solution. Once the nickel is deposited, a layer of gold is applied over the nickel for oxide prevention. Figure 2.11 illustrates this process.

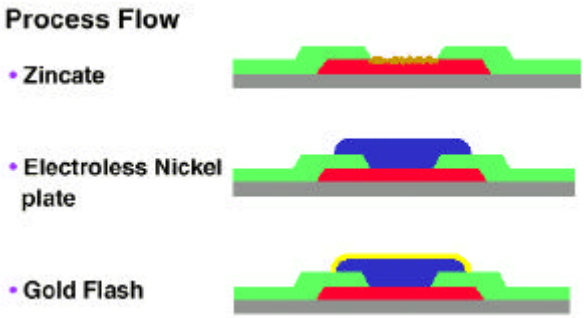


Figure 2.11. Zincation enables the electroless plating of nickel on top of the aluminum bond pad [1].

Electroless nickel technology presents many challenges. For example, since electroless nickel only adheres to the bond pad and not to the passivation, good coverage must be ensured or corrosion can become an issue. The chemical baths must be well understood and controlled to avoid uneven or no plating. In addition, the wafer must be compatible with the process. Except for the Al bond pads, all exposed metal must be passivated. Furthermore, the wafers should not be back ground and should also be free of contaminants. This second issue is especially important since the introduction of foreign material can significantly affect the yield on an entire batch.

Figure 2.12 illustrates the use of an electroless nickel UBM with a conductive adhesive to yield a very low profile attachment. Figure 2.13 shows a cross section of an electroless nickel UBM with eutectic Pb/Sn solder deposited on top.

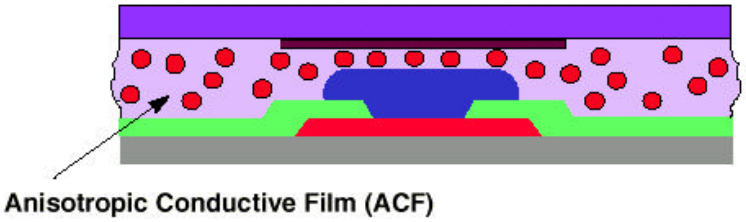


Figure 2.12. Illustration of an electroless nickel UBM assembled to a substrate with conductive adhesive. This produces a very low profile assembly [1].

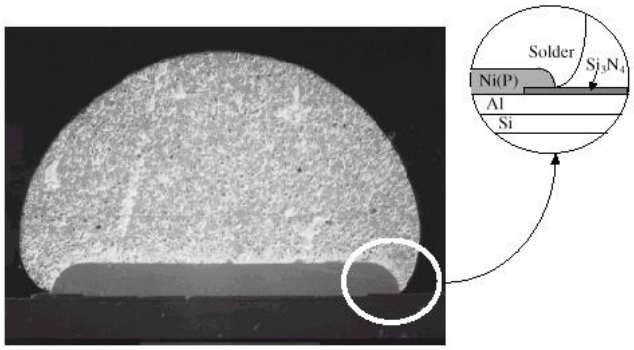


Figure 2.13. Scanning electron micrograph of an electroless nickel UBM with eutectic 63Sn/37Pb solder deposited on top [1].

2.1.6 Microball Mounting

Solder ball mounting on BGA package and CSP substrates has been practiced for several years [13-14]. Ball size range from 10 to 35 mil. In recent years, micro solder balls are becoming available. Micro solder balls are made by melting pieces previously prepared to a constant weight. The extremely uniform diameters and high sphericity are achieved by

controlling the weight of the pieces precisely and by using the surface tension of the molten metals. Micro solder balls can be made for any solder composition, such as ternary, lead-free, and eutectic solder alloys. Figure 2.14 shows ball size distribution of micro solder balls 100 μm in diameter.

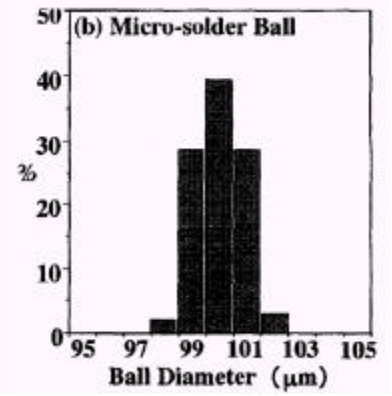


Figure 2.14. Ball size distribution of micro solder balls 100 μm in diameter [13].

The process of assembling the micro solder balls on a chip or wafer is shown in Figure 2.15. It can be seen that the micro solder balls are sucked onto through-holes in the arrangement plate by reducing the pressure on the other side of the plate. The through-holes are located at positions corresponding to those of the pads of the individual chip or wafer. It is possible to form bumps on a variety of chips or wafers by selecting this arrangement plate fixed on the bonding head. These arranged balls are transferred to the pads on the chip or wafer in order to form the solder bumps. A micro solder ball mounter has been developed and it is illustrated in Figure 2.16. Figure 2.17 shows SEM picture of area-arrayed micro solder balls.

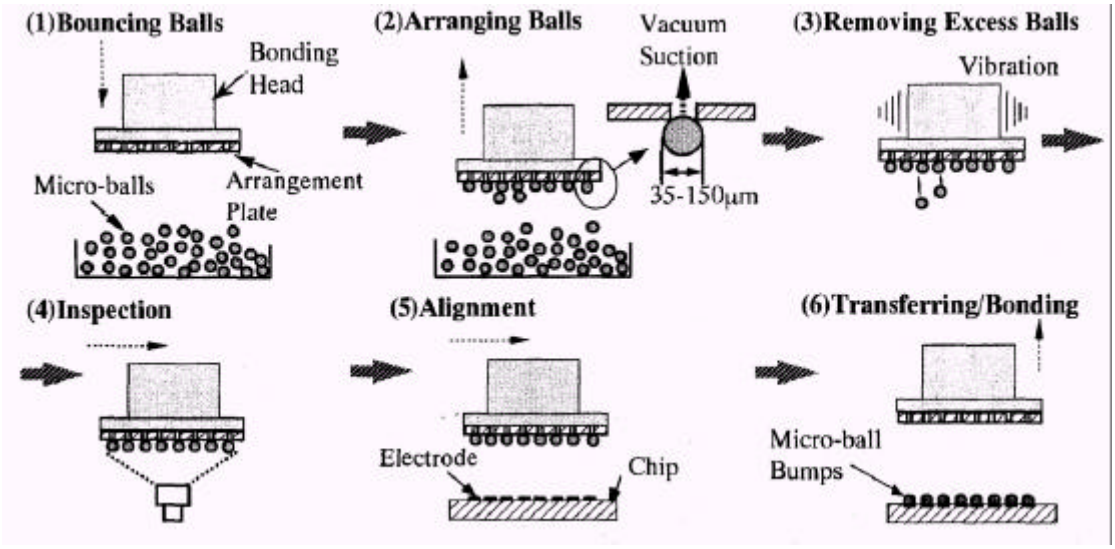


Figure 2.15. Flow chart of the microball arranging and transferring process [13].

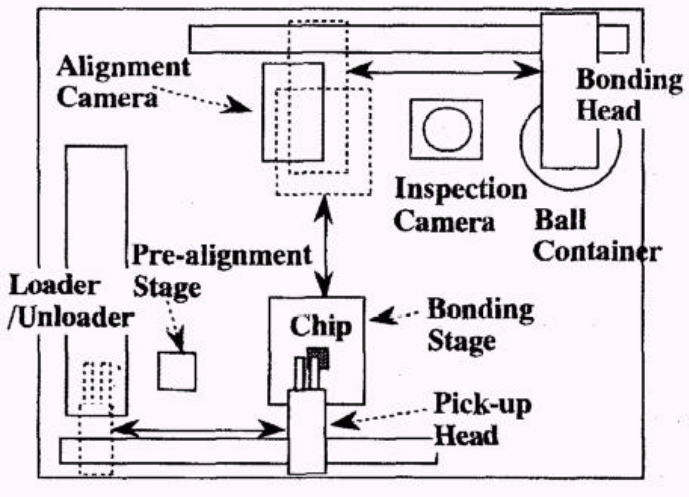


Figure 2.16. Schematic diagram of microball mounter [13].

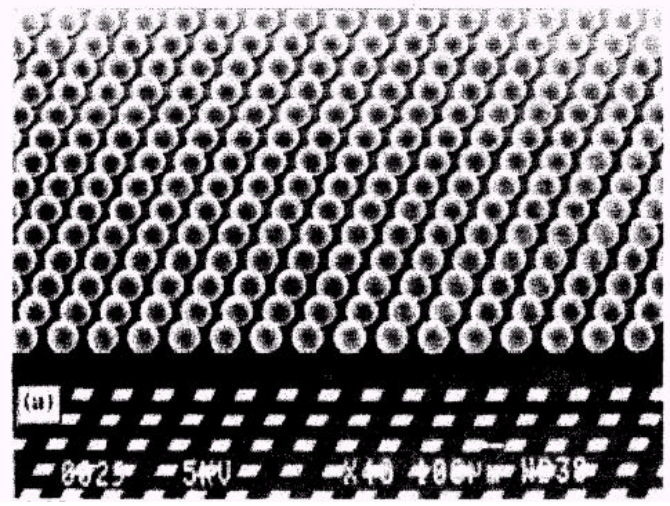


Figure 2.17. SEM image of area-arrayed micro solder balls [14].

2.1.7 Tacky Dots™

The Tacky Dot™ film is a DuPont Invention [15-17] produced by coating a proprietary photopolymer adhesive between a polyimide (Kapton) carrier film and a Mylar cover sheet. Texas Instrument (TI) joined with DuPont to codevelop Tacky Dots. The Tacky Dots assembly flow is shown in Figure 2.18. The Tacky Dot film is imaged using a photo tool and UV light to form a pattern of Tacky Dots. The dot size is customized to hold only one solder sphere per dot. The pattern, populated with the desired solder balls, is aligned with a receiving substrate, such as wafer, and the solder balls are reflowed and transferred as solder bumps. Figure 2.19 shows the once-reflowed Tacky Dots solder bumps and cross section picture.

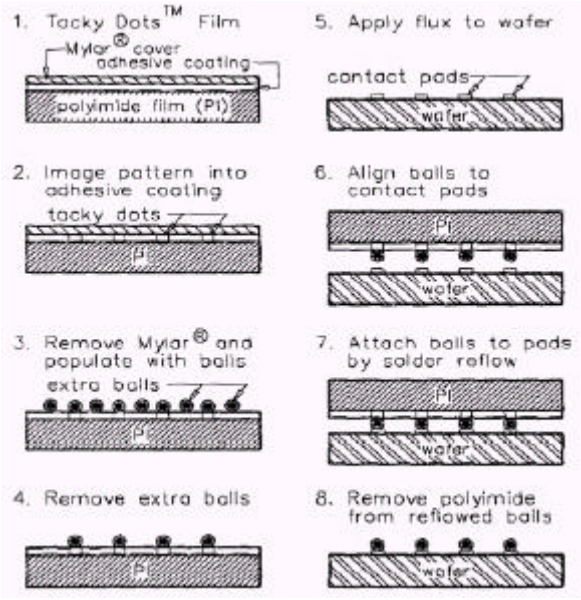


Figure 2.18. Tacky Dots™ assembly flowchart [17].

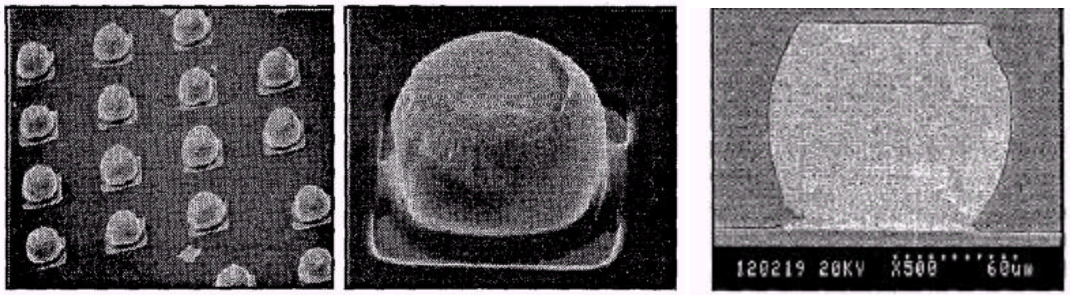


Figure 2.19. Once-reflowed Tacky Dots solder bumps and cross section view [17].

The CTE for Tacky Dot Kapton film is on the order of 12 ppm/°C; that for silicon is about 2.5 ppm/°C. For Sn63Pb37 solder and a 100-mm wafer, the Tacky Dot pattern is shrunk by 0.15 percent, allowing for the growth that will occur in the Kapton film going from 25 to 183°C. Thus, the room temperature alignment of the scaled Tacky Dot pattern is done so that all balls at the same distances from the center are equally off their corresponding targets. As the reflow profile proceeds, the film and wafer heat up and grow linearly with temperature, until at 183°C the patterns match and the transfer take place.

The advantages of this solder bumping process are: Compatibility with any metal alloy or thermoplastic composition; independence from the applied UBM; high throughput; fine pitch; cleanliness; potential low cost and self-centering. One of the challenges is peeling off the Mylar cover sheet from the adhesive layer. This tends to generate a static charge and affects the

handling of the tiny spheres. In addition, an agitated solder sphere bath tends to oxidize the solder sphere surface, which further aggravates the sensitivity toward static.

2.2 Summary of Existing Processing Technologies for Improving Solder Joint Reliability

Solder joint fatigue is the principle failure mechanism of a area array package, such as solder bump flip chip package and BGA package. Thermal stresses caused by CTE mismatch are the main causes of fatigue failure in solder joint interconnections. Numerous factors affect solder joint fatigue performance, such as chip size, joint geometry, interface metallurgy, underfill and substrate. Of these factors, solder joint geometry plays an important role. The solder joints processed by the conventional solder bumping technologies take on the shape of a spherical segment. Several approaches have been taken to increase the standoff height and control the shape of solder bump connection [18-25]. These approaches are reviewed in the following paragraphs.

2.2.1 Stacked Solder-Bump Interconnection

Researchers at NTT Electrical Communications Laboratory have developed a flip chip interconnection using stacked solder bumps supported by polyimide films, which allowed improved reliability of large size chips [18]. In a stacked bump structure, as shown in Figure 2.20, the chip is joined with bumps supported by a polyimide film. Bump-limiting metal pads are used to separate solder bump at different levels. The ball limiting metallurgy consists of two copper layers sandwiching a titanium layer in between, which acts a diffusion barrier layer. This technology is based on the principle that the higher the equivalent bump height is, the smaller is the shear strain obtained. Thermal shock results indicate that the double-stacked solder bumps joining 20×20 mm silicon chips to alumina ceramic boards have sixty times longer lifetime than the conventional un-stacked solder bumps. This interconnection technique can be applied to large size chips since the number of stacks can be easily increased. Moreover, various chips with different thermal expansion coefficients can be mounted on a single substrate, providing high terminal counts, self alignment during joining, high joint strength and excellent electrical properties at very high frequencies.

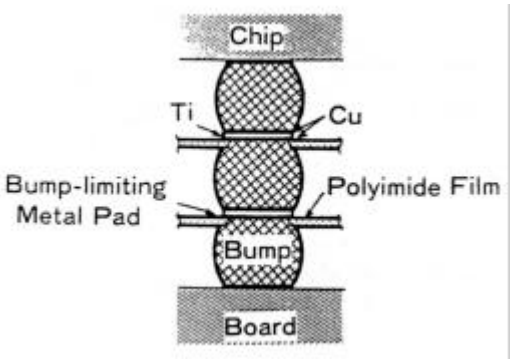


Figure 2.20. Stacked solder-bump interconnection [18]

2.2.2 Double-Bump Technology

AT&T Bell Laboratories developed double-bump technology to improve solder joint reliability [20]. This double-bump technology entails the controlled overlapping of two molten solder bumps on both package and substrate to form a nearly cylindrical joint. A mechanical standoff is used to control the final separation between the IC package and the printed circuit board, and hence the solder joint height and shape. Figure 2.21 shows the double-bump assembly process. This assembly technology offers several advantages. It is an evolutionary development of the well established solder-bump technology, but it provides a column like joint geometry and thus offers potential for better reliability and higher density. It provides a large process window because it allows for the inspection of wettability of package and substrate before assembly, and the assembly process itself involves the melting together of two molten solder surfaces. It offers the potential for the electrical inspection of hidden solder joints.

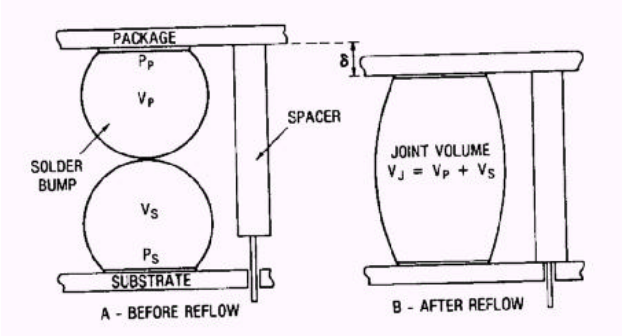


Figure 2.21. Double-bump assembly process [20]

2.2.3 Ceramic Column Grid Array

Ceramic Column Grid Array (CCGA) technology was introduced by IBM several years ago [21-22]. The purpose of the Column Grid Array was to improve reliability of the device

interconnections (as compared to Ball Grid Arrays) by adding height and compliance. There are altogether four types of CCGAs: wire, cast, CLASP (Column Last Attach Solder Process) and recently coated CCGA was developed [21]. Schematic cross sections of these four types of columns are shown in Figure 2.22. In all the processes, wire segments with a nominal composition of Pb90/Sn10 solder alloy and 0.50mm in diameter, are loaded into a graphite mold with an array of holes matching the I/O pad array of the module. Similar in structure to ceramic ball grid array (CBGA), there are wire columns in which the wires of 90Pb/10Sn are attached to the ceramic substrate using eutectic Pb/Sn solder. A drawback with the wire CCGA technology is that during card rework a majority of the columns may be left behind on the card. The columns require manual removal before a new CCGA module can be placed and joined to the card. In the case of cast columns, the wires are cast directly on the substrate by melting Pb10/Sn10 solder columns in a graphite mold and joining them directly to the Ni/Au I/O pad on the substrate. Since the melting point of Pb90-Sn10 solder is 302 °C, these columns have to be attached after chip join, but prior to the remaining bond / assembly processes. In the cast column process, however, the Pb90/Sn10 solder is molten during the attachment process. This results in a high-melt solder fillet bonding the column to the module I/O pads. However, the molten columns expand to fill the approximately 0.57mm diameter holes of the graphite mold. As a result, extraction from these graphite molds is a difficulty experienced in manufacturing cast CCGA modules. In addition, the cast CCGA module, due to its requirement of high temperature attach, goes through more handling during module assembly resulting in more column damage. It is clear that a column last attach process is the preferred process. However, to minimize separation of the columns from the module during module rework from the card, it is desirable to use a higher melting solder interface between the column and the module I/O pad. The CLASP process was developed to accomplish both column attach at the end of the module assembly, and module rework from card with majority of the columns removed with the module. This has been done by adding a small percent of Pd to the Sn/Pb eutectic paste. During the joining of the solder columns to module I/O pads, Pd reacts with Sn to form palladium-tin intermetallics. These intermetallics, which melt around 280°C, add structural support to the CLASP CCGA during card assembly and rework processes. The coated CCGA was developed to use a higher temperature solder alloy than eutectic Sn/Pb solder, and still allow column attach at the end of module assembly to minimize handling of CCGA modules and damage to columns. In the

coated CCGA structure, Sb5/Sn95 alloy, which has a melting point of 235°C, was chosen to attach the solder column to the substrate pad. A Cu-Sn barrier layer is first coated on the Pb90/Sn10 column to prevent reaction between the Sn in the Sn/Sb interface solder and Pb in the solder columns during column attachment, and subsequent assembly and rework of the coated CCGA modules to organic cards or boards. Eutectic solder is used as the card side connection. These structures were typically attached to a ceramic substrate using no-clean flux and the columns could be reworked during module fabrication. Figure 2.23 shows cross sections of wire and cast CCGAs after initial card attach. Fatigue life modeling and thermal cycling tests were performed on these structures to prove their reliability. It was reported that the reliability improvement is on the order of 10X longer fatigue life [22].

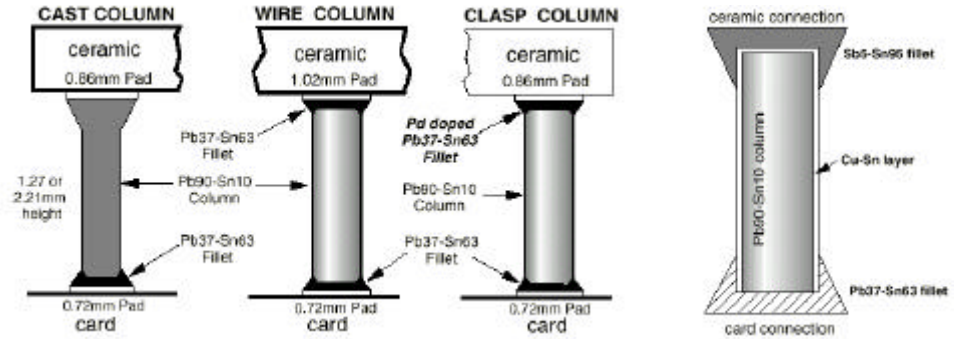
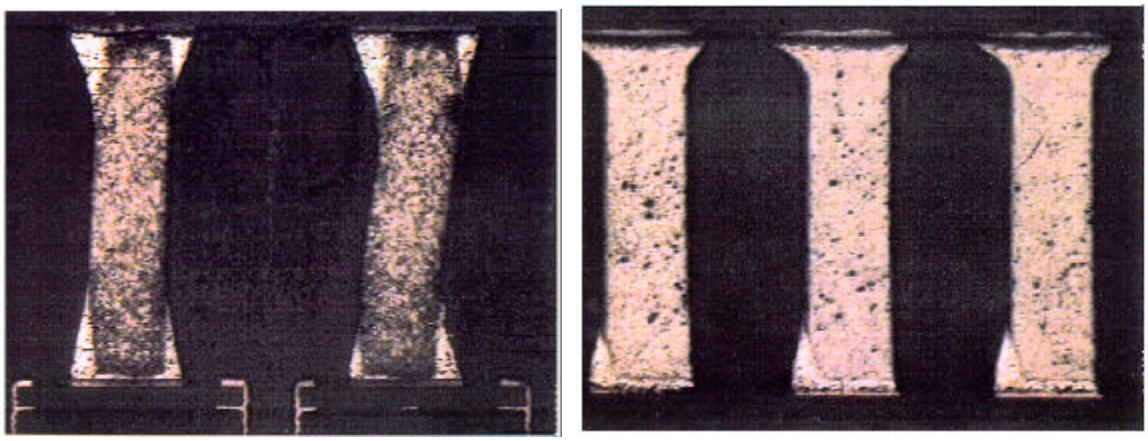


Figure 2.22. Schematic depicting Ceramic Column Grid Array (CCGA) structures assembled to a card [21].



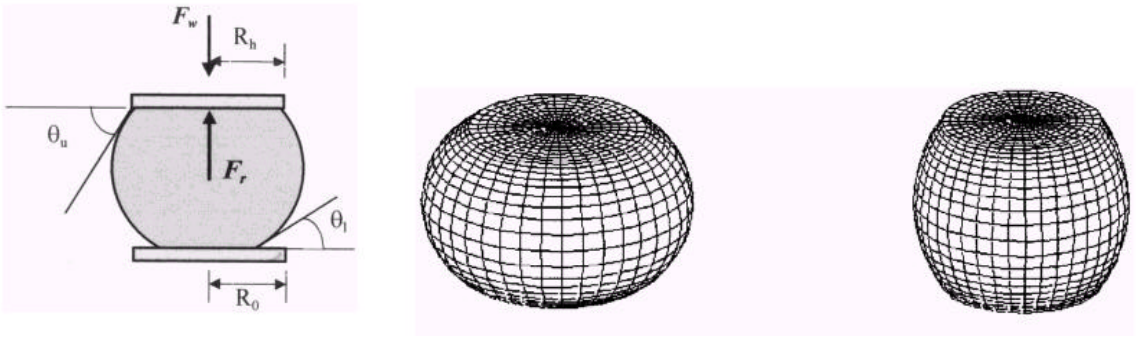
(a) (b)

Figure 2.23. Cross sections of wire (a) and cast (b) CCGAs after initial card attach [23].

2.2.4 Second-Reflow-Process Approach

A second-reflow-process approach was proposed to increase solder joint standoff height and improve contact angle, and thus achieve the reliability enhancement of typical BGA

assemblies, including PBGA and SuperBGA assemblies [19]. The idea is based on the fact that in the first board-level reflow process, each ball in the package is subjected to a compressive loading of package weight. In contrast, in the second reflow process it is subjected to tensile loading of the package weight since the BGA package as well as the board that is mounted are flipped over. Figure 2.24 shows a solder ball subjected to an external load and the solder ball geometry for the first and second reflow. The modeling results show that for a typical PBGA assembly, the ratio of the enhancement by application of the second-reflow-process approach is 2.03 based on the Coffin–Manson criterion and 1.4 based on the energy density based method, and for a typical SuperBGA assembly, it is 7.17 and 2.422, respectively.



(a) (b) (c)

Figure 2.24. (a) Schematic of a solder ball subjected to an external load; (b) First and (c) second reflow geometry of the solder ball in a BGA assembly [19].

2.2.5 S^3-Diepack

Technical University of Berlin with the Europeab ESPRIT project ESCHETA developed a S^3-Diepack wafer-level chip scale package which uses stacked solder spheres with a solder support structure (S^3) to improve board level reliability [25]. In this structure, two layers of solder spheres are used to increase the standoff height. A first layer of solder spheres with a diameter of 300 μm is attached to the Polyimide or BCB redistrubution layer. These solder balls are reinforced by a solder support structure (S^3) using a filled epoxy. This S^3-layer is needed to avoid collapsing of the stacked solder spheres during reflow. A second layer of solder spheres increases the standoff height. A schematic cross section is shown in Figure 2.25 and Figure 2.26 shows the side view of an assembled S^3-Diepack. Due to the stacked solder spheres, a stand-off height of about 0.4 mm is achieved after assembly. 1000 cycles -40 to +100 °C have been

achieved on a thin FR5 board before electrical failure. Over 750 cycles -55 to +125 °C were passed on thick FR4 board.

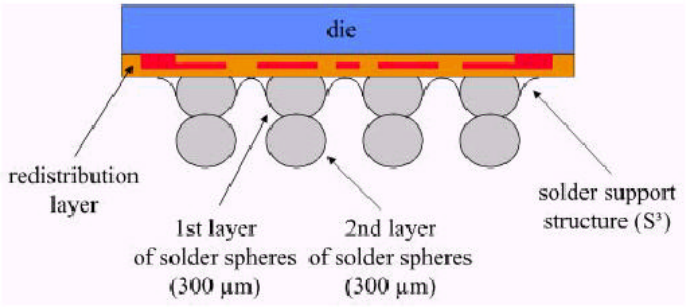


Figure 2.25. Schematic cross section of the S^3-diepack [25].

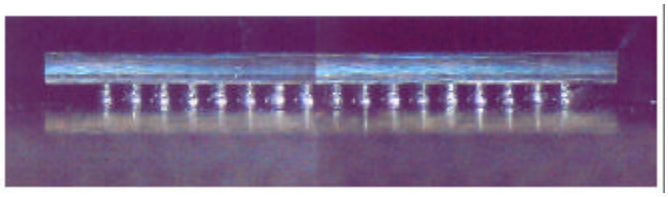


Figure 2.26. Side view of an assembled S³-Diepack [25].

2.2.6 SolderQuik™ Chip Carrier Mounting Device and Column Grid Array

Winslow Automation, Inc. has introduced SolderQuik™ (formerly a Raychem Corporation product line) CCMD (Chip Carrier Mounting Device) and SolderQuik ™ CGA (Column Grid Array), which provides solder columns to surface mount the leadless ceramic chip carriers and land grid array components on to circuit boards, as shown in Figure 2.27 [26-27]. Figure 2.28 illustrates the CCMD assembly process. The columns consist of a copper ribbon wrapped around a high lead core. These columns can be of different heights and pitches for different applications; typically the height of the column varies from 0.05 to 0.1 inch with a typical diameter of 0.022 inch. By using solder columns, stresses are spread over a relatively long solder column, rather than focused on one small area. This defocusing of stress eliminates solder joint fatigue and greatly improves reliability. Due to the innovative construction, the columns are very ductile, which helps them to absorb more stress as well. Furthermore, even if the high lead core cracks completely in half, electrical failure still will not occur immediately, because the copper ribbon serves as an electrical lead. Numerous thermal and power cycling tests have been performed to prove the reliability of the SolderQuik™ CCMD and CGA structures.

Figure 2.27. SolderQuik™ Chip Carrier Mounting Device (CCMD) and Column Grid Array (CGA) [27].

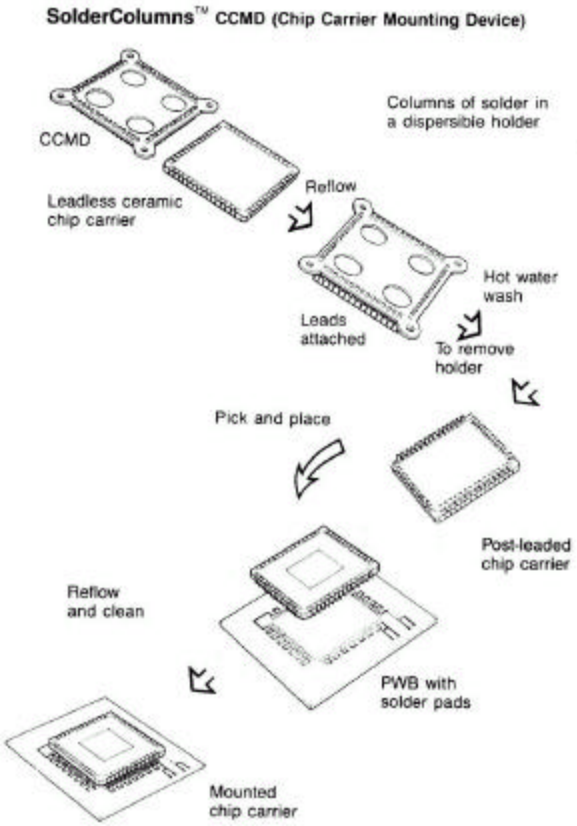


Figure 2.28..Flowchart of chip carrier mounting device assembly process [27].

2.3 Solder Joint Structure Design of This Study

In section 2.2, we reviewed the alternative solder joint process technologies that are intended to improve solder interconnection reliability. However, solder joints made by some of the above reviewed processes still have joint geometries that concentrate stresses and strains at the package and substrate metallization interfaces and require large joint-to-joint separation to obtain reliable joint heights, some of these technologies are not easily implementable in a manufacturing environment and some of them have yet to prove their cost-effectiveness. In this section, we introduce our solder joint structure design.

2.3.1 Solder Joint Structure Design

Thermally induced stresses are the main causes of failure in flip-chip and BGA packages. Local CTE mismatch among the silicon chip, solder bump, underfill encapsulant, and substrate is one of the sources of thermal stresses. The other major thermal stress source is the global CTE mismatch between the silicon chip and the substrate. Global CTE mismatch is the dominant failure source for area array solder joints, thus in this study, we mainly consider global CTE mismatch. Global CTE mismatch causes high shear strain in the solder bump interconnection during thermal cycling. The Coffin-Manson equation [28] is widely used to predict solder bump fatigue lifetime [29-30]

$$N_f = q(\Delta g_p)^{-f}$$

where N_f is the number of cycles to failure; $\Delta\gamma_p$ is plastic strain range and θ and ϕ are material constants. For eutectic solder joints, θ is about 1.3 and ϕ is about 2 [31-32]. The strain imposed on solder joints can be estimated by the following simplified expression,

$$\Delta g = \Delta a \Delta T a / h,$$

where $\Delta\gamma$ is the shear strain imposed, $\Delta\alpha$ is the difference in the coefficients of thermal expansion between the joined materials, ΔT is the temperature change, *a* is the distance from the neutral expansion point of the joined materials, and h is the height of the interconnect. In practice, the above oversimplified expression is not sufficient to calculate the thermal strain [30]. Also Coffin-Manson equation is modified to more accurately predict the solder bump lifetime. However, in modified Coffin-Manson models, the number of cycles to fail is still proportional to $(\Delta\gamma)^{-\phi}$. In order to maximize the fatigue lifetime, we need to minimize the thermal strain. In a packaged module, an optimized solder joint geometry for device interconnection reduces the shear strain. As we can see from the simplified thermal strain expression, the shear strain decreases as the height of the solder bump increases. Thus, one potential approach is to use greater standoff solder interconnects with an aspect ratio much greater than unity [18, 33]. A tall compliant solder joint would enhance the CTE mismatch absorption capability. Figure 2.29 presents a few typical solder bump structures that could be used for solder joint interconnections. For the same solder material volume and same chip and substrate pad sizes, hourglass type solder joint has the greatest standoff height.

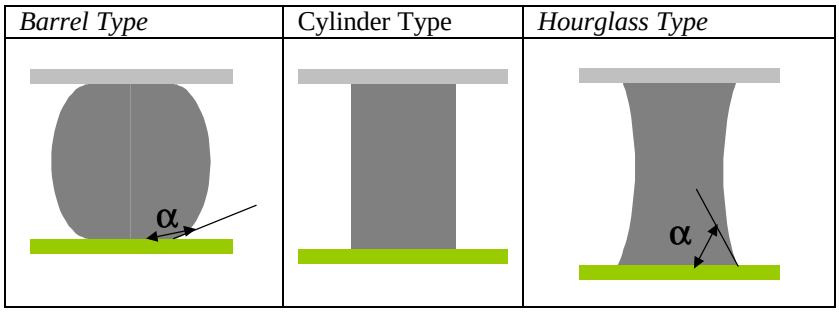


Figure 2.29. Types of common solder joints.

Solder joint shape is another factor that could affect solder joint reliability. Commonly, the flip chip solder bump takes on the shape of a spherical segment. Deviations from the spherical shape can significantly increase (stretched joint) or decrease (squashed joint) the thermal cycle lifetime [34-35]. Mathematical calculations and finite element modeling have shown that the stress-strain behavior in the BGA solder joints is greatly affected by the shape of BGA bumps and a symmetric hourglass-shaped solder bump experiences the lowest plastic strain and has the longest lifetime [36-41]. Generally, solder joint failure occurs first at the interfaces between solder bump and silicon chip, or solder bump and substrate. This is due to the high thermal stress concentration at these adhering interfaces, especially at the corners [29, 39, 41]. It is commonly known that, for fatigue failure, minute cracks start at one or more points that have high localized stress and gradually spread by fracture of the material at the edges of the cracks where the stress is highly concentrated. The stress and strain field near bi-material bonding or contact edges show singular behavior, which can induce a considerably larger stress than the nominal stress. Therefore, it is very important to reduce the stress singularity as much as possible to improve the reliability of solder joints. Among the several common solder joints shown in Figure 2.29, the contact edges of the hourglass type shows the smallest singularity, compared with the other two types of solder joints, as can be qualitatively explained according to the analysis in [42-43]. It is shown in [42-43], as the contact angle increases, the singularity increases and becomes more significant. The smaller contact angle of the hourglass-shaped solder joint structure reduces the order of the singularity. Furthermore, the waisted configuration of the hourglass-shaped solder joint is more compliant and flexible, so stresses imposed at the interfaces between solder bump and silicon chip, and solder bump and substrate are less than those for barrel and cylinder solder joints. As a result, solder bump lifetime and thus the whole assembly lifetime can be much improved by using hourglass shaped solder joints.

Having discussed the effects of solder bump height and shape on reliability, it becomes clear that the optimum solder bump design would be a high standoff hourglass-shaped structure. The solder joints made by conventional solder bump technologies are barrel shaped, concentrating stresses and strains at the chip pad and substrate metallization interfaces and requiring large pitch to obtain reliable joint heights. In an effort to optimize solder bump connection geometry and shape, we have developed a novel stacked solder bumping technology for enhanced reliability of the joints. Figure 2.30 illustrates the detailed structures of conventional solder joints as well as the triple-stacked solder joints. As can be seen from the figures, a structure of triple-stacked solder bumps consists of an inner cap, middle ball and outer cap. The stacked solder bumping technology controls the solder bump geometry and shape easily and offers improvement in solder joint height and shape.

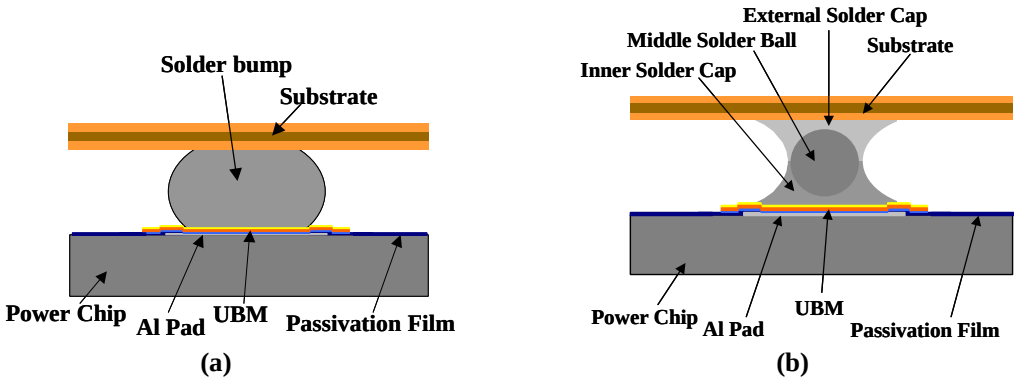


Figure 2.30. (a) Single bump solder joint structure; (b) Triple-stacked high standoff solder joint structure.

2.3.2 Geometry Parameter Determination

In order to use the stacked solder bump structure effectively, we must understand the influence of the major design and process parameters on the shape of joints that can be achieved and the manufacturing margins available when producing them. An adequate understanding of the interrelationship among the principal parameters and their influence on joint shape can be obtained from a first order analysis of a simple geometry model of the solder joints. The principal design parameters included in the analysis are joint height, h, the chip and substrate diameter, d, the radius of the joint at the mid-point, R, the joint volume, V, and the geometry of the joint as represented by a shape factor that we define as the ratio of the diameter of the joint at the mid-point to the diameter of the pads. Thus, a shape factor of unity would correspond to a cylindrical joint, values greater then unity correspond to barrel-shaped joints and values less than

unity correspond to hourglass-shaped joints. Stacked solder bumping technique offers the opportunity of achieving different solder joint shapes according to different design. In literatures, normally solder volume is fixed when the solder joint geometry is designed and different solder joint reliability is analyzed [29-30, 38-39]. In our study, solder volume is also fixed for different solder geometry designs, including single bump solder joint. The total solder volume is determined by stencil thickness, stencil aperture size, the gap between the printed surface and stencil, and middle solder ball volume. In order to keep total volume constant, we used the same stencil, same spacer (to maintain the gap between the printed surface and stencil) and same solder ball volume for all the solder joint structures. Thus, we obtain same solder volume for all the four solder joint structures: Single bump barrel-shaped joint, triple-stacked hourglass-shaped joint, triple-stacked barrel-shaped joint and triple-stacked column-shaped joint, as shown in Figure 2.31.

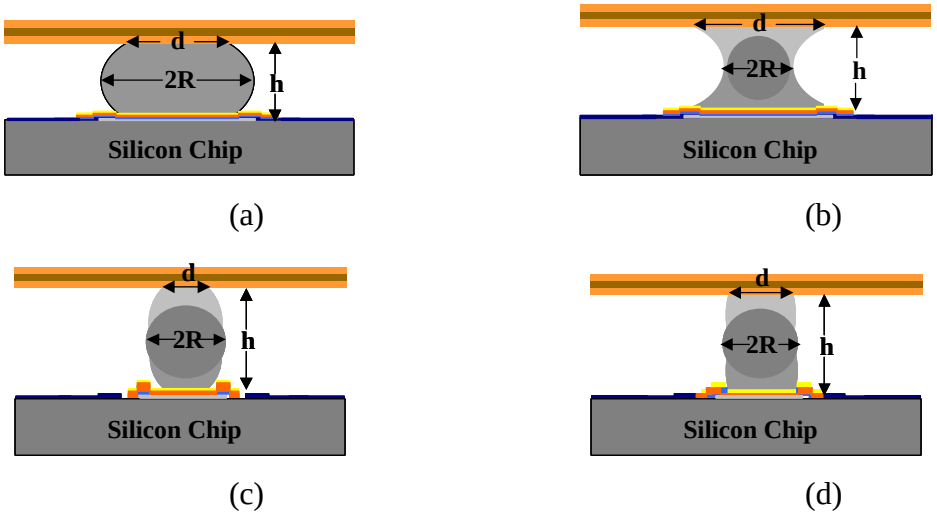


Figure 2.31. Cross section schematics of the dimension parameters of four solder joint structures, (a) Single bump barrel shape; (b) Triple-stacked hourglass shape; (c) Triple-stacked barrel shape; and (d) Triple-stacked column shape.

An analytical truncated sphere model was used to predict conventional solder bump height which has been found to be very consistent with simulation and experimental validation [44-45]. We also adopt the truncated sphere model to characterize single bump barrel-shaped solder joint and calculate the solder volume based on pad diameter, solder joint mid-point radius and bump height as equation 1. This formula is used to guide the design of the parameters.

$$V = \frac{\eth h}{12}(8R^2 + d^2) \qquad \text{Equation 1.}$$

For the triple-stacked hourglass-shaped solder joint, we used hyperboloid of one sheet model as the outside surface of solder joint, which is

$$\frac{x^2}{a^2}+\frac{y^2}{b^2}-\frac{z^2}{c^2}=1 \qquad \text{Equation 2.}$$

we can get the volume of the solder joint based on this model. If the planes normal to z-axis are circular, then a = b=R, which is the case for our triple-stacked hourglass-shaped solder joint. . Equation (2) becomes

$$\frac{x^2+y^2}{R^2}-\frac{z^2}{c^2}=1 \qquad \text{Equation 3.}$$

We can get c in terms of h, R and d. We know the parameter of one point x=d/2, y=0, z=h/2. Thus we can get from equation (3)

$$c=\frac{hR}{\sqrt{d^2-4R^2}} \qquad \text{Equation 4.}$$

If we set $x = \tilde{n}\cos(\grave{e}), y = \tilde{n}\sin(\grave{e})$, Equation (3) can be written as follows

$$\frac{r^2}{R^2}-\frac{z^2}{c^2}=1 \qquad \text{Equation 5.}$$

and

$$r=\sqrt{(1+\frac{z^2}{c^2})R^2} \qquad \text{Equation 6.}$$

The volume enclosed can be expressed as follows

$$\begin{aligned}&\iiint \tilde{n}d\grave{e}d\tilde{n}dz\\ &=\int_0^{2\eth}\left(\int_{-h/2}^{h/2}\left(\int_0^{\sqrt{(1+\frac{z^2}{c^2})R^2}}\tilde{n}d\tilde{n}\right)dz\right)d\grave{e}\\ &=R^2\left(h+\frac{h^3}{12\times c^2}\right)\eth\end{aligned} \qquad \text{Equation 7.}$$

Substituting equation (4) into (7), we have

$$V=R^2h\left(1+\frac{d^2-4R^2}{12R^2}\right)\eth \qquad \text{Equation 8.}$$

This is the relationship among joint height, h, the chip and substrate diameter, d, the radius of the joint at the mid-point, R, the joint volume, V, for triple-stacked hourglass-shaped solder joint. We used this equation to guide our design for triple-stacked hourglass-shaped solder joint.

Truncated ellipsoid model and cylinder model were used for triple-stacked barrel-shaped solder joint and triple-stacked column-shaped solder joint, respectively, which are expressed as

$$V = \frac{\eth h}{15}(8R^2 + 2Rd + \frac{3}{4}d^2) \qquad \text{Equation 9.}$$

$$V = \eth R^2 h \text{ with (2R=d)} \qquad \text{Equation 10.}$$

As we knew, the solder volume of the all the four solder joint structures is the same. The pad sizes of those structures in our design are: d=1.1 mm for both single bump barrel-shaped solder joint and triple-stacked hourglass-shaped solder joint; d=0.7 mm for triple-stacked barrel-shaped solder joint and d=0.9 mm for triple-stacked column-shaped solder joint. We can use equations (1), (8), (9) and (10) to calculate the height and the ratio o those different solder joint structures. Figure 2.32 shows some solder joints fabricated based on the above design.

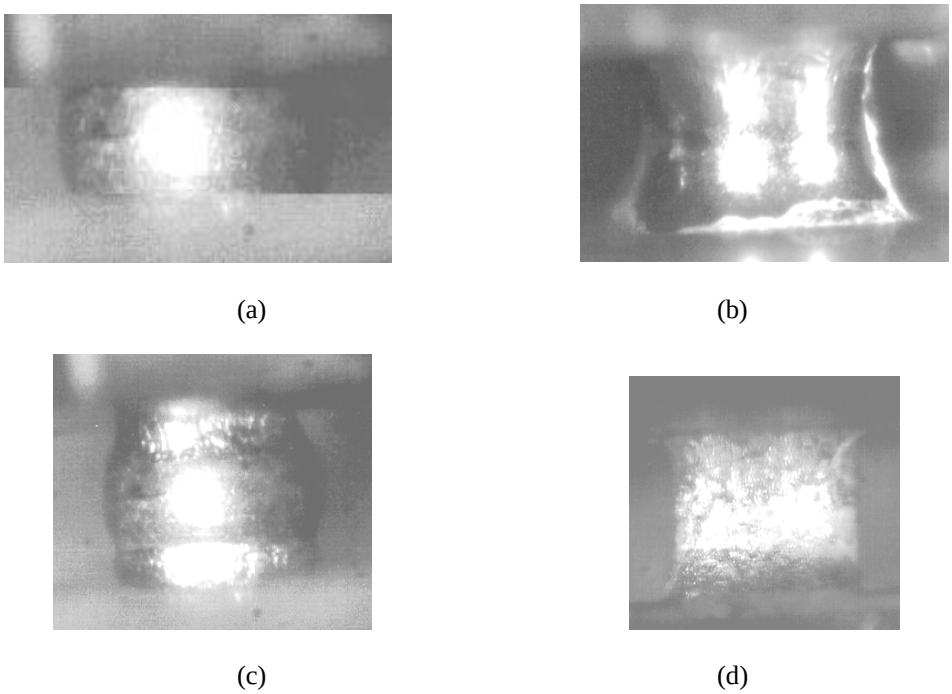


Figure 2.32. Microphotographs of solder joints with different heights and shapes; (a) Single bump barrel-shaped; (b) triple-stacked hourglass-shaped; (c) triple-stacked barrel-shaped; and (d) triple-stacked column-shaped.

2.3.3 Materials Selection

The designed solder joint structure incorporates materials with different properties. It contains silicon power chips, solder joints (single or stacked), underfill material, and substrate. Reliability, and manufacturability are the major issues addressed in the materials selection process. Reliability is related to CTE of materials, flexibility of the substrates and the whole structure. Manufacturability is concerned with the material process conditions, the availability of equipments to process the materials and so on.

Solder paste is the raw material for the solder joints, and its quality and consistency is very important. The paste consists of solder powder and flux vehicle. For stencil printing application, the solder paste selected should be suitable for printing. For wafer bumping applications with stencil aperture widths less than 150 m, solder powder needs to be as small as possible. Fine powder is the most efficient way to reduce fine pitch printing defects (missing, in-sufficient, and bridges). As shown in Figure 2.30, the single bump solder joint is made of one solder material. Thus, there is some freedom to select solder materials. Considering reliability performance and process requirement, eutectic lead-tin solder (Sn63/Pb37) or eutectic silver-tin solder (Sn96.5/Ag3.5) is desired. It was reported that Sn96.5/Ag3.5 solder has better reliability performance than Sn63/Pb37 solder [29-30]. In our research, eutectic lead-tin solder (Sn63/Pb37) is used for the reliability study of the single bump solder joints though in some other cases, eutectic silver-tin solder (Sn96.5/Ag3.5) is also used for demonstration. For the stacked solder joint structures, they consist of inner cap (adjacent to die), middle ball and external cap. The middle ball is Sn10/Pb90 solder, whose melting temperature being 268°C. We select this high-lead, high-temperature solder is due to the temperature hierarchy consideration and manufacture consideration. In our design, we do not want this middle solder ball to be melted at any time during the process. Also this middle ball is critical from reliability point view since this middle neck in hourglass-shaped structure could failure first and it was reported that high-lead solder is more fatigue resistant. Eutectic solder (Sn63/Pb37) with a melting temperature of 183°C is chosen as the external cap to obey the temperature hierarchy and to have low temperature reflow. For the inner cap, there may have different choices of solder composition depending on different application and design. However, the melting temperature of that solder has to be below the melting point of Sn10/Pb90 solder. Also the melting temperature cannot be too low or else it is difficult to select the right solder for the next

level packaging. In our original design of the stacked solder joint for power chip interconnection and applications, we chose eutectic silver-tin (Sn96.5/Ag3.5) alloy with a melting temperature of 221°C as the inner cap material considering that Sn96.5/Ag3.5 has better fatigue performance and its melting temperature is in between the melting points of Sn10/Pb90 and Sn63/Pb37. Thus, in the first solder bumping reflow process, only the inner cap solder melts and the middle ball remains solid, while during the second flip chip bonding relow, only the outer cap solder melts. The other excellent choice of the inner cap solder is eutectic lead-tin, same as outer cap, in this way, the inner cap melts again during the second flip chip bonding reflow. It was reported that there is no degradation of Sn63/Pb37 solder for the second reflow [23, 29]. In our reliability test samples, we used Sn63/Pb37 solder as the inner cap for the purpose of comparing with the reliability results of single bump solder joint and other groups' work. In power module fabrication, we used Sn96.5/Ag3.5 as the inner cap material.

There are three types of stencils available: chemical etch, laser cut, and electroformed. Chemical etch stencils are inexpensive, but dimension limitations and accuracy can not meet the fine pitch application requirements. Electroformed and laser cut stencils provide better fine pitch accuracy than chemical etched stencils. The electroformed stencil uses a parallel build up process, with no added cost for large numbers of apertures, as in the serial-processed laser stencils. For our application, the pitch and accuracy requirement is not very high, thus chemical etched stencils were selected in our process development.

The most widely used substrate is FR4 printed circuit board (PCB). In our research, PCB is used as rigid board in our temperature cycling test to evaluate solder joint fatigue. Flexible substrates are emerging as they find applications a several area due to their cost effectiveness, performance and low volume. The flex substrate used in our research is a double-sided, copper-clad laminate, which is an adhesiveless composite of polyimide film bonded to copper foil. This copper-clad is commercially available. This laminate has excellent handling characteristics for fabrication, outstanding dimensional stability, excellent assembly performance over a wide range of processing temperatures, low thermal expansion coefficient, excellent thermal resistance for high-temperature assembly processes and is compatible with conventional oxide treatments and wet chemical plated-through-hole desmear processes. The thickness of both the polyimide film and copper foil is 2 mil. However, the copper sheet on the power device side is thickened to 5

mil by electroplating to increase current-carrying capacity. After processing, the substrate retains very good bend and crease flexibility.

Underfills are used primarily to improve the reliability of the flip chip interconnection systems. These materials fill the gap between the chip and substrate around the solder joints reducing the thermal stresses imposed on the solder joints. The cure time and temperature of the underfill is a major factor in the selection of an underfill material for a flip chip interconnection system. Since the underfill process follows the flip-chip bonding step, cure temperatures lower than the melting point of the solder joint is necessary. The glass transition temperature of the underfill material should be well above the service temperatures of the module. Other factors, which influence the performance of an underfill, are its CTE, elastic modulus and adhesion to the interconnection system materials. The CTE of the underfill material must match those of the solder joint as closely as possible [29]. High elastic modulus underfill materials are preferred. With an elastic modulus close to that of the solder, the underfill forms a quasi-continuum with the joints, thus reducing the stress rise associated with the sharp contact angle between the solder and the die and substrate [29]. Good adhesion of the underfill material to the substrate and the die generally improves the reliability of the interconnection system. Several underfill materials have been investigated. These materials and relevant properties are listed in Table 2.1 [30, 46-47]. Underfill material D is the preferred material for the structure since this material has lower CTE, high elastic modulus and furthermore it is thermally conductive. It has a T_g of 120°C and it has superior adhesion to Cu foil and the commonly used IC passivation materials, including polyimide. This underfill material is a fast-curing compound, with a cure time of 15 minutes at 150°C.

Table 2.1. Properties of various packaging materials.

Materials	Elastic Modulus (Gpa)	CTE (ppm/°C)	Thermal Conductivity (W/m·K)
Silicon	112	4.1	136
Underfill A	3.6	50	X
Underfill B	3.1	35	X
Underfill C	5	29	X
Underfill D	11	23	3.14
Flex substrate	4.1	20	X
Solder	16	25	51

2.4 Process Development

In the section, we describe the stacked solder bumping technology for fabricating high standoff hourglass-, column- and barrel-shaped solder joints as well as the conventional solder bumping process for fabricating single layer solder joint.

2.4.1 Selection of a Solder Deposition Process

As we introduced in section 2.1, several processes have been demonstrated to deposit solder bumps on a wafer or chip. The choice of one technology over another is influenced primarily by the bump dimensions and pitch, composition, and cost. Evaporation, electroplating and stencil printing are the most popular wafer solder bump processes in production today. Evaporation is high cost, and can not produce eutectic solder bumps due to the Sn and Pb vapor pressure difference. Also, as the size of wafers is increasing, they would require large vacuum chambers which may not be economically feasible. Moreover, an evaporation process can be relatively slow and quality problems may result from damage to the solder bumps in the metal mask removal process with the plugged holes. Electroplating is a relatively low cost option, and the 60 Sn/40 Pb electroplated bump process has been developed. Electroplating requires photoresist steps that add to the cost, and plated bump composition is not easy to control due to differences in Sn and Pb electrochemical behavior. Furthermore, device structures can be extremely sensitive to the electro-chemical baths and as a result, these processes require extreme control to maintain the desired chemical state of the chemical solutions [48]. Additionally, the electroplating process involves a blanket deposition method, which demands an etching process to remove the shorts between pads. Stencil or screen printing of solder paste is a well proven process for surface mount components. Technology advances in solder paste, stencil fabrication, and printing equipment make it possible to print Sn/Pb solder paste onto wafers or chips to form bumps. Figure 2.33 shows the solder deposition process using a stencil printing. Stencil thickness needs to be less than the aperture diameter, which sets a practical limit on the bump diameter. However, the stencil can not be too thin either since the squeegee motion may damage or even break the stencil. In this deposition process, stencil needs to be aligned with the pads on the device, which assures printing accuracy. Normally, power chip pad size is much larger than that of IC chips, and the pitch requirement is not high. Stencil-printing technique has no problems in fulfilling the size and pitch requirements for power chips. Also due to the stacked

solder joint structure design, a combination of stencil printing and microball mounting process is preferred. Therefore, for the solder deposition process, stencil printing is selected.

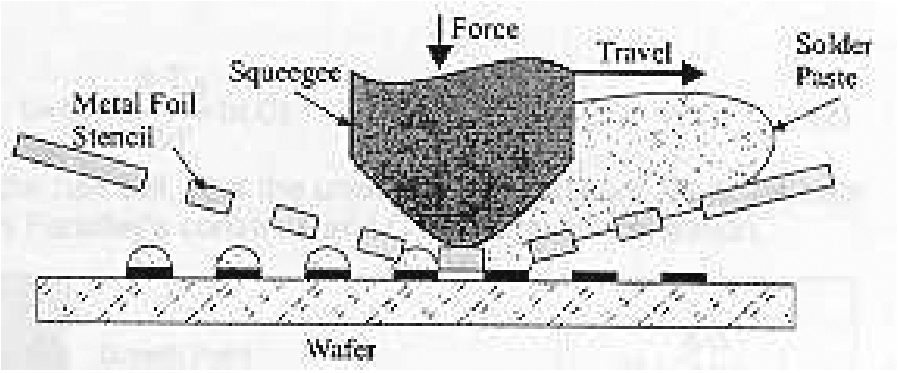


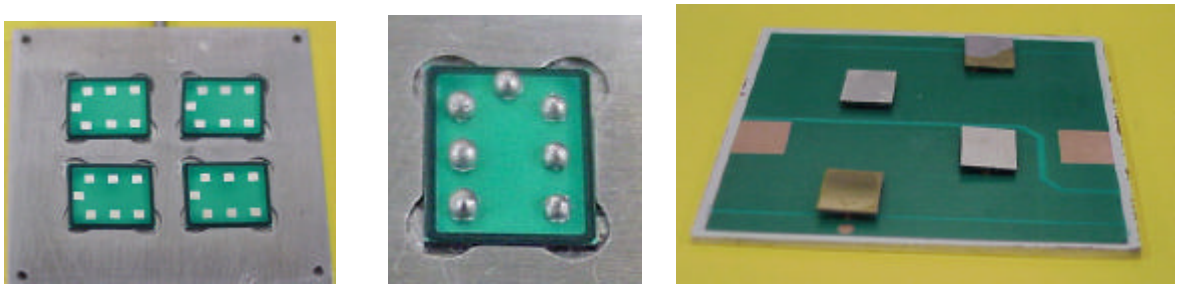
Figure 2.33. Stencil printing process for solder deposition [49].

2.4.2 Process for Single Bump Solder Joint

As we introduced in section 2.1.2, in principal, stencil printed solder bumping process consists of three steps: UBM formation, stencil printing and reflow. In practice, the detailed processes need to be developed for a specific device. The IGBT and diode chips we bought from IXYS were originally solderable for the whole source/anode surface. Thus, we skipped the UBM formation process. The IXYS IGBT and diode UBM is Ti/Ni/Ag. Since we already have solderable chip surface, it is essential to treat the chip surface in order to get ready for the solder bumping process. This treated surface should have the following characteristics:

- Provide solderable surface for solder joints;
- Achieve self-alignment of solder joint during the reflow;
- Have controlled collapse of solder during the reflow process;
- Protect power chip from damage or degradation.

Considering these requirements, we used permanent solder mask to confine the solder joint as well as act as protective coating. Therefore, our whole process step of forming solder joints on power chips would be: solder mask patterning, solder bumping and flip chip bonding. Figure 2.34 shows the solder joint formation process for power chip. For the solder mask patterning process, a photoimagable solder mask was applied on power chip source or anode surface using spin coating. Photolithography allowed definition of openings in the solder mask for all the solder bump pads on power chips.



(a) (b) (c)

Figure 2.34. Process for solder joint formation on power chip; (a) solder mask patterning; (b) solder bumping; and (c) flip chip bonding.

As we mentioned, in this research, we used vender supplied solderable IGBT and diode chips. For diode chips, the whole anode surface is solderable, while for IGBT chips, the gate pad is separated from the six source pads though both parts are solderable. From electrical performance considerations, most of the time we only put seven solder joints on the seven pads of IGBT. As demonstrated in Figure 2.35, actually we can form solder joint arrays of different pitch and size depending on different designs of solder mask and stencil pattern.

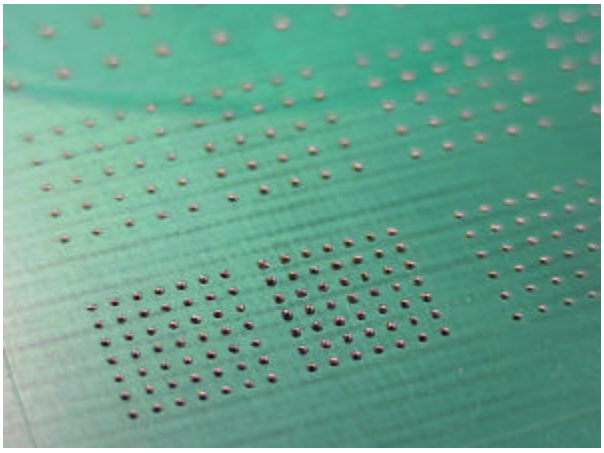


Figure 2.35. Solder joint arrays of different pitch and size.

Figure 2.36 illustrates the solder bumping process. The solder paste is pushed into the holes in the stencil by a squeegee and solder paste makes contact with the bond pads on the chip. Stencil printing is a dynamic and multifactor process. A stencil with apertures is mounted on the printer frame. A wafer/chip is placed on the substrate, and after vision alignment, a squeegee travels at a certain pressure and speed to push the solder paste through the stencil apertures. A gap may be maintained between the stencil bottom and the substrate top during print. The squeegee may be set to force itself a certain distance into the apertures during printing. Solder

paste is transferred to the chip pads while the stencil is retracted. Finally, reflow is conducted and solder paste forms metallurgical bonds with under bump mental. Solder bumps were cleaned to remove solder flux residues. The whole process consists of solder paste transport, transfer, and transformation. For solder bumping process, some important parameters are solder paste, stencil, and hardware and process parameters associated with the printer. Deposition of a uniform solder volume, without misalignment, bridging, or missing bumps, is the desired output. Solder deposit uniformity is closely related to the solder paste used and the print process parameters. The solder deposit volume depends mainly on the stencil aperture size and thickness. In order to reduce oxidation of the surfaces and minimize voids contents in the interfaces, the reflow operation is performed in a reducing atmosphere of nitrogen-hydrogen. In Figure 2.36 we show the microphotograph of fabricated solder bump on IGBT device.

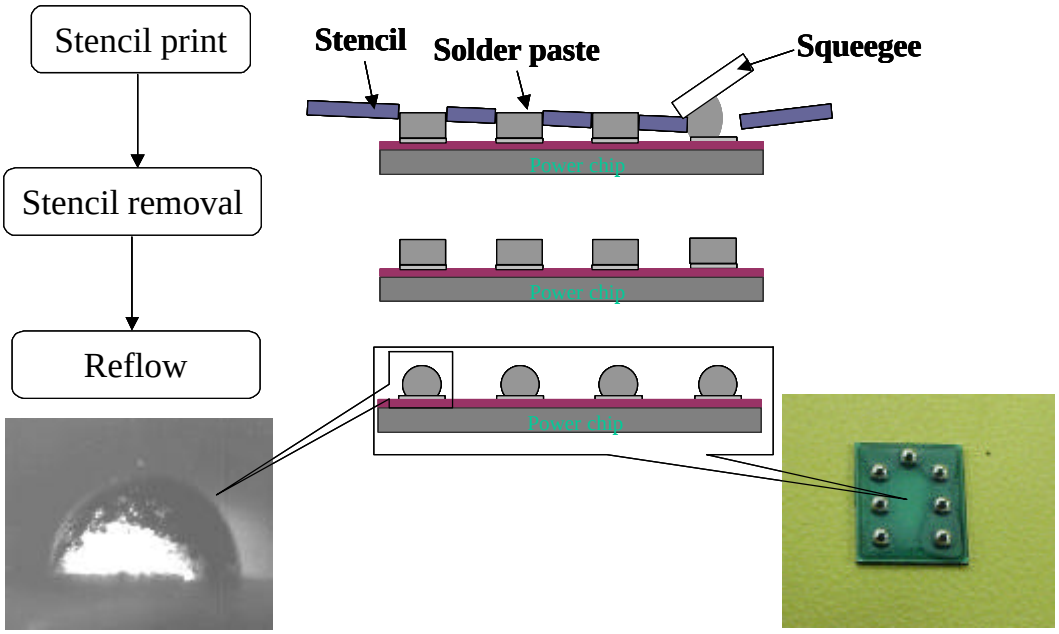


Figure 2.36. Solder bumping process using stencil printing for single bump solder joint fabrication.

Flip chip bonding is the process that attaches the bumped chip to a substrate and form connection between the chip and the substrate. In order to remove the oxidation layer on the bonding pads and form a reliable bonding, flux is first dispensed on pads of the flex substrate. Then the bumped die is aligned and attached to the bond pads on the flex. Lastly the assembly is heated so that the solder melts and forms a metallurgical bond with the bond pad. Figure 2.37 shows flip chip bonding process single bump solder joint fabrication and a microphotograph of the solder join interconnect of IGBT on flex.

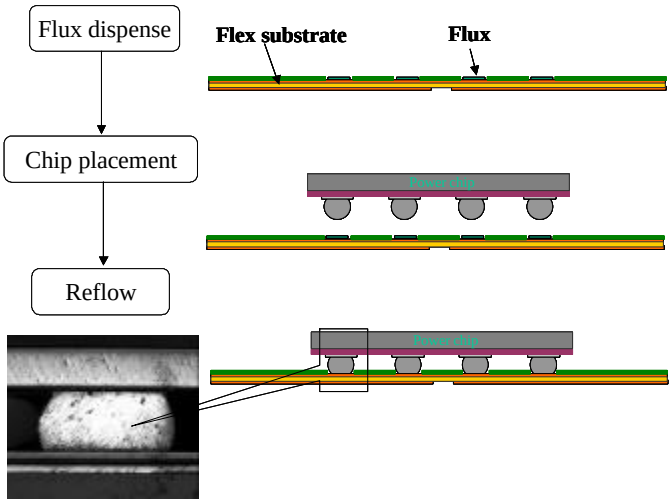


Figure 2.37. Flip chip bonding process for single bump solder joint fabrication.

2.4.3 Process for High Standoff Stacked Solder Joints

The new "stacked solder bumping" technology is an extension and combination of the stencil printed solder bump technology and microball mounting technology. This assembly technology offers several advantages. It offers an improvement and choice in the solder joint height and shape. This new solder bump process can not only increase the standoff height, but also achieve different shapes, including hourglass shape, by keeping the other design parameters such as pad size unchanged. The process is compatible with the surface mount technology and is feasible for volume production, thus it is potentially low cost. In conventional solder bump technology, because of the tolerances on the height of the solder bumps, size of pads, and the warpage of the package and substrate, it is a potential problem that not all the bumps are in contact with their pad mates. However, this problem is solved in this stacked solder bumping technology as described in the following sections. The major disadvantage of this stacked solder bumping process is that it involves additional steps of printing and reflow. In the following paragraphs, stacked solder joint fabrication process is described. In the process drawings, we will only use hourglass shape to demonstrate the stacked solder joint fabrication process. However, the process is actually same for all the stacked solder joint configurations with the only difference of designs as we discussed in section 2.3.2.

The basic process steps of this stacked bumping technique is same as single solder bumping process: solder mask patterning, solder bumping and flip chip bonding. The major difference of these two techniques is the detailed process of solder bumping and flip chip

bonding. The stacked solder bumping process consists of three basic processes: stencil printing, solder ball placement and reflow. Figure 2.38 shows the stacked solder bumping process. The stencil-printing process involved three steps. The solder paste was first pushed into the holes of the stencil by a squeegee, making contact with the bond pads on the chip. Then, the paste was transferred to the chip pads while the stencil was retracted. Finally, the solder paste was prebaked in order to retain its shape during the next process. The solder ball placement process was quite straightforward. First a stencil was placed on top of the chip, and then commercial solder balls were dropped through the windows of the stencil and sticked to the prebaked inner solder cap. In our research, the power chip pad size was 1.1 mm. According to our design of forming hourglass-shaped solder joint, 35 mil (0.9 mm) diameter solder balls were used. The last process of the stacked solder bumping was reflow. As we stated earlier, the inner solder cap was Sn96.5/Ag3.5 alloy with a melting temperature of 221°C. The solder ball was of Sn10/Pb90 solder with a melting temperature of 268°C. During the reflow process, the stacked solder bump was heated to 250 °C. This temperature is above the inner solder cap melting temperature, but below the solder ball melting point. When the inner solder melted, it formed metallurgical bonds with both the chip bond pad metallization and the top solder ball. In order to reduce oxidation of the surfaces and minimize voids contents in the interfaces, the reflow operation was performed in a reduced atmosphere of nitrogen-hydrogen. Figure 2.39 (a) shows the stacked solder bumps on IGBT pads and Figure 2.39 (b) is a magnified photograph of a solder bump.

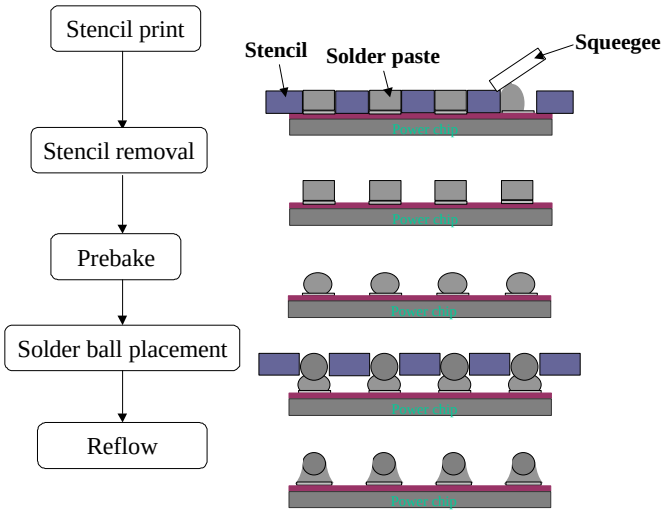
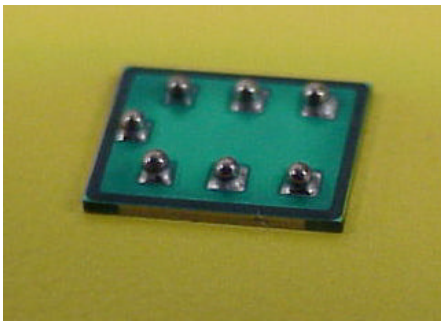
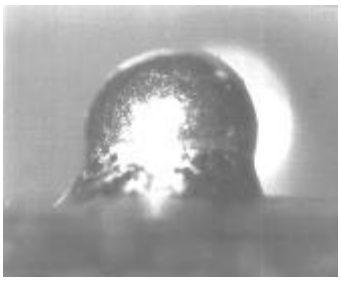
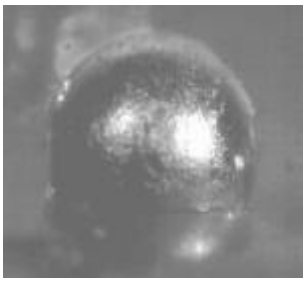


Figure 2.38. Stacked solder bumping process.



(a)





(b) (c) (d)

Figure 2.39. (a) Stacked solder joints on IGBT pads; (b), (c) and (d) are magnified photographs of stacked solder bumps which make ready for fabricating triple-stacked hourglass-shaped, barrel-shaped and column-shaped solder joints.

Flip chip bonding for stacked solder joint involves several detailed steps. First a photoimagable solder mask was applied to the prepatterned substrate with conventional screen-printing. Photolithography allowed definition of openings in the solder mask around all the chip site pads and surface mount footprints on the substrate. This also offered the alignment mark for the chips. Figure 2.40 shows the triple-stacked solder bump bonding process. During flip chip bonding, outer solder paste was first stencil-printed on the substrate. Then the bumped die was aligned and attached to the printed solder paste on the substrate. Lastly the assembly was heated so that the outer solder melted and formed a metallurgical bond with the bond pad. Also as the melting of the outer solder occurred, the surface tension for the melted solder and gravity of the bumped die caused the bumped die to be pulled down, thus allowing all the solder bumps to be connected. Again, the temperature hierarchy principle must be obeyed. The outer cap was eutectic solder (Sn63/Pb37) with a melting temperature of 183°C. We reflowed the assembly at 210°C. Figure 2.41 shows the flip chip assembly before underfill. Figure 2.42 is the cross-section image of the triple-stacked solder bump.

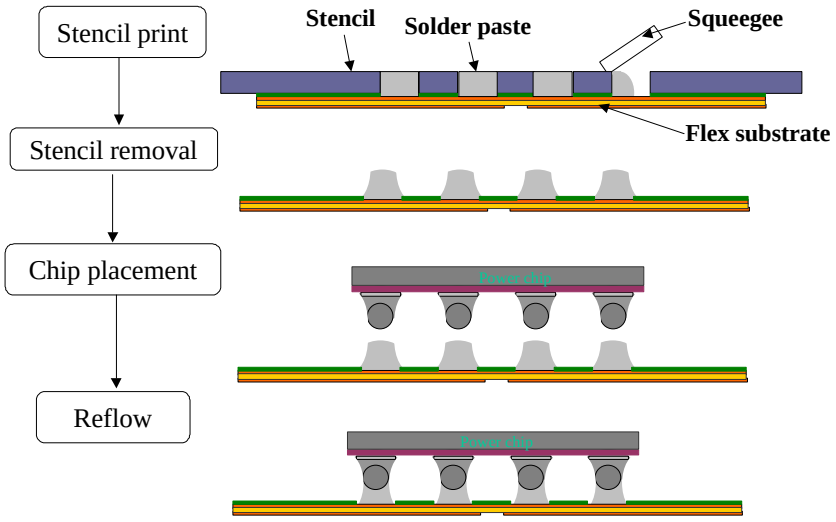


Figure 2.40. Triple-stacked solder bump bonding process.

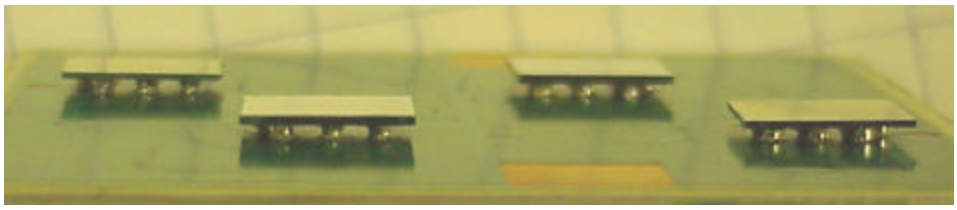
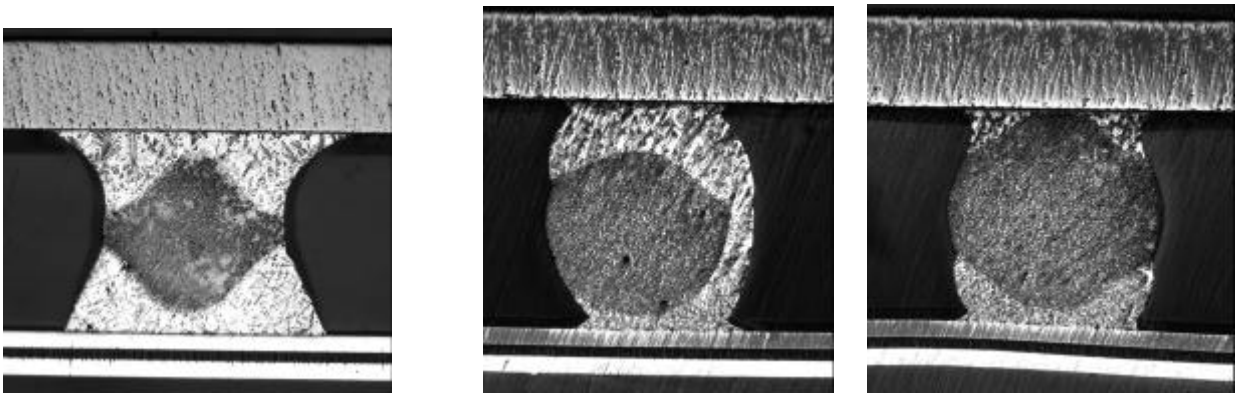


Figure 2.41. Flip chip on substrate assembly before underfill.



(a) (b) (c)

Figure 2.42. Photographs of stacked solder joints; (a) hourglass-shaped; (b) barrel-shaped; and (c) column-shaped.

2.4.4 Underfill Process

It is widely accepted that underfilling of flip chip assembly can improve solder joint reliability and thus the whole assembly reliability significantly [29-30]. Underfill encapsulant reduces the effect of the global thermal expansion mismatch between the silicon chip and

substrate. Actually, after underfilling, the chip, underfill, and substrate are deformed together as a unit, thus the relative deformation between the chip and substrate being very small. As a result, the shear deformation of the solder joint is very small. Furthermore, underfill encapsulant protects the chip from moisture, ionic contaminats, radiation, and hostile operating environments. Additionally, some underfill encapsulants can asc as heat path from the chip to the substrate. However, underfill is not mandatory if the solder joint itself already fulfill the reliability requirements.

After flip chip bonding and cleaning, electrical test was performed prior to the optional underfilling of the solder joints. During underfill, the assembly is placed on a hot plate with 90 °C. Underfill is normally dispensed through a syringe and it is placed around two chip sides in an "L" pattern. After the underfill materials are dispensed, the chip and substrate remain on the hot plate for some time until the gap is completely filled. Finally, the chip on board with underfill is put into a curing oven and cured. Figure 2.43 shows an underfilled flip chip on flex assembly.

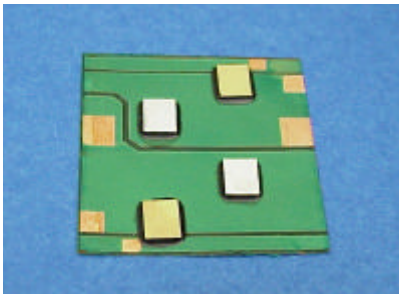


Figure 2.43. Flip chip on flex (FCOF) assembly after underfill.

2.4.5 Process Control Issues for Solder Joint Fabrication

For both single bump and stacked solder joint fabrication, there are some issues and concerns for the process. It is highly desirable that each type of solder joint has a uniform height and shape as designed and has few defects, such as voids, contaminants. However, the stencil printing process inherently has many variables and it is very hard for us to control these variables since we do all the process steps manually. It was identified that five major categories that may influence the quality of solder printing on wafer or chip [7]:

Operators: training, awareness, authority;

Environment: temperature, humidity, dust;

Methods: snap-off, squeegee pressure; alignment;

Materials: solder paste, stencil, squeegee;

Equipment: printer, stencil holder.

It was reported that high-quality solder joint could be produced by using that state of the art stenciling printing equipments and materials [7, 29, 44]. For our manually process and limited resources, it is very difficult to obtain uniform solder joint height and shape, especially for the stack solder joint structures since they are more complicated. The most difficult task for us is to control solder paste volume, which is related to stencil thickness, stencil aperture size and the gap height between stencil and chip. Solder paste volume variation is the major reason for our solder joint height and shape variation. The other important factor is solder paste. Some of our solder pastes did not release well from the stencil, some exhibited slumped deposit, and some contained chemical components that created difficulty to remove residues. Because stacked solder joint structures need two stencil printing processes, their variation is more severe than that of single bump solder joint. However, the main objective of this research is to develop and realize the concept of using solder joint as power chip interconnection, to develop new solder bumping process for improved solder joint reliability and to evaluate the reliability of different solder joint geometries. The variation in the solder joint height and shape does not prevent us from achieving these goals though it does affect our research.

2.5 References

[1] D.S. Patterson, A comparison of Popular Flip Chip Bumping Technologies", Flip Chip Technology, Phoenix, AZ, 1997.

[2] D. Hayes, and D. Wallace, "Solder Jet Printing for Wafer Bumping and CSP applications," Chip Scale Rev., 75-80, September 1998.

[3] D. Hayes, D. Wallace, M. Boldman, and R. Marusak, "Picoliter Solder Droplet Dispensing," International Journal of Microcircuits and Electronic Packaging, 16 (3): 173-180, 1993.

[4] E. Muntz, M. Orme, G. Pham-van-Diep, and R. Godin, 'An analysis of precision, Fly-Through Solder Jet Printing," Proceedings of International Symposium on Microelectronics, pp. 671-680, October 1997.

[5] Y. Kato, Y. Ueoka, E. Kono, and E. Hagimoto, "Solder Bump Forming Using Micron Punching Technology," Proceedings of IEEE Japan IEMTS, pp. 117-120, Dec. 1995.

[6] Greer, S. E., Proceedings of the 1996 IEEE 46th Electronic Components and Technology Conference, Orlando, FL, 1996.

[7] Joachim Kloeser, Katrin Heinricht, Kai Kutzner, Erik Jung, Andreas Ostmann, and Herbert Reichl, "Fine Pitch Stencil Printing of Sn/Pb and Lead Free Solders for Flip Chip Technology," IEEE Transactions on Components, Packaging, and Manufacturing Technology—Part C, pp. 41-50, VOL. 21, NO. 1, 1998.

[8] Deborah S. Patterson, Peter Elenius, James A. Leal, "Wafer Bumping Technologies - A Comparative Analysis Of Solder Deposition Processes And Assembly Considerations," Flip Chip Technology, Phoenix, AZ, 1997.

[9] Bessho Yoshihiro et al, "Stud Bump Bonding Technique for High Density Multichip Modules," Proc. IEEE-CHMT European International Electronic Manufacturing Technology Symposium, Kanazawa, Japan, 1993, pp. 362-365.

[10] T. Ogashiwa, T. Arikawa, and A. Inoue, "Development of reflowable Sn-Pb Alloy Bump for Al Pad," Proceedings of IEEE ECTC, pp. 664-669, May 1997.

[11] T. Ogashiwa, T. Arikawa, H. Murai, A. Inoue and T. Masumoto, "Reflowable Sn-Pb Bump Formation on Al Pad by a Solder Bumping Method," Proceedings of IEEE ECTC, pp. 1203-1208, May 1995.

[12] Ogashiwa, T., Akimoto, H., Shigyo, H., Murakami, Y., Inoue, A., Masumoto, T., Japan Journal of Applied Physics 1, Regulation Paper Short Notes (Japan), Volume 31, Number 3, March 1992.

[13] Shimokawa, K.; Hashino, E.; Ohzeki, Y.; Tatsumi, K."Micro-ball bump for flip chip interconnections,"Proceedings of IEEE ECTC, pp. 1472 – 1476,25-28 May 1998.

[14] Shimokawa, K.; Tatsumi, K.; Hashino, E.; Ohzeki, Y.; Konda, M.; Kawakami, Y. "Micro-ball Bump Technology For Fine-pitch Interconnections," IEMT/IMC Symposium, pp.105 – 109, April 16-18, 1997.

[15] A. Cairncross and K. Klabunde, "Method and Product for Particle Mounting," U.S. Patent 5,356,751, Oct. 1994.

[16] Beikmohamadi, A.; Cairncross, A.; Gantzhorn, J.E., Jr.; Quinn, B.R.; Saltzberg, M.A.; Hotchkiss, G.; Amador, G.; Jacobs, L.; Stierman, R.; Dunford, S.; Hundt, P."Tacky Dots/sup TM/ technology for flip chip and BGA solder bumping," Proceedings of IEEE ECTC, pp. 448 –453, 1998.

[17] Hotchkiss, G.; Amador, G.; Jacobs, L.; Stierman, R.; Dunford, S.; Hundt, P.; Beikmohamadi, A.; Cairncross, A.; Gantzhorn, O.; Quinn, B.; Saltzberg, M." Tacky Dots/sup TM/ transfer of solder spheres for flip chip and electronic package applications," Proceedings of IEEE ECTC, pp. 434 –441, 1998.

[18] Matsui N, Sasaki S and Ohsaki T, "VLSI Chip Interconnection Technology Using Stacked Solder Bumps", IEEE Transactions on Components, Hybrids, and Manufactory Technology, 1987; vol. CHMT-12:566-570.

[19] Chiang KN, Lin YT and Cheng HC, " On enhancing eutectic solder joint reliability using a second-reflow-process approach," IEEE Transactions on Advanced Packaging, 2000:Vol. 23, No.1: 9 -14.

[20] Lovasco F, Oien MA, " Double-bump surface-mount technology for very high IO interconnections," Proceedings of the Fourth IEEE/CHMT European International Electronic Manufacturing Technology Symposium, pp. 41 -44, 1988.

[21] Hong BZ; Ray SK, " Ceramic column grid array technology with coated solder columns," Proceedings of the IEEE 50th Electronic Components & Technology Conference, pp.1347 - 1353, 2000.

[22] Master RN, Cole MS, Martin GB, Caron A, " Ceramic column grid array for flip chip applications," Proceedings of the IEEE 45th Electronic Components and Technology Conference, pp. 925 -929, 1995.

[23] S. K. Ray, M. Interrante, L. Achard, M.S. Cole, I. DeSousa, L. Jimarez, G. Martin, and C. Reynolds, "CLASP Ceramic Column Grid Array Technology for Flip Chip Carriers," Advanced Packaging Technology Tutorial, Proceedings of SEMICON West, July 13-14, 1999.

[24] Corbin JS, "Finite Element Analysis for Solder Ball Connection (SBC) Structural Design Optimization," IBM J. Res. Devel., 37 (5): pp.585-596, 1993.

[25] Simon, J.; Reichl, H. "Board level reliability of a waferlevel CSP using stacked solder spheres and a solder support structure (S3)," Proceedings of the IEEE ECTC, pp. 81-86, May, 2000.

[26] G. Cherian, "Solder Columns for Surface Mounting of Leadless Ceramic Chip Carriers on Glass/Epoxy Printed Circuit Boards", Raychem Corporation, Menlo Park, California.

[27] http:// www.winslowautomation.com.

[28] Manson SS, Thermal Stress and Low Cycle Fatigue, McGraw-Hill, New York, 1996.

[29] Lau JH, Flip Chip Technologies, McGraw Hill, 1995.

[30] Tummala RR, Rymaszewski EJ and Klopfenstein AG, Microelectronics Packaging Handbook, Chapman & Hall, 1996.

[31] Solomon HD, "Fatigue of 60/40 Solder," IEEE Transactions on Components, Hybrids, and Manufactory Technology, CHMT-9: 423-432, 1986.

[32] Norris KC and Landzberg AH, "Reliability of Controlled Collapse Interconnections," IBM J. Research Devel., Vol. 13, No. 3, 266-271, May 1969.

[33] Baba S, Tomita Y, Matsuo M, Matsushima H, Ueda N and Nakagawa O, “Molded Chip Scale Package for High Pin Count”, Electronic Components and Technology Conference, pp. 1251-1257, 1996.

[34] R. Satoh, M. Ohshima, H. Komura, I. Ishi, and K. Serizawa, “Development of a New Micro-solder Bonding Method for VLSIs,” Proc. 1983 IEPS, pp. 455-461, 1983.

[35] L. S. Goldman, “Geometric Optimization of Controlled Collapse Interconnections,” IBM J. Research Devel., 251-269, May 1969.

[36] Satoh R, Ohshima M, Komura H, Ishi I, and Serizawa K, “Development of a New Micro-solder Bonding Method for VLSIs,” Proc. 1983 IEPS, pp. 455-461.

[37] Satoh R, Arakawa K, Harada M, Matsui K, " Thermal fatigue life of Pb-Sn alloy interconnections," IEEE Transactions Components, Hybrids, and Manufacturing Technology, 1991;Vol. 14: 224 -232.

[38] Goldman LS, “Geometric Optimization of Controlled Collapse Interconnections,” IBM J. Research Devel., 1969; 251-269.

[39] Ho TH, Lee JY, Lee RS, and Lin AW, “Linear Finite Stress Simulation of Solder Joints on 225 I/O Plastic BGA Packages Under Thermal Cycling,” ECTC, pp. 930, 1995.

[40] Kitano M and Honda M, "Shape Prediction of Sodler Bump Joint by Surface Tension Analysis and Fatigue Strength Evaluation," ASME Advances in Electronic Packaging 1997, EEP-Vol. 19-2, 1407-1413.

[41] Yu Q, Shiratori M, and Ohshima Y, " A study of the effects of BGA solder geometry on fatigue life and reliability assessment," Proceedings of Thermal and Thermomechanical Phenomena in Electronic Systems, 1998. ITHERM'98. Pp. 229 -235.

[42] Body DB, "Two Edge-Bonded Elastic Wedges of Different Materials and Wedges Angles under Surface Tractions", Journal of Applied Mechanics, pp 526-528, Dec., 1952.

[43] Willams ML and Pasadena C, "Stress Sigularities Resulting From Various Boundary Conditions in Angular Corners of Plates in Extension", Journal of Applied Mechanics, pp 377-386, June, 1971.

[44] Li Li and Pat Thompson,"Stencil Printing Process Development for Flip Chip Interconnect," IEEE transactions on electronics packaging manufacturing, pp. 165-170, vol. 23, no. 3, July 2000.

[45] M. Pfeifer, "Solder bump size and shape modeling and experiment validation," IEEE Trans. Comp., Packag., Manufact. Technol. B, vol. 20, pp. 452–457, Nov. 1997.

[46] C. R. M. Grovenor, Microelectronic Materials, 2nd Ed., Oxford Press, London, 1989.

[47] Material data sheets from vendors.

[48] P.A. Magill, J.D. Mis and G.A. Rinne, "Considerations for an Electroplated Flip Chip Process", Proceedings of IMAPS conference, Boston, MA, May 1998.

[49] M. Cho, S, Kang, Y. Kwon, D. Jang and N. Kim, Flip Chip Bonding on PCB with Electroless Ni-Au and Stencil-printing Solder Bump," Proceedings of SMTA International Conference, pp. 159-164, September, 1999.