Characterizing Devices Using the IEC 61000-4-5 Surge Stress

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50 Words Abstract – Many systems need to survive the IEC 61000-4-5 surge stress. Characterizing protection devices and input circuitry using this stress pulse provides information useful when designing such systems. Data taken with this surge pulse can also be used to determine ESD behavior.

I. Introduction

Designing products and devices to survive ESD stress is commonplace. There are several standard tests such as HBM, CDM, and the IEC 61000-4-2 system-level ESD stress. Surge testing using the IEC 61000-4-5 specification [1] is less well known but gaining in importance. In this paper we discus several types of useful information that can be obtained using the IEC 61000-4-5 surge pulse.

II. The 61000-4-5 Surge Stress

A. What the Surge Stress Represents

The IEC 61000-4-5 Surge Immunity stress is meant to be representative of voltage or current pulses induced on power networks by events outside of the equipment under test. These surges can come from power system switching transients such as capacitor bank switching or load changes. Surges can also be induced on power lines by lightning, either a direct strike to a power line or induced by a nearby lightning strike.

B. Electrical Details of the Surge Stress

The IEC 61000-4-5 surge pulse is formed by a *combination wave generator*. It is called this because for a given stress level the generator output pulse must meet both a specification of the open circuit voltage and a specification of the short circuit current. Obviously these are not tested simultaneously, one must be checked and then the other.

1. Open Circuit Voltage
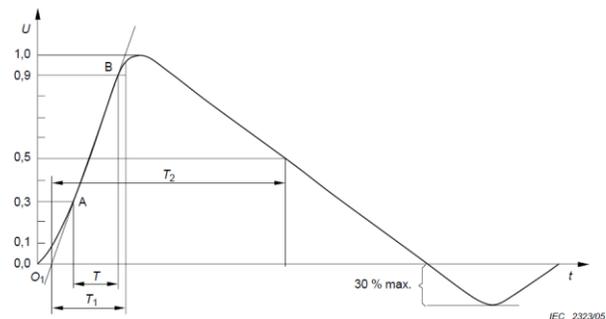
Front time: $T_1 = 1,67 \times T = 1,2\ \mu s \pm 30\ \%$
Time to half-value: $T_2 = 50\ \mu s \pm 20\ \%$.

Figure 1: The Open Circuit Voltage Surge Pulse

The open circuit voltage pulse (figure 1) has the following characteristics:

- Front time = 1.2 µs ± 30%
- Time to half-value = 50 µs ± 20%

2. Short Circuit Current

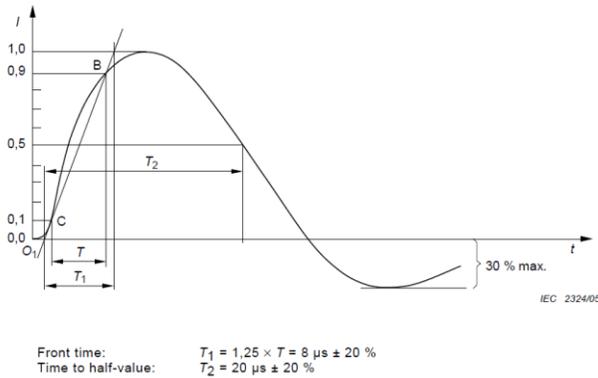

Figure 2: The Short Circuit Current Surge Pulse

The short circuit current pulse (figure 2) has the following characteristics:

- Front time = 8 µs ± 20%
- Time to half-value = 20 µs ± 20%

In both cases, the Front time is approximately the risetime and the Time to half-value is approximately the pulse width.

C. Why Use the Surge Stress?

Some systems are exposed to surge stresses which are much slower than ESD but more powerful. Surge stress can come from direct or indirect lightning strikes as well as other high energy events such as inductive spikes or load dumps.

Highly specialized ESD protection schemes have been shown ineffective against such slow transient, low voltage, but high current stresses. [2]

Systems that can be exposed to surge stresses must be checked for their protection effectiveness against this stress. Specialized surge protection may need to be added.

Transient Voltage Suppressors (TVS) have been characterized using the IEC surge stress for years. Performance when subjected to the IEC surge stress is frequently found in TVS datasheets. [3] [4]

III. Test Hardware and Setup

Most surge pulse generators are large, producing current pulses with peak currents in the range from 250 A to 2000 A. These currents are far too high for stressing integrated circuits and small Transient Voltage Suppressor (TVS) devices. The data presented in this paper were taken with a custom built surge pulse generator that produces peak currents from 3 A to 25 A.
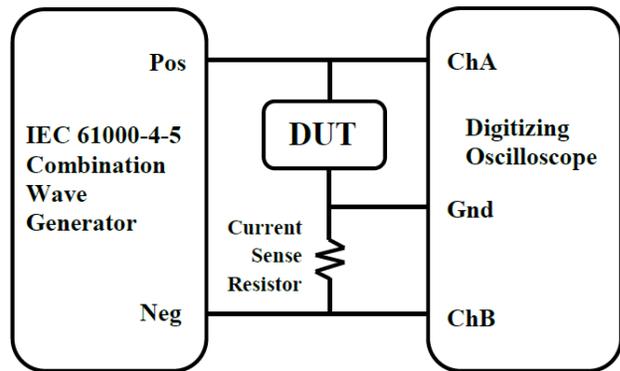

Figure 3: Test Setup Block Diagram

Figure 3 shows a simplified block diagram of the equipment used in preparing this paper. The Device Under Test (DUT) is stressed using the custom surge pulse generator. The voltage across the DUT is sampled directly. A small value resistor of 90 mΩ is used to convert the current through the DUT into a voltage proportional to the current, this voltage is also sampled. This small resistance is not enough to impact the readings.

To produce a curve, the DUT is subjected to a single surge stress. During this surge stress the DUT voltage and DUT current are sampled simultaneously every 50 ns by the digitizing oscilloscope. Displaying the voltage and current as an "XY" plot produces the parametric curve of Current versus Voltage.

IV. Visualizing Current Distribution

Even distribution of current flow through a protection device is critical for obtaining the highest failure current using the smallest device area – the largest $mA/\mu m^2$. Emission microscopy (EMMI) is often used to visualize the flow of current through semiconductor devices. The EMMI will show "hot spots" of above average current flow. Using that information one can change the metal routing or device layout to more evenly distribute the current. The key is to provide the right stress to the device.

The ESD stress itself provides the actual current distribution within the device, but the total energy of the ESD stress is so low that on the EMMI the image from the ESD induced emissions is lower than the noise level and difficult to see.

Stress from a Transmission Line Pulser (TLP) is very similar to the ESD stress but suffers from the same drawback – the image from the stress current flow is buried in the noise. In spite of this, several

researchers have obtained usable images using repeating pulses of TLP stress. [5] [6] [7]

Often a DC bias is used to induce the current to be visualized. This is easy to do and provides excellent images of the current flow but the maximum current that can be used is limited by the device power dissipation and is typically a few mA or tens of mA.
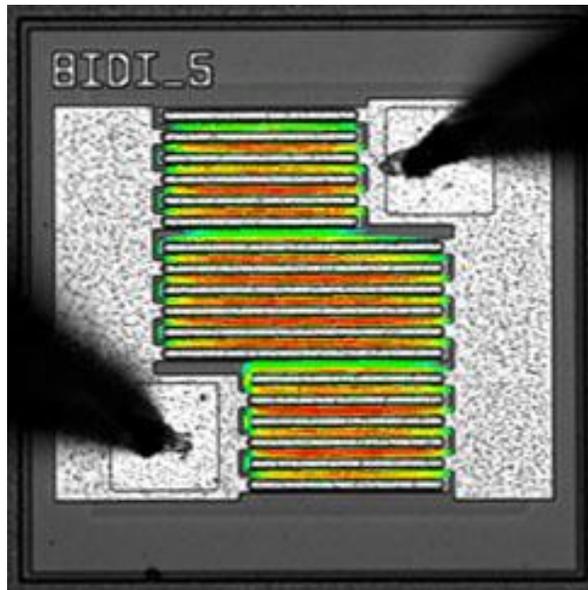

Figure 4: Current Distribution in a Bidirectional Zener diode. Stress is 2 mA DC.

Figure 4 shows the metal layout and DC current distribution in a bidirectional Zener diode test device. Red indicates high current flow, green indicates low current flow. With a stress current of 2 mA DC the current distribution is very even. Most fingers are "lighting up" to the same degree, indicating that all are carrying about the same current.

The device layout looks good, but 2 mA is not the current at which the device will be expected to perform. ESD/EOS currents are in the range of amperes, not milliamperes. Voltage drops in the metal system will be about three orders of magnitude higher for ESD/EOS events and that will impact the current distribution.

What is needed is a pulse that is high enough in current to show the current distribution at levels corresponding to the ESD event. This current pulse needs to be longer duration than the ESD event in order to increase the signal to noise ratio on the EMMI but not so long as to damage the device being stressed.

The IEC 61000-4-5 surge pulse works well in this application. The surge current has a much slower risetime and is a wider pulse than an ESD stress, but

still allows operation at current levels close to those of ESD. Having a pulse that is approximately two orders of magnitude longer than that from a TLP yet also two orders of magnitude shorter than that of a conventional pulsed curve tracer is very useful in this case.
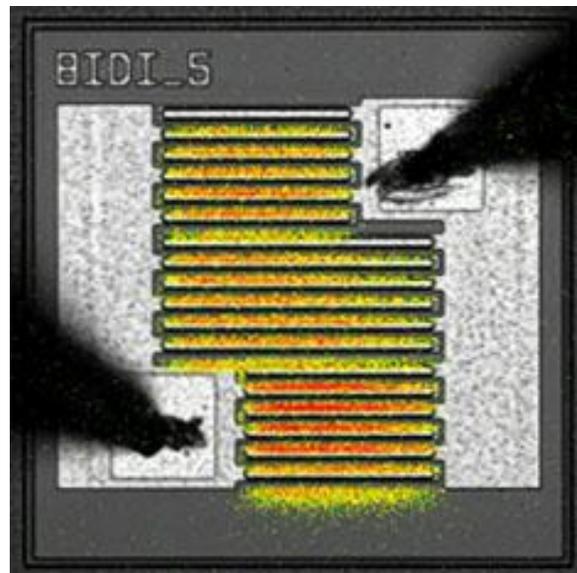

Figure 5: Current Distribution in a Bidirectional Zener diode. Stress is three 4 ampere pulses of IEC 61000-4-5 surge current.

Figure 5 shows the same device as figure 4 when it is stressed by an IEC 61000-4-5 surge pulse with a peak current of 4 amperes. The IEC surge pulse has a short enough duration that many devices will survive a pulse with current in the range of amperes – the total power dissipated in the device is still within the design limits.

At 4 amperes the device layout is not performing as well as it did at 2 milliamperes. It is clear from the image that the fingers in the lower section are carrying a much higher current density than the rest of the fingers. In use this is where the device will fail, as the lower fingers will reach their maximum current capacity while the other fingers are still well below their maximum current capacity.
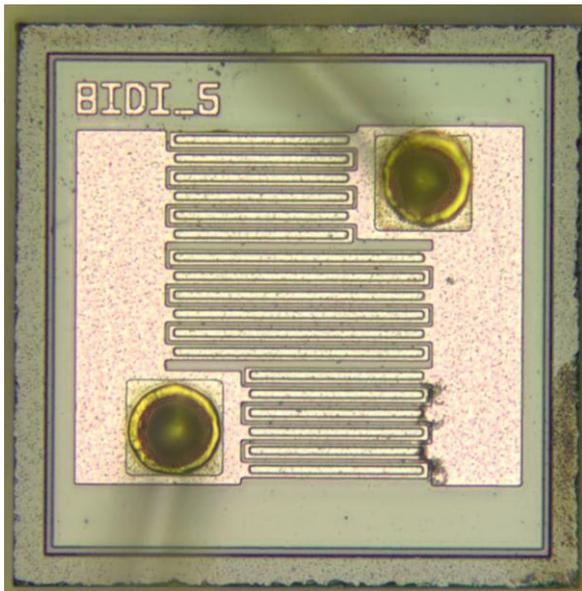
Figure 6: Damage in a Bidirectional Zener diode. Stress was 30 kV IEC 61000-4-2 ESD, same polarity as surge stress of Figure 5.
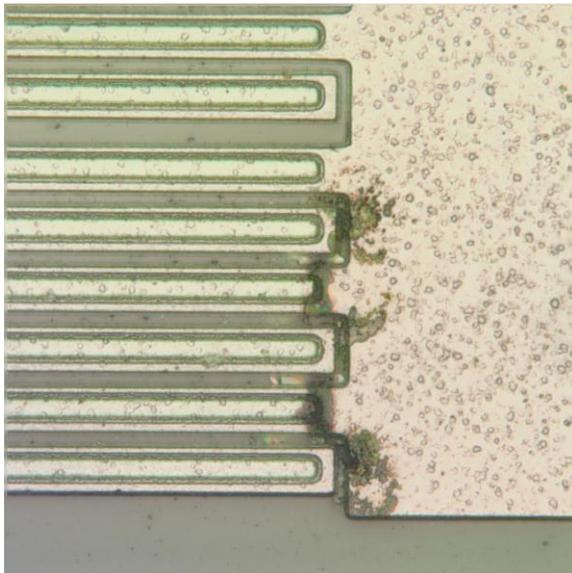

Figure 7: Close-up of the damage seen in Figure 5A.

Figures 6 and 7 are failure analysis photos of a fresh device of the same type as used in Figures 4 and 5. This device was subjected to 30 kV IEC 61000-4-2 ESD stress; the polarity of the ESD stress was the same as the polarity of the surge stress in figure 5.

Figure 6 shows the ESD damage in the lower right part of the structure. It is at the end of the fingers that "lit up" in Figure 5. Close-up Figure 7 shows the damaged and reflowed metal from excessive ESD current flow in these fingers.

In this experiment we did not attempt to compare damage caused by surge stress to damage caused by ESD stress.

V. Understanding Exactly When Devices Fail

Many EOS stress tests are pass/fail. The device is subjected to the stress at a given level and then tested; either it still functions correctly and passes or it does not function correctly and fails.

A careful examination of the voltages and currents in a device while it is being stressed by an IEC 61000-4-5 surge pulse can provide insight into *why* the device failed – what happened to cause the failure?
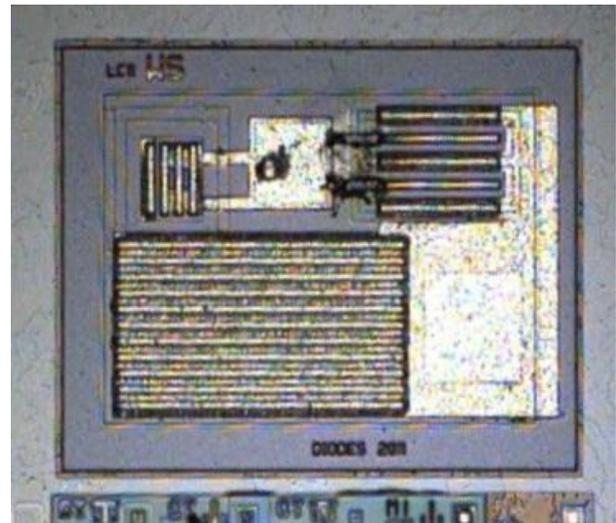
Case Study #1

Figure 8: Photomicrograph of a low capacitance clamp stressed to failure using the surge pulse. Note the damage to the metal to the right of the top bond pad.

Figure 8 shows a photo from the failure analysis of a low capacitance clamp that was stressed to failure using the surge pulse. Metal damage is visible in the two metal fingers located to the right of the top bond pad. Probing revealed that the metal at this location was open. Probing the diodes past the blown metal showed that they were still functional.
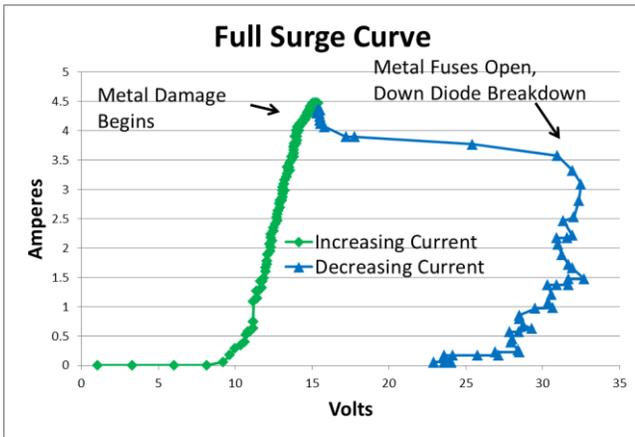
Figure 9: Full surge curve of a low capacitance device
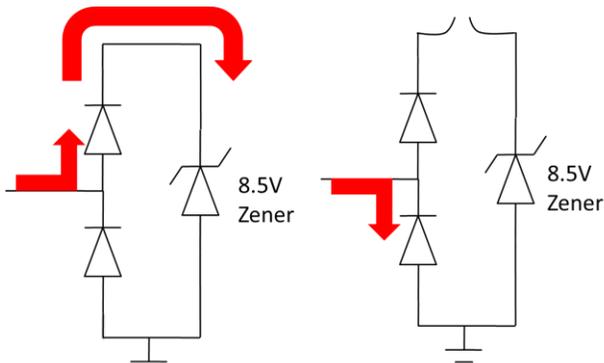

Figure 10: Current flow before and after metal failure

Figure 9 shows the full surge curve, both rising and falling edges, taken on the above device. On the rising edge of the current, just over 4 amps, there is an abrupt change in the slope of the IV curve where the metal is beginning to be damaged. Beyond that point one can see where the metal fused open and the voltage across the device increased to the reverse breakdown voltage of another diode in the structure. Figure 10 shows the schematic of the clamp and indicates the current path before the lead opened (on the left) and after the lead opened (on the right).
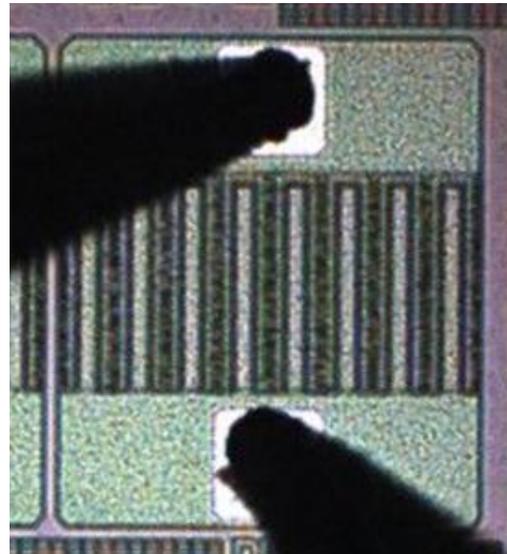
Figure 11: An 8 fingered device prior to surge stressing

Figure 11 shows a device prior to surge stressing. There are 8 metal fingers connected to the bottom bond pad. This device was subjected to several identical surge stresses, each having a peak current of about 10 amperes. After the first surge stress a slight amount of damage was seen in some of the metal fingers. After the second surge stress a little more damage was seen, shown in the next two figures.
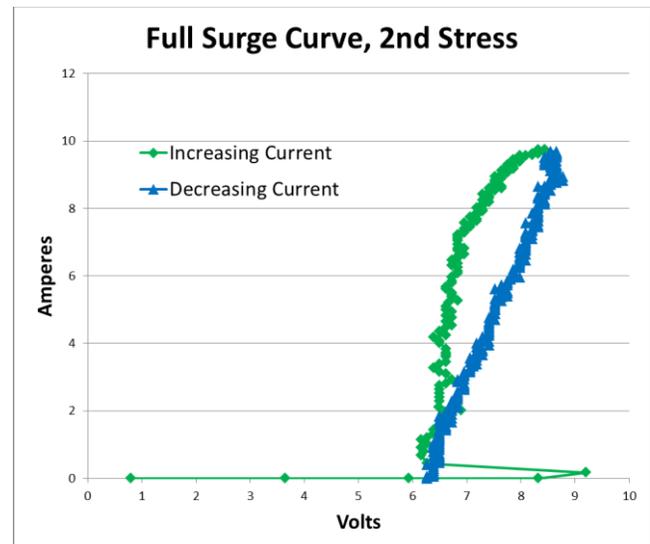

Figure 12: I-V curve of 8 fingered device taken on the second surge stress
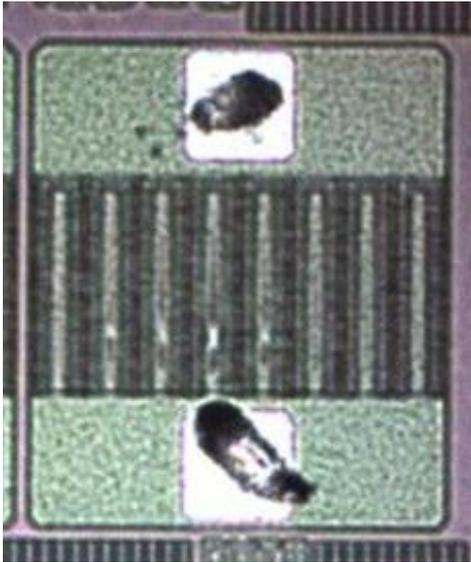
Figure 13: The 8 fingered device after 2 surge stresses

Figures 12 and 13 show the same 8 fingered device during and after its second surge stress. The curve in figure 12 looks as expected, but some damage to the metal is visible on fingers 2 through 5 (counting from the left) in figure 13.
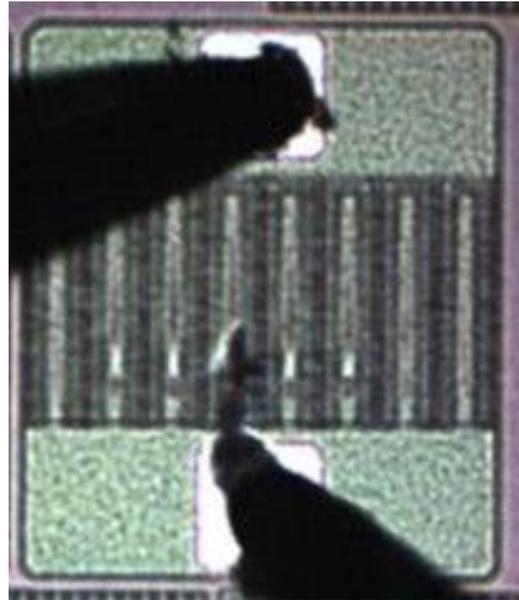

Figure 15: The 8 fingered device after 3 surge stresses

Figures 14 and 15 show the same 8 fingered device again during and after its third surge stress. Note the abrupt drop in voltage in figure 14 while the current was decreasing as well as its equally abrupt recovery. Figure 15 now shows damage in fingers 2 through 6, with finger 4 having much more damage than the others.
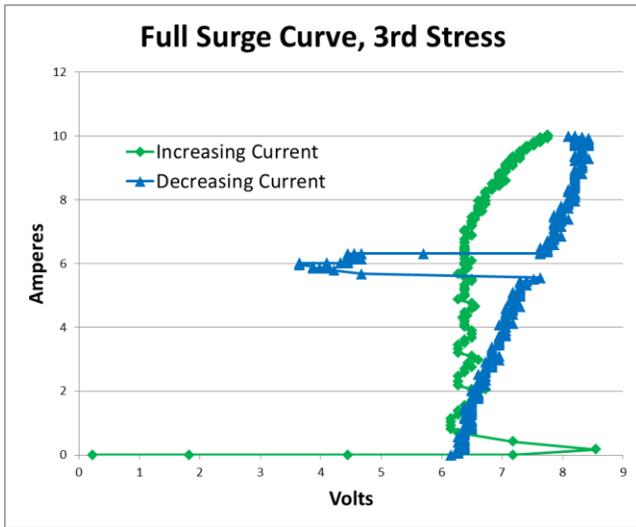

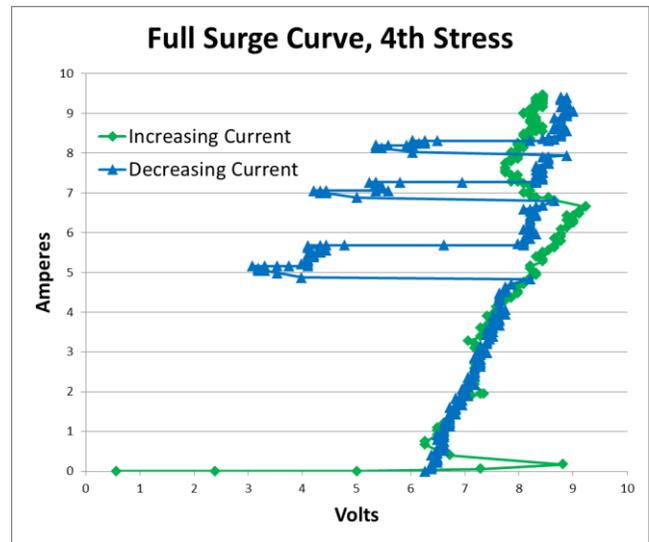Figure 14: I-V curve of 8 fingered device taken on the third surge stress

Figure 16: I-V curve of 8 fingered device taken on the fourth surge stress

Figure 17: The 8 fingered device after 4 surge stresses

Figures 16 and 17 show the same 8 fingered device during and after its fourth surge stress. This time the part of the I-V curve in figure 16 taken as the current was decreasing shows 3 abrupt dips in voltage. Inspecting figure 17 reveals serious damage in 4 of the fingers, fingers number 2 through 5.

Our hypothesis is that during this sequence of stresses we are seeing the metal on the fingers blow open sequentially. Something happens within the device to cause a low impedance on one of the fingers. The voltage across this finger drops and all the current flows through the one finger until the metal blows open, at which time the voltage recovers and the current spreads out among the remaining fingers.

Figure 16 shows 3 fingers blowing in rapid succession. As the stress current is decreasing, the first finger shorts and then blows open at 8 amps. At 7 amps the second finger of the three shorts and blows open, followed by the third finger between 5 and 6 amps.

Note that the dip at 8 amps is narrower than the dip at 7 amps and both are narrower than the dip at 5 amps. Since the data points are taken equally spaced in time, this shows that the lead blew quicker at 8 amps than at 7 amps or 5 amps.

The energy dissipated in each metal finger when the underlying junction shorts can be determined by numerically integrating the power (volts * amperes) over the time that the DUT voltage was lowered.

Comparing the energy in each of the dips shows that it took about the same amount of energy to blow each finger (note that the first dip in figure 14 corresponds

to finger 4 blowing, but we do not know which dip in figure 16 corresponds to each of the three other fingers that blew open):

- 1st dip: 42.8 μJ
- 2nd dip: 44.9 μJ
- 3rd dip: 38.5 μJ
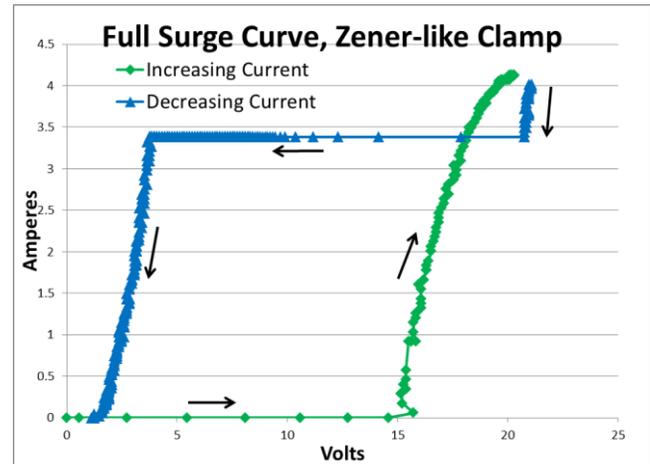- 4th dip: 42.7 μJ

Case Study #3

Figure 18: Current versus Voltage of Zener-like ESD Clamp Plotted during Surge Stress of 4.2 Amp Peak Current

Figure 18 shows the current versus voltage curves of a high performance "Zener like" ESD clamp device having >30 kV IEC 61000-4-2 performance when subjected to a surge pulse of 4.2 amps peak current.

As the current was increasing the device behavior was as expected. Upon reaching the device breakdown the rapid increase in the device voltage slowed dramatically, showing the device's dynamic resistance for the first couple of amperes. At higher currents some "bending" of the curve suggests that the device is beginning to heat up, but no failure is seen.

As the current was decreasing (as the arrows indicate, this part of the curve is properly viewed as beginning at the peak current and ramping down to zero current at its end) the voltage initially stayed high but abruptly dropped when the current was about 3.4 amps. This is where the device failed.

These curves show that the device successfully withstood the peak voltage of 22V and peak current of 4.2 amps, it was the total power that caused the failure. Even as the current (and thus the power) was decreasing the power was still high with 22 volts across the device and several amperes of current flowing. Before the power could decrease to a safe

level the device temperature got high enough that the device failed.

VI. As a TLP Alternative

A Transmission Line Pulser (TLP) is an excellent tool to use when characterizing devices to determine their behavior under ESD conditions. Its pulses are similar in duration and energy to the standard ESD events so the I-V curves it generates are representative of how the device will perform when subjected to ESD stress.

A downside to using a TLP is the complexity of the equipment. If one has a well-stocked lab it is possible to build a "homemade" TLP for much lower equipment cost than purchasing a commercial TLP, but this option does entail some engineering time and development work that must be factored into the total effort. Many organizations that could benefit from the use of a TLP do not have one due to budget or engineering time constraints.

As seen in Figure 3, a surge-based curve tracer is simple to build. We found that in many cases the surge stress can be used to obtain I-V data similar to that of a TLP. Using the surge stress to take I-V curves is quicker than using a TLP, which allows many more devices to be tested in the same length of time, useful when characterizing a test chip. A surge based curve tracer also allows the possibility of a company having one TLP for detailed analysis of devices and several surge based curve tracers for more widespread access to such high current curves.
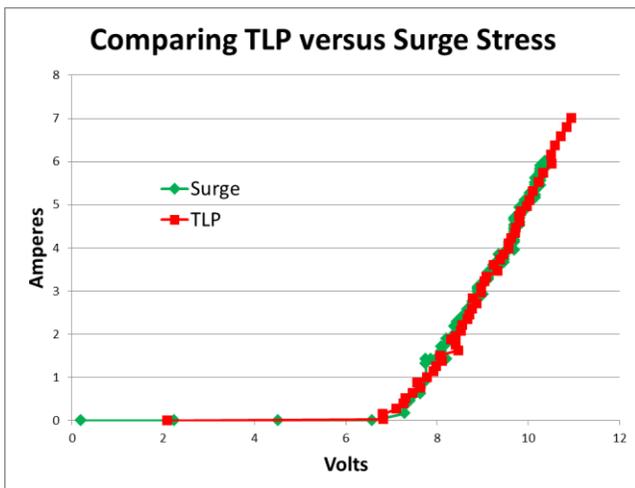

Figure 19: Comparing current versus voltage plots of a trench device made using a 100 ns TLP with plots made using the surge stress
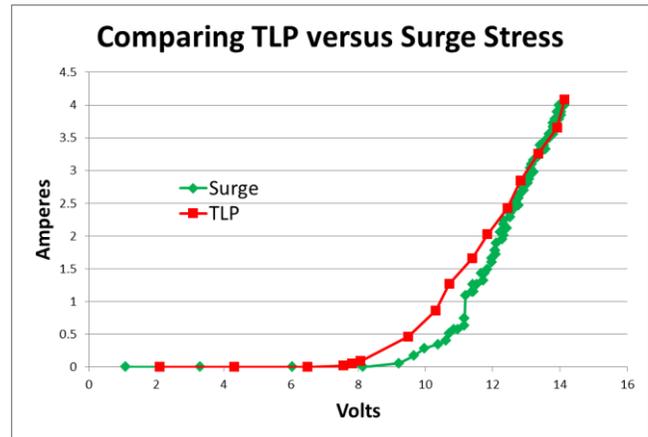

Figure 20: Comparing current versus voltage plots of a low capacitance device made using a 100 ns TLP with plots made using the surge stress
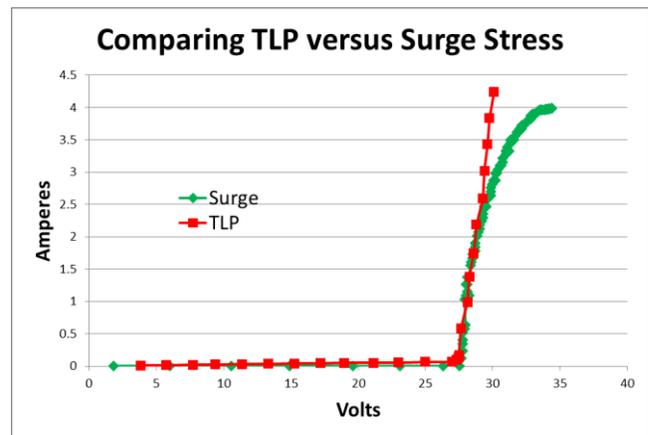

Figure 21: Comparing current versus voltage plots of a high voltage device made using a 100 ns TLP with plots made using the surge stress

Figures 19, 20, and 21 show current versus voltage curves of the several devices, each taken with both a TLP (100 ns pulse width) and a surge curve tracer. In most cases the correlation is quite good. At currents over 2.5 amperes figure 21 shows the effects of self-heating due to the wider surge pulse width.

This shows that in many cases a simple surge based curve tracer can replace a much more complex TLP. Both provide similar information at currents up to a few amperes, the region of most interest to integrated circuit designers.

VII. Conclusions

Stressing devices using relatively low level (up to 10 or 20 amperes) surge stresses based on the IEC 61000-4-5 specification provides several types of useful information for designers.

The high current and high, yet limited, energy is useful to show how metal routing and device layout impact current flow within the device.

Taking an I-V curve on both the rising and falling current curve differentiates between devices that fail due to excessive voltage or current and those that fail due to excessive energy.

The surge stress equipment is simpler than a TLP yet for many devices will provide similar information.

Acknowledgements

References

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