Chip Embedding in Laminate based on Cu Leadframe for Thin Die Packaging

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Session: Innovative Component, Reliability and Manufacturing 3D Power Packaging Solutions

Content

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Motivation: Major trends in packaging

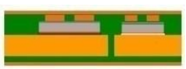
› SiP integration everywhere, also for power devices

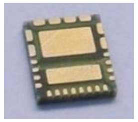
› Chip – package and even board/system technologies merge

› Trend to thin chips => in power electronics **thin chips** are required for reduced Rdson and improved heat dissipation

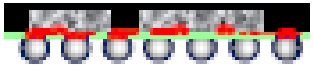
⇒ Trend to new chip embedding technologies applying redistribution layers that allow thin dice packaging (one key is low parasitics)

i) chip embedding in laminate





ii) Chip embedding in mold (fan-out WLP)



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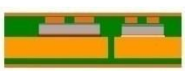

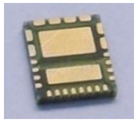

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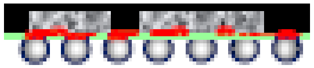

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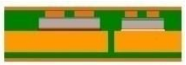

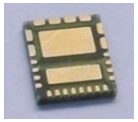

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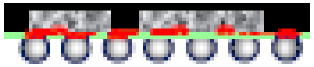

=> In packaging increasing mix of new materials

In the last 10 years: all package materials changed

- Wirebonding => Al, Au => Cu (e.g. Pd coated), Ag
- Green packaging: mold compound move to Pb-free and halogen free

  Move away from PbSn => SnAgCu (SAC) etc.
- Composite materials e.g. advanced mold compound (> 200°C)
  (liquid mold compounds, e.g. flip chip under-fill, fine filler mold compound)
- Dielectrics e.g. isolation in film RDL or (C, L, transformers, ….)
- Barrier layers e.g. diffusion barrier, ...
- Adhesives e.g. for die attach, …
- Nano-materials e.g. for sintering (Ag, Cu, …)
- New research: investigation of Cu composites
- etc.

→ in the next 10 years all package materials will change

Market situation:
Changing reliability requirements

Request to stand higher temperatures (e.g. for GaN, SiC etc.)

Importance of chemical environment

(e.g motor rooms of ships, off shore wind power, electronics in transmission)

Packaged chips in battery

New requirements due to new applications, e.g. full autonomous driving

- Today: 8.000 hours on time (approx. 1,5 hours per day 15 years)
- Tomorrow: 121.500 hours on time (approx. 22,5 hours per day 15 years)

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=> Package materials must stand these new reliability requirements

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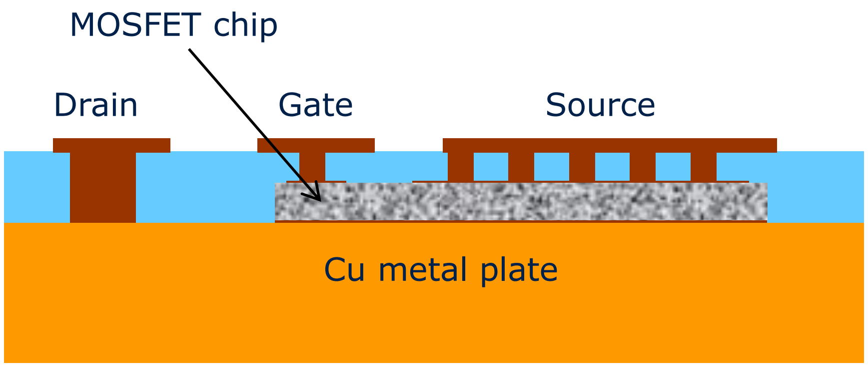
Laminate chip embedding technology

Combination of

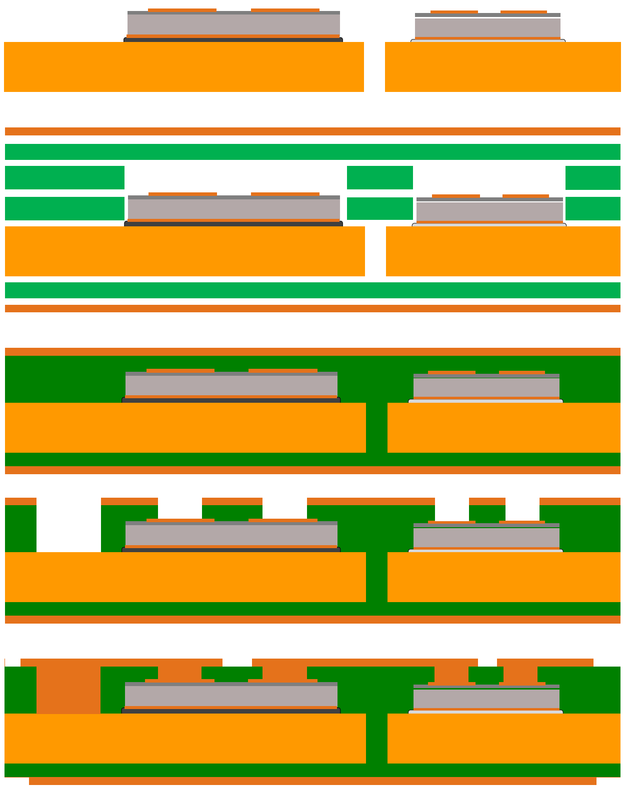
- wafer frontend-processes,
- chip packaging processes,
- board processes



Target of this work

- find the best combination within the chip/laminate regime under consideration of the two key processes:
    - layer stack lamination and laser via drilling
- the lamination process relies on the proper choice of laminate material class and parameters such as resin content.

Laminate chip embedding process chain for thin die packaging



Die attach (diffusion soldering),
Copper roughening
Die shift inspection

Lay-up

Lamination

Via definition
laser drilling

Copper plating,
RDL structuring

Package separation

Die
Leadframe
Copper foil/ platedcopper
FR4 laminate
Prepreg (non-cured laminate)

see also A. Munding, A. Kessler, T. Scharf, B. Plikat, K. Pressel, Laminate Chip Embedding Technology, ECTC 2017, Lake Buena Vista (Fl)

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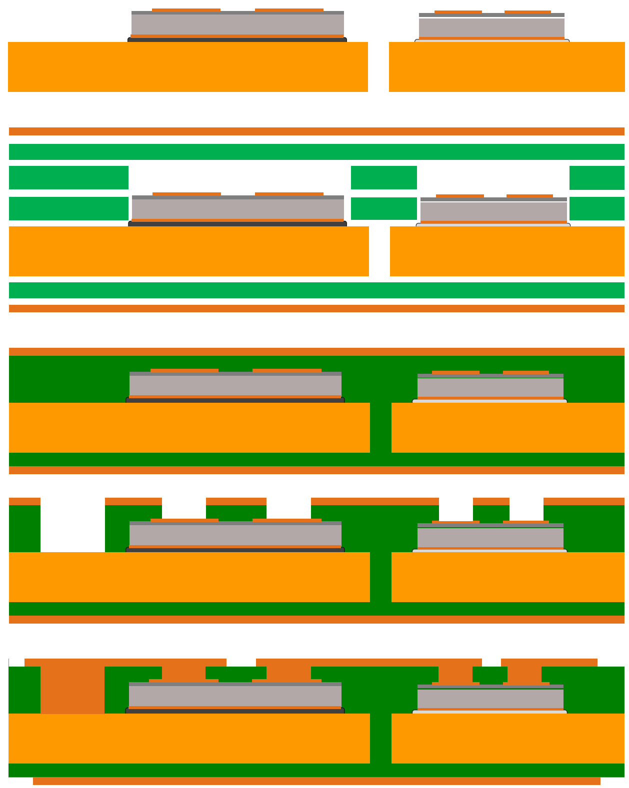

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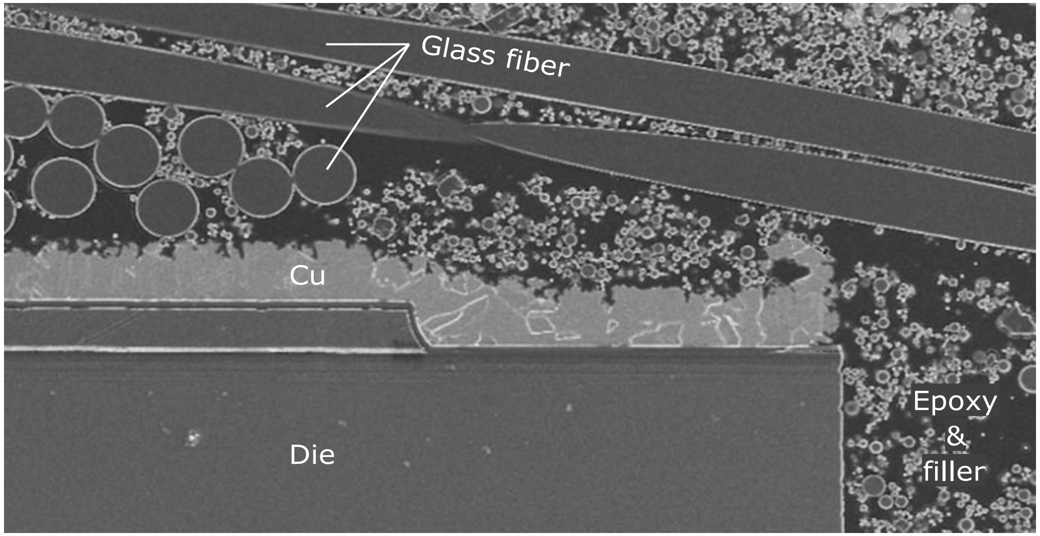
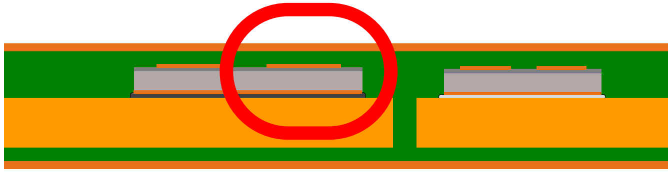
Laminate chip embedding technology

SEM cross-section of a die with roughened Cu





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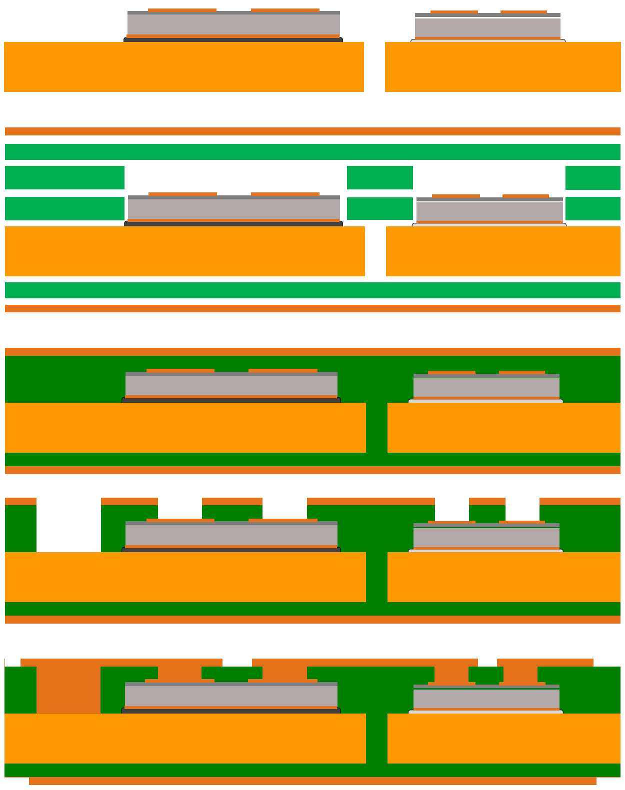

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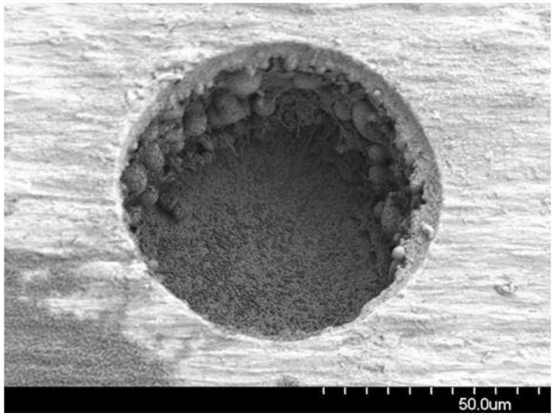
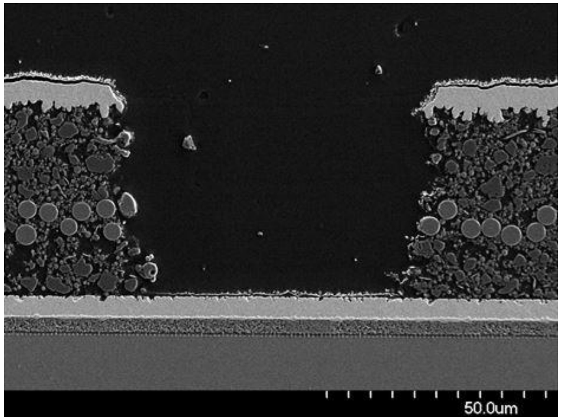
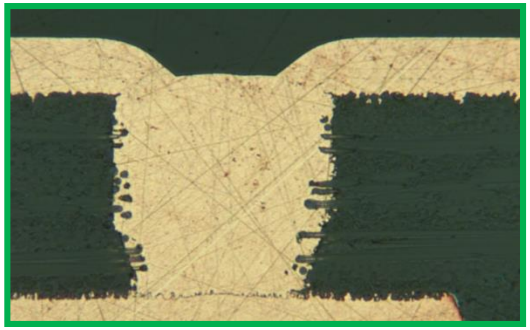
Laminate chip embedding technology

Drilling of via hole by laser



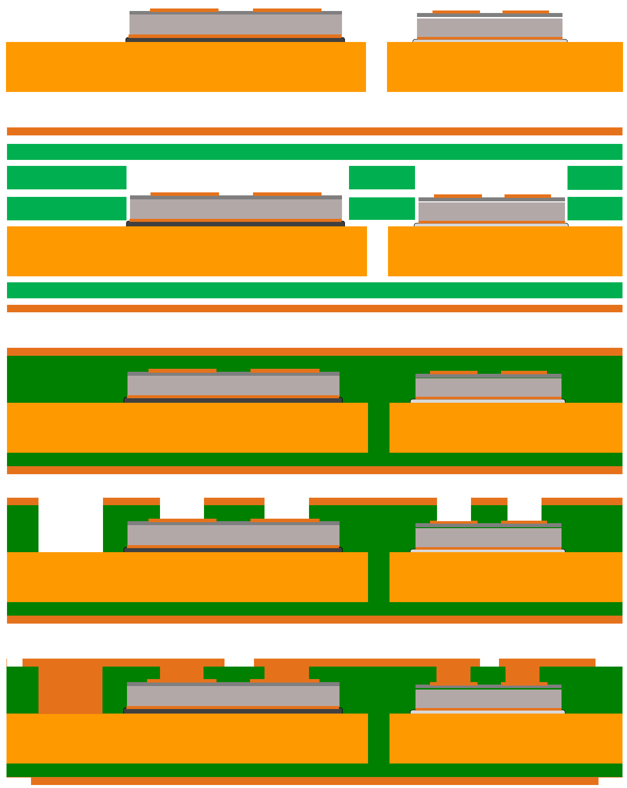
SEM cross-section of a laser drilled via





filled via

Laminate chip embedding process chain for thin die packaging



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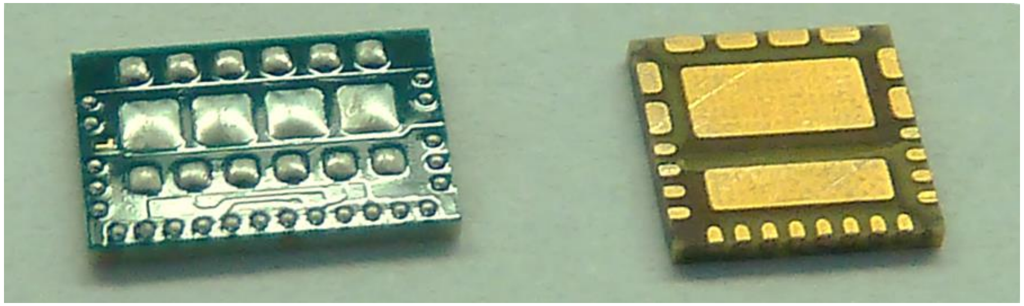
Laminate chip embedding technology

We structure the copper layers to shape the redistribution layer by photolithography

Additional layers can be applied afterwards either on one or both sides of the panel to allow for more complex products.



Left: Package to board interface; right: interface with final finish only

package-to-board interface can be either finished by plating of a solderable metallization or by application of solder resist.

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1 Motivation

2 Laminate chip embedding processes and technologies

3 **The importance of Chip-Package-Board Interaction**

Improvement of reliability by glass fiber filled resin

Void free lamination by application of Monte Carlo simulations

Avoidance of chip metallization damages by laser

4 Application examples

5 Conclusion

Reliability improvement by glass fiber filled resin

Highly filled resin has a lower CTE and therefore better matches the CTE of silicon => low thermo-mechanical stress

Evaluation of two extremes:

- low filled RCC (resin coated copper)
- Highly filled prepreg material

At the initial state after assembly both material classes performed well.

But we saw clear differences after application relevant stress tests:

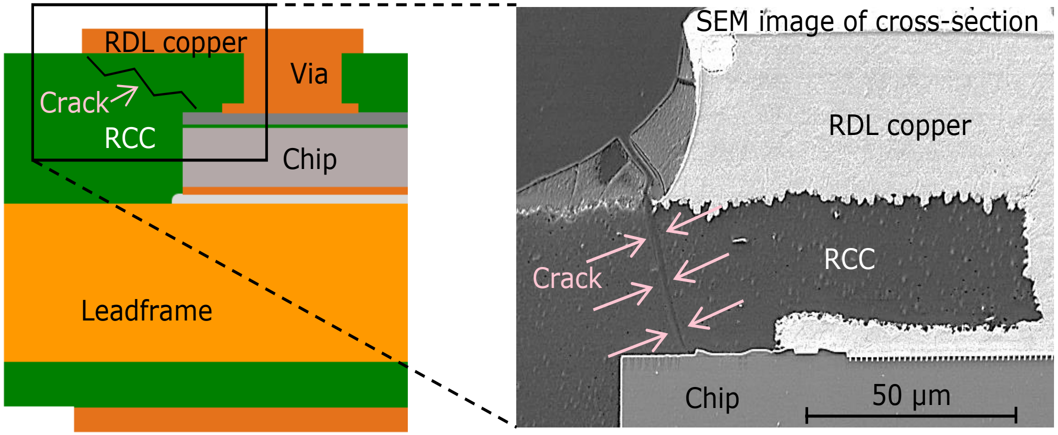
- Temperature cycling from −55 °C to 150 °C
- High temperature storage at 150 °C

=> resulted in a clear degradation of the RCC material.

see also A. Munding, A. Kessler, T. Scharf, B. Plikat, K. Pressel, Laminate Chip Embedding Technology, ECTC 2017, Lake Buena Vista (Fl)

Reliability improvement by glass fiber filled resin

We observed that cracks started to form from the corners of the RDL copper towards the chip surface



Cross-section of an RCC laminated system after stress. Cracks in the RCC material form between RDL copper and the chip surface.

A clear difference can be seen in dynamic mechanical analysis curves:

- the high-T_g FR4 material remained almost unchanged after 500 h at 150 °C;
- the RCC showed strong degradation already after 240 h.

Reliability improvement by glass fiber filled resin

- The lower CTE of filled material strongly reduces the intrinsic stress within material.
- In addition, the glass fibers can stop an initiated crack before it reaches the chip surface.
- T-stable materials are required

Conclusions:

- high quality materials are needed for this application.
- for FR4 materials this usually means that a high-T_g and high filling is required.

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=> more cost

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The two challenges of the lamination process

There are two major challenges we have to consider for the lamination:

i) Gaps must be completely filled with resin
ii) Secure that deviations of the free volume can be compensated

for i)
The first challenge is that after lamination we have to ensure that all gaps in the system are completely filled with resin, because voids are a well-known reliability risk.

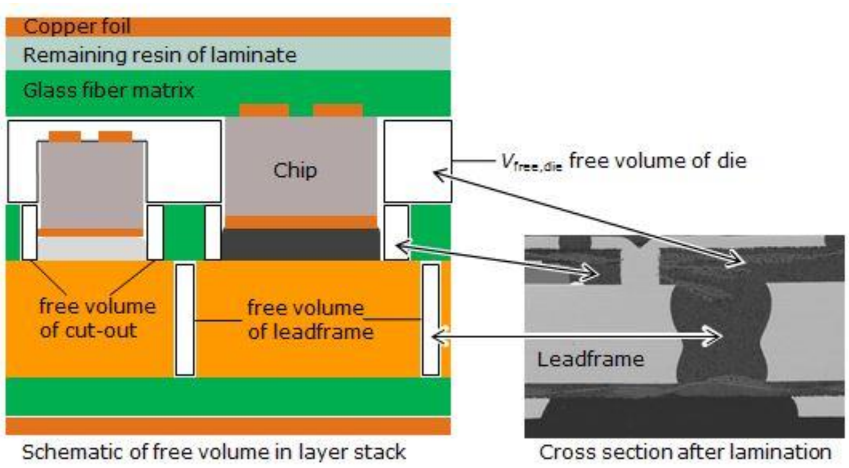


Illustration for definition of the free volume

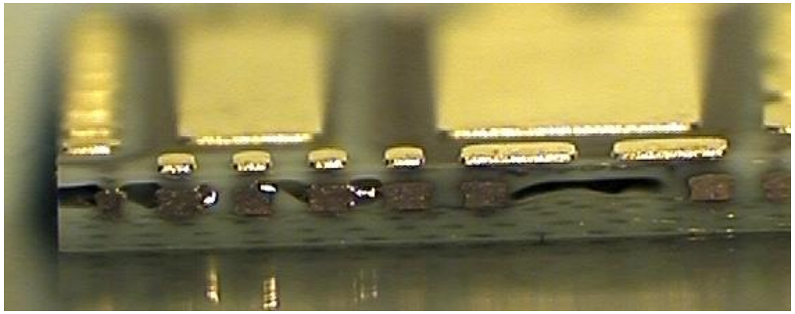
The free volume needs to be smaller than the total available amount of resin provided by the laminate material stack

see also A. Munding, A. Kessler, T. Scharf, B. Plikat, K. Pressel, Laminate Chip Embedding Technology, ECTC 2017, Lake Buena Vista (Fl)

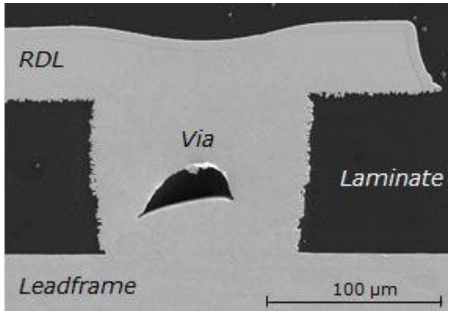
The two challenges of the lamination process

for ii)
ensure that the deviations of the *free volume* can be compensated at all time with the resin of the prepreg layer stack including its deviations in height and resin content.

A stable and safe process window is essential: In case of insufficient resin we obtain voids in the laminate, in case of too much resin we obtain voids in the vias.



Cross-section of a laminate chip embedding package showing voids in the laminate



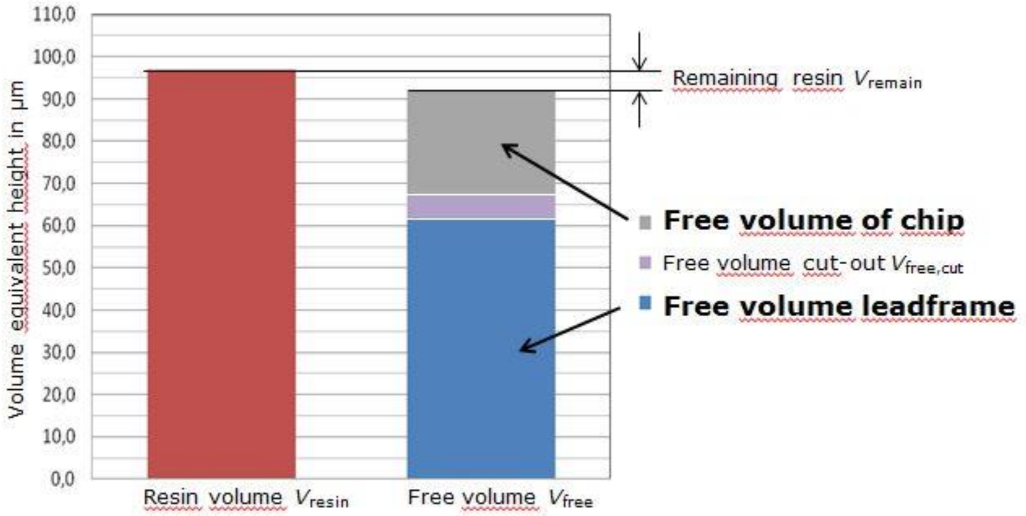
SEM cross-section view of an RDL to leadframe via with a void => reliability risk

2018-03-07 Klaus Pressel, Infineon

Process Simulation

- We found out that the lamination of a leadframe based chip embedding system is limited to a maximum *free volume* (otherwise we face problems with voids in laminate or voids in vias).
- We showed that the two most critical contributors to the free volume are the leadframe and the chip

Contributors to the free volume, the largest amount is from the gaps in the leadframe.



By Monte-Carlo simulation we calculated the cumulative distribution function of the remaining resin height vs. sample count

see also A. Munding, A. Kessler, T. Scharf, B. Plikat, K. Pressel, Laminate Chip Embedding Technology, ECTC 2017, Lake Buena Vista (Fl)

Process Simulation Results

- After analyzing cause and effect of the free volume we showed that the leadframe needs the largest amount of resin
- Our measurements also showed that the leadframe is the largest contributor to deviations in *free volume*. The leadframe is essential for applications with vertical current flow and the need of a good heat transfer.
- Special care has to be taken to approach the challenge of lamination with leadframes.
- Regarding the chip height we specified upper and lower limits. Furthermore we implemented a process control step which measures the chip height and die attach height.
- With these process control measures and a proper specification of all incoming materials we were able to proof that we can ensure a reliable quality in volume production.

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=> but more cost because of careful process control

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Via Drilling Process

<u>Micro-via process in PCB technology:</u>
(laser drilling of holes and subsequent galvanic filling of these connecting holes)

A standard Al chip metallization - as it is typical for wire bonding processes - is not suitable for the micro-via process:

- it is easily damaged by laser drilling
- it is not compatible to the subsequent chemical cleaning and galvanic filling processes

=> different last metal on the landing pads is required

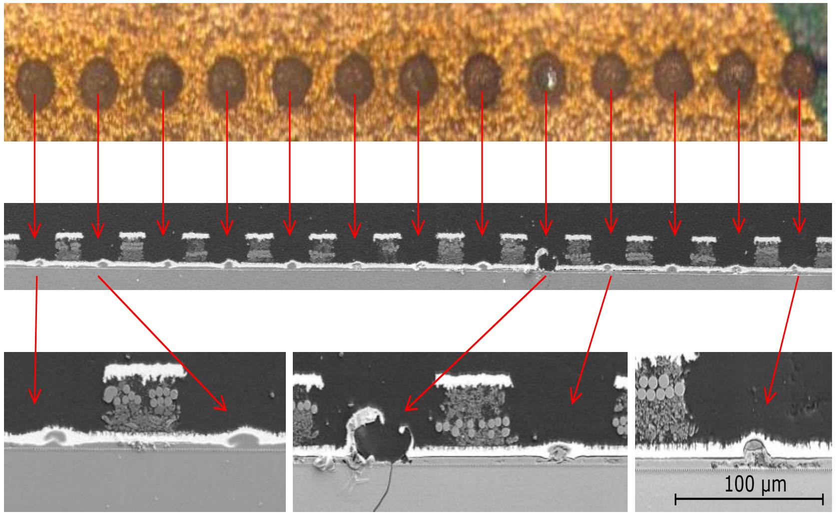
=> Cu is the obvious first choice.

Comment: This landing pad issue is a major difference to a PCB technology

Via Drilling Process

We used laser drilling machine for PCB micro-vias with 9.4 µm wave-length and variable spot size, pulse power, and pulse duration:

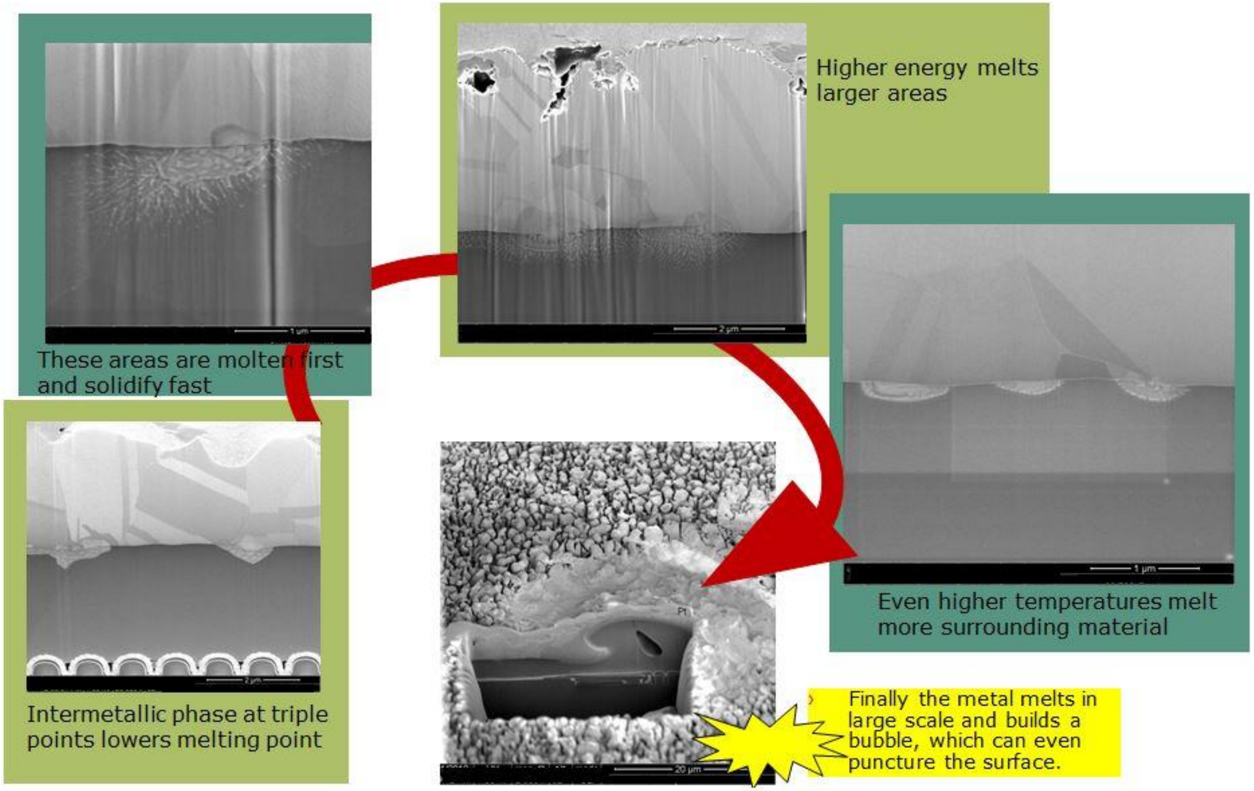
We have 2 extremes:
too weak laser parameters => holes are not formed properly
Too strong laser parameters => damage of landing pads



Optical microscope image of a row of micro-vias with different degrees of damage; bottom: SEM cross-sections of these micro-vias

Via Drilling Process

To avoid these laser damages: systematic analysis of physical mechanisms



- The laser drilling process consists of the evaporation of the covering material and the formation of plasma
- The whole process has to be driven in a way that the heat affected zone (HAZ) is extremely small

Via Drilling Process: Conclusions to prevent damage

- The single pulse energy has to be limited to a safe range.
- A possible measure to gain a wider safety margin is the introduction of a diffusion barrier layer between Cu and Al (inhibits the formation of the AlCu phase and the solution of Cu in Al).
- Another approach is to increase Cu thickness such that the heat affected zone remains completely within the Cu layer (Cu thicknesses above 11 µm are proper; expensive)
- In addition, a smooth, reflective surface is very advantageous for reducing the absorption and therefore reducing the HAZ (interferes with use of typical adhesion promotion mechanism)
- Comment: A complete avoidance of low melting materials strongly increases the possible process window for a laser drilling process

⇒ We defined that no changes in any metal layer are allowed, clearly no melting and also no recrystallization.

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- Comment: A complete avoidance of low melting materials strongly increases the possible process window for a laser drilling process **(=> another cost constraint)**

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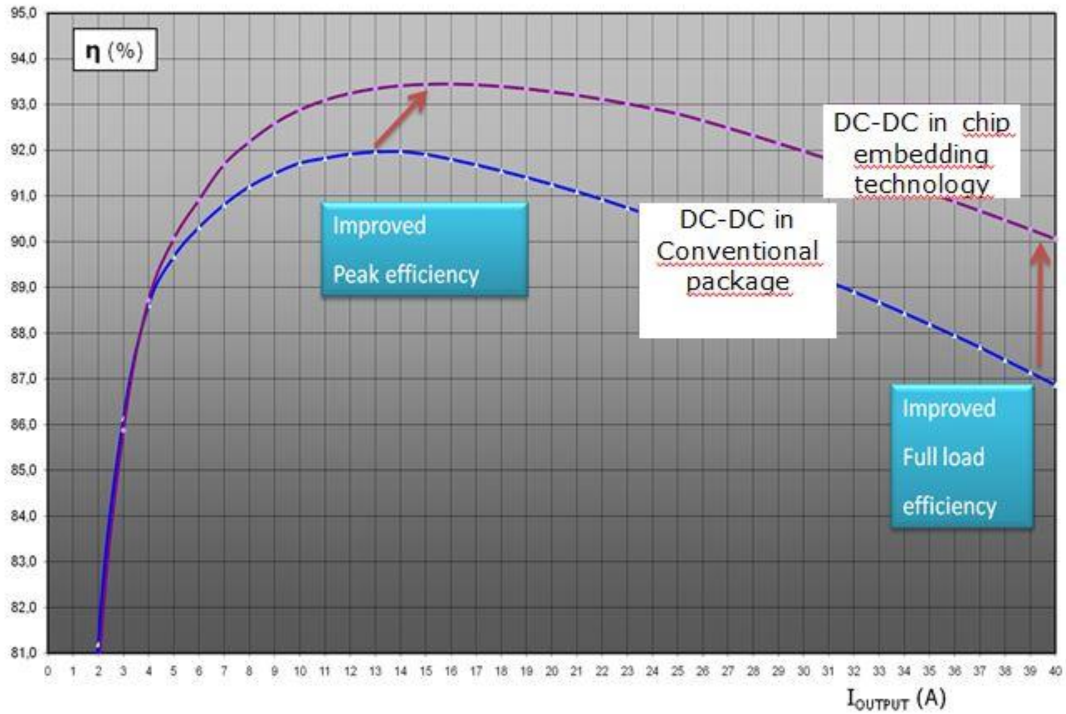
Application example I: Improved DC-DC Converter performance by chip embedding

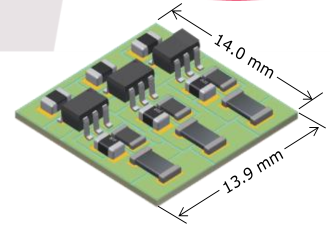
Comparison of Chip embedding device versus conventional technology:

- Significant reduction (~25%) of conversion losses
- 30% footprint size reduction



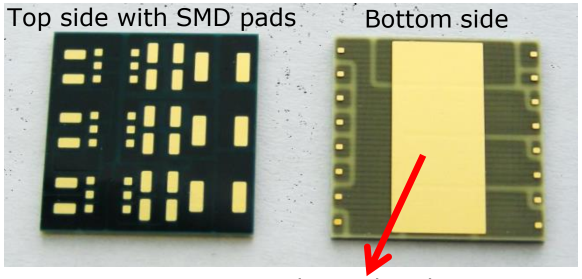
Excellent performance achieved for Infineon's chip embedding technology based on Cu leadframe

Application example II: System integration capability demonstrated LED module



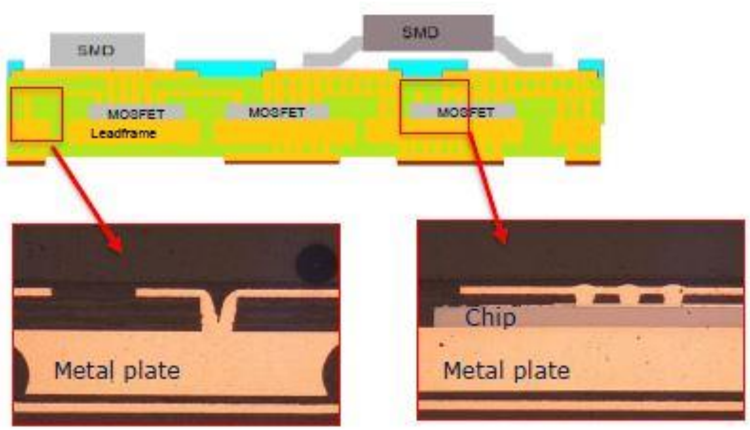
Laminate module with 7 embedded MOSFET chips

European research project with focus on energy efficiency (26 research partners from 6 countries)



Results:

- Die embedding is a suitable integration technology, especially for power packages due to the thick copper on chip backside
- Performance and dimensions are main drivers for the technology
- For the demonstrator fulfillment of the targets finally was proven



Cross section of embedded die demonstrator

Final eRamp LED demonstrator: The area for power components can be reduced by a factor of about 3 using chip embedding in laminate technology

Source: ENIAC JU Project "eRamp"

Content

Conclusion for thin die chip embedding

- Chip embedding technologies with fan-out capabilities require competence from chip, package, and board/system community
- Proper material choice and processing are key for a reliable technology

  - Glass fiber based material is more robust than resin coated copper
  - A careful choice of laser parameters is required to avoid laser damages

- Careful inspection and process monitoring is required
- Cu-based leadframe chip embedding technologies show excellent application potential for DC-DC converter and system integration
- Close collaboration between Si frontend, packaging and board experts is needed.

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=> cost trade-offs need to be considered

Thank you for your attention

Thank you to my Infineon colleagues who supported this work, especially to Andreas Munding, Boris Plikat, Thorsten Scharf and Angela Kessler

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see also A. Munding, A. Kessler, T. Scharf, B. Plikat, K. Pressel, Laminate Chip Embedding Technology, ECTC 2017, Lake Buena Vista (Fl)

