Circuit Sizing w/ Corner Models
Challenges & Applications

Matthias Sylvester

April 11th, 2013

Agenda

- Introduction
- Corners & Process Monte Carlo
- Application: Performance Tuning
- Application: Customer Cases

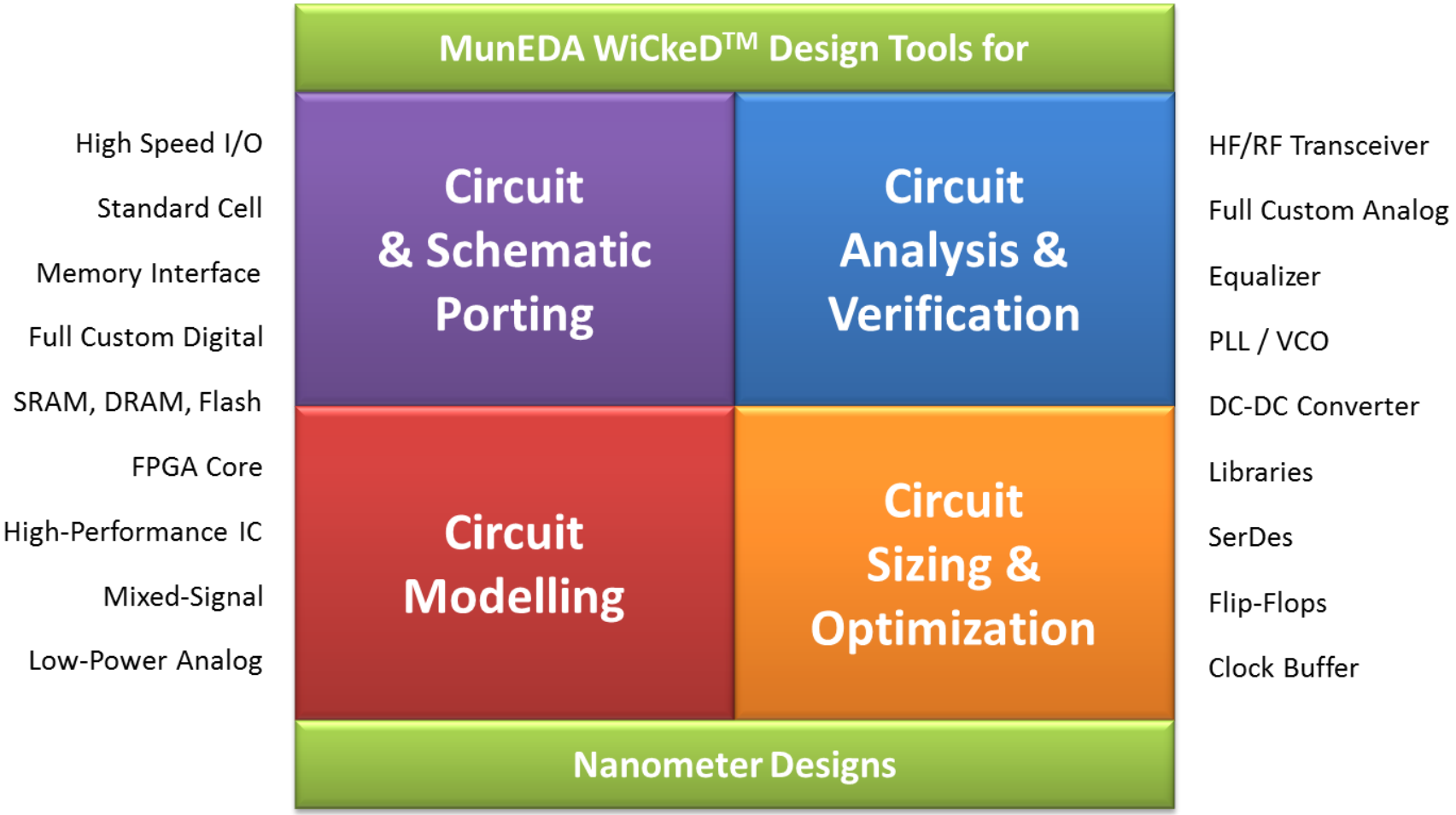
MunEDA Corporate Overview

- **EDA Software Vendor – Design Tool Suite WiCkeD™ for Porting, Analysis, Modeling & Sizing of nanometer IC designs**
- **Founded in 2001 – Headquarters in Munich Germany**
- **Worldwide Sales & Support Offices in USA, Korea, Taiwan, Japan, UK, Ireland, Scandinavia, South America**
- **Worldwide Customer Base of Semiconductor IDMs, Fabless Design Houses & Foundries**

MunEDA Corporate Headquarter in Munich, Germany

MunEDA Inc. (US Office) in Sunnyvale, CA, USA

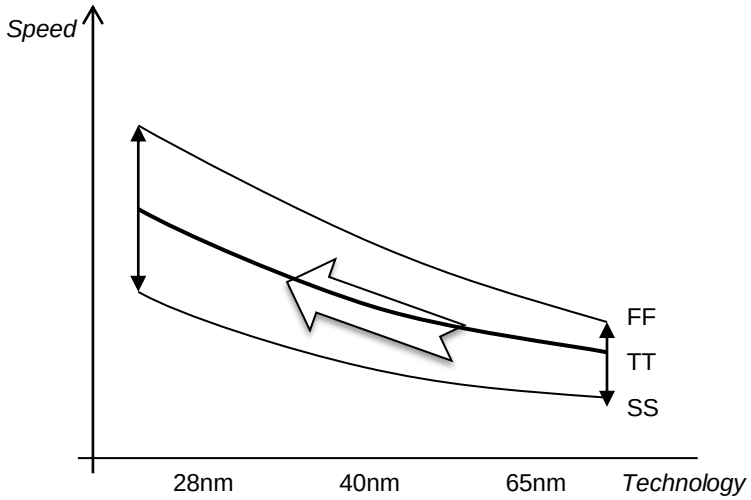
MunEDA WiCkeD™ Circuit Design & Sizing Environment



Challenges of advanced node design

- **Circuit sizing: Designers have to carefully set circuit parameters like W, L, R, C, …**
  - to meet performance targets
  - to reduce sensitivities vs. Vdd, temperature, process, LDE, mismatch

- **Creating a robust design becomes more challenging in advanced nodes**
  - higher sensitivity vs. supply voltage
  - higher sensitivity vs. temperature
  - reduced voltage headroom
  - wider corner spread
  - increased local variation
  - layout dependent effects (LDE)



See Beacham et al. (Synopsys Inc.): “Mixed-Signal IP Design Challenges in 28 nm and Beyond”. www.design-reuse.com

Process corner support

- **Process variation is usually modeled in two ways**
  1. Process corners (ss/ff/sf/fs/ …)
  2. Process Monte Carlo
     vth ~ $N(\mu_{vth}, \sigma^2_{vth})$
     tox ~ $N(\mu_{tox}, \sigma^2_{tox})$
     …

Most foundry PDKs contain both models.

Local variation (mismatch) is always modeled by MC statistics.

- **What‘s the advantages / disadvantages of using corners or process MC?**

Corners & Process Monte Carlo

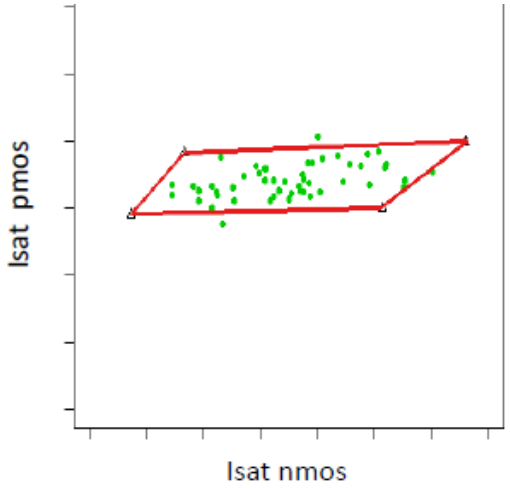
Comparison: Corners vs Process Monte Carlo

	Corners	Process MC
Simulation effort for pure CMOS	low	medium
Simulation effort for large # of device types (MOS/BJT/res/cap/…) per design	high	medium
Check timing for full-custom digital designs	yes	no
Correct device correlation	no	yes
Check operating conditions of analog designs	yes	yes
Check analog performance variability	no	yes
Estimate yield	no	yes
Process parameter sensitivities	no	yes

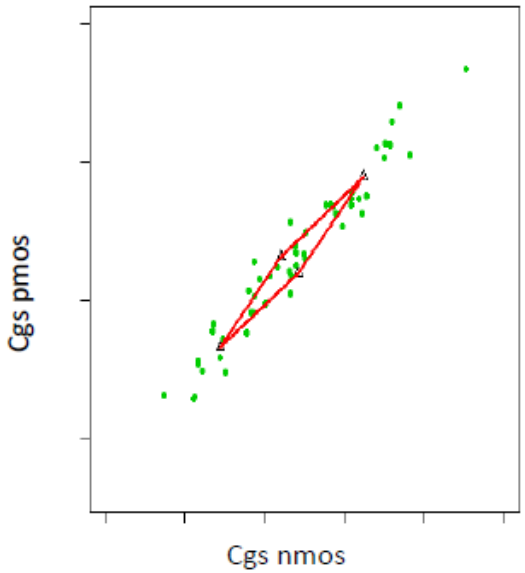
Analog performance variability

→ **Compare ss/ff/fs/sf corner results with global MC for a popular 65nm process that's used by analog designers worldwide:**

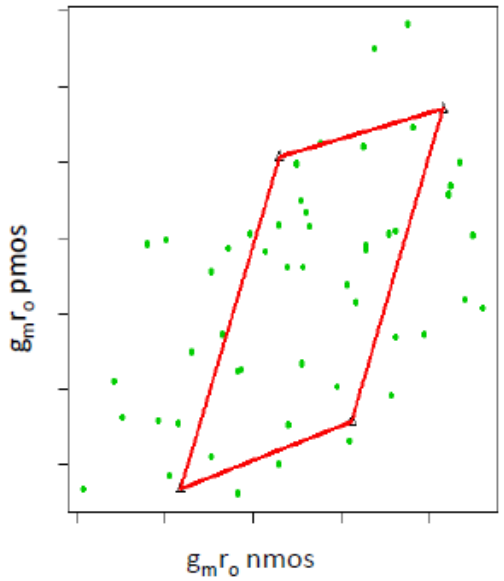
Red line connects corners (ff,ss,fs,sf).
Green dots: global MC samples



Isat: realistic corner results, fits very well



Cgs: analog feature, error >80%.



Gain: analog feature, error >30%.

→ Good estimate for Isat, Vth; difference at analog small signal parameters.

Tools of WiCkeD – Analysis & Verfication – WCO Worst-Case Operation

Circuit Analysis & Verification

- Find worst-case operating condition & corner
- Includes structural constraints
- Can handle non-linear dependency (=worst-case not in the corner)

File Analysis Options Help

Performance	Specification Type	Specification	Nominal Value	Worst-Case Value	temp	vdd
cmrr	Lower	> 70	134.7	131.3	80 C	3.2 V
Ft	Lower	> 5 meg	6.378 meg	5.747 meg	80 C	2.8 V
gain	Lower	> 80	83.85	79.71	80 C	3.2 V
offset	Lower	> -4 m	8.34 u	4.638 u	0 C	2.8 V
	Upper	< 4 m	8.34 u	15.6 u	80 C	3.2 V
output_voltage_range	Lower	> 2.6	2.805	2.641	80 C	2.8 V
phase_margin	Lower	> 70	88.44	87.68	0 C	2.8 V
power	Upper	< 200 u	172.9 u	213.3 u	80 C	3.2 V
psrr	Lower	> 70	97.5	93.51	80 C	3.2 V
slewF	Lower	> 2 meg	3.834 meg	3.219 meg	0 C	2.8 V
slewR	Lower	> 2 meg	3.55 meg	2.978 meg	0 C	2.8 V

Tools of WiCkeD- Analysis & Verification — CRN Corner Run Analysis

Circuit Analysis & Verification

- Check all corners, show corner overview and summary
- Distributed simulation in a network of hosts

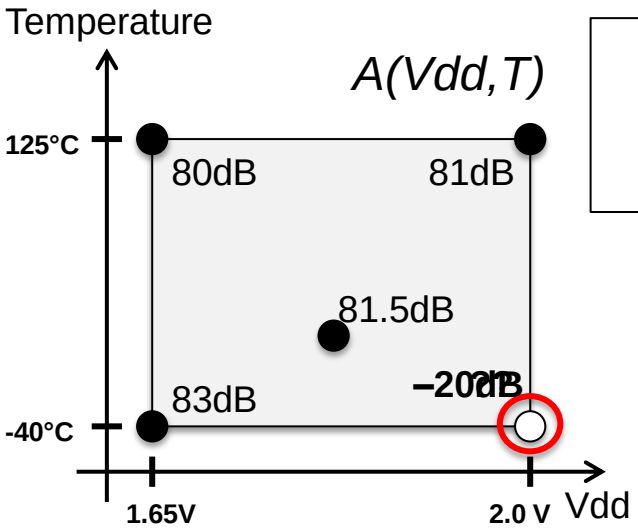
File Analysis Options Help

Summary | Details

Performances	Max. Value	Min. Value	Diff.	Rel. Delta (Max.)	Rel. Delta (Min.)	Upper Margin	Lower Margin	Upper Guard Band	Lower Guard Band
cmrr	125.2 @ ss	124.2 @ ff	939 m	0.37%	0.38%	---	54.25	---	> 100%
Ft	3.13 meg @ ss	3.03 meg @ ff	100 k	1.63%	1.62%	---	-969.8 k	---	< -100%
gain	73.56 @ ss	73.39 @ ff	173.4 m	0.12%	0.12%	---	-6.611	---	< -100%
offset	13.41 u @ ff	13.31 u @ ss	96.3 n	0.38%	0.34%	3.987 m	4.013 m	> 100%	> 100%
output_voltage_range	2.765 @ ff	2.764 @ ss	530 u	0.01%	0.01%	---	164.4 m	---	> 100%
phase_margin	89.53 @ _default	89.53 @ ss	600 u	0%	0%	---	29.53	---	> 100%
power	140.8 u @ ss	138.3 u @ ff	2.484 u	0.92%	0.86%	109.2 u	---	> 100%	---
psrr	45.86 u @ ff	44.38 u @ ss	1.476 u	1.69%	1.58%	454.1 u	544.4 u	> 100%	> 100%
slewF	2.986 meg @ ss	2.91 meg @ ff	75.44 k	1.30%	1.26%	---	910.5 k	---	> 100%
slewR	2.71 meg @ ss	2.641 meg @ ff	68.69 k	1.32%	1.25%	---	641.4 k	---	> 100%

Use Analysis->Define Analysis to start analysis

Finding worst-case conditions



If you simulated all but one corner, is there a reliable way to guess its value?

Unfortunately, no.

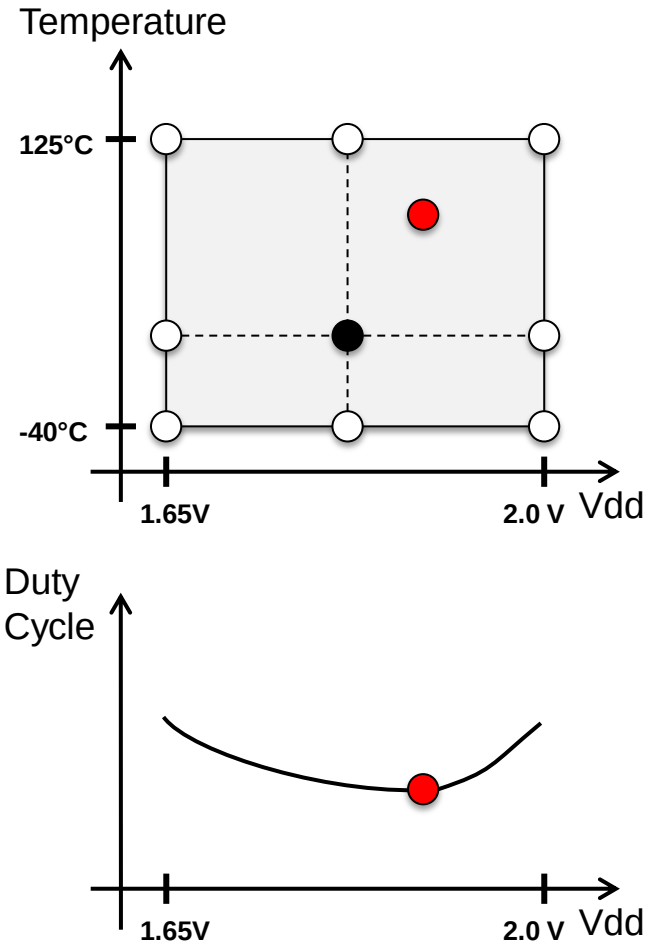
No matter what kind of model you use and no matter how many parameters there are, extrapolating models over a large distance is unreliable.

WiCkeD uses methods to build models over operating parameters to guess where's the worst-case condition before simulating it.

This is very useful to speed up optimization inside the optimizer's loop.

But for verification, better don't skip corners just because they are OK in a model.

WiCkeD WCO modeling



For continuous operating parameters:

- Star + Box DOE
- Quadratic model to detect non-linearities, resimulating estimated minima
- Checking corners

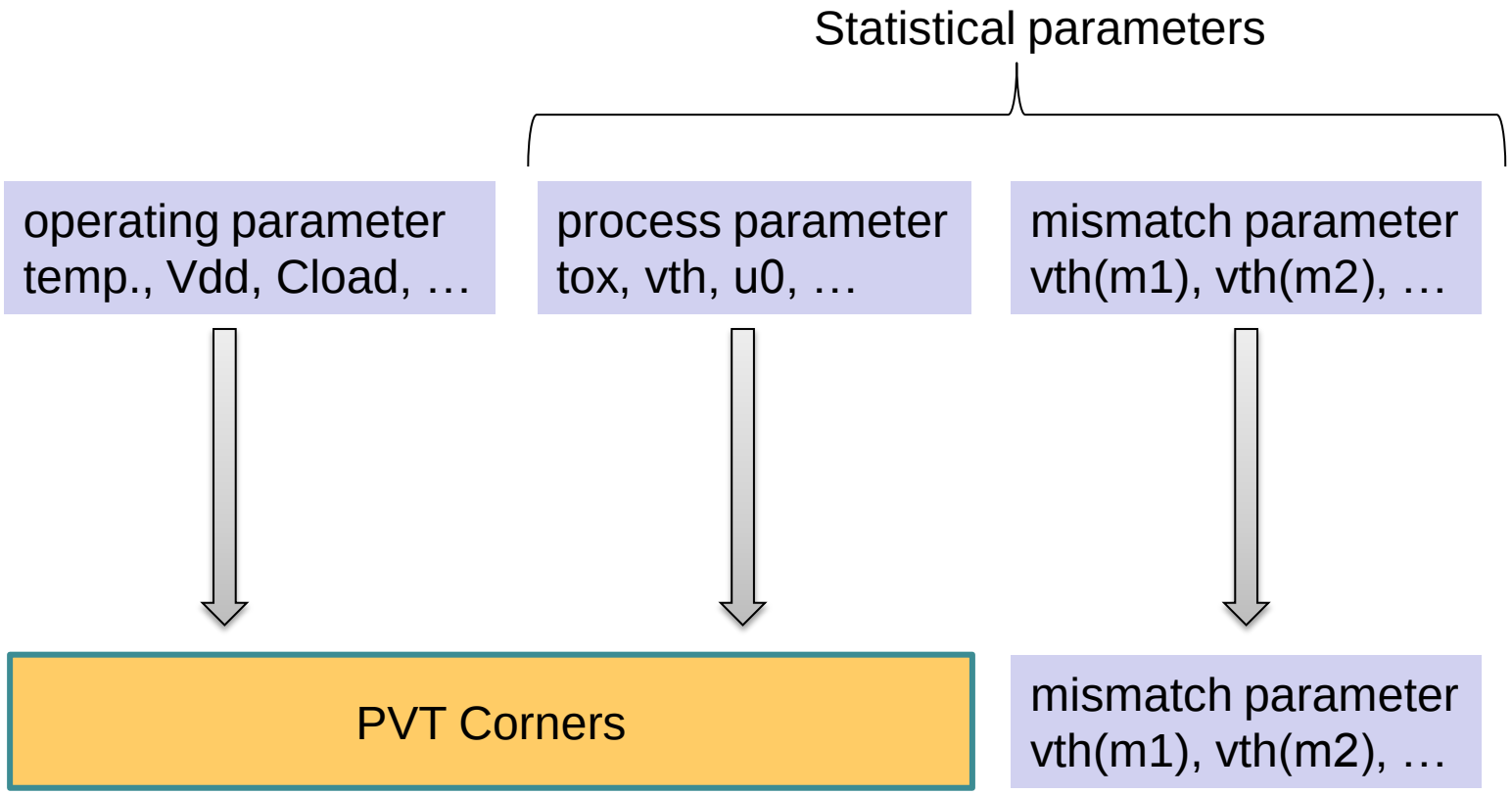
For larger # of operating parameters:

- Option to run only Star DOE, create quadratic model and re-simulate

For enumerated corners:

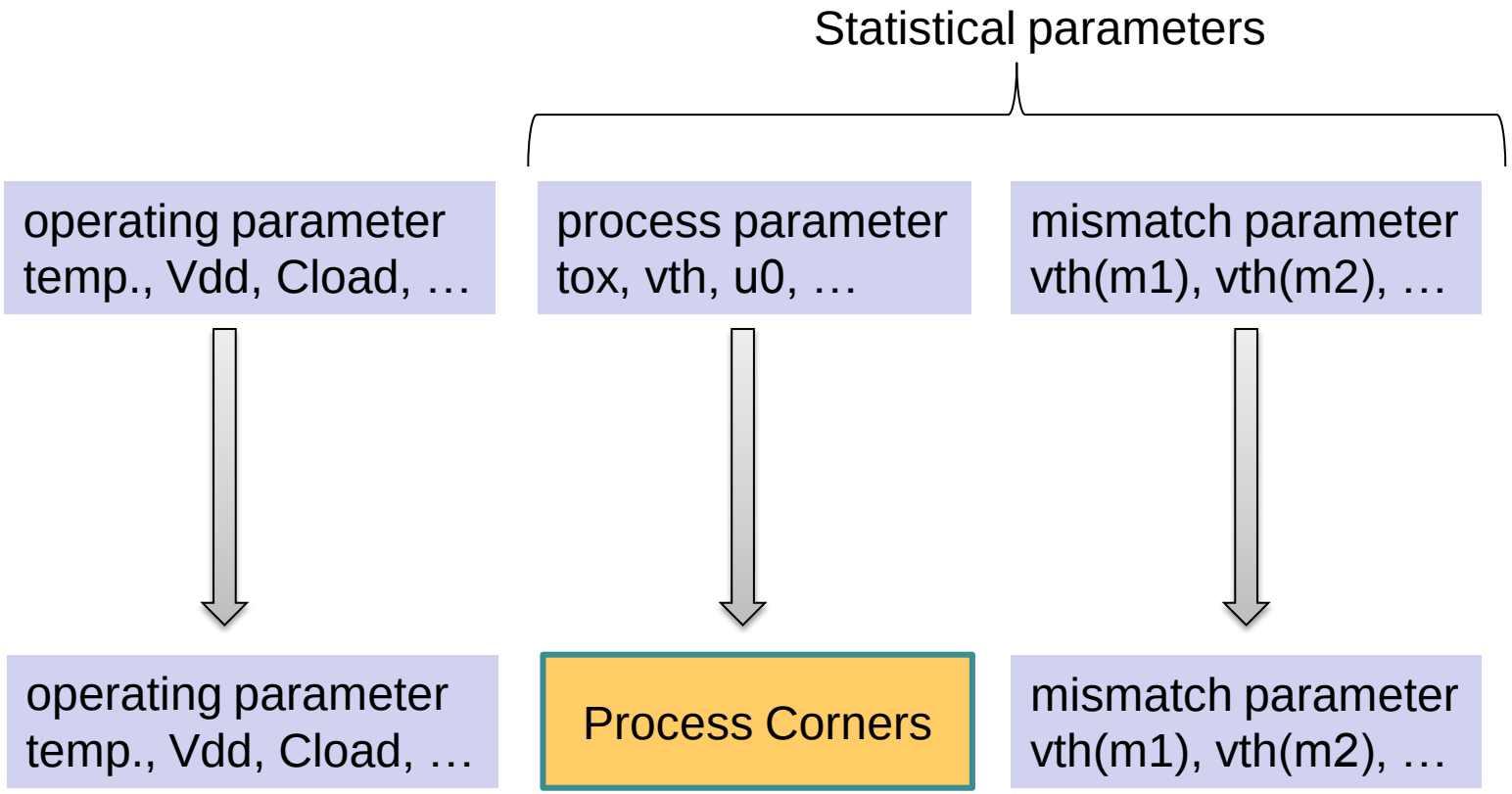
- Full run, no short-cuts

PVT corners and parameters (1)



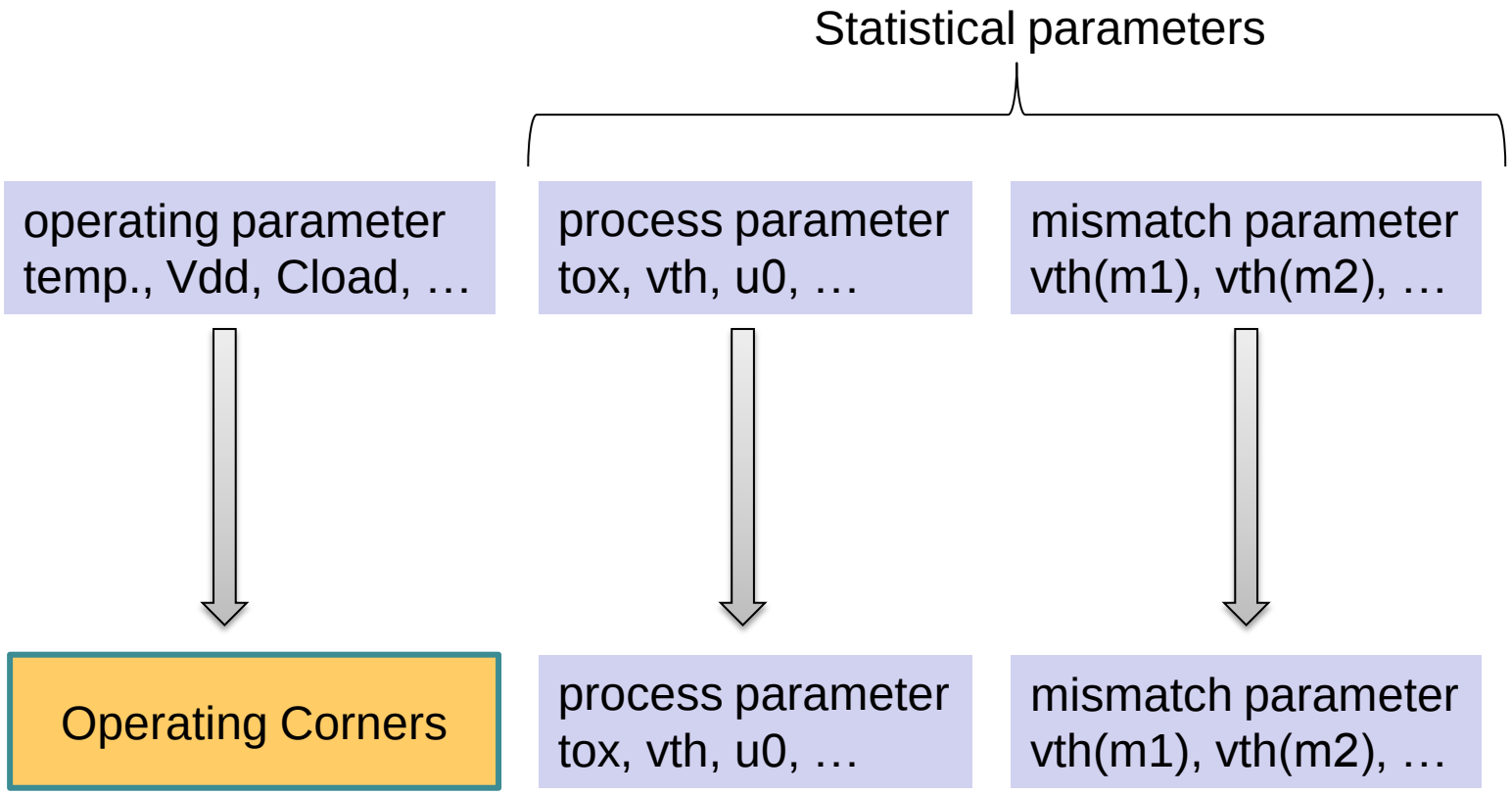
- **Most usual case: instead of operating parameters and process parameters, corners are defined.**
- **But there are alternatives …**

PVT corners and parameters (2)



- **WCO can handle continuous operating parameter together with corners**
- **Allows temperature sweeps at corners**

PVT corners and parameters (3)



- **MCA can vary process parameters also if there are corners defined**
- **Enables running process MC for selected corner conditions**

Performance Tuning

Performance Tuning

- **Many circuits require precise tuning of fast transient signals, noise, transfer characteristics, …**

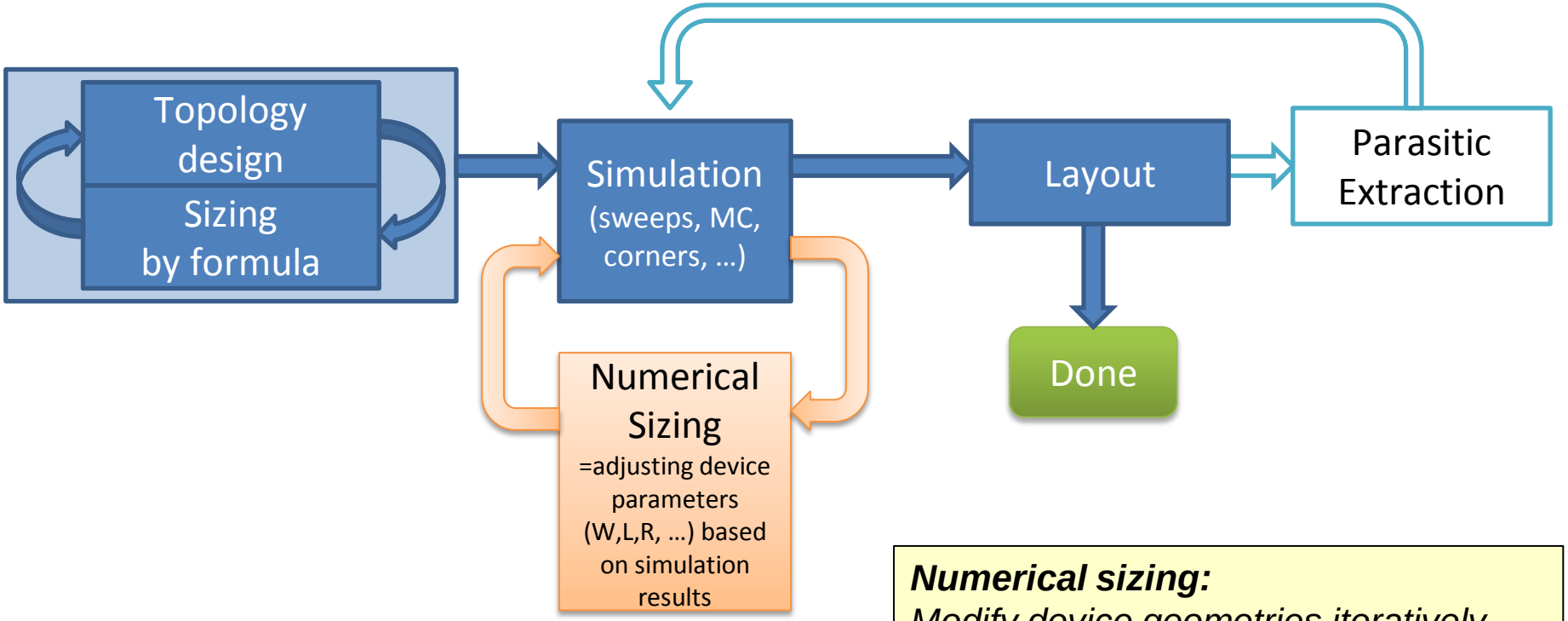
- **Designers have to find good values for all transistors‘ W and L that fulfill all specs considering**
  - Operating conditions
  - Process variation (global Monte Carlo statistics, or corners)
  - Mismatch (on-chip variation)

- **Designers re-size the circuit whenever**
  - specs get updated
  - model files get updated
  - multiple versions are to be generated (low-leakage, high-speed, …)
  - IP is ported to a new process (IP reuse, design migration)

→ Designers spend much time with iterative simulation-based sizing.

Numerical Sizing in Advanced Circuit Design

Circuit Sizing & Optimization



Traditional analog design method:
Simulation is used as a verification tool only, but not as a design tool.

Good for small low-speed analog design.

Numerical sizing:
Modify device geometries iteratively based on simulation results (after traditional initial design).

Needed for high-speed design, RF, custom digital.

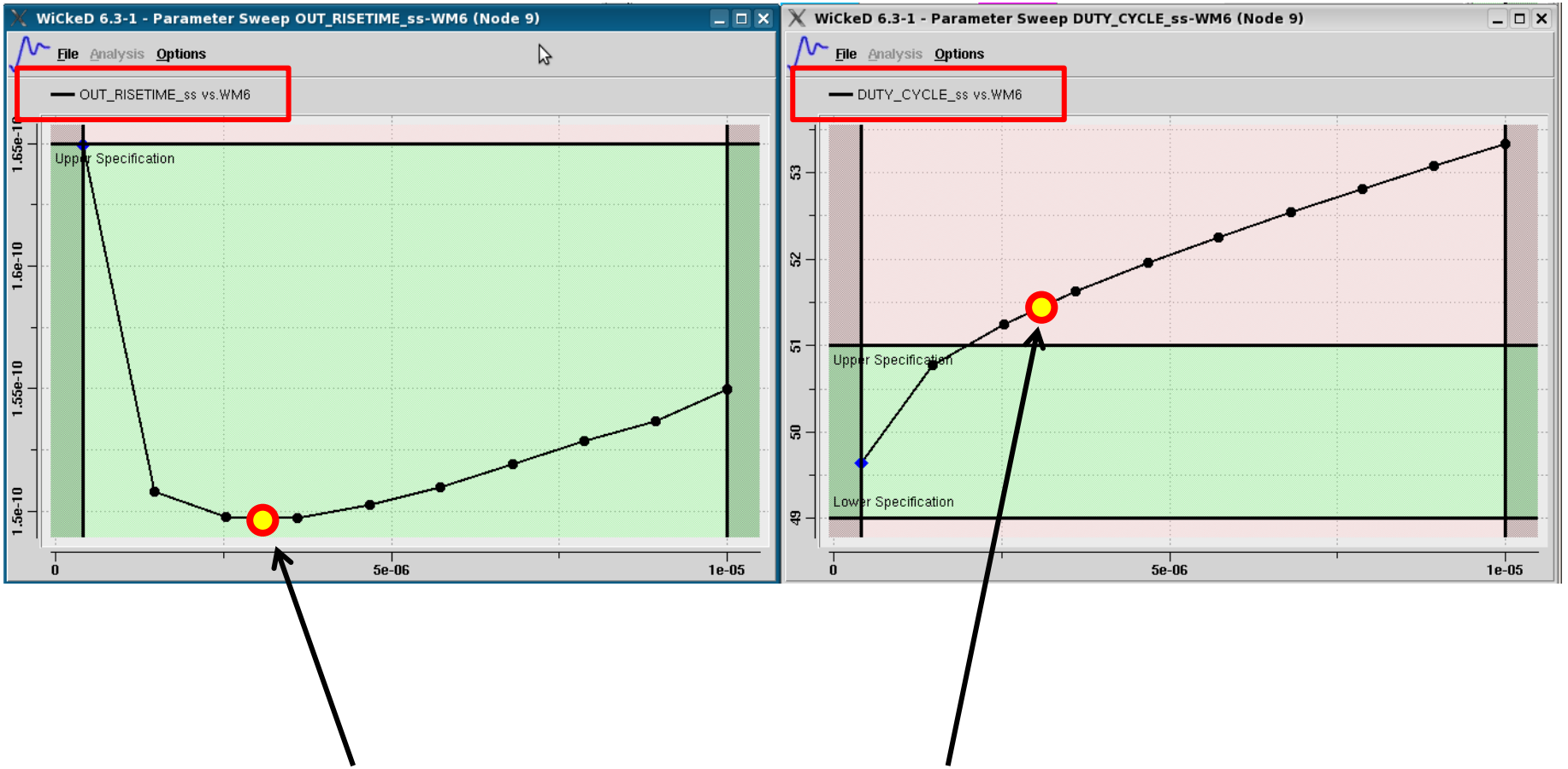
What makes sizing difficult?

- **Manual sizing is easy, as long as**
  - symbolic small-signal approximations are sufficiently accurate
  - there are no tough trade-offs between multiple hard specs
  - process variation and mismatch can be compensated by safety margins and structural solutions (feedback, symmetry, trimming, …)
  - there are only few design variables, best case with a 1:1 relationship to specs

- **Reality is not as easy as an analog textbook example …**
  - Large impact of second order effects, parasitics, noise, …
  - Non-linear specs with no good symbolic estimate
  - Impact of PVT variation and mismatch to be compensated by sizing
  - Tight specs, multiple trade-offs
  - Many design variables, *m:n* dependency to specs

What makes sizing difficult?

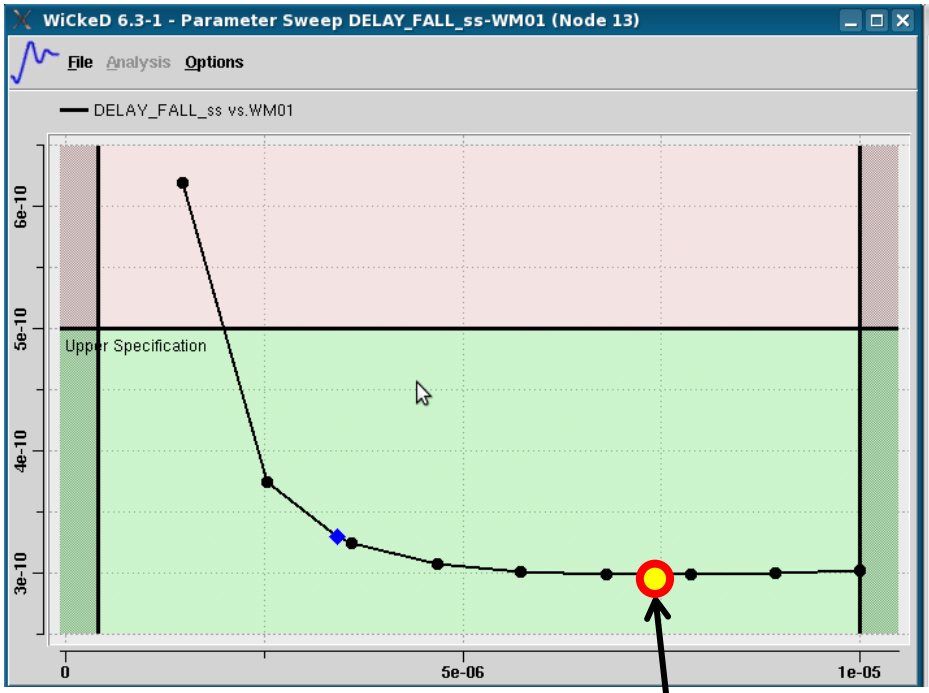
↗ Trade-offs :

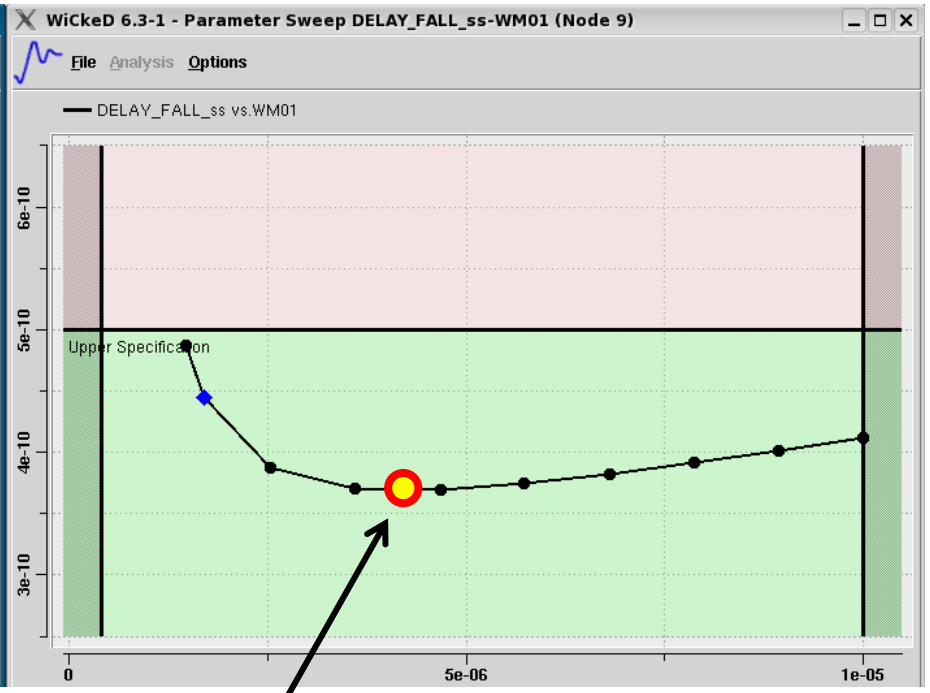


The optimum of one spec violates another spec

What makes sizing difficult?

↗ Non-linear parameter dependency with mixed effects

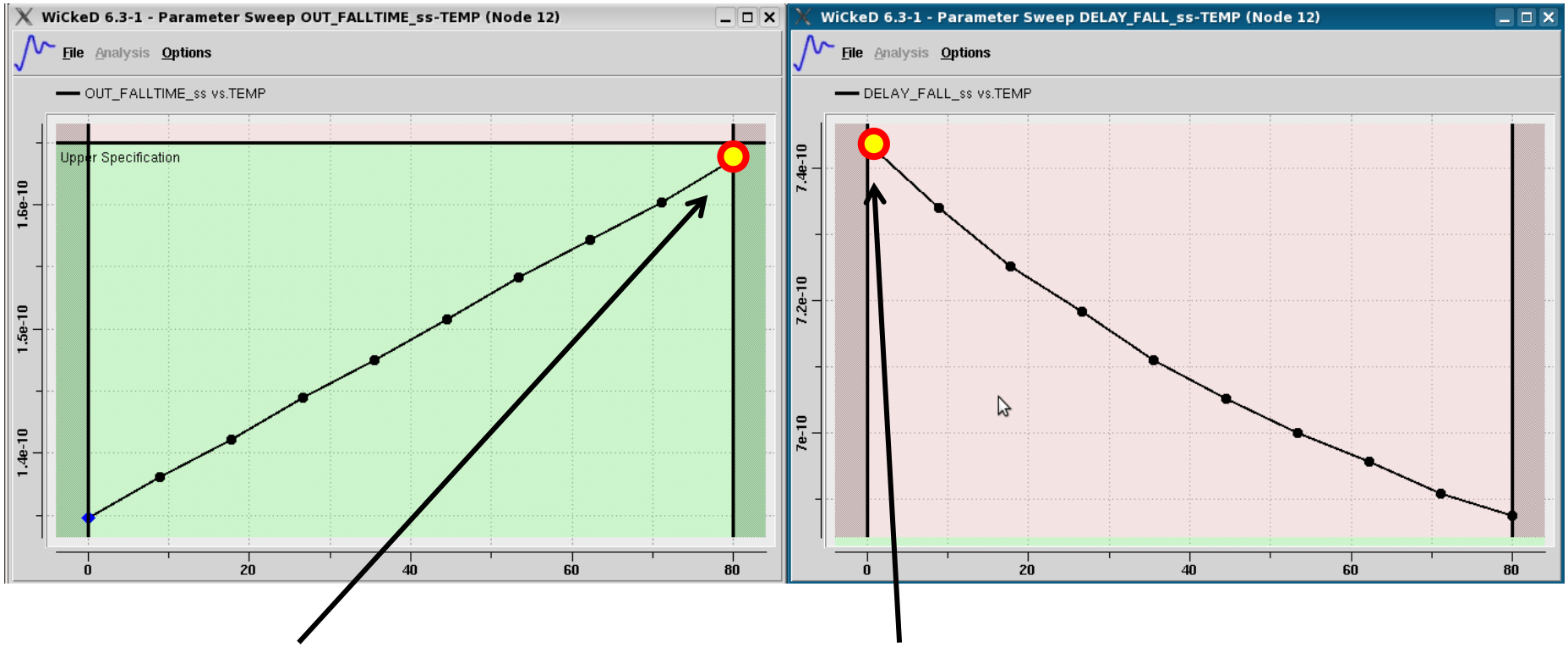




The optimum of one parameter depends on the value of other parameters

What makes sizing difficult?

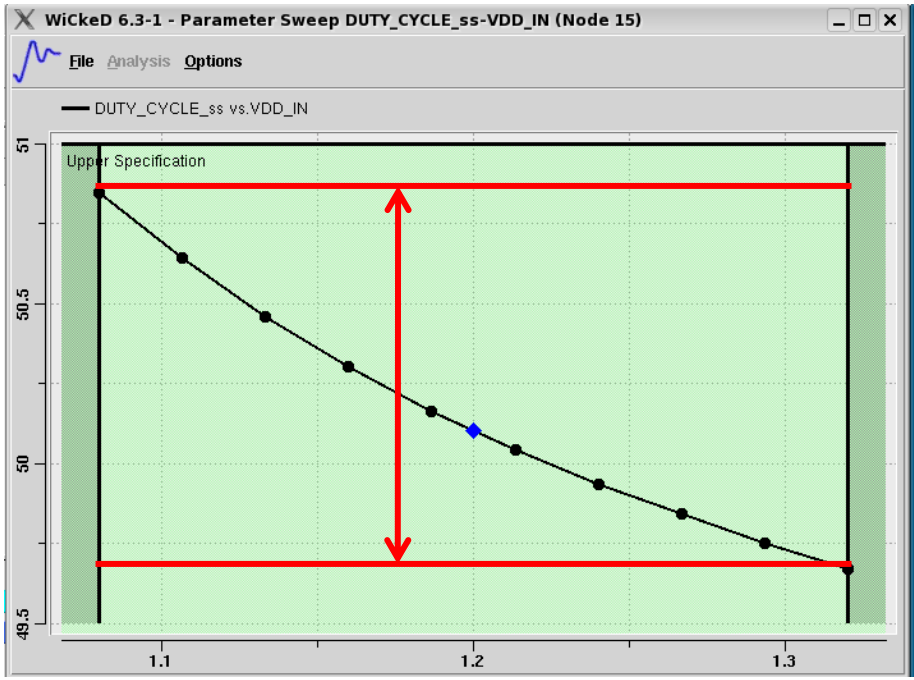
Different worst-cases regarding temperature / Vdd / load / …

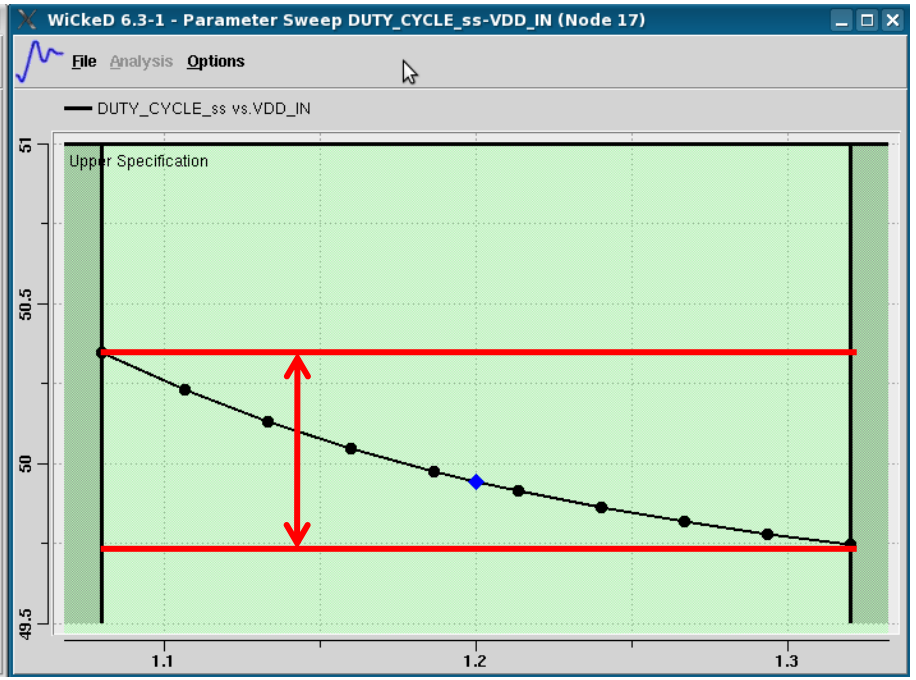


falltime worst-case: 80°C, delay_fall worst-case: 0°C

What makes sizing difficult?

- **Sensitivities have to be minimized.**





For some specs, it's not enough to shift the nominal value;
you can reduce sensitivities, too.

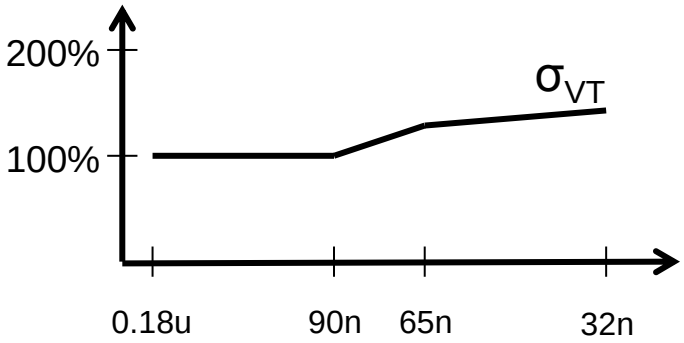
What makes sizing difficult?

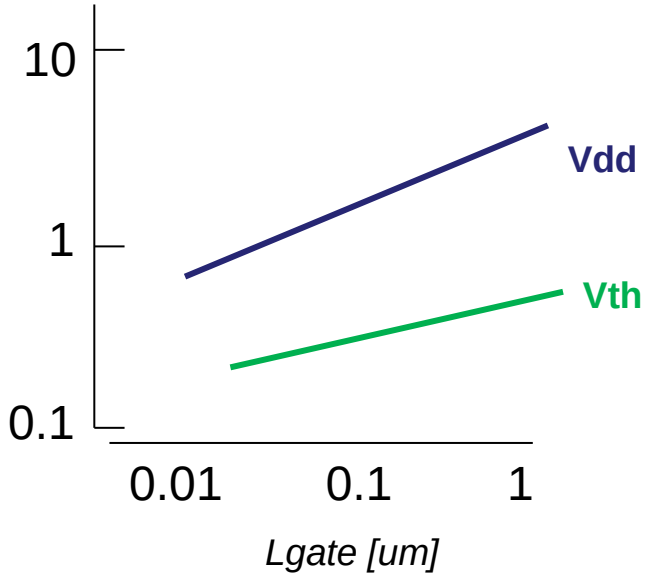
- **Local variation (mismatch) has a significant influence**

- **Scaling trend**
  - Absolute Vth variation of the minimum device grows
  - Vth shrinks, Vdd shrinks faster

⇒ **Relative impact of local variation $\sigma_{VT} / (V_{dd}-V_{th})$ grows**

⇒ **We have to size the circuits for robustness vs. local variation in addition to PVT corners**





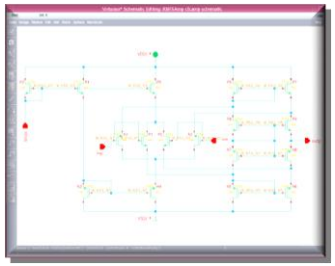
Typical WiCkeD Applications in I/O designs and Libraries

- **Common tasks:** sizing, statistical analysis, performance optimization, modeling, robustness optimization, reduce area, reduce power consumption, initial design (low voltage), …

- **Libraries, I/O**
  - Circuits: Transmitter, PCIe equalizer, LVDS drivers, level shifter, bandgap, voltage regulators, impedance control, short/overload detector, power-on-reset, SerDes, …
  - Performance metrics: jitter, eye diagram opening, duty cycle, temperature stability, voltage levels, delays, PSRR, stability, …

Software: Data flow

Input



Schematics

OR

<file_1>.cir
<file_2>.cir
- .....
<file_n>.cir

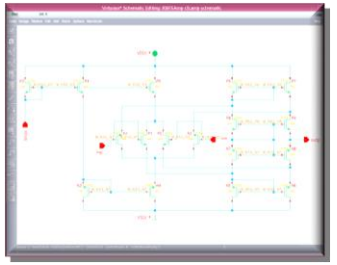
Netlists

WiCkeD
Circuit Design Optimization

- **Design Centering**
- **Yield & Robustness**
- **Modeling**

SPICE

Output



Sized & Optimized Circuit Schematic or Netlist(s)

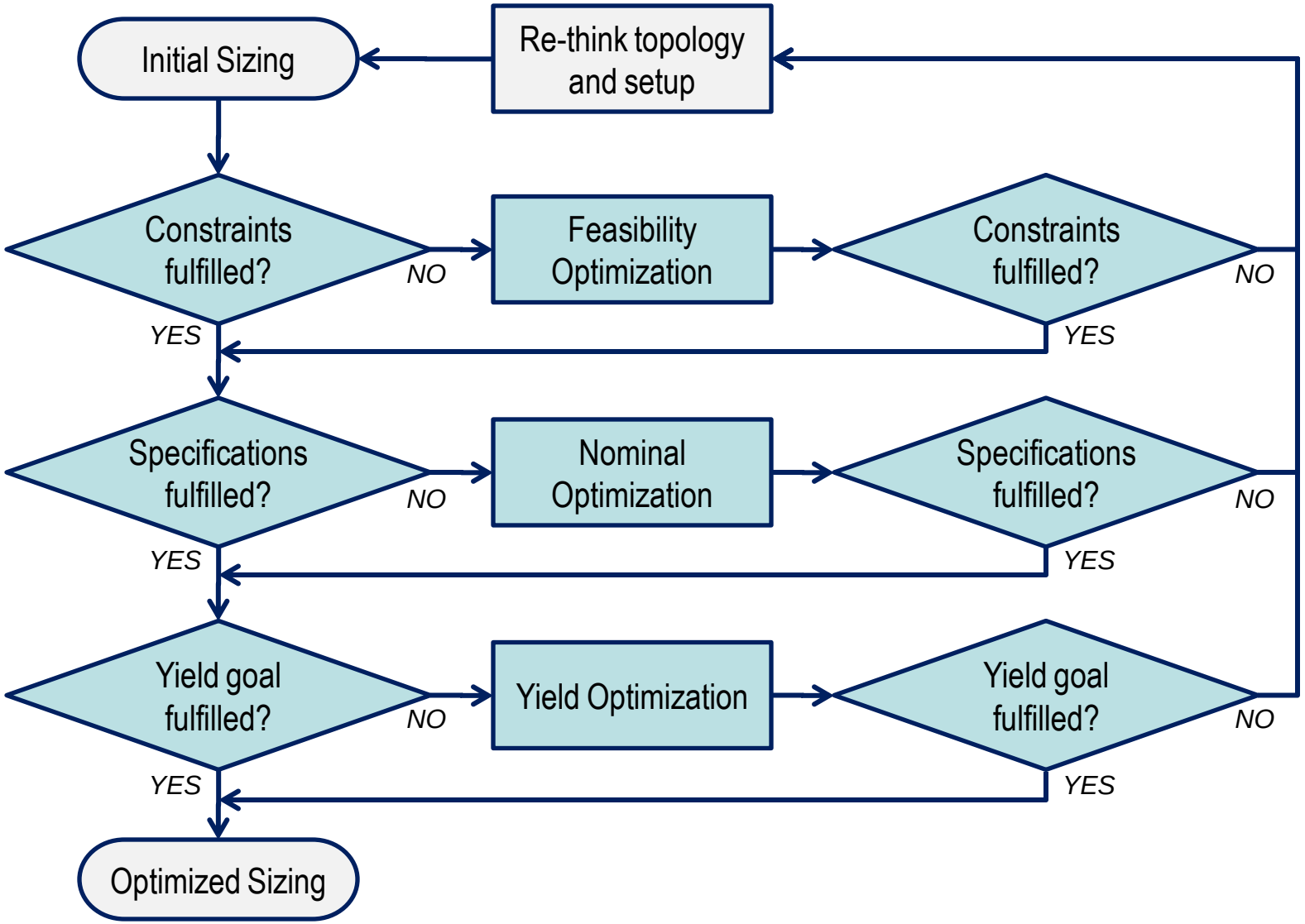
Three Optimization Steps

1. **Feasibility Optimization**
   - Fulfills constraints on DC operating conditions (saturation, inversion, current symmetries, overdrive, …)
   - Is optional (some circuits don't have such constraints)
   - May include constraints on SOA (aging), becoming more important in <28nm

2. **Nominal Optimization**
   - Optimizes performance (delays, eye diagram, jitter, power …) over PVT corners
   - Keeps constraints on DC operating conditions fulfilled
   - Not considering local variation (mismatch), therefore "nominal" optimization

3. **Yield Optimization**
   - Optimizes design yield (robustness) considering local variation (mismatch)
   - Should start from a design point after nominal optimization to save time

Optimization Steps (Vastly Simplified Flow Chart)



Solution Search

all possible designs

Feasibility Optimization

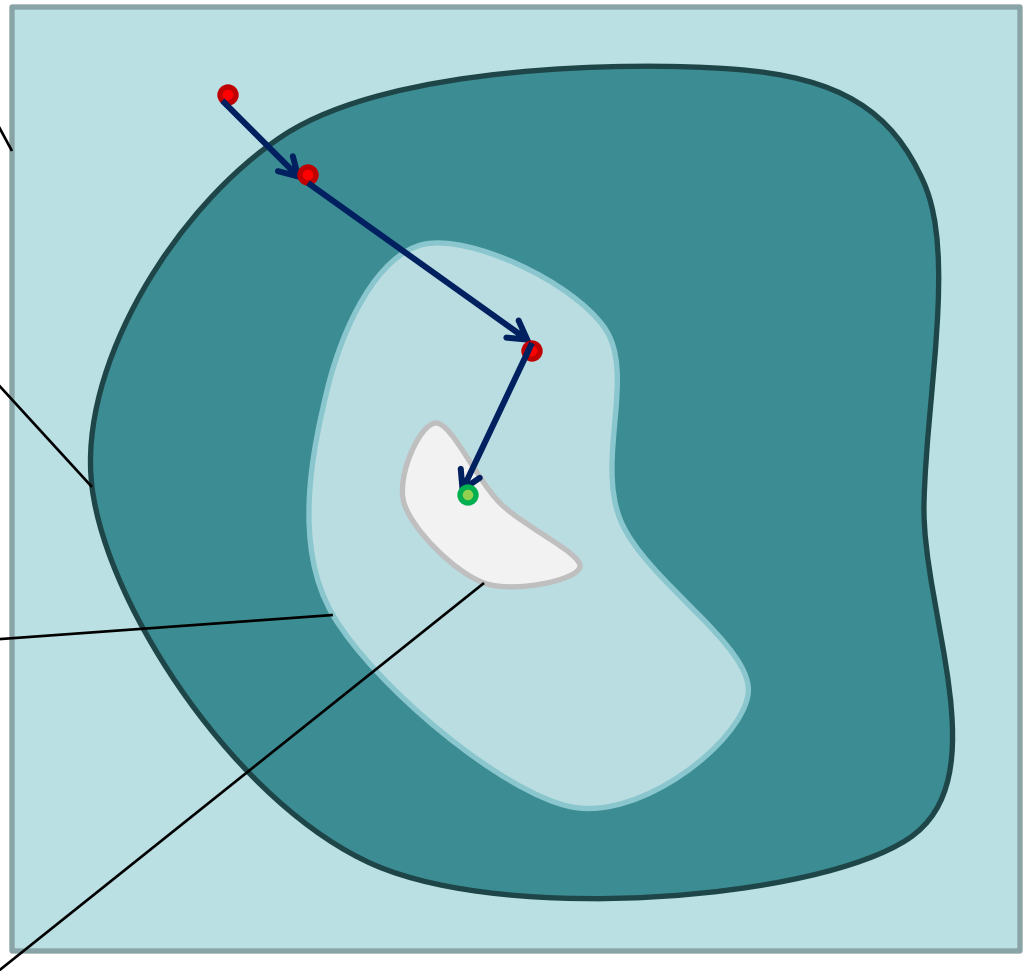
all designs with constraints fulfilled

Nominal Optimization

all designs with specifications fulfilled at TT

Yield Optimization

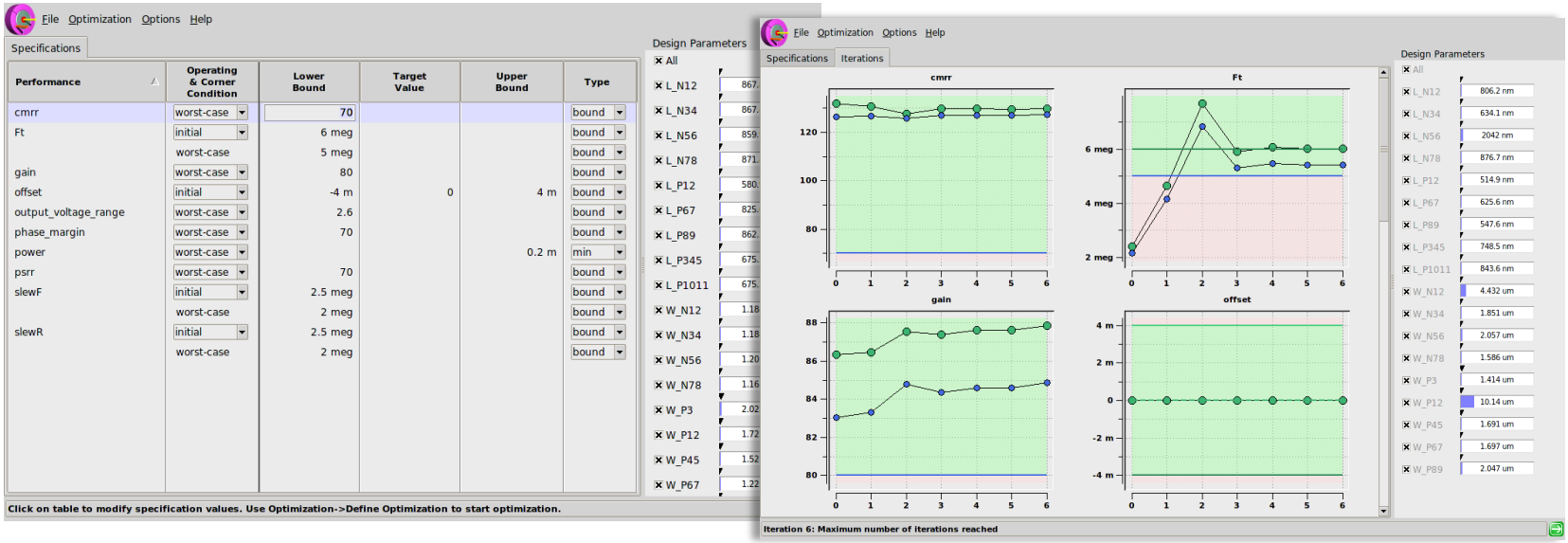
all designs with high enough parametric yield



Tools of WiCkeD – Sizing & Optimization— DNO & GNO Nominal Optimization

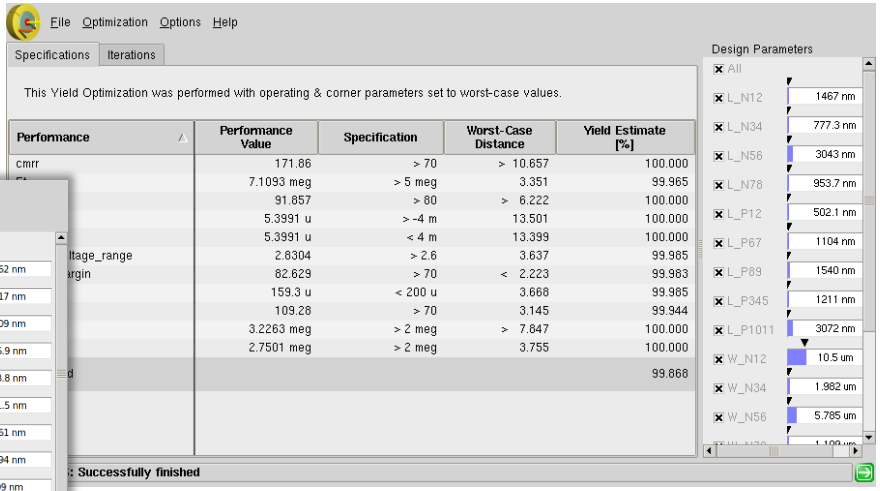
Circuit Sizing & Optimization

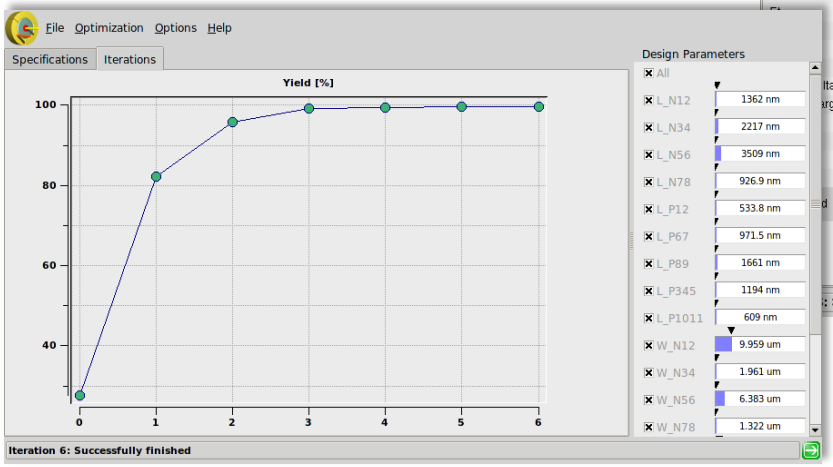
- **Fast and efficient. Scales well also for larger circuits.**
- **Multiple parameters, goals, corners & test benches optimized simultaneously**
- **Pre- and post-layout**
- **Broad simulator support, scriptable.**



The unique flagship:
Automated Yield Optimization

- **Improve robustness vs process variation and mismatch**
- **Multiple performances simultaneously**
- **Based on worst-case distance and sigma measures**





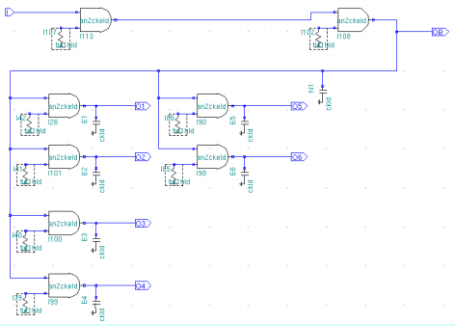
Customer Cases

Customer Example – Faraday – Batch-mode optimization of standard cells

Circuit Sizing & Optimization

FARADAY TECHNOLOGY CORPORATION

Standard cell: Clock buffers



- Task: Balance slopes
- Challenge: many cell & process variants, multiple slews and output loads, frequent model update

Solution:

MunEDA **Nominal Optimization in Batch Mode**

	PTNT (%)				PFNF (%)				PSNS (%)			
	0.00 1500 P	0.00 7287 P	0.01 6060 P	0.03 5400 P	0.00 1500 P	0.00 7287 P	0.01 6060 P	0.03 5400 P	0.00 1500 P	0.00 7287 P	0.01 6060 P	0.03 5400 P
BAL1	2	1.5	1	~1	3.3	3.3	3.2	3.3	2.8	2.9	3.1	3.5
BAL2	1.8	1.4	~1	~1	3.2	3.1	3.1	3.1	2.9	3.0	3.2	3.6
BAL3	1.5	1	~1	~1	2.9	2.9	2.9	2.9	3.0	3.1	3.3	3.7
BAL4	~1	~1	~1	~1	2.3	2.3	2.3	2.5	3.2	3.4	3.5	3.8
BAL5	~1	3.8	1.5	1.9	1.1	1.1	1.2	1.5	3.7	3.9	3.9	4.1
BAL6	3.7	1.1	3.9	4.1	~1	~1	~1	~1	5.1	5.2	5.2	5.3

Complete automation reduces design time significantly.

Equal or better results than manual design.

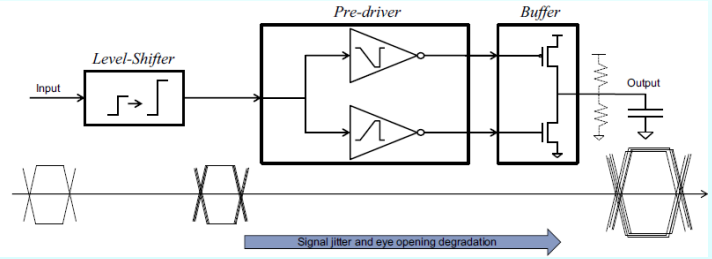
Results published by Faraday at MTF Anaheim 2008

Customer Example – Sizing & Design Centering with MunEDA WiCkeD Optimization Tools
STMicroelectronics - Optimization of High-Speed I/O circuits in 28nm

Circuit Sizing & Optimization

STMicroelectronics

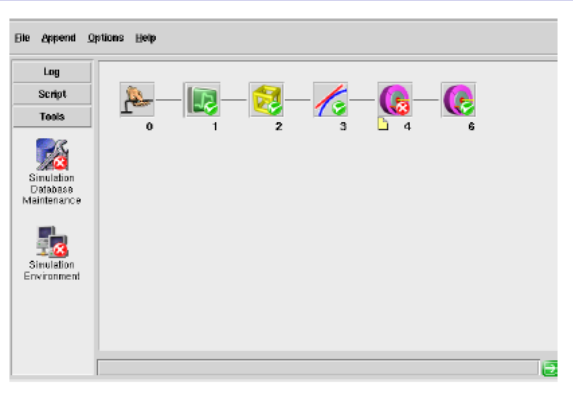
28nm DDRx High-Speed I/O



- Task: Reduce jitter and duty cycle
- Challenge: Manual tuning takes 2 weeks

Solution:

Use MunEDA **Sensitivity Analysis** and **Corner Optimization**



Design Time reduced from 2 weeks to only 3 hours

Corner spread reduced by 50%

Easy analysis of circuit sensitivities

Optimization of a 2.133GHz level shifter in 28nm (with WiCkeD)

Nicolas Seller – STMicroelectronics (Crolles)

November, 25th 2011

MUGM 11 Europe

STMicroelectronics

Results published by STMicroelectronics at MUGM 2011

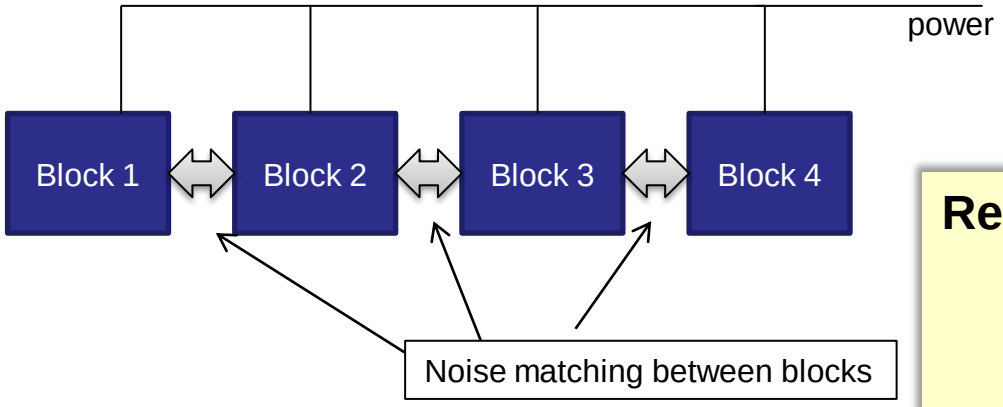
Customer Example – Sizing & Design Centering with MunEDA WiCkeD Optimization Tools

TOP Microprocessor Company - Using MunEDA tools to optimize AMS/RF IP in 65nm

Circuit Sizing & Optimization

TOP Microprocessor Company - RF receiver path in advanced node

- Task: reduce power consumption while keeping noise low
- To see the noise vs power trade-off, the complete path has to be considered
- Circuit size: ~2000 MOS, ~8000 parasitics.
  Simulation time: 40min. for a single run (dc+pss+pnoise)
- Optimization complexity: 80 specs, 50 design parameters
  Three process corners + temperature + Vdd



Results:

- Power consumption significantly reduced.
- Sizing task performed completely automatically.
- Designer attention time is reduced from 4 weeks to a few hours.