# Class 11: Transmission Gates, Latches

Topics:

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2. Transmission Gate Logic Design
3. X-Gate 2-to-1 MUX
4. X-Gate XOR
5. X-Gate 8-to-1 MUX
6. X-Gate Logic Latch
7. Voltage Drop of n-CH X-Gates
8. n-CH Pass Transistors vs. CMOS X-Gates
9. n-CH Pass Transistors vs. CMOS X-Gates
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13. Static CMOS Digital Latches
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15. Static CMOS Digital Latches



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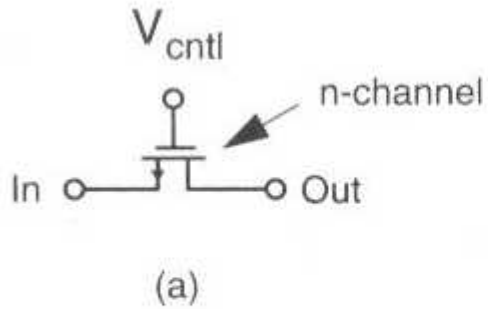
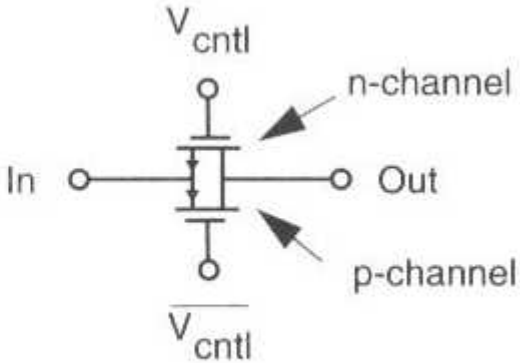
# Class 11: Transmission Gates, Latches

## Transmission Gates (Martin, c5.1)

- Pass Transistors, a.k.a., Transmission Gates are same as a relay
- Why? Usually allows for a reduction in number of transistors




(a)




(b)

NMOS

| | | |
|---|---|---|
| Vcntl | H | L |
| Out | In | Z |

CMOS

| | | |
|---|---|---|
| Vcntl | H | L |
| Vcntl’ | L | H |
| Out | In | Z |

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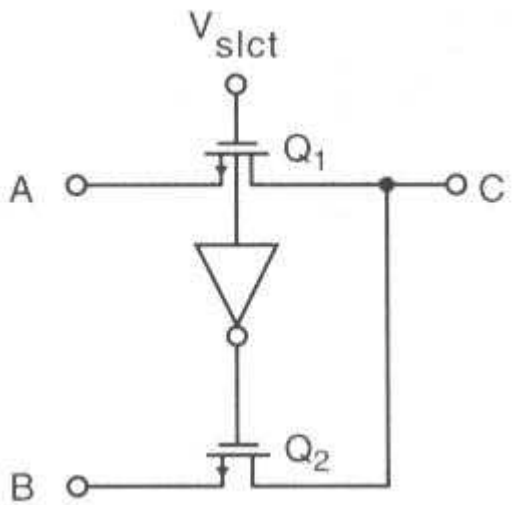
## Transmission Gate 2-to-1 MUX (Martin, c5.1)




| Vslct | A | B | Q1(n) | Q2(n) | C |
|---|---|---|---|---|---|
| 0 | 0 | 0 | off | on | B |
| 0 | 0 | 1 | off | on | B |
| 0 | 1 | 0 | off | on | B |
| 0 | 1 | 1 | off | on | B |
| | | | | | |
| 1 | 0 | 0 | on | off | A |
| 1 | 0 | 1 | on | off | A |
| 1 | 1 | 0 | on | off | A |
| 1 | 1 | 1 | on | off | A |

This same design will be revisited shortly for an 8-to-1 MUX



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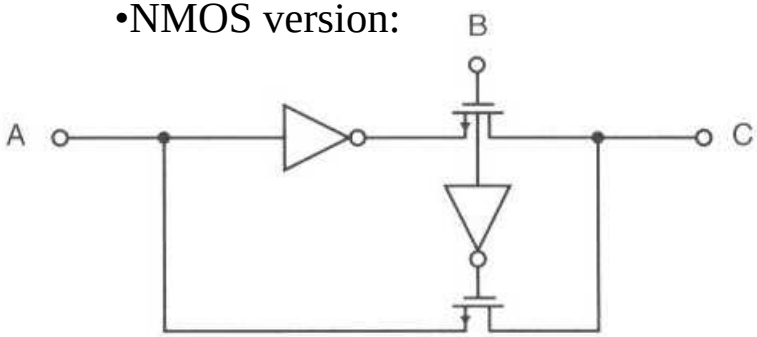
## Transmission Gate XOR (Martin, c5.1)

- XOR similar to 2-to-1 MUX
- NMOS version:




| B | A | Q1(n) | Q2(n) | C |
|---|---|---|---|---|
| 0 | 0 | off | on | 0 (A) |
| 0 | 1 | off | on | 1 (A) |
| 1 | 0 | on | off | 1 (A’) |
| 1 | 1 | on | off | 0 (A’) |

- CMOS version:

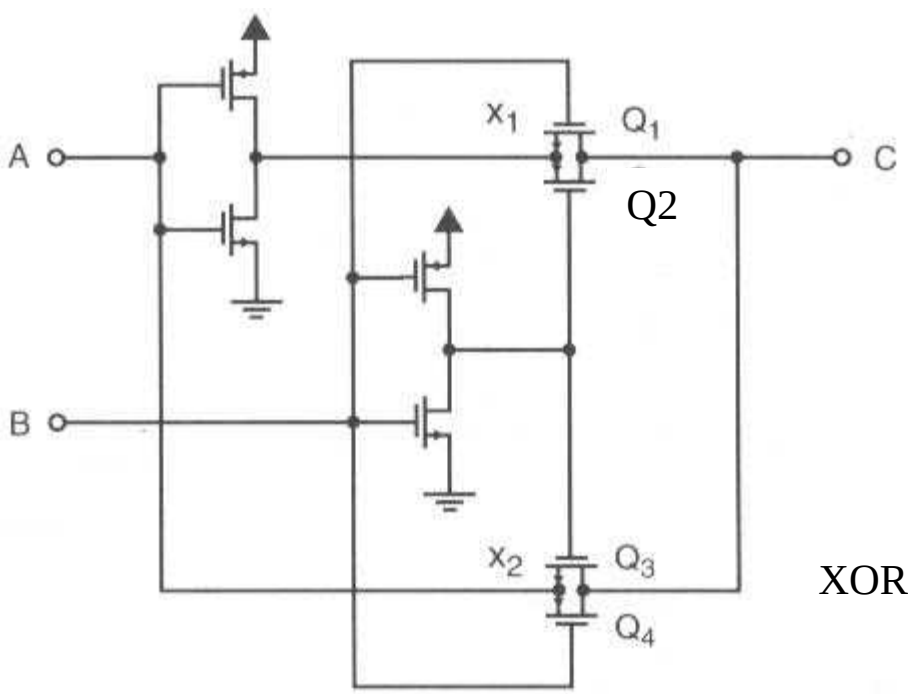



**Table 5.1** The Truth Table of the *exclusive-or* Function

| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

| | NMOS X-Gate | pseudo-NMOS traditional | CMOS X-Gate | CMOS traditional |
|---|---|---|---|---|
| XOR | 6 | 7 | 8 | 10 |

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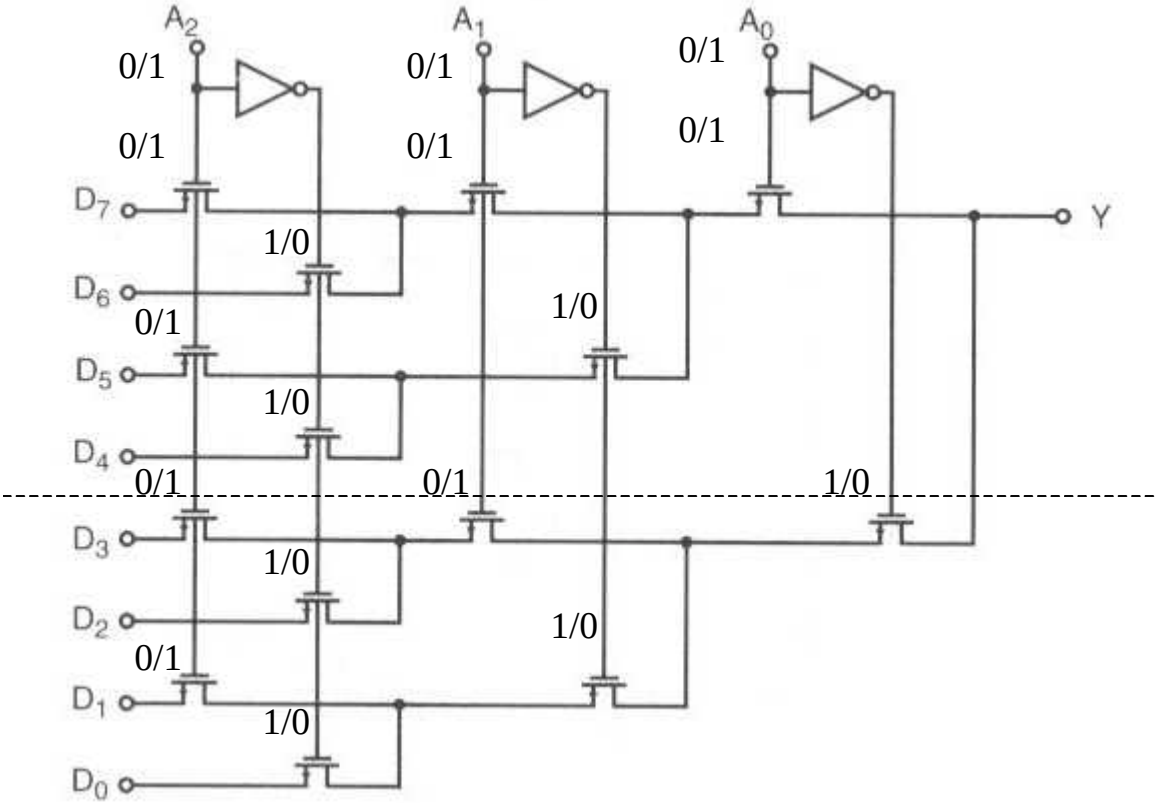
## Transmission Gate 8-to-1 MUX (Martin, c5.1)




| A2 | A1 | A0 | Y |
|---|---|---|---|
| 0 | 0 | 0 | D0 |
| 0 | 0 | 1 | D4 |
| 0 | 1 | 0 | D2 |
| 0 | 1 | 1 | D6 |
| | | | |
| 1 | 0 | 0 | D1 |
| 1 | 0 | 1 | D5 |
| 1 | 1 | 0 | D3 |
| 1 | 1 | 1 | D7 |
| (E / O) | (T / B) | (D0-D3), (D4-D7) | |

Typically, one would not use more than 8-to-1 MUX. Why?

# Class 11: Transmission Gates, Latches

## Transmission Gate Clocked Latch (Martin, c5.1)

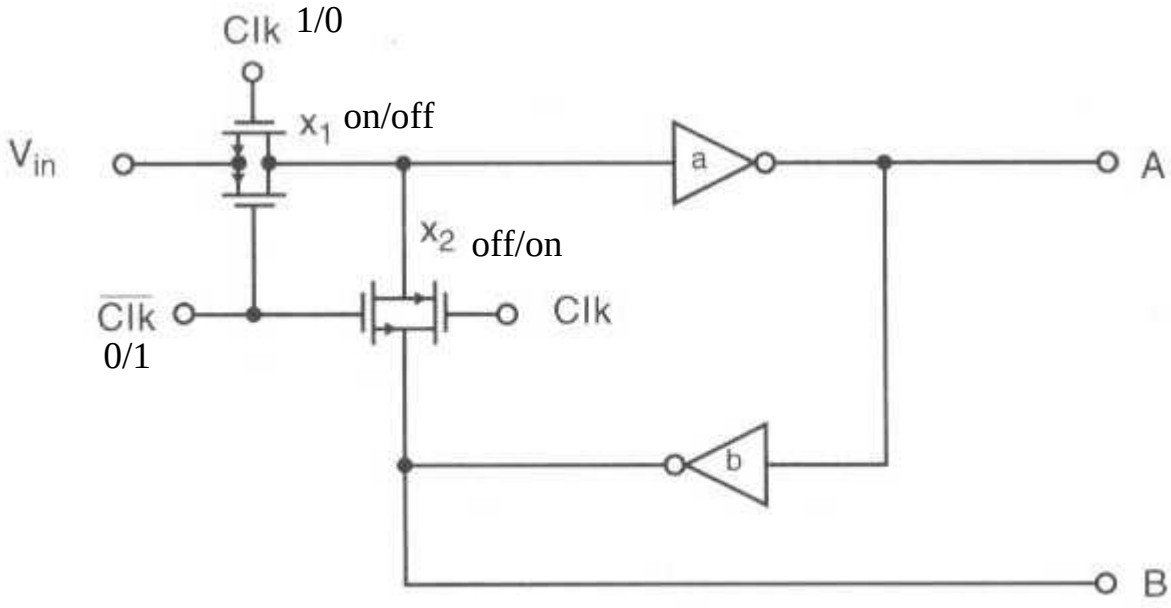
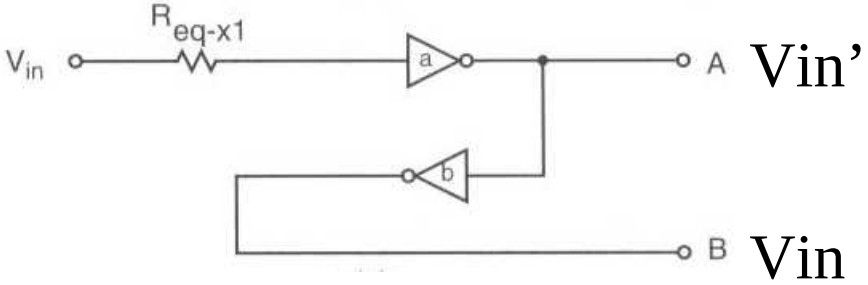


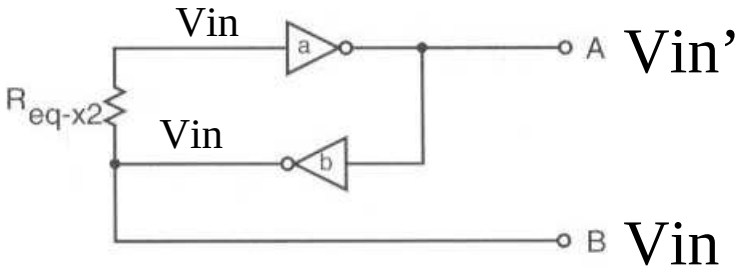

**Figure 5.6** A transmission-gate-based clocked latch.

When CLK is high:




"track mode", latch is loaded

When CLK is low:

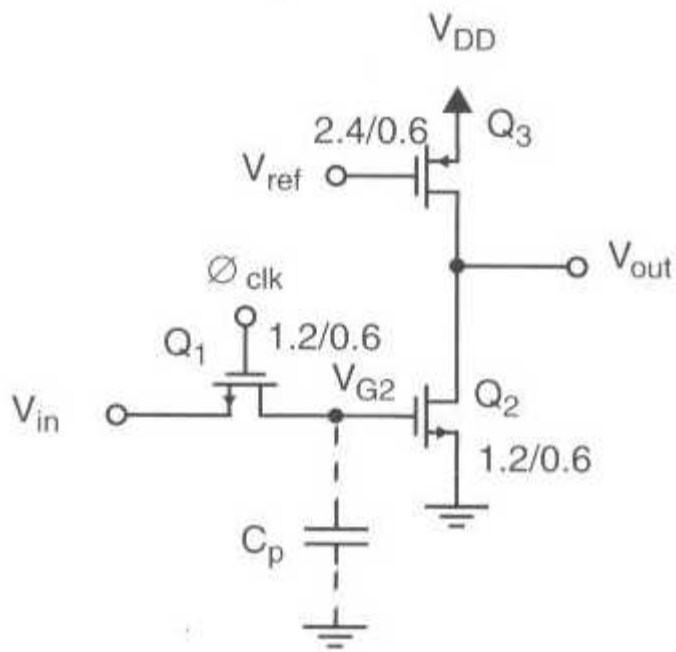



data is latched to Vin at time of clock transition

# Class 11: Transmission Gates, Latches

## Voltage Drop of n-CH X-Gates (Martin, c5.1)

Pseudo-NMOS X-Gate
delay line cell




Desired operation:

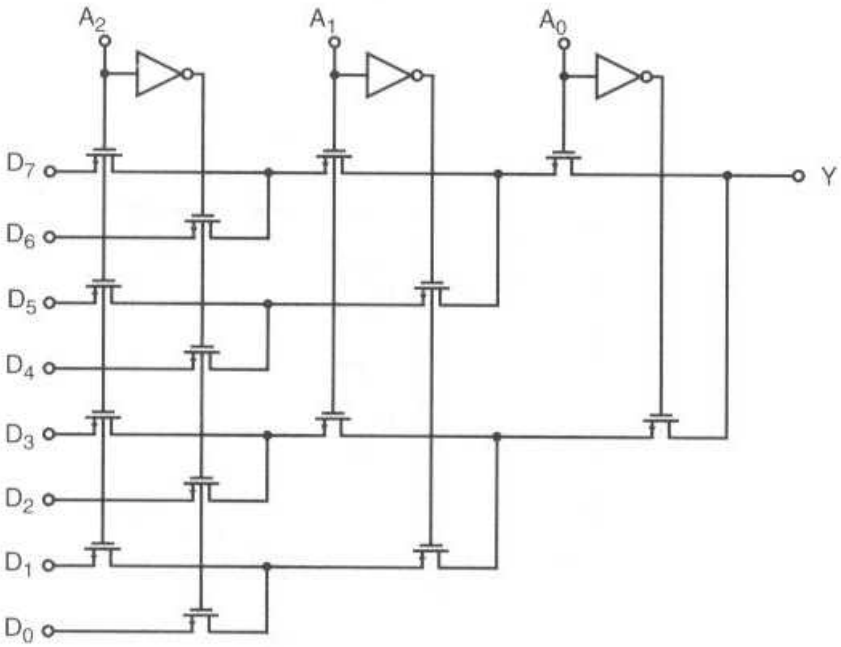
- Start with $\phi_{clk} = 1$, $V_{G2} = V_{in}$
- Transition, $\phi_{clk}$ 1->0, Q1 on->off, Cp keeps voltage
- AKA source follower or common drain buffer
- Cp is due to what?
- Vout = Vin'

Problems with circuit:

- Start with Vin=0, and $\phi_{clk}$ 0->1
- $V_{G2} = V_{in} = 0V$, so Q1 S/D are at ground (Q1 is in what region?)
- If Vin -> VDD, while $\phi_{clk} = 1$, initially LHS of Q1 is drain
  RHS is the source, and Vgs=VDD, and Vgd=0
  (Q1 is in what region?)
- $V_{G2}$ charges up to VDD-Vtn
- Veff for Q1 will become zero (Vgs-Vtn=0)
- Q1 shuts off when Vgs=Vtn, or when $V_{G2}$ = VDD-Vtn
- Thus $V_{G2}$ never gets to VDD, and body effect determines
  how far from VDD the node ends up
- As body effect goes up, Vtn goes up, $V_{G2}$ goes down
- So what is the problem?

# Class 11: Transmission Gates, Latches

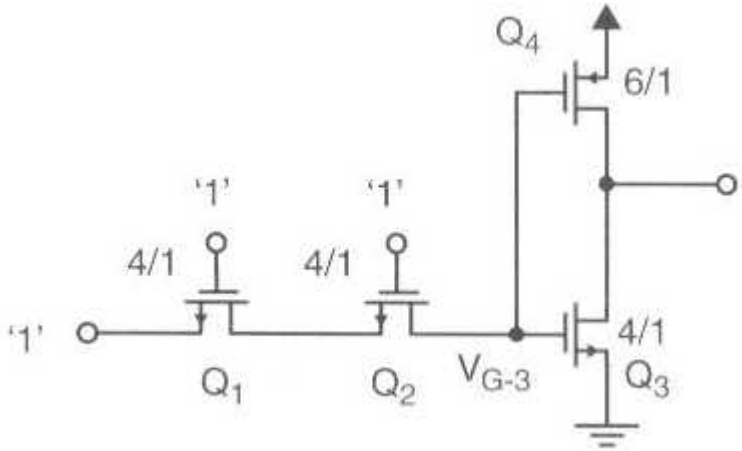
## Voltage Drop of n-CH X-Gates (Martin, c5.1)



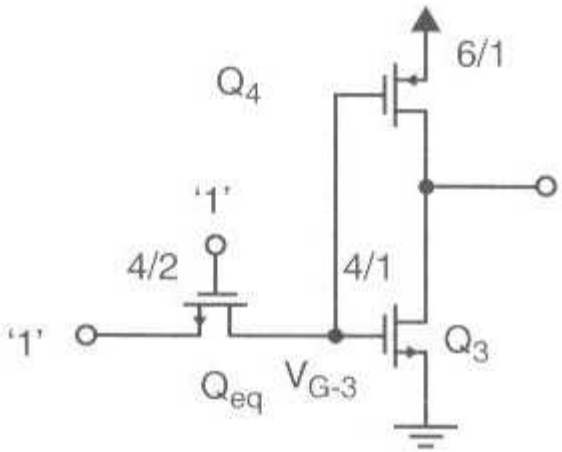

Through how many series transistors does the data pass?

•Equivalency says that two series transistors with W/L is the same as one transistor with W/2L

•Voltage at gate of Q3 is the same, it just takes longer to rise

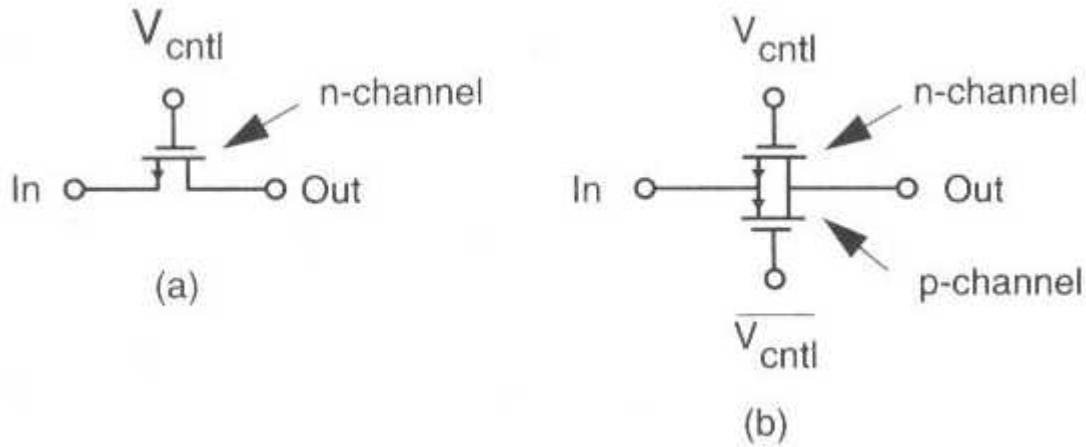



=>



# Class 11: Transmission Gates, Latches

n-CH vs. CMOS X-Gates (Martin, c5.1)

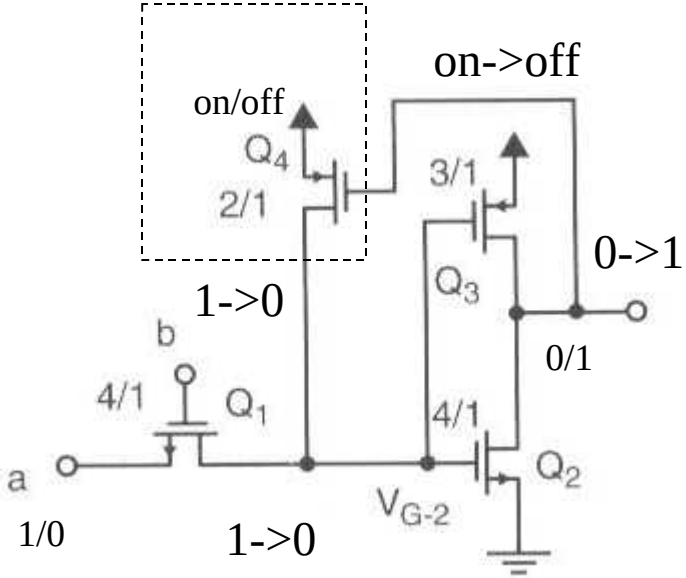



•Area may be smaller if NMOS used vs. CMOS
•CMOS X-Gates transfer “1” and “0” efficiently. Why?
•CMOS X-Gates after faster in 0->1 transition. Why?
•N-CH voltage drop a major disadvantage, but can be eliminated

Speed:
•When junction capacitance dominates, which should be used?
•When load capacitance dominates, which should be used?
Power:
•Which is more sensitive to Vt value?

# Class 11: Transmission Gates, Latches

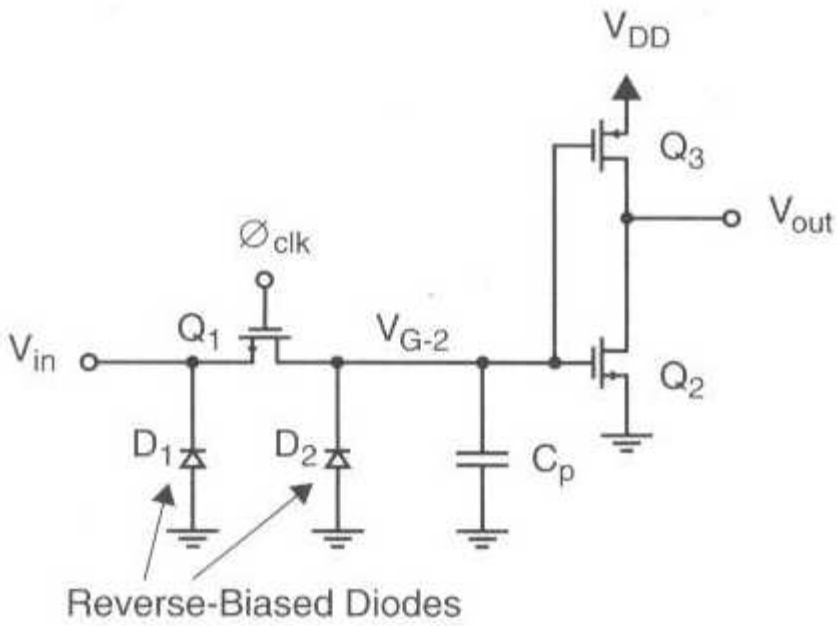
## Full-Swing n-CH X-Gates (Martin, c5.1)




- Applicable when an inverter follows a pass transistor
- Q4 must have W/L small compared to Q1 for 1->0 at Q2 gate. Why?
- p-ch load (Q3) will be completely turned off with the addition of Q4. If not, what would occur?

# Class 11: Transmission Gates, Latches

Leakage Currents (Martin, c5.1)

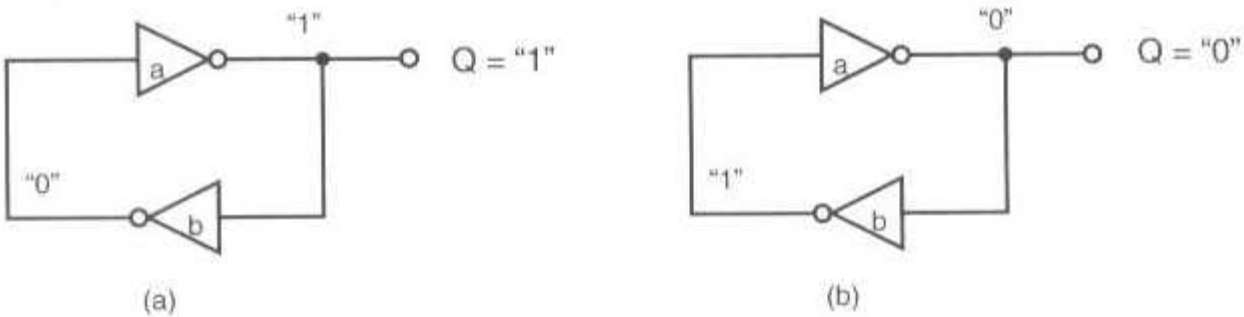



- What happens to voltages when $\phi_{clk}$ is high and Vin=1?
- Cp obtains what value?
- What happens to Cp if $\phi_{clk}$ remains low
- How does this vary with temperature?
- What else would cause this to vary?

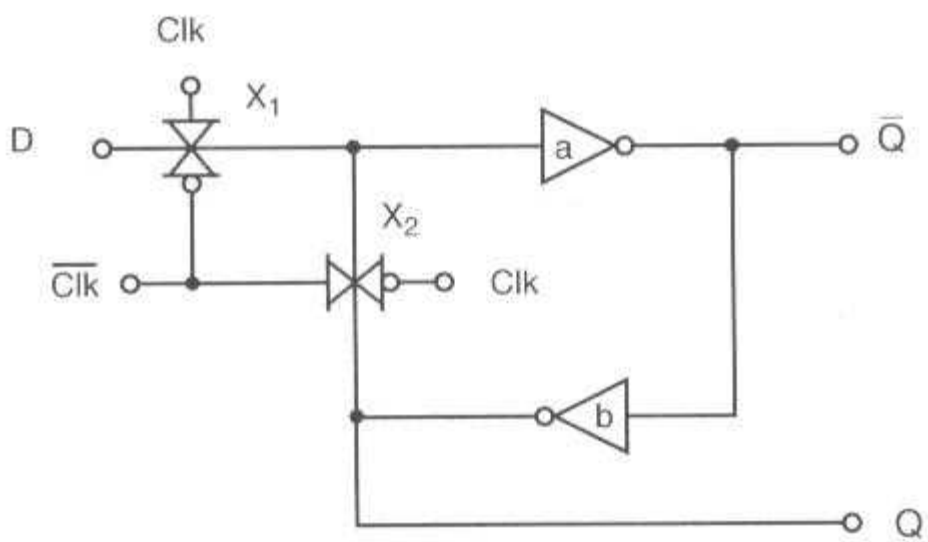
# Class 11: Transmission Gates, Latches

## Static CMOS Digital Latches (Martin, c7.1)

Example of a two cross coupled inverters, having positive feedback:




Latch realized below using what type of logic?



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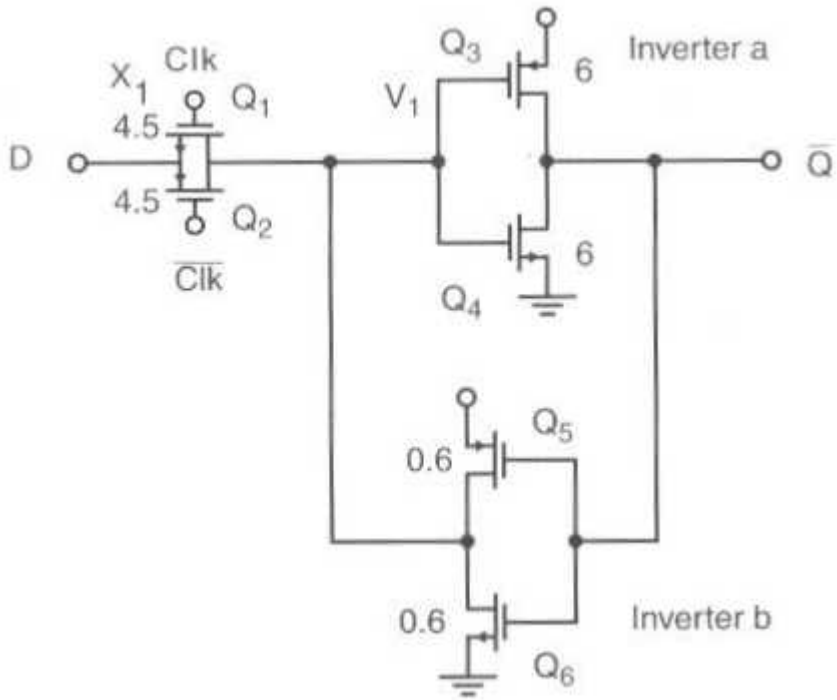
## Static CMOS Digital Latches (Martin, c7.1)




- What has changed from previous slide for latch?

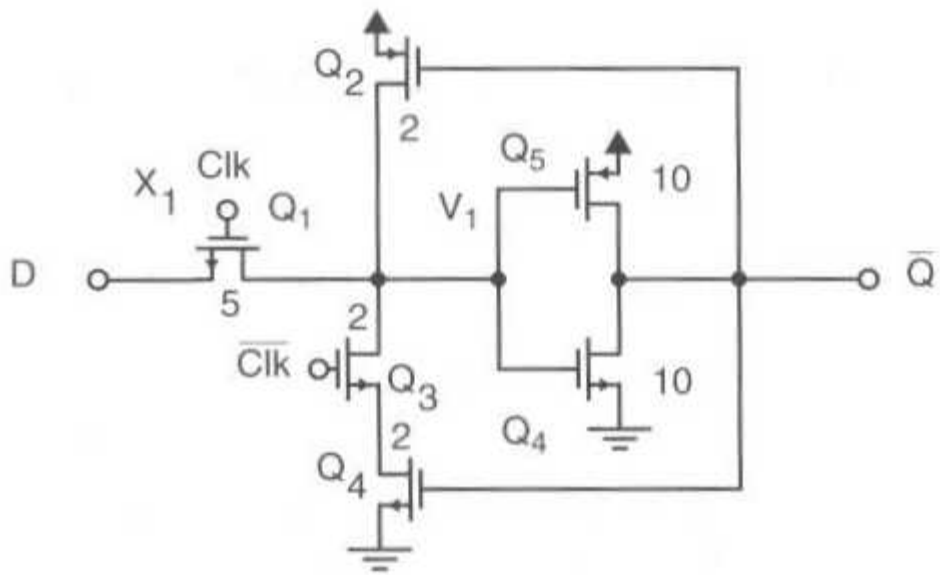
- When CLK is high, D is passed to V1, but why is it not inverted by Q5/Q6?

Good: hysteresis is added, noise immunity for slow-moving signals, less area than latch of previous foil

Bad: Only inverter a is a driver. Why?

# Class 11: Transmission Gates, Latches

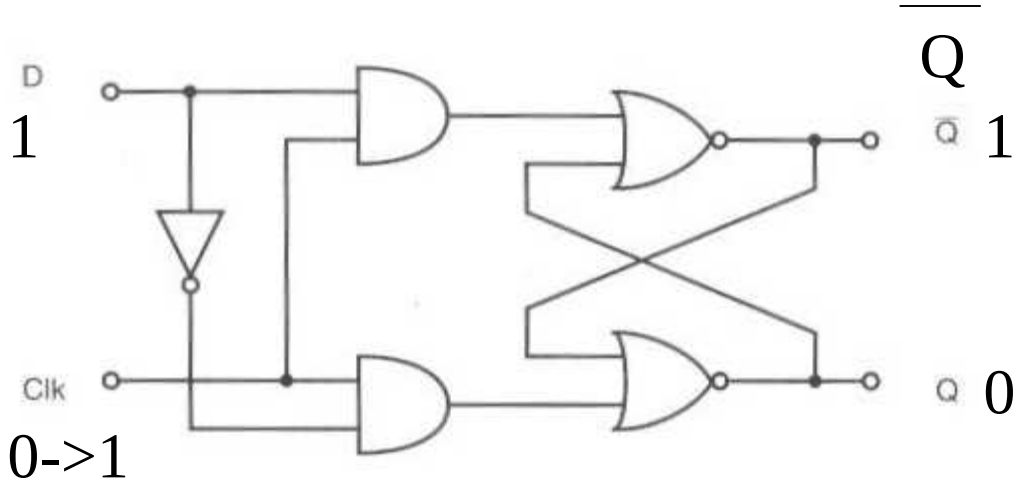
## Static CMOS Digital Latches (Martin, c7.1)



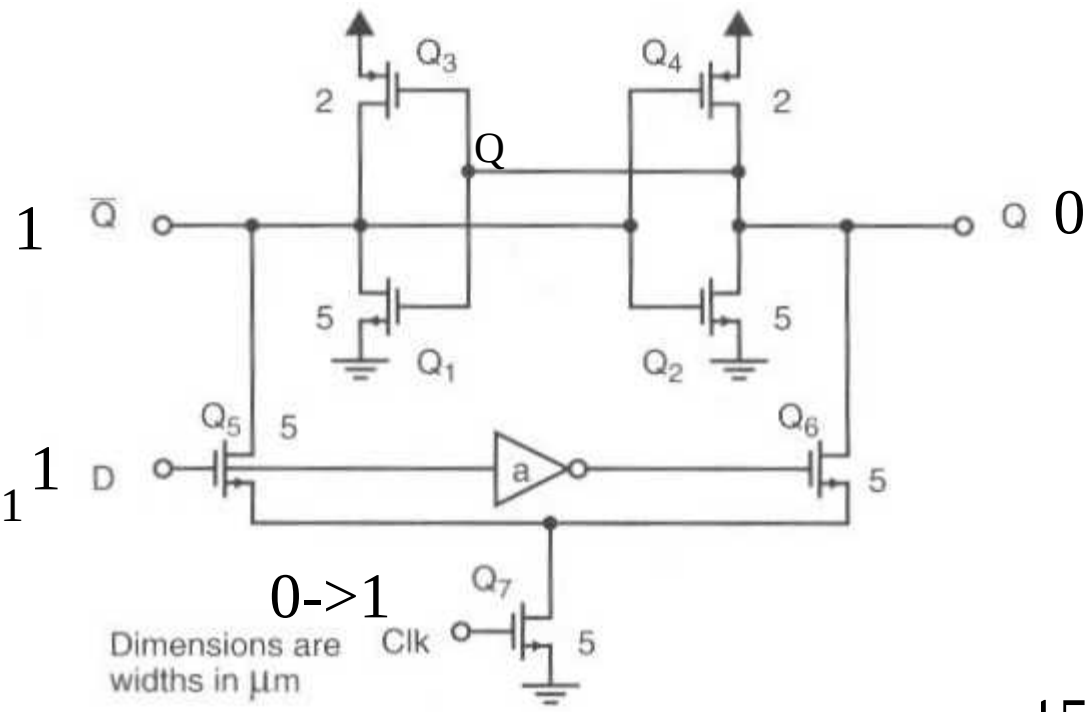

- Q1 is used as a pass transistor, so why is Q2 in the circuit?
- Q2 ratio W/L should be small or large compared to Q1?
- When CLK is low, Q3 is on, reinforcing a stored “0” at V1.
- What reinforces the stored “1” at V1 when CLK is low?

# Class 11: Transmission Gates, Latches

## Static CMOS Digital Latches (Martin, c7.1)




- Cross coupled NOR gates
- Q=D when Clk=1
- Q preserved when Clk=0




- As CLK 0->1, Q'->gnd if Q5/Q7 widths are larger than Q3
  Q5 series with Q7 gives what width?
- Compare to what width of Q3?
- When Q' is low, Q4 is on, Q2 off, Q is 1
- This means one inverter delay