CMOS Analog Integrated Circuits: Models, Analysis, & Design

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EE448

MOS Circuit Level Models

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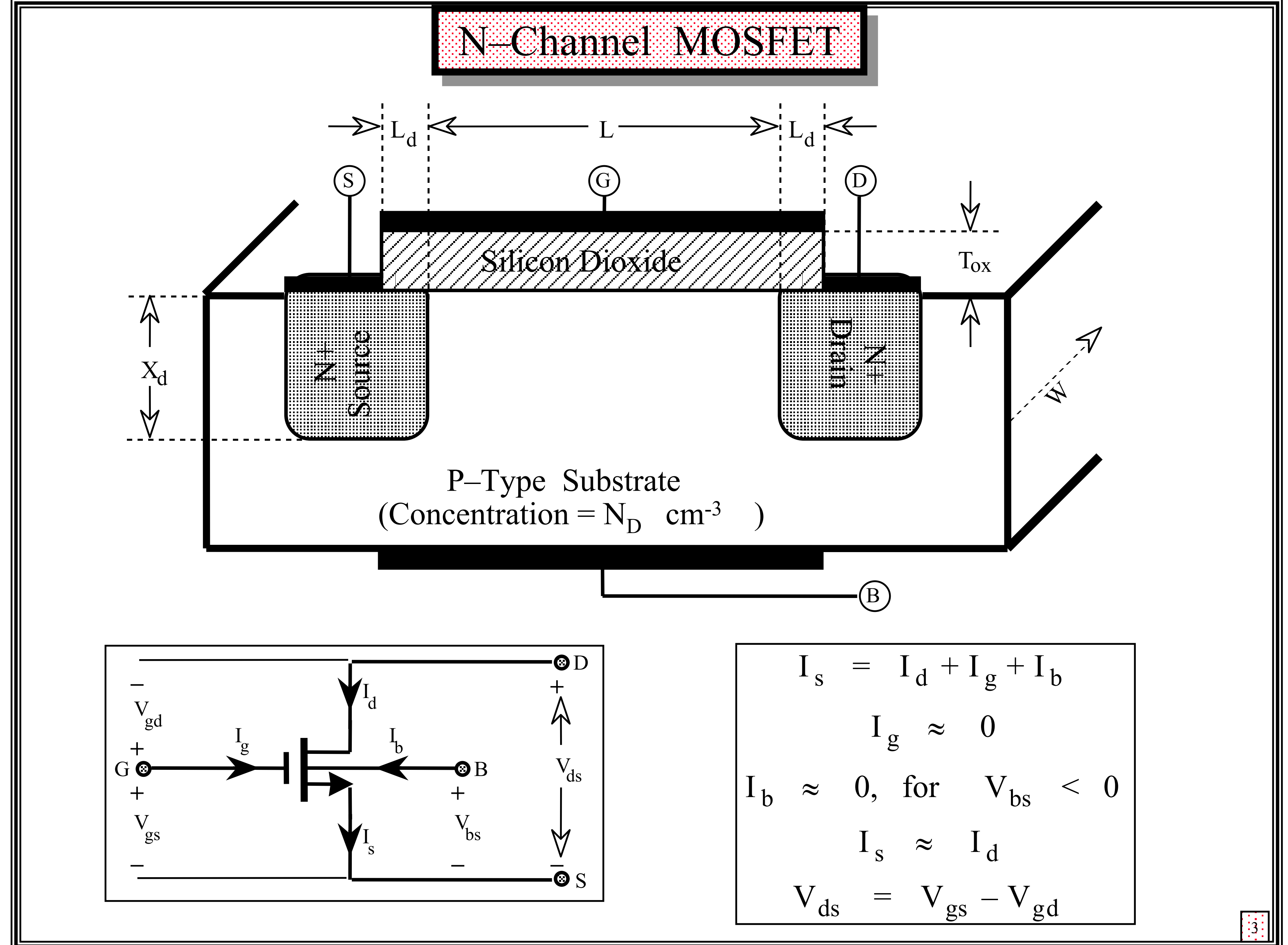
Lecture Overview

- Static Model
  - Cutoff Region
  - Ohmic (Triode) Region Model
  - Saturation Region Model
  - Subthreshold Model

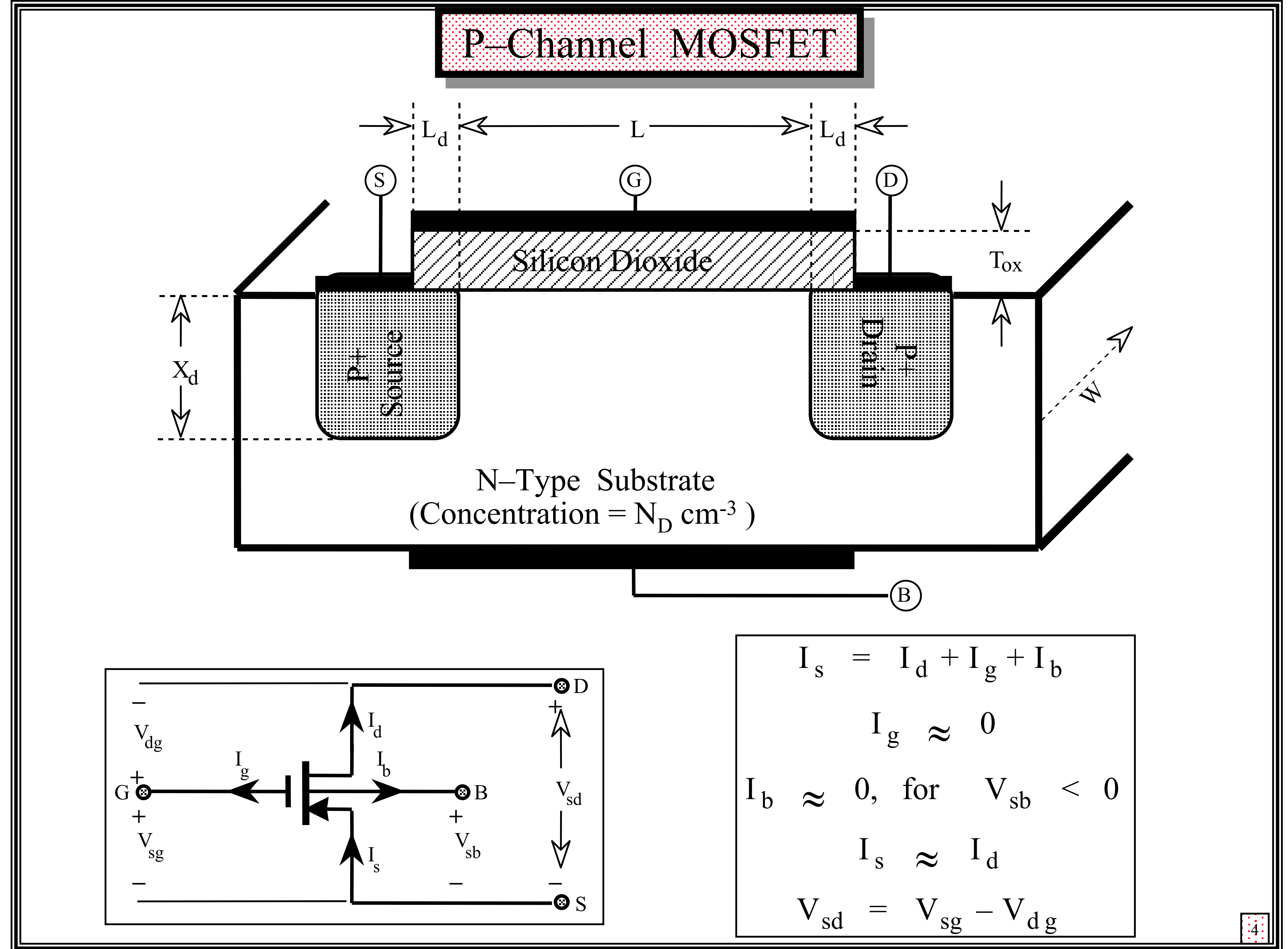
- Short Channel Effects In Saturation
  - Channel Length Modulation
  - Substrate/Bulk Phenomena
  - Mobility Degradation
  - Carrier Velocity Saturation

- Small Signal Model In Saturation
  - Forward Transconductance
  - Bulk Transconductance
  - Capacitances

- Sample Circuit Analysis (Inverter)
  - Gain
  - Bandwidth



N–Channel MOSFET
L
Ld
S
G
D
Silicon Dioxide
Tox
Xd
N+
Source
Drain
N+
W
P–Type Substrate
(Concentration = ND cm-3)
B
D
Id
Vgd
Ig
Ib
G
B
Vds
Vgs
Is
Vbs
S
Is = Id + Ig + Ib
Ig ≈ 0
Ib ≈ 0, for Vbs < 0
Is ≈ Id
Vds = Vgs – Vgd



P–Channel MOSFET
L_d
L
L_d
S
G
D
Silicon Dioxide
T_{ox}
X_d
P+ Source
P+ Drain
W
N–Type Substrate
(Concentration = N_D cm^{-3})
B
D
I_d
V_{dg}
I_g
I_b
G
B
V_{sd}
V_{sg}
I_s
V_{sb}
S
$I_s = I_d + I_g + I_b$
$I_g \approx 0$
$I_b \approx 0,$ for $V_{sb} < 0$
$I_s \approx I_d$
$V_{sd} = V_{sg} - V_{dg}$

Characteristic Curves: Cutoff And Ohmic Regimes

- **Cutoff Regime:** $V_{gs} < V_{hn}$
  - $I_d = 0$
  - $V_{hn} \rightarrow$ Threshold Voltage, Function Of Bulk–Source Voltage

- **Ohmic Regime:** $V_{gs} \geq V_{hn}$ and $V_{ds} < V_{gs} - V_{hn}$
  - $I_d = K_n \left(\frac{W}{L} \right) V_{ds} \left(V_{gs} - V_{hn} - \frac{V_{ds}}{2} \right)$
  - $K_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{T_{ox}}$ (Hundreds Of μmhos/Volt)

- **Comments**
  - W/L Is Gate–Channel Aspect Ratio, <u>A Designable Parameter</u>
  - $V_{ds} = V_{gs} - V_{gd} < V_{gs} - V_{hn}$ Implies $V_{gd} > V_{hn}$
  - Temperature Effects (Holes And Electrons): $\mu(\mathbf{T}) \approx \mu(\mathbf{T_o}) \left(\frac{\mathbf{T_o}}{\mathbf{T}} \right)^{3/2}$
  - Resistance For Small Drain–Source Voltage:

$$\frac{\partial I_d}{\partial V_{ds}} \triangleq \frac{1}{R_{ds}} = K_n \left(\frac{W}{L} \right) \left(V_{gs} - V_{hn} - V_{ds} \right) = \frac{I_d}{V_{ds}} \left(\frac{V_{gs} - V_{hn} - V_{ds}}{V_{gs} - V_{hn} - \frac{V_{ds}}{2}} \right) \approx \frac{I_d}{V_{ds}}$$

Characteristic Curves: Saturated Regime

- **Saturation Regime:** $V_{gs} \geq V_{hn}$ & $V_{ds} \geq V_{gs} - V_{hn}$
  - $I_d = \frac{K_n}{2}\left(\frac{W}{L}\right)\left(V_{gs} - V_{hn}\right)^2$
  - $V_{dss} \triangleq V_{gs} - V_{hn} \rightarrow$ Drain Saturation Voltage
  - $I_{dss} = \frac{K_n}{2}\left(\frac{W}{L}\right)V_{dss}^2 \rightarrow$ Drain Saturation Current

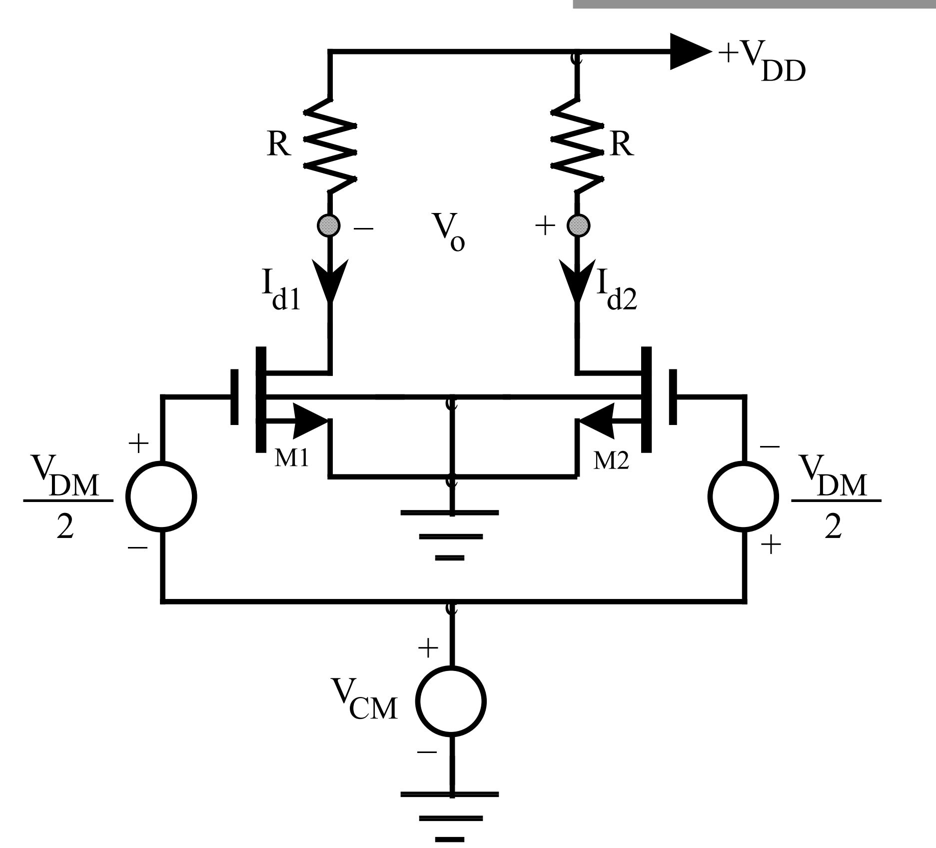
- **Comments**
  - Square Law Voltage–Controlled Current Source
  - Drain Current Shows Negative Temperature Coefficient Because Of Its Proportionality To Mobility
  - Differential Current Of Two Matched Devices Is Linear With Differential Gate–Source Voltage $\left(V_{DM}\right)$ Provided Common Mode Gate–Source Voltage $\left(V_{CM}\right)$ Is A Constant

$$I_{d1} - I_{d2} = \frac{K_n}{2}\left(\frac{W}{L}\right)\left[\left(V_{gs1} - V_{hn}\right)^2 - \left(V_{gs2} - V_{hn}\right)^2\right]$$

$$I_{d1} - I_{d2} = K_n\left(\frac{W}{L}\right)\left(\frac{V_{gs1} + V_{gs2}}{2} - V_{hn}\right)\left(V_{gs1} - V_{gs2}\right)$$

$$I_{d1} - I_{d2} = K_n\left(\frac{W}{L}\right)\left(V_{CM} - V_{hn}\right)V_{DM}$$

Simple Differential Pair



- Inputs

$$V_{gs1} = V_{CM} + \frac{V_{DM}}{2}$$

$$V_{gs2} = V_{CM} - \frac{V_{DM}}{2}$$

$$V_{gs1} + V_{gs2} = 2\,V_{CM}$$

$$V_{gs1} - V_{gs2} = V_{DM}$$

- Response

$$I_{d1} - I_{d2} = K_n \left(\frac{W}{L}\right)(V_{CM} - V_{hn})V_{DM}$$

$$V_o = R(I_{d1} - I_{d2}) = K_n R\left(\frac{W}{L}\right)(V_{CM} - V_{hn})V_{DM}$$

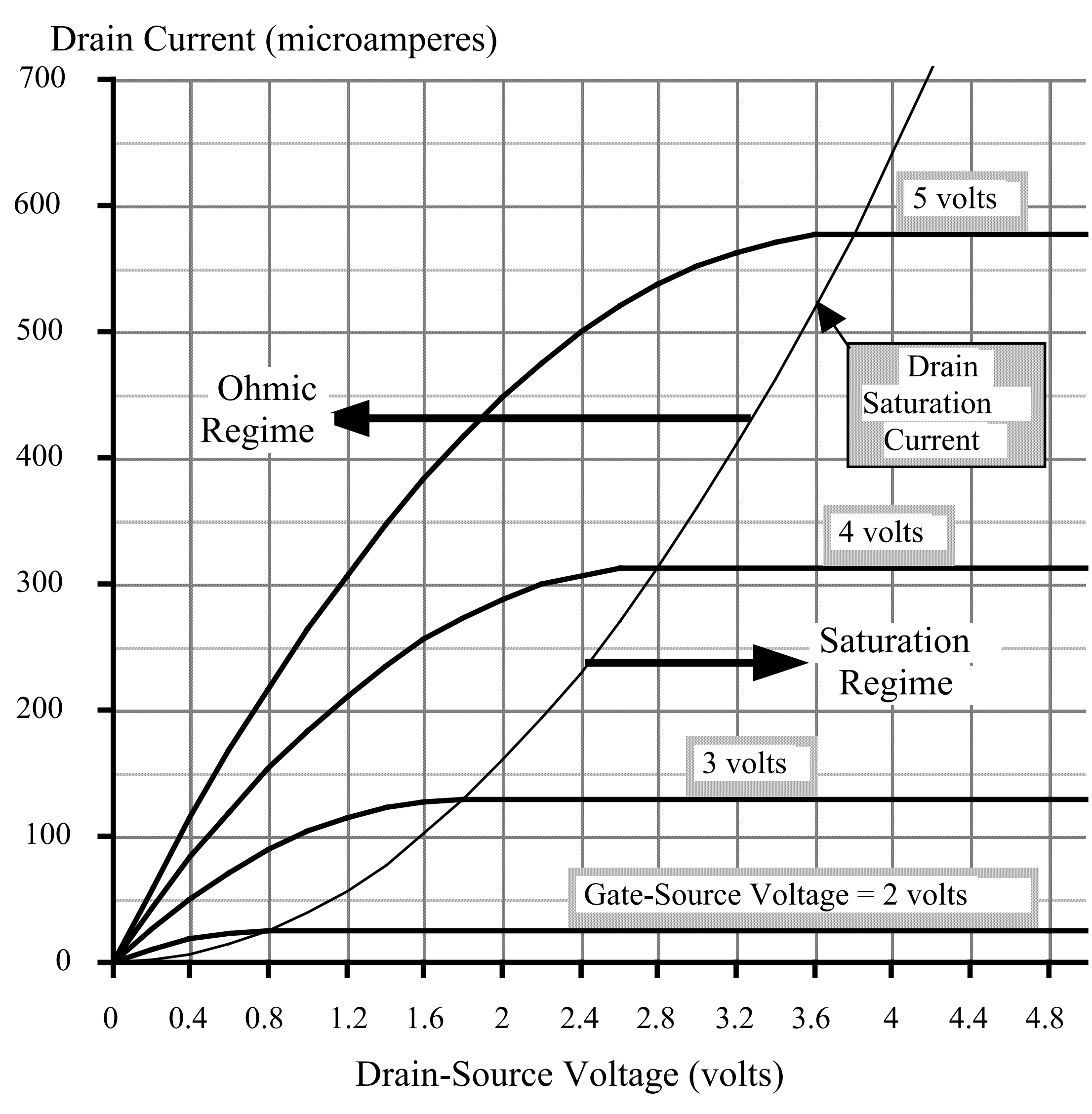
- Note Differential Output Current And Voltage Are Linear With Respect To Differential Input Voltage Without Invoking Small Signal Approximation

Characteristic Curves: Subthreshold Regime

- **Subthreshold Regime:** $V_{gs} < V_{hn} + 2 n V_T \;\&\; V_{ds} \quad 3 V_T$
  - $V_T = \dfrac{k T}{q} = 26 \text{ mV} @ 27 \quad 8C$
  - $1.2 < n < 2.0$
  - $I_d = 2 K_n \left(\dfrac{W}{L} \right) \left(\dfrac{n V_T}{\varepsilon} \right)^2 \mathbf{e}^{(V_{gs} - V_{hn}) / n V_T}$

- **Comments**
  - Bipolar Type I–V Action Indigenous To Subthreshold Regime
  - Subthreshold Operation Corresponds To Gate–Channel Interface Potentials Lying Between One And Two Fermi Potentials
  - Useful Only For Low Speed, Low Power Applications

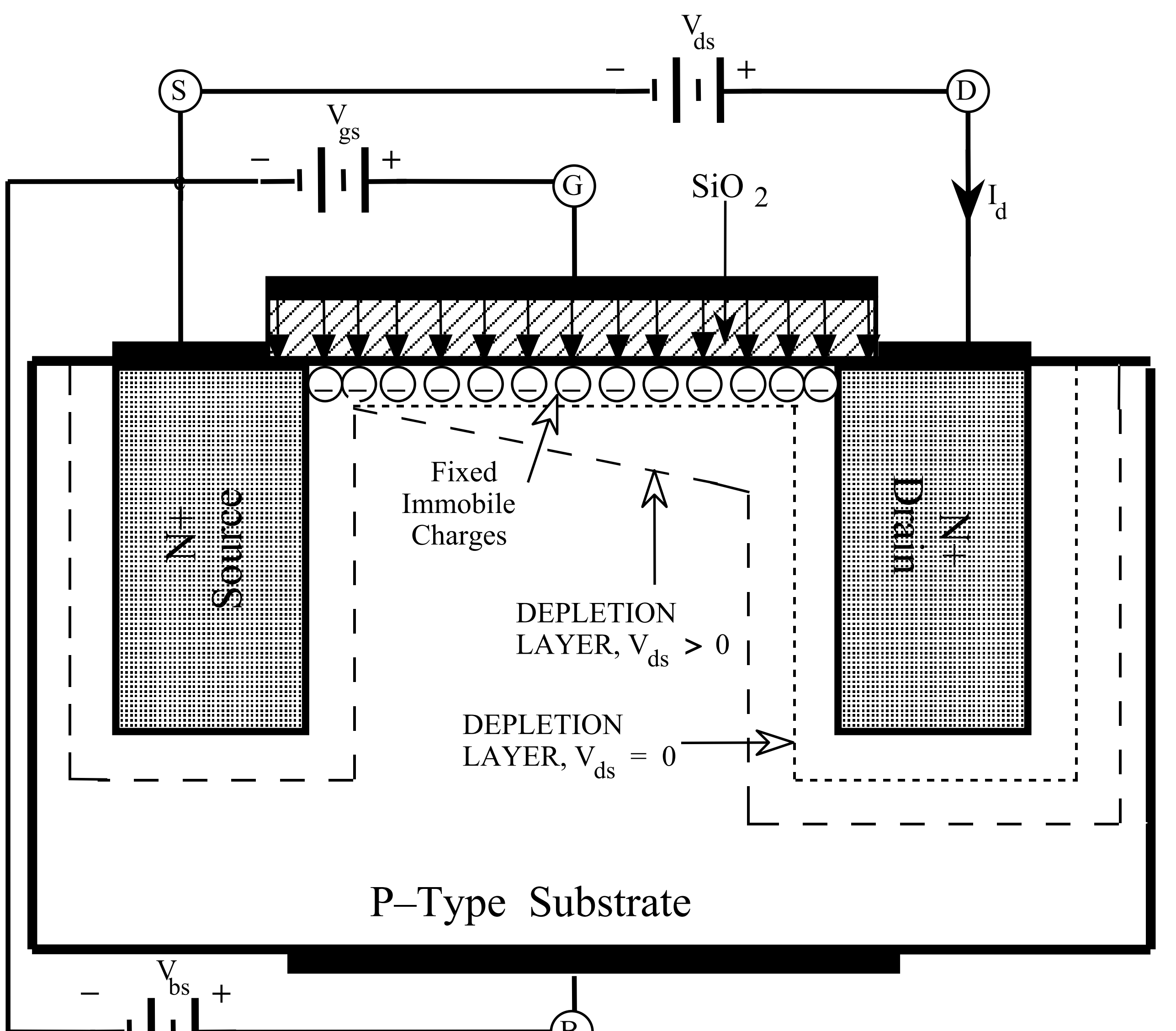
Sample Simplified MOS Static Characteristics



$$K_n \left(\frac{W}{L} \right) = 80 \ \mu\text{mho/volt}$$

$$V_{hn} = 1.2 \text{ volts}$$

Cutoff Regime



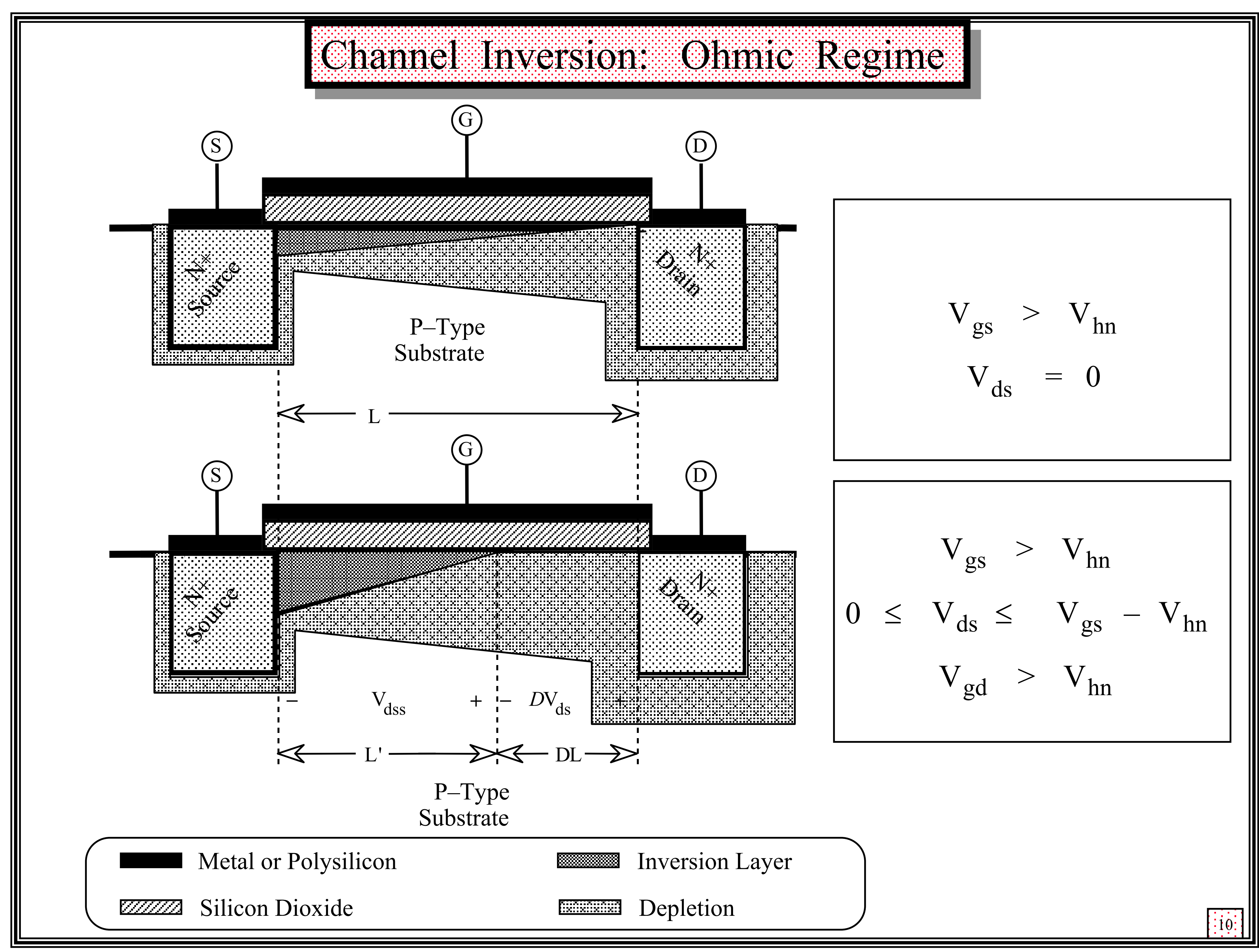
- Depletion

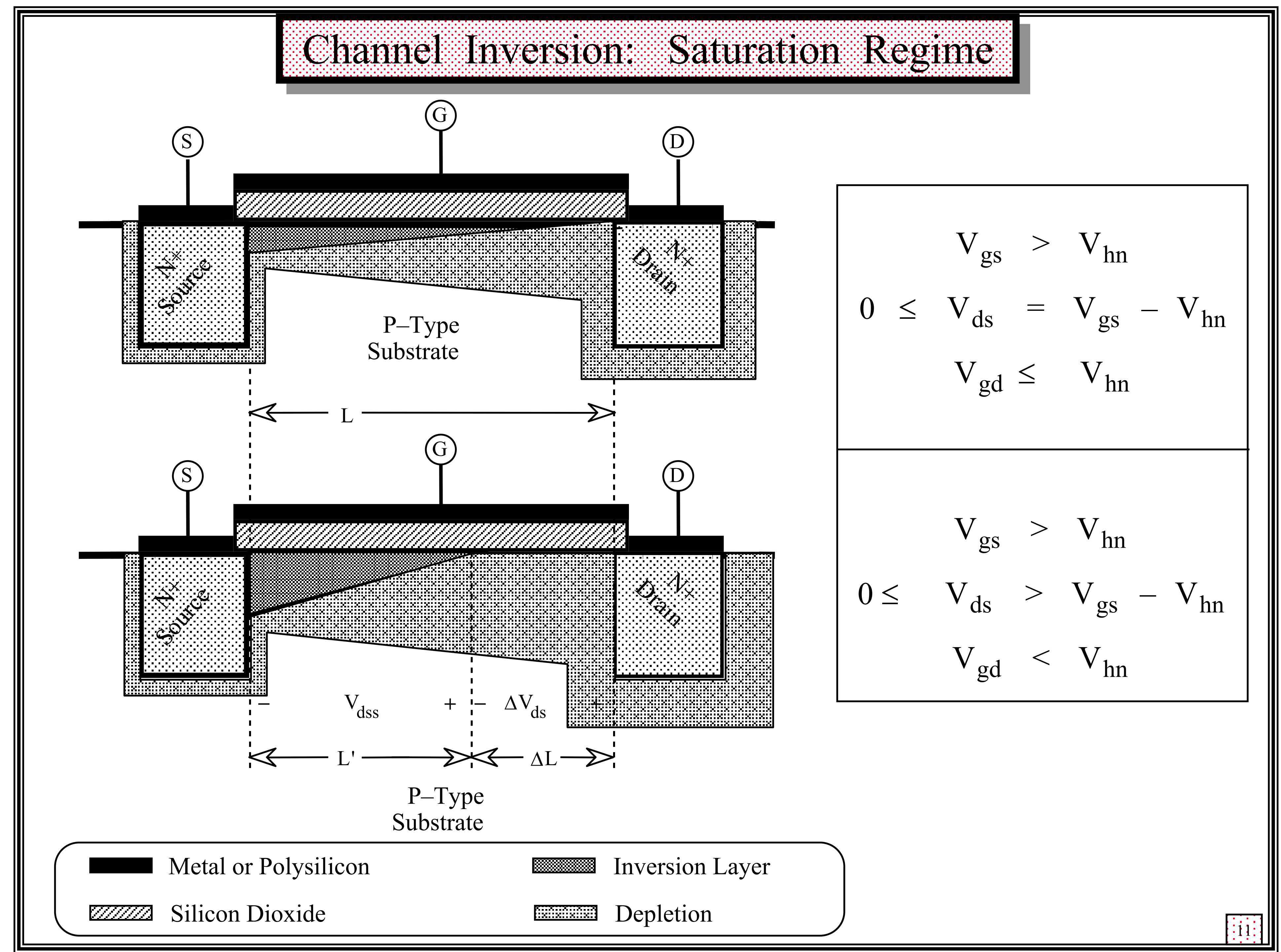
  $V_{ds} \geq 0$

  $0 < V_{gs} < V_{hn}$

  $V_{bs} \leq 0$

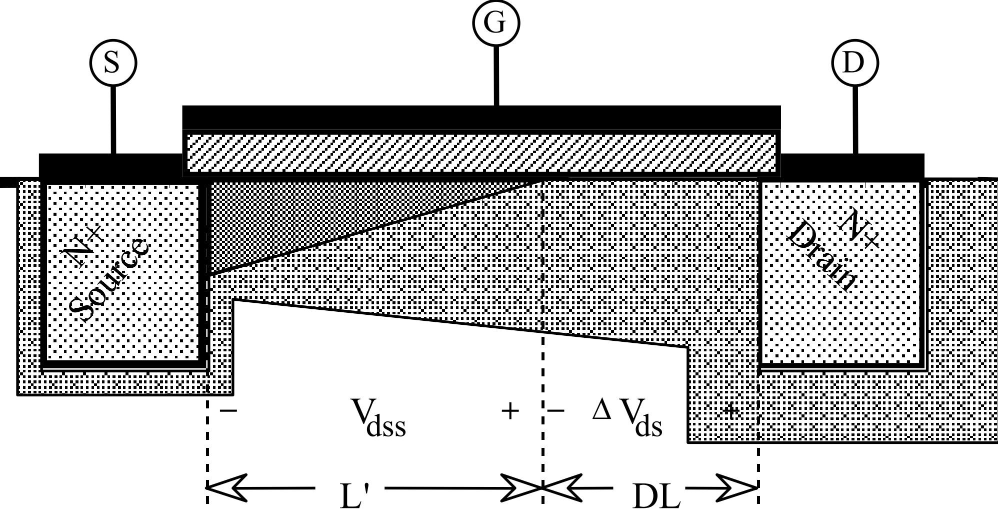
- Zero Current
- $V_{gs} = V_{ox} + V_y$
- $V_{ox} \rightarrow$ Voltage Across Oxide
- $V_y \rightarrow$ Interface Potential


Channel Inversion: Ohmic Regime
G
S
D
N+
Source
N+
Drain
P–Type
Substrate
L
$V_{gs} > V_{hn}$
$V_{ds} = 0$
G
S
D
N+
Source
N+
Drain
– V_{dss} +
– DV_{ds} +
L'
DL
P–Type
Substrate
$V_{gs} > V_{hn}$
$0 \leq V_{ds} \leq V_{gs} - V_{hn}$
$V_{gd} > V_{hn}$
Metal or Polysilicon
Inversion Layer
Silicon Dioxide
Depletion
10



Channel Inversion: Saturation Regime
G
S
D
N+ Source
N+ Drain
P–Type Substrate
L
$V_{gs} > V_{hn}$
$0 \leq V_{ds} = V_{gs} - V_{hn}$
$V_{gd} \leq V_{hn}$
$V_{gs} > V_{hn}$
$0 \leq V_{ds} > V_{gs} - V_{hn}$
$V_{gd} < V_{hn}$
– V_{dss} +
– ΔV_{ds} +
L'
ΔL
Metal or Polysilicon
Inversion Layer
Silicon Dioxide
Depletion
11

Channel Length Modulation



- Modified Saturation Regime Current

$$I_d\Big|_{V_{ds} > V_{dss}} = I_{dss}\left(\frac{L}{L - \Delta L}\right) = \frac{K_n}{2}\left(\frac{W}{L}\right)\left(V_{gs} - V_{hn}\right)^2\left(1 + \frac{V_{ds} - V_{dss}}{V_\lambda}\right)$$

- Channel Modulation Voltage

$$V_\lambda = L\sqrt{\left(\frac{2\,q\,N_A}{\varepsilon_s}\right)\left(V_{ds} - V_{dss} + V_j\right)}$$

(Typically Under 20 Volts And As Small As 1/3 Volt For Deep Submicron MOSFETs)

$$V_{dss} = V_{gs} - V_{hn}$$

$$V_j = \frac{k\,T}{q}\ln\frac{N_D N_A}{N_{iB}^2}$$

Channel Length Modulation Parameters

- Modified Saturation Regime Current

$$I_d \Big|_{V_{ds} > V_{dss}} = I_{dss}\left(\frac{L}{L - \Delta L}\right) = \frac{K_n}{2}\left(\frac{W}{L}\right)\left(V_{gs} - V_{hn}\right)^2\left(1 + \frac{V_{ds} - V_{dss}}{V_\lambda}\right)$$

$$V_{dss} = V_{gs} - V_{hn}$$

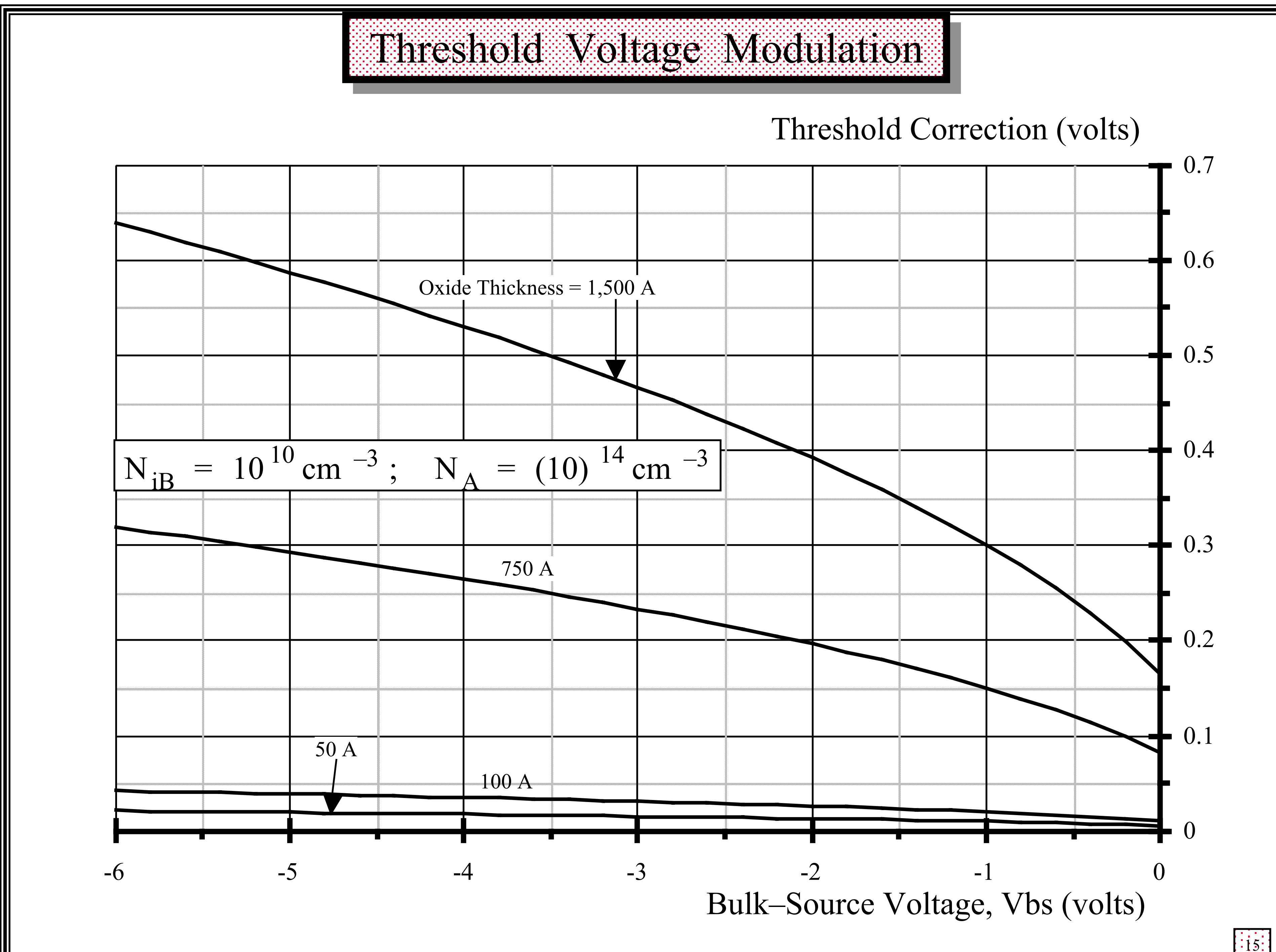
$$V_j = \frac{kT}{q}\ln\frac{N_D N_A}{N_{iB}^2} \qquad V_\lambda = L\sqrt{\left(\frac{2qN_A}{\varepsilon_s}\right)\left(V_{ds} - V_{dss} + V_j\right)}$$

- Parameters
  - $\mathbf{N_A}$ → Average Substrate Impurity Concentration
  - $\mathbf{e_s}$ → Dielectric Constant Of Silicon (1.05 pF/cm)
  - $\mathbf{q}$ → Electronic Charge Magnitude
  - $\mathbf{V_l}$ → Channel Length Modulation Voltage
  - $\mathbf{V_j}$ → Built In Substrate–Drain/Source Junction Potential

- Note
  - Large Channel Length Reduces Channel Modulation
  - Small Substrate Concentration Increases Channel Modulation

Substrate/Bulk Phenomena

- Effect On Threshold Voltage
  - $I_d = \frac{K_n}{2}\left(\frac{W}{L}\right)\left(V_{gs} - V_{hnc}\right)^2\left(1 + \frac{V_{ds} - V_{dss}}{V_\lambda}\right)$
  - $V_h = V_{ho} + 2\sqrt{V_\theta\left(V_F - V_T\right)}\left[\sqrt{\left(1 - \frac{V_{bs}}{2\left(V_F - V_T\right)}\right)} - 1\right]^2$
  - $V_\theta = \frac{q N_A \varepsilon_s}{C_{ox}^2} = q N_A \varepsilon_s \left(\frac{T_{ox}}{\varepsilon_{ox}}\right)^2$ (High Hundreds Of μVolts)
  - $V_F = V_T \ln\left(\frac{N_A}{N_{iB}}\right)$ (Few Tenths Of Volts)
- Parameters
  - $\mathbf{V_F}$ → Fermi Potential; Renders Channel Surface Intrinsic
  - $\mathbf{N_{iB}}$ → Intrinsic Carrier Concentration In Substrate
  - $\boldsymbol{\varepsilon_{ox}}$ → Dielectric Constant Of Silicon Dioxide (345 fF/cm)
- Note
  - Small Oxide Thickness Reduces Threshold Modulation
  - Small Substrate Concentration Reduces Threshold Modulation


Threshold Voltage Modulation
Threshold Correction (volts)
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Oxide Thickness = 1,500 A
$N_{iB} = 10^{10}\ cm^{-3}$; $N_A = (10)^{14}\ cm^{-3}$
750 A
50 A
100 A
-6
-5
-4
-3
-2
-1
0
Bulk–Source Voltage, Vbs (volts)

Mobility Degradation Due To Vertical Field

- Electric Field Problems
  - Thin Oxide Layers Conduce Large Gate -To- Channel Fields For Even Small -To- Moderate Gate–Source Voltages
  - These Enhanced Fields Impart Increasing Energies To Carriers, Thereby Causing More Carrier Collisions And Degraded Mobilities

- Mobility:

$$\mu_{neff} \approx \frac{\mu_n}{1 + \dfrac{V_{gs} - V_{hnc}}{V_E}}$$

$$V_E \approx (500)(10^6)T_{ox} \quad \text{(Low Hundreds Of Volts)}$$

- Parameters
  - μ_{neff} → Effective Carrier Mobility In Channel
  - V_E → Vertical Field Degradation Voltage Parameter
  - Crude One Dimension Approximation To Two Dimensional Problem
  - T_{ox} in MKS Units Yields V_E In Volts

Impact Of Mobility Degradation

- Static Drain Current
  - $K_n = \mu_n C_{ox} \longrightarrow K_{neff} = \mu_{neff} C_{ox}$
  - $$I_d = \frac{K_n}{2}\left(\frac{W}{L}\right)\left[\frac{\left(V_{gs} - V_{hnc}\right)^2\left(1 + \frac{V_{ds} - V_{dss}}{V_\lambda}\right)}{\left(1 + \frac{V_{gs} - V_{hnc}}{V_E}\right)}\right]$$

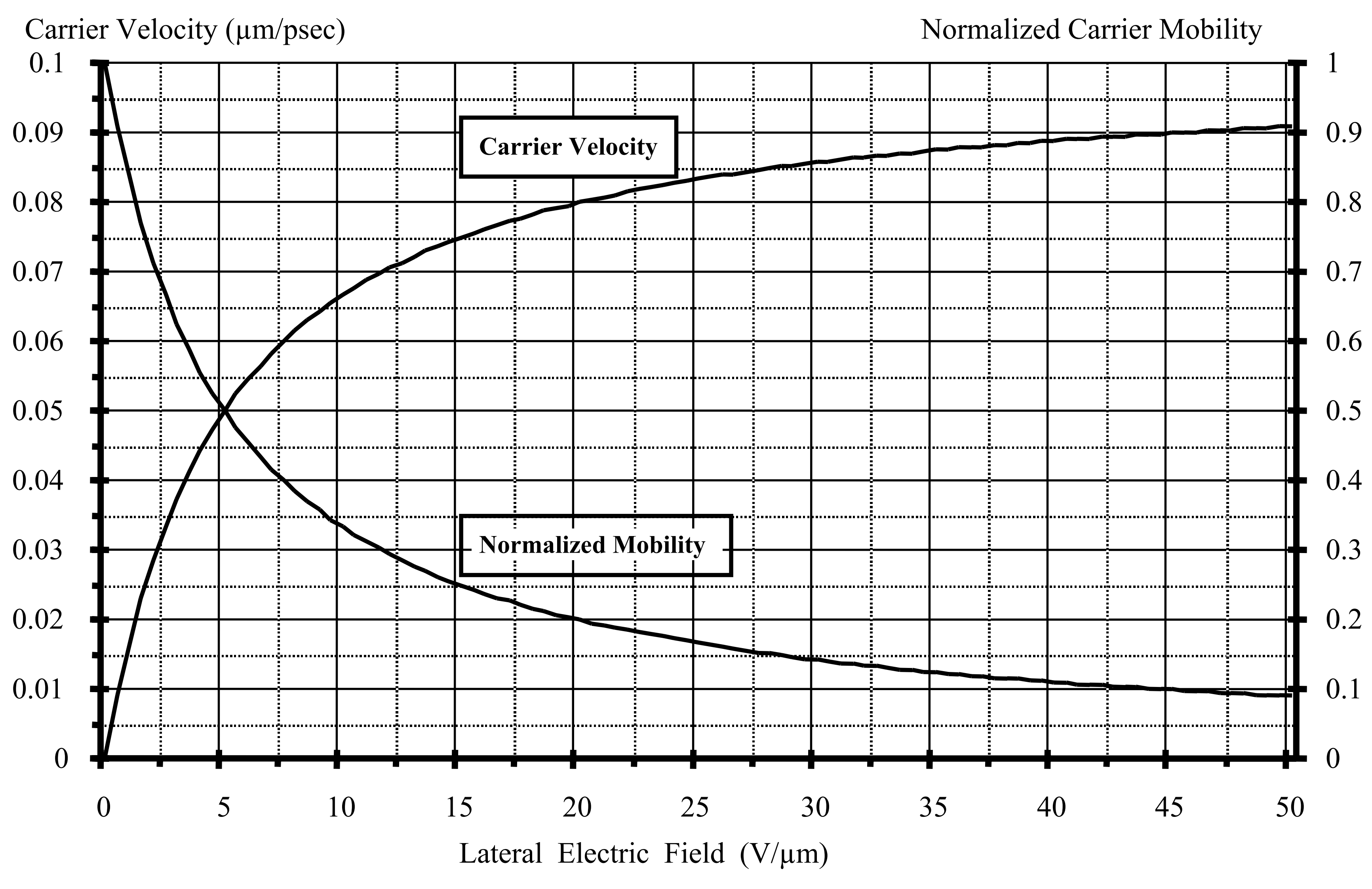
- Other Effects
  - Reduced Bandwidth And Increased Carrier Transit Time
  - Smaller Current For Given Gate–Source Bias
  - Reduced Forward Transconductance

Mobility Degradation Due To Lateral Field

- Electric Field Problems
  - Short Channels Conduce Large Drain -To- Source Fields For Even Small -To- Moderate Drain–Source Voltages
  - These Enhanced Fields Impart Increasing Energies To Carriers, Thereby Causing More Carrier Collisions And Degraded Mobilities
  - At Very Large Horizontal Fields, Carrier Velocities Ultimately Saturate To A Value Of v_{sat}, Which Is About 0.1 µm/pSEC
  - Saturation Occurs When Horizontal Field, E_h, Equals Or Exceeds A Critical Value, E_c, Which Is About 5 V/µm

- Mobility And Field
  - $$\mu_{ne} \approx \frac{\mu_n}{1 + \frac{E_h}{E_c}} = \frac{v_{sat}}{E_c + E_h}$$
  - $$v_{sat} = \mu_n E_c$$
  - $$v = \mu_{ne} E_h \approx \frac{\mu_n E_h}{1 + \frac{E_h}{E_c}}$$
  - $$E_h \approx \frac{V_{gs} - V_{hn}}{L}$$

Velocity – Mobility – Field Relationships



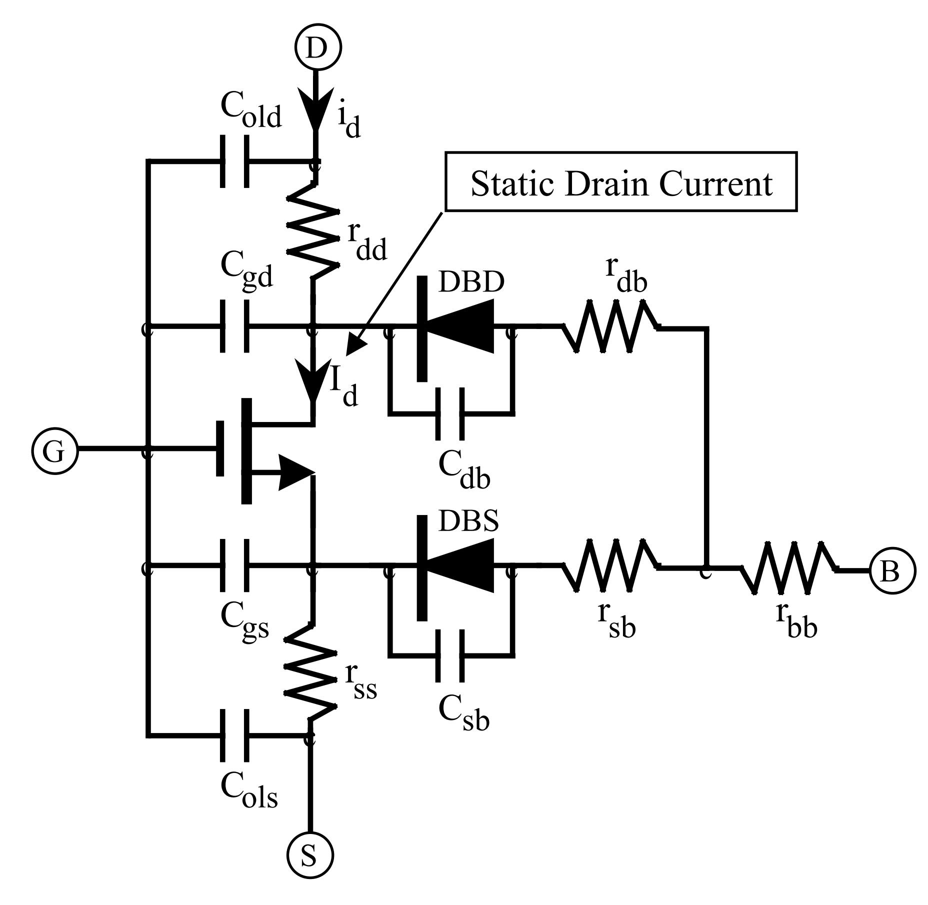
Mobility And Lateral Field

- Mobility And Field
  - $$\mu_{ne} \approx \frac{\mu_n}{1 + \frac{E_h}{E_c}} \approx \frac{\mu_n}{1 + \frac{V_{gs} - V_{hnc}}{L E_c}} = \frac{\mu_n}{1 + \frac{V_{dss}}{L E_c}}$$
  - $$E_h \approx \frac{V_{gs} - V_{hnc}}{L} = \frac{V_{dss}}{L}$$
- Electric Field Problems
  - Crude Approximation For Horizontal Field, E_h
  - Free Carriers Exist Only Over Channel Where Voltage With Respect To The Source Is At Most $V_{dss} = \left(V_{gs} - V_{hnc}\right)$
  - Channel Length, L, Should Be Effective Channel Length, L', But This Shrinkage Is Already Accounted For By Channel Length Modulation Voltage Parameter, V_λ
  - $L E_c$ Is About 1.75 Volts For L = 0.35 μm

Volt–Ampere Impact Of High Lateral Field

- Static Drain Current
  - $K_n = \mu_n C_{ox} \longrightarrow K_{neff} = \mu_{neff} C_{ox}$
  - $$I_d = \frac{K_n}{2}\left(\frac{W}{L}\right)\frac{(V_{gs} - V_{hnc})^2\left(1 + \frac{V_{ds} - V_{dss}}{V_\lambda}\right)}{1 + \frac{V_{gs} - V_{hnc}}{L E_c}}$$
- Very High Fields
  - $V_{gs} - V_{hnc} \gg L E_c$
  - $$I_d \approx \left(\frac{W C_{ox} v_{sat}}{2}\right)\left(V_{gs} - V_{hnc}\right)\left(1 + \frac{V_{ds} - V_{dss}}{V_l}\right)$$
- Comments
  - Drain Current Scales Approximately With W, As Opposed To W/L
  - Drain Current Almost Linear W/R To Gate–Source Voltage

MOS Large Signal Model



DBD → Bulk-Drain Diode

DBS → Bulk-Source Diode

C_{gd} → Gate-Drain Capacitance

C_{gs} → Gate-Source Capacitance

C_{db} → Drain-Bulk Capacitance

C_{sb} → Source-Bulk Capacitance

C_{old} → Drain Overlap Capacitance

C_{ols} → Source Overlap Capacitance

r_{dd} → Drain Ohmic Resistance

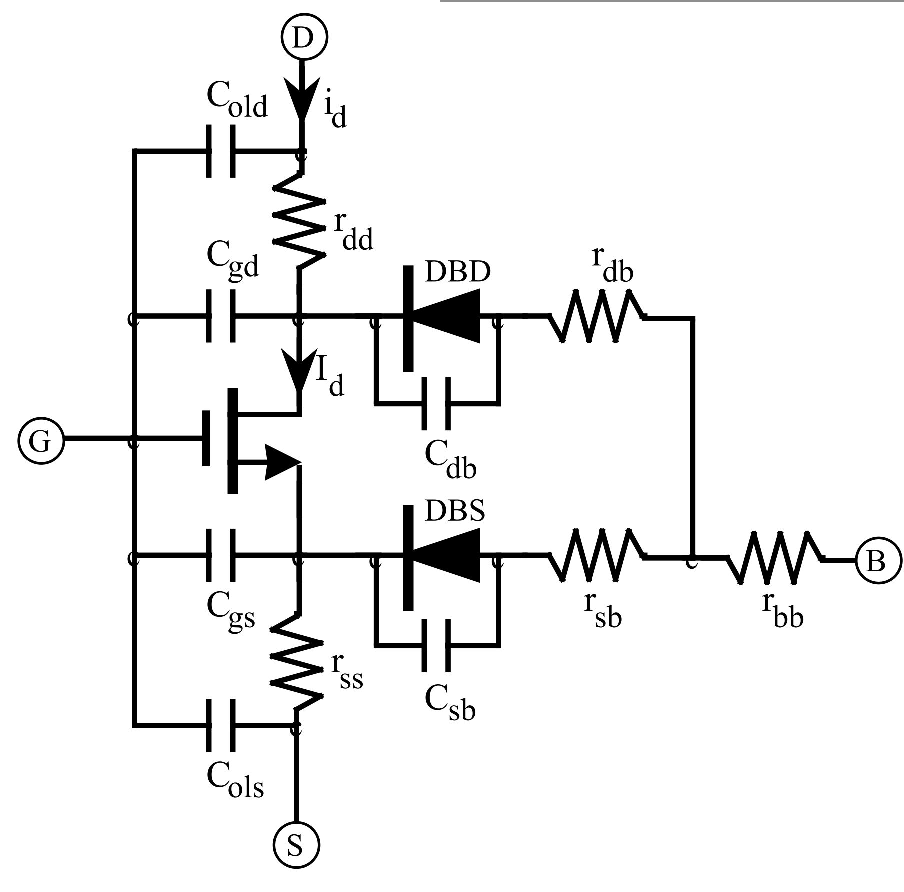
r_{ss} → Source Ohmic Resistance

r_{bb} → Bulk Ohmic Resistance

r_{sb} → Bulk Spreading Resistance

r_{db} → Bulk Spreading Resistance

Device Capacitances In Saturation



C_{db} → Large (Hundreds Of fF)

C_{sb} → Large (Hundreds Of fF)

C_{gs} → Moderate (High Tens Of fF)

C_{gd} , C_{old} , C_{ols} → Small (Tens Of fF)

$$C_{gd} + C_{old} \approx C_{old} = W L_d C_{ox}$$

$$C_{gs} = W L C_{ox} \left(\frac{2}{3} + \frac{L_d}{L} \right)$$

$$C_{db} = \frac{A_d C_{jo}}{\sqrt{1 - \frac{V_{bd}}{V_j}}}$$

$$C_{sb} = \frac{(A_s + W L) C_{jo}}{\sqrt{1 - \frac{V_{bs}}{V_j}}}$$

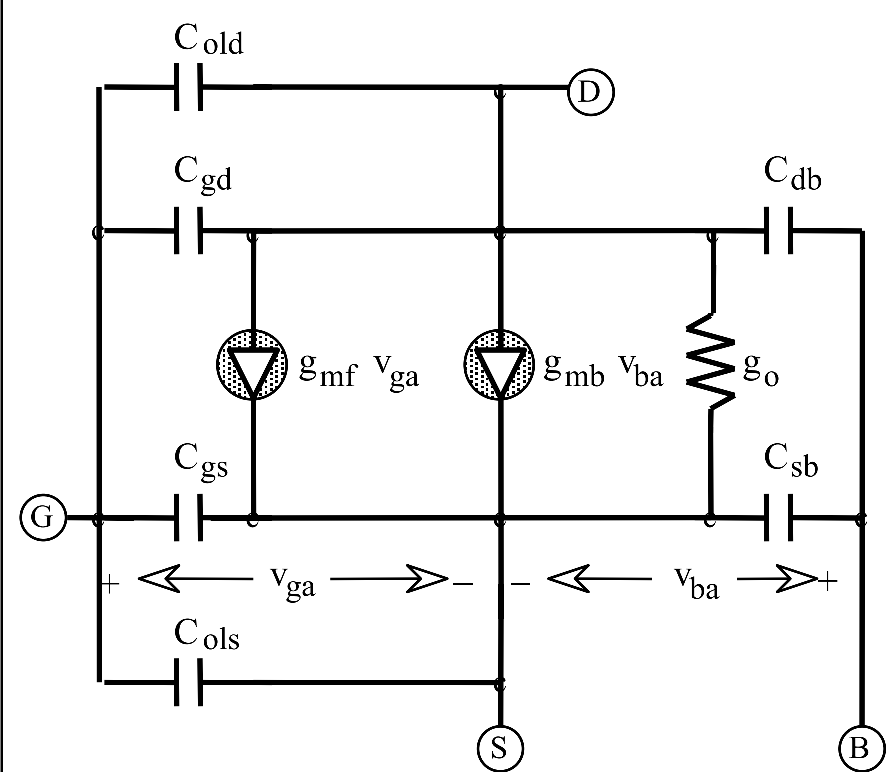
$$C_{ols} = W L_d C_{ox}$$

A_d → Drain-Bulk Junction Area

A_s → Source-Bulk Junction Area

C_{jo} → Zero Bias Depletion Capacitance Density

Approximate (Long Channel) Small Signal Model



$$g_{mf} \triangleq \left.\frac{\partial I_d}{\partial V_{gs}}\right|_Q \approx \sqrt{2K_n\left(\frac{W}{L}\right) I_{dQ}}$$

$$g_{mb} \triangleq \left.\frac{\partial I_d}{\partial V_{bs}}\right|_Q = \lambda_b g_{mf}$$

$$\lambda_b = \sqrt{\frac{V_\theta / 2}{2(V_F - V_T) - V_{bsQ}}}$$

$$g_o \triangleq \left.\frac{\partial I_d}{\partial V_{ds}}\right|_Q \approx \frac{I_{dQ}}{V_\lambda + V_{ds} - V_{dss}}$$

- Assumptions
  - All Series Ohmic Resistances Are Negligible
  - Transistor Operates In Saturation Regime
  - "Long Channel" Approximation Invoked For Static Drain Current
  - Model To Be Used As A Precursor To Computer–Based Studies

Short Channel Small Signal Model

- Drain Current:

$$I_d = \frac{K_n}{2}\left(\frac{W}{L}\right)\frac{\left(V_{gs} - V_{hnc}\right)^2\left(1 + \frac{V_{ds} - V_{dss}}{V_\lambda}\right)}{1 + \frac{V_{gs} - V_{hnc}}{L E_c}}$$

- Intermediate Parameters:

$$f_\lambda = \frac{V_{ds} - V_{dss}}{V_\lambda} \qquad f_c = \frac{V_{dss}}{L E_c}$$

$$g_{mf} = \sqrt{2 K_n\left(\frac{W}{L}\right) I_{dQ}}$$

$$\lambda_b = \sqrt{\frac{V_\theta / 2}{2\left(V_F - V_T\right) - V_{bsQ}}}$$

- Forward Transconductance:

$$g_{mfs} = g_{mf}\sqrt{\frac{1 + f_\lambda}{1 + f_c}}\left(1 - \frac{V_{dss}/2V_\lambda}{1 + f_\lambda} - \frac{f_c/2}{1 + f_c}\right)$$

- Bulk Transconductance:

$$g_{mbs} = \lambda_b\, g_{mfs}$$

- Output Conductance:

$$g_o = \frac{I_{dQ}}{V_\lambda + V_{ds} - V_{dss}}$$

Hypothetical Device

- **Physical Parameters**

  $N_A = 5\,(10)^{14}\ cm^{-3}$

  $N_D = 5\,(10)^{20}\ cm^{-3}$

  $N_{iB} = (10)^{10}\ cm^{-3}$

  $\varepsilon_s = 1.05$ pF/cm

  $\varepsilon_{ox} = 345$ fF/cm

  $\mu_n = 400\ cm^2/$ volt-sec

  $E_c = 4$ volts / µm

- **Device Parameters**

  $T_{ox} = 50$ Angstroms

  $L = 0.35$ µm

  $V_{hn} = 0.65$ volts

  $T = 300$ 8K

  $W/L = 5$

- **Circuit Parameters**

  $V_{ds} = 2$ volts

  $V_{gs} = 1.2$ volts

  $V_{bs} = -3$ volts

Static Performance

- Peripheral Calculations

  V_F = 280.0 mV (Fermi Potential)

  V_j = 917.4 mV (Junction Potential)

  V_u = 176.4 μV (Body Effect Potential)

  V_{hnc} = 685.2 mV (Compensated Threshold) → ΔV_{hn} = 35.2 mV

  V_{dss} = 514.8 mV (Drain Saturation Voltage)

  V_λ = 669.7 mV (Channel Length Voltage)

  $L E_c$ = 1.4 volts (Lateral Field Voltage)

  K_n = 276.0 μmho / volt (Transconductance Parameter)

  f_λ = 2.218 (Channel Length Parameter)

  f_c = 0.368 (Lateral Field Parameter)

- Static Drain Current
  - I_d = 182.9 μA (Long Channel Drain Current)
  - I_d = 430.2 μA (Short Channel Drain Current)
  - Note Short Channel -To- Long Channel Ratio of 2.35; Ratio Is Generally Between 1.5 And 3.0

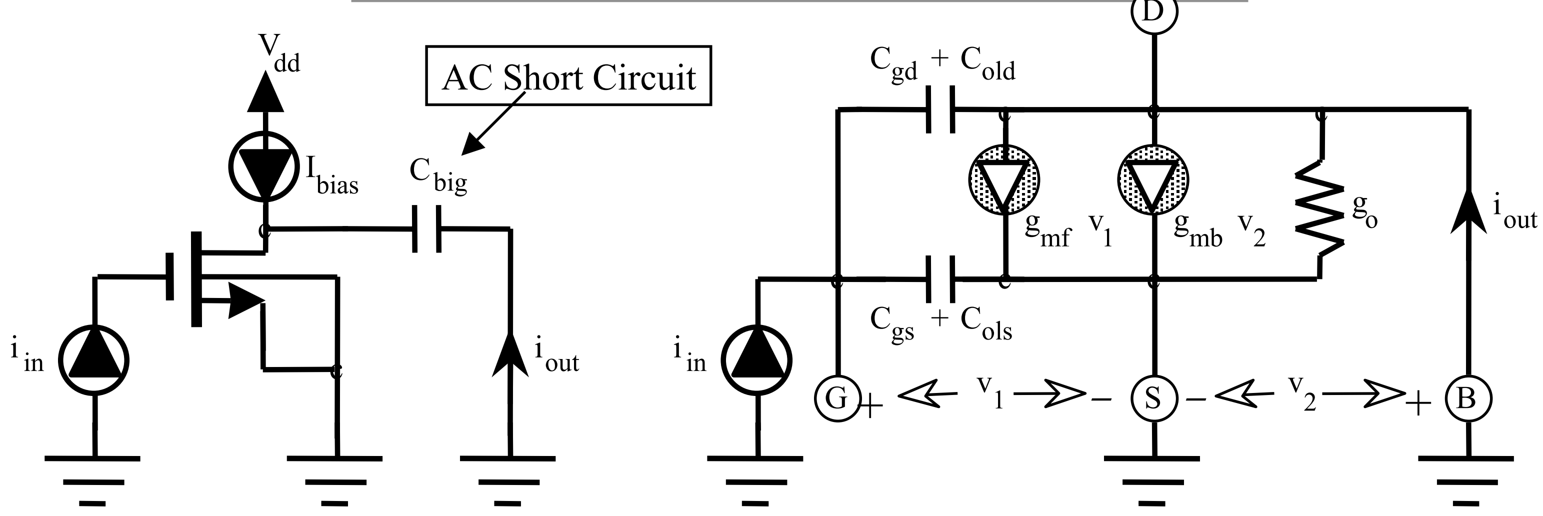
Small Signal Parameters

- **Forward Transconductance**
  - g_{mf} = 1.09 mmho (Ignoring Short Channel Effects)
  - g_{mf} = 1.25 mmho (Incorporating Short Channel Effects)
  - Note Short Channel -To- Long Channel Ratio of 1.14; Ratio Is Generally Between 0.5 And 2.0

- **Bulk Transconductance**
  - λ_b = 5.0 2 $(10)^{-2}$ (Bulk Parameter)
  - g_{mb} = 6.25 μmho (Incorporating Short Channel Effects)
  - Note Bulk Transconductance Is About 200 Times Smaller Than Forward Transconductance

- **Drain–Source Conductance**
  - g_o = 199.7 μmho (Incorporating Short Channel Effects)
  - Corresponds To Shunt Output Resistance Of About 5 KΩ
  - Mandates Conductance Enhancement Strategies When Designing High Performance Transconductors

Device Unity Gain Frequency

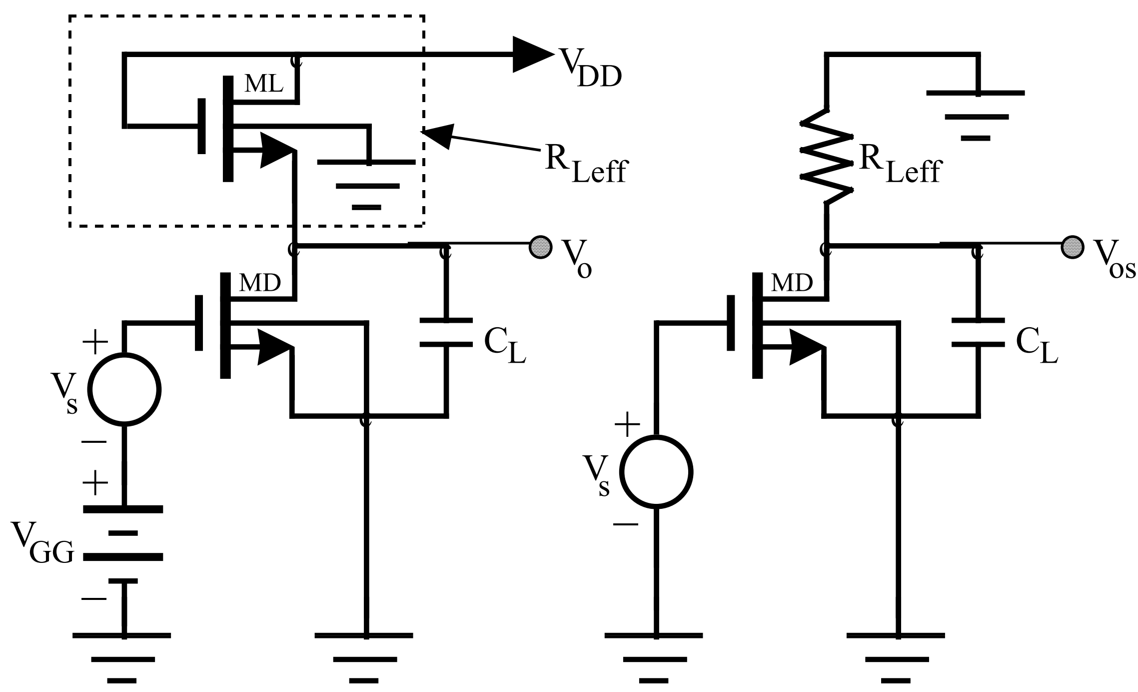


- $$\frac{i_{out}}{i_{in}} = \frac{g_{mf} - s\left(C_{gd} + C_{old}\right)}{s\left(C_{gs} + C_{ols} + C_{gd} + C_{old}\right)}$$

- $$\omega_T \approx \frac{g_{mf}}{C_{gs} + C_{ols} + C_{gd} + C_{old}} \approx \frac{\mu_n\left(V_{gs} - V_{hn}\right)}{L^2\left(\frac{2}{3} + \frac{3L_d}{L}\right)}$$

- **Comments**
  - Unity Gain Frequency Is Good Device Figure Of Merit; Crude Circuit Performance Figure Of Merit
  - Result Assumes $\omega_T C_{gd} \ll g_{mf}$

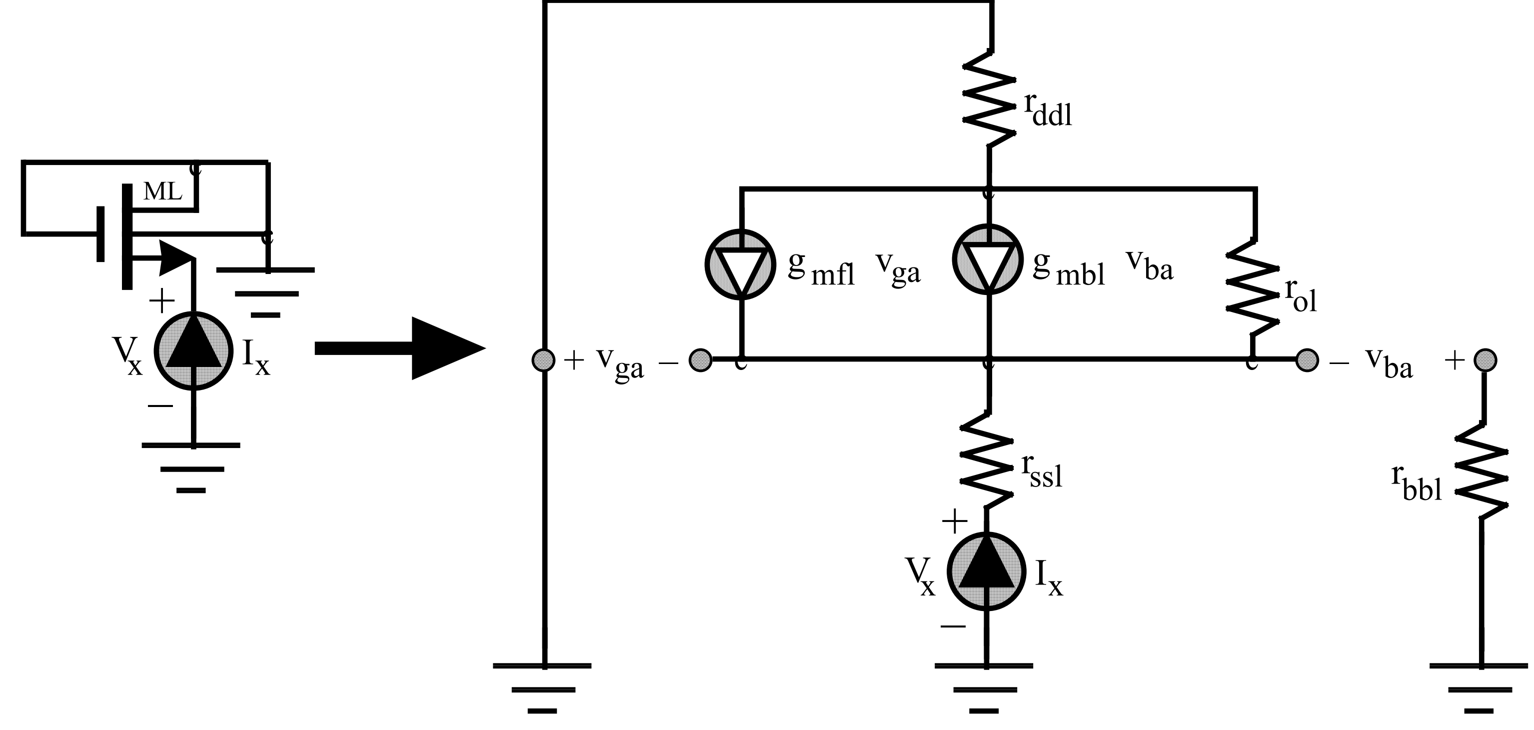
Common Source Inverter



Schematic Diagram

AC Schematic Diagram

Inverter Load Resistance Calculations

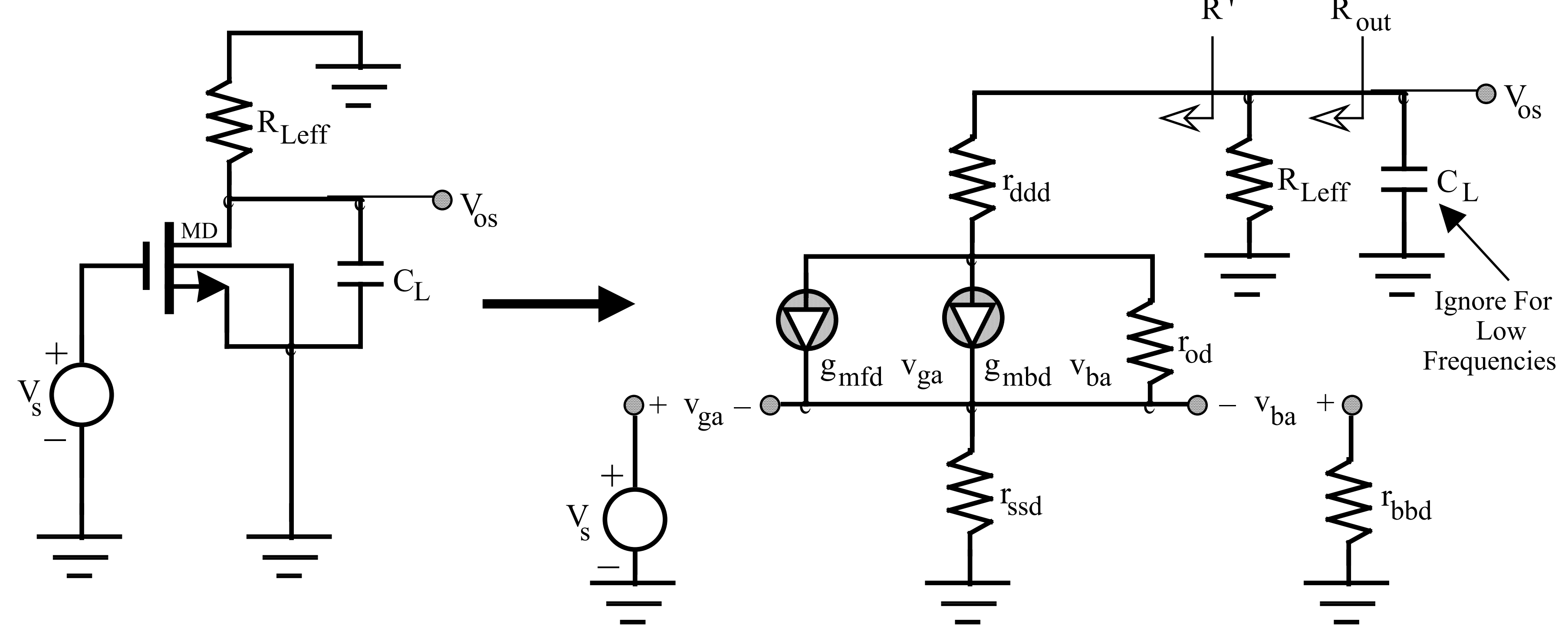


$$v_{ga} = v_{ba} = -V_x + r_{ssl} I_x$$

$$V_x = \left(r_{ssl} + r_{ddl}\right) I_x + r_{ol}\left(I_x + g_{mfl} v_{ga} + g_{mbl} v_{ba}\right)$$

$$R_{Leff} \triangleq \frac{V_x}{I_x} = r_{ssl} + \frac{r_{ddl} + r_{ol}}{1 + \left(1 + \lambda_{bl}\right) g_{mfl} r_{ol}} \approx \frac{1}{\left(1 + \lambda_{bl}\right) g_{mfl}}$$

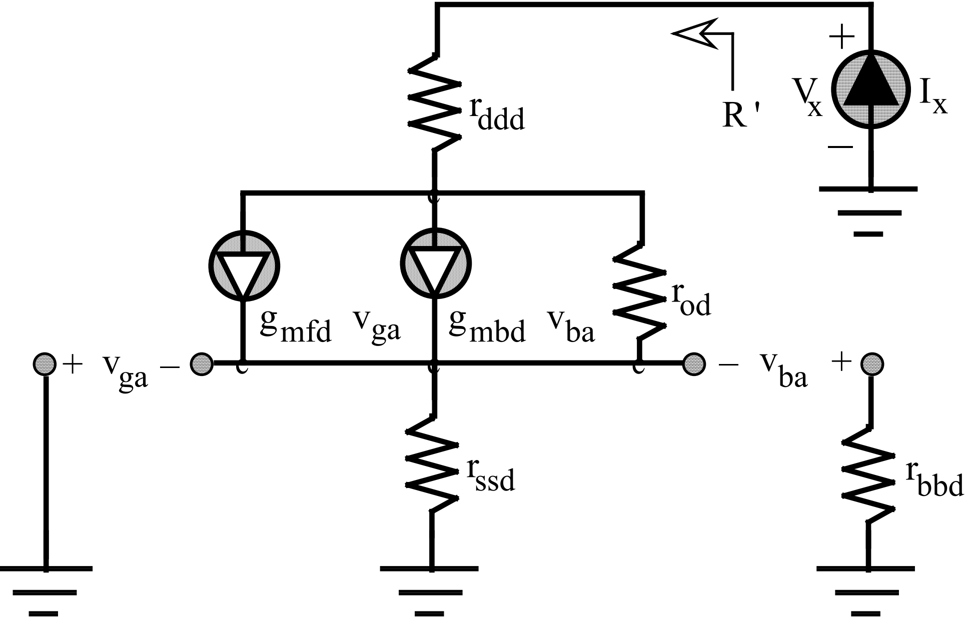
Inverter Gain Calculations



$$A_v = \frac{V_{os}}{V_s} = -\frac{g_{mfd}\, R_{Leff}}{1 + (1+\lambda_{bd})\, g_{mfd}\, r_{ssd} + \dfrac{R_{Leff} + r_{ddd} + r_{ssd}}{r_{od}}} \approx -g_{mfd}\, R_{Leff} \approx -\frac{g_{mfd}}{(1+\lambda_{bl})\, g_{mfl}}$$

$$A_v \approx -\left(\frac{1}{1+\lambda_{bl}}\right)\sqrt{\frac{W_d/L}{W_l/L}}$$

Inverter Bandwidth Calculations



$$B_{3dB} = \frac{1}{R_{out}\, C_L} = \frac{1}{\left(R' \,|\, R_{Leff}\right) C_L} \approx \frac{1}{R_{Leff}\, C_L}$$

$$R' = \frac{V_x}{I_x} = r_{ddd} + r_{ssd} + \left[1 + \left(1 + \lambda_{bl}\right) g_{mfd}\, r_{ssd}\right] r_{od}$$

$$B_{3dB} \approx \frac{1}{R_{Leff}\, C_L} \approx \frac{\left(1 + \lambda_{bl}\right) g_{mfl}}{C_L}$$

$$GBP \;\triangleq\; \left| A_v B_{3dB} \right| = \frac{g_{mfd}}{C_L}$$