Chapter 5

CMOS Compatible Bulk Micromachining

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Additional information is available at the end of the chapter

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1. Introduction

The last two decades have seen the emergence and prevalence of Micro-Electro-Mechanical Systems (MEMS) technology. The reduction in size, low power consumption and low cost is the ultimate goals of application specific MEMS devices. One way to achieve these goals is the monolithic integration of MEMS technology with the standard integrated circuit (IC) technology. The utilization of the conventional IC technology as a platform for design of the fast-growing MEMS technology has led to development of numerous devices and technologies in the past years. Much effort has been made and large capital has been invested into mainstream Complementary Metal-Oxide Semiconductor (CMOS) compatible MEMS technology. This approach has enabled MEMS devices to be directly integrated with CMOS circuits, allowing smaller device sizes and higher performances. This integration of MEMS technology with the mainstream CMOS technology is referred to as CMOS-MEMS technology [1].

1.1. Bulk micromachining technologies

Among all micromachining technologies, Bulk micromachining is the oldest one. To make small mechanical components using bulk micromachining technology, substrate material such as silicon wafer is selectively etched. There are two major classes of bulk micromachining: wet bulk micromachining (WBM) and dry bulk micromachining (DBM).WBM gives nice feature resolution and vertical sidewalls for deep trenches in the substrate but have numerous disadvantages such as incompatibility with microelectronic circuits and higher cost due to mask requirement. The fabrication cost, time and simplification of micromachining for MEMS devices is reduced by using dedicated MEMS foundry and making the prototyping development cycle much shorter by reducing number of masks and photolithography steps. CMOS MEMS technology is a good solution for post micromachining because in this technology CMOS circuitry is protected completely by the top metal layer and the same top metal layer

is used as mask to define MEMS structures in MEMS region during the post-CMOS micromachining. That is why this post micromachining process is known as CMOS-compatible.

1.1.1. Wet bulk micromachining

Wet bulk micromachining is done normally with the help of chemicals. In chemical wet etching, the silicon substrate is immersed into the solution of reactive chemicals which etches the exposed regions of substrate at measureable rates. Wet etching typically uses alkaline liquid solvents, such as potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) to dissolve silicon which has been left exposed by the photolithography masking step. These alkali solvents dissolve the silicon in a highly anisotropic way, with some crystallographic orientations dissolving up to 1000 times faster than others. Fig. 1 shows the three major crystal planes in a cubic unit of silicon.

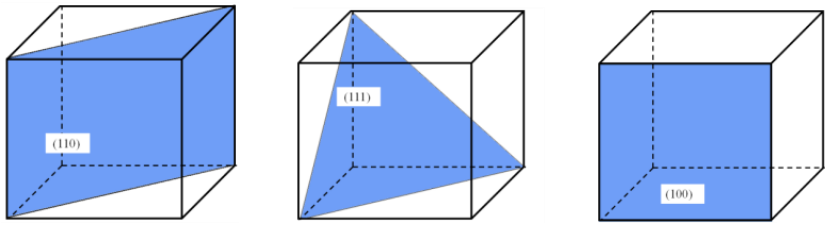

Figure 1. The three orientations <110>, <111> and <100> are the respective directions normal to the plane

For example in silicon anisotropic etching, planes <111> are etched at slower rate than all other planes. The reasons for the slow etch rate of planes <111> are, high density of silicon atoms exposed to the etchant solution in this direction and three silicon bonds laying below the plane. Fig. 2 (a) shows a schematic and (b) three dimensional photo of a typical wet anisotropic etching of a silicon substrate.

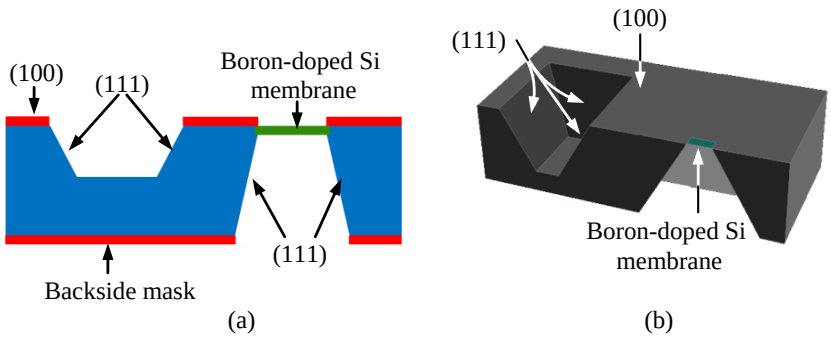

Figure 2. a) 2-D Schematic and (b) 3-D diagram of a typical wet bulk micromachining of Si

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Wet chemical micromachining technology is popular in MEMS industry because of high etch rate and selectivity. There is one drawback and that is the mask is also etched during normal etching process so it is suggested to find a mask that doesn't dissolve or at least dissolves at a much slower rate than the silicon substrate. In wet etching, etch rates and selectivity can be modified by various methods such as: (a) chemical composition of etching solution, (b) dopant concentration in the substrate, (c) adjusting temperature of etching solution and finally (d) Modifying crystallographic planes of the substrate.

Chemical wet etching in bulk micromachining may be further subdivided into two parts: isotropic wet etching where the etch rate is not dependent on crystallographic orientation of the substrate and etching proceeds in all directions at equal rates as shown in Fig.3 (a) and anisotropic wet etching where the etch rate is dependent on crystallographic orientation of substrate as shown in Fig. 3 (b). Often in order to control etching process and uniform etch depths across the wafer, etch stops are used. Generally three types of etch stops are used in micromachining: Dopant etch stops, Electrochemical etch stops and Dielectric etch stop.

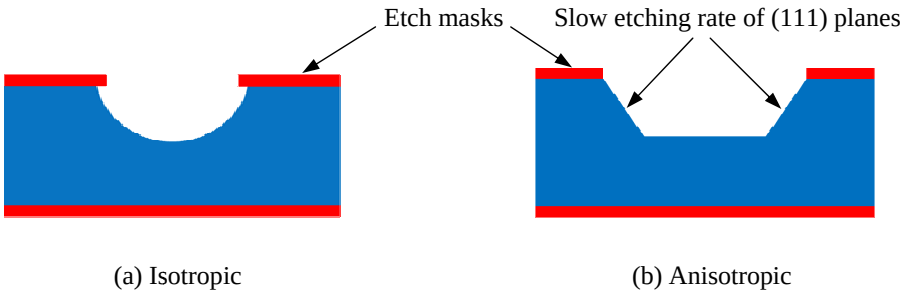

Figure 3. Difference between (a) isotropic and (b) anisotropic wet etching

Usually in order to control etching process and uniform etch depths across the wafer, etch stops are used. Generally three types of etch stops are used in micromachining: Dopant etch stops, Electrochemical etch stops and Dielectric etch stop [2].

1.1.2. Dry bulk micromachining

Dry etching in bulk micromachining is classified into three groups: Reactive ion etching (RIE), Vapor phase etching and Sputter etching. Reactive ion etching (RIE) uses both physical and chemical mechanisms to achieve high levels of resolution. The process is one of the most diverse and most widely used processes in industry and research. Since the process combines both physical and chemical interactions, the process is much faster. The high energy collision from the ionization helps to dissociate the etchant molecules into more reactive species. In the RIE-process, cations are produced from reactive gases which are accelerated with high energy to the substrate and chemically react with the silicon. The typical RIE gasses for Si are CF_4, SF_6 and $BCl_2 + Cl_2$.

Both physical and chemical reaction is taking place with the physical part similar to the sputtering deposition. If the ions have high enough energy, they can knock atoms out of the material to be etched without a chemical reaction. It is very complex task to develop dry etch processes that balance chemical and physical etching, since there are many parameters to adjust. By changing the balance it is possible to influence the anisotropy of the etching with the chemical part being isotropic and the physical part highly anisotropic and therefore the combination can form side walls that have shapes from rounded to vertical.

A special subclass of RIE which continues to grow rapidly in popularity is deep RIE (DRIE). In this process, etch depths of hundreds of microns can be achieved with almost vertical sidewalls. The primary technology is based on the so-called "Bosch process", named after the German company Robert Bosch which filed the original patent, where two different gas compositions are alternated in the reactor. The first gas composition etches the substrate, and the second gas composition creates a polymer on the surface of the substrate. The polymer is immediately sputtered away by the physical part of the etching, but only on the horizontal surfaces and not the sidewalls. Since the polymer only dissolves very slowly in the chemical part of the etching, it builds up on the sidewalls and protects them from etching and working as pasivation, as illustrated in fig. 4. In fig.4 (a) SF_6 is etching the silicon while in fig. 4 (b) C_4F_8 is playing the role of passivation and in fig. 4 (c) again SF_6 is etching. As a result, etching aspect ratios of 1 to 50 can be achieved. The process can easily be used to etch completely through a silicon substrate, and etch rates are 3-4 times higher than wet etching. In the following part more details are given on DRIE. Under our MEMS research group in Universiti Teknologi PETRONAS, high aspect ratio of 3 to 50 μm and complete etch through is achieved as shown in fig.5.

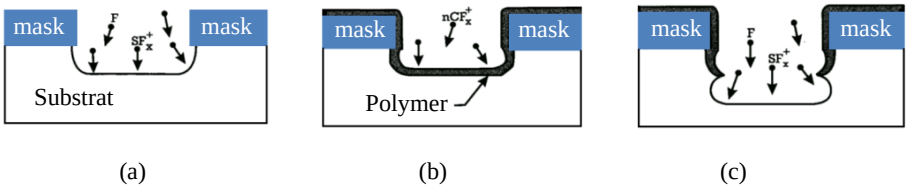

Figure 4. Illustration of etching and passivation in DRIE

Vapor phase etching (also called Chemical dry etching) does not use liquid chemicals or etchants. This process involves a chemical reaction between etchant gases to attack the silicon surface. The chemical dry etching process is usually isotropic and exhibits high selectively. Anisotropic dry etching has the ability to etch with finer resolution and higher aspect ratio than isotropic etching. Due to the directional nature of dry etching, undercutting can be avoided. Some of the ions that are used in chemical dry etching is tetrafluoromethane (CH_4), sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), chlorine gas (Cl_2), or fluorine (F_2) [3]. Vapor phase etching can be done with simpler equipment than what RIE requires. The two most common vapor phase etching technologies are silicon dioxide etching using hydrogen fluoride (HF) and silicon etching using xenon diflouride (XeF_2), both of which are isotropic in nature.

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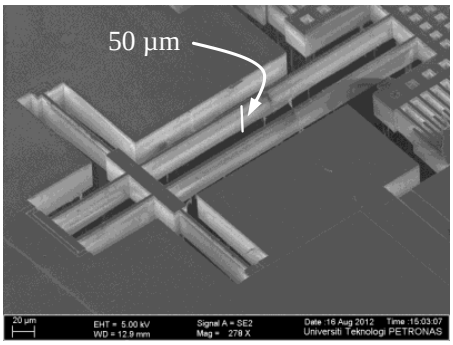

Figure 5. FESEM image of a high aspect ratio plasma etching using DRIE with inhibitor

Usually, care must be taken in the design of a vapor phase process to not have bi-products formed in the chemical reaction that condense on the surface and interfere with the etching process.

Sputter etching is essentially RIE without reactive ions. The systems used are very similar in principle to sputtering deposition systems. The big difference is that the substrate is now subjected to ion bombardment instead of the material target used in sputter deposition [4].

2. CMOS compatible micromachining

CMOS compatible micromachining is now commonly known as CMOS MEMS technology. During post processing in CMOS MEMS technology, the top metal layer acts as mask to define MEMS structures. For the front side processing of the die no photolithographic steps are required. CMOS MEMS technology facilitates the wiring of MEMS structures to integrated circuits due to many metal layers. Through monolithic integration of the CMOS-MEMS devices with circuits, the parasitic capacitances is reduced and overall high performance devices is achieved. Dry post CMOS MEMS technologies are divided into two classes: Thin film micromachining technology (Thin-film Post-CMOS MEMS Technology) and DRIE bulk micromachining technology (DRIE Post-CMOS MEMS Technology).

2.1. Thin-film post-CMOS MEMS technology

The process flow of thin-film CMOS-MEMS with three metal layers is shown in Fig. 6. The CMOS circuit region is designed to be covered by the top metal layer and the MEMS structures are also pre-defined by the top metal layer or the other interconnect metal layers. Fig.6 (a) shows the cross-section of the original chip after CMOS foundry fabrication, with a passivation layer on top. Two processing steps are performed only on the front side of the chip. First, the pre-defined MEMS structure is opened by etching the SiO_2 dielectric stack layer as shown in Fig.6 (b). This is done by an anisotropic SiO_2 plasma etch using Tegal SS110 A DRIE system

based on Bosch technology [5]. Next, an anisotropic silicon DRIE is performed using the same Tegal DRIE system as shown in Fig.6 (c), followed by isotropic silicon etch, which releases the MEMS structure by undercutting the silicon beneath as shown in Fig.6 (d). The depth of the anisotropic etch into the silicon controls the gap between the released structure and the silicon substrate. This gap should be large enough to eliminate the parasitic capacitance between the MEMS structures and the silicon substrate. In practice, it is normally on the order of 30 μm [6].

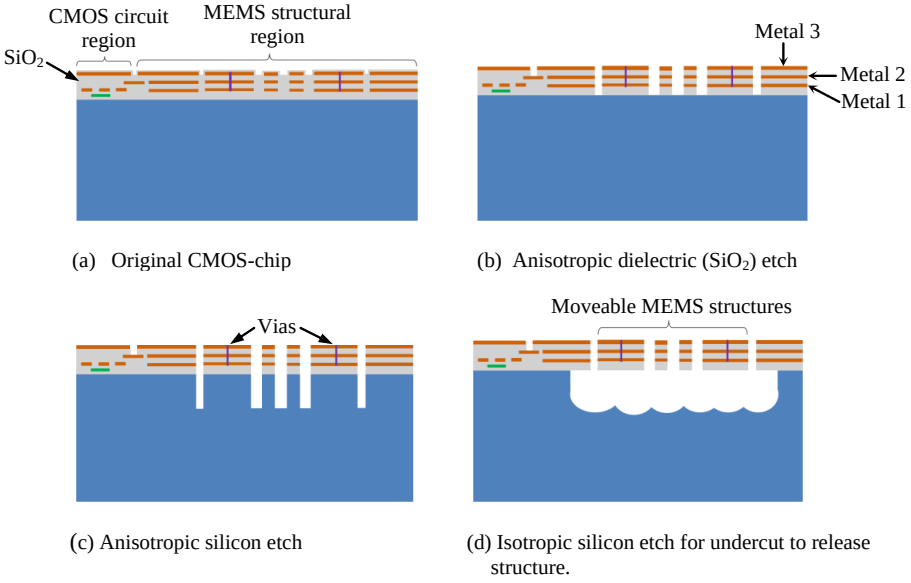

Figure 6. The process-flow for thin film DRIE post-CMOS micromachining

A resonant magnetic field sensor and piezoresistive accelerometer are examples of devices fabricated using this technology [7, 8]. This simple fabrication process yields much smaller parasitic effects as compared to the other processes such as poly MUMPs and it provides flexible wiring by using the multiple metal layers. However, there are some drawbacks in this technology, which limit the performance of the fabricated accelerometers. First, there is large vertical curling in the comb fingers of the suspended MEMS structures caused by the residual stress gradient existing in the composite SiO_2/Al layers as shown in Fig. 7. Additionally, due to different thermal expansion coefficients (TEC) of Al and SiO_2, the curled MEMS devices exhibit a strong temperature dependence, which limits their utility. Although particular compensation technology was employed to reduce the structure mismatch by using a specially designed frame, the device fabricated using this thin film process still has a stringent size limit.

Second, for sensors which require proof mass like inertial sensors fabricated using this technology, the requirement of holes on the proof mass reduces the proof mass, resulting in a lower mechanical sensitivity of the sensors. To achieve a capacitance change large enough for

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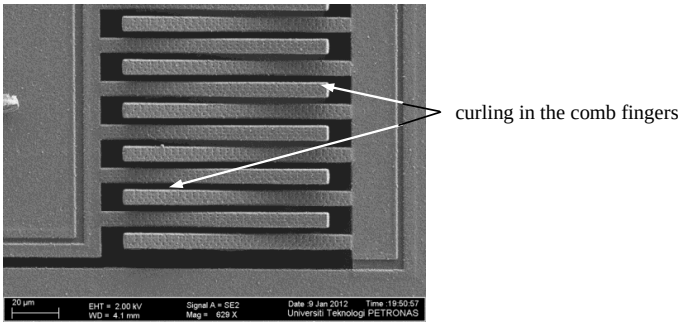

Figure 7. FESEM image of typical comb fingers fabricated using thin film CMOS-MEMS technology

the readout circuit to detect, the dimension of the sensors may need to be considerably large, which is in conflict with the dimensional limit imposed by the possibility of structure curling. Third, in-plane curling of the thin film structures due to fabrication variations also limits the maximum size of the device.

Although there are some specific processes designed for low residual stress thin films [9], Farooq et al utilized the Malaysian Institute of Microelectronic Systems (MIMOS Bhd) 0.35 μm CMOS foundry processes to reduce the curling of the MEMS structures by proper design of the structures as described in [10]. Fig. 8 shows the successfully released central shuttle of magnetic field sensor fabricated using this process. It can be clearly observed that the curling in the structure has been significantly reduced as indicated by the minor curling in the fingers. In addition to the collection of technological data directly from the employed CMOS foundries, systematic post-CMOS process calibration must be conducted to characterize the process variations and their effects on the MEMS devices.

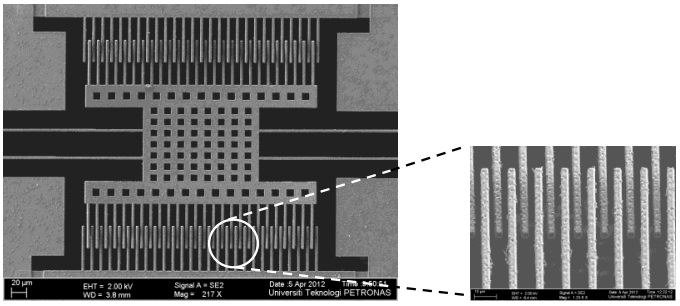

Figure 8. FESEM image showing comb fingers of the central part of a magnetic field sensor

Lastly, since the last release step is an isotropic etch, it undercuts the silicon close to the circuit and structure anchors. The ratio of the vertical and lateral etching rate is approximately 3:5. To protect the silicon underneath the circuit region from being etched away during the

structure release, the CMOS circuitry must be placed far away from the microstructures, especially when a large separation between the microstructures and substrate is needed. As a result, significant chip area is wasted due to the protection margin around the MEMS structures. Since the silicon underneath the mechanical anchors of the MEMS structures is also etched away, the suspension of the mechanical structures is softened, which results in a lower mechanical performance and less robustness of the device [10].

2.2. DRIE post-CMOS MEMS technology

To reduce the disadvantages of the above thin-film post-CMOS MEMS process, DRIE post-CMOS MEMS technology is developed to incorporate bulk single crystal silicon (SCS) into the MEMS structures that are formed by CMOS thin films. Due to the improvement in DRIE technology, high aspect ratio CMOS MEMS structures have been exhibited as shown in Fig. 9. The achievement of maximum aspect-ratio in DRIE system is an important factor in the MEMS structure design [5]. It decides the dimensional limit of the structures fabricated using that DRIE system. Once a lateral feature to be etched is fixed, the maximum thickness is uniquely defined.

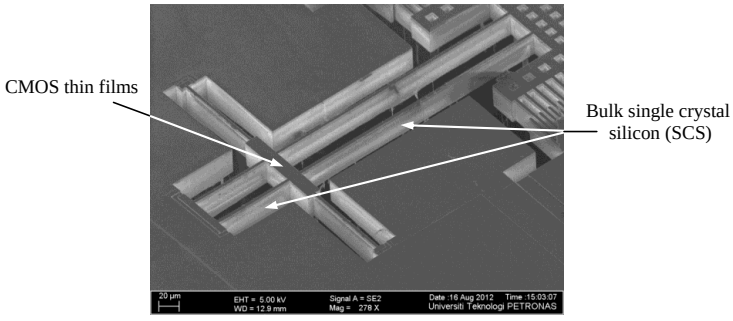

Figure 9. FESEM image showing the incorporation of bulk SCS to the CMOS thin films.

2.2.1. Process flow

The DRIE post-CMOS MEMS technology branches from the thin film technology described in the previous section. DRIE CMOS-MEMS provides an approach to implement thick and flat MEMS structures with improved mechanical performance and device strength due to advantage of both flexible wiring with multiple metal layers in CMOS technology and the capability of high aspect ratio etching. Fig.10 shows the process flow of the DRIE post-CMOS MEMS technology.

To define the MEMS structure thickness (thin film plus substrate), the process starts with backside silicon DRIE etching by the selective application of photoresist at the back-side as shown in Fig.10 (a). The maximum thickness of this structure is limited by the smallest etching pattern on the front side of the MEMS structure and the maximum etch aspect-ratio. Next, to

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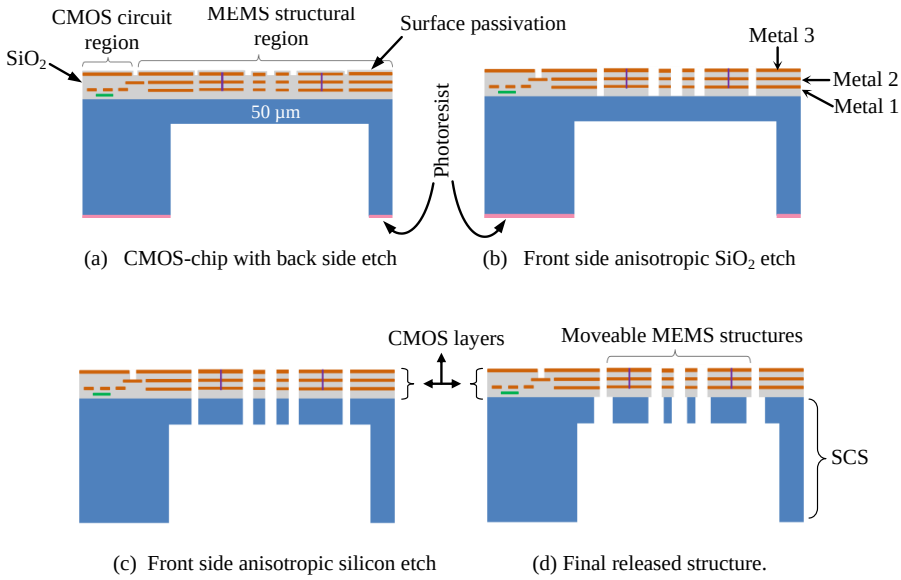

Figure 10. The process-flow for DRIE CMOS micromachining

define the MEMS structures, an anisotropic SiO_2 etch is performed on the front side of the chip as shown in Fig. 10 (b) similar to the thin film process. In the following step, the structure is released by etching through the remaining SCS substrate. This step differs from the thin film process in that an anisotropic DRIE, instead of isotropic Si etch, is performed to release the structure as shown in Fig.10 (c). Flat and large MEMS structures can be obtained by incorporating SCS underneath the CMOS interconnect layers because the residual stresses in the SiO_2/Al thin-films are mitigated by the thick SCS, showing very little out-of-plane curling as shown in Fig. 11 where it can be seen that the sense fingers are perfectly flat and aligned.

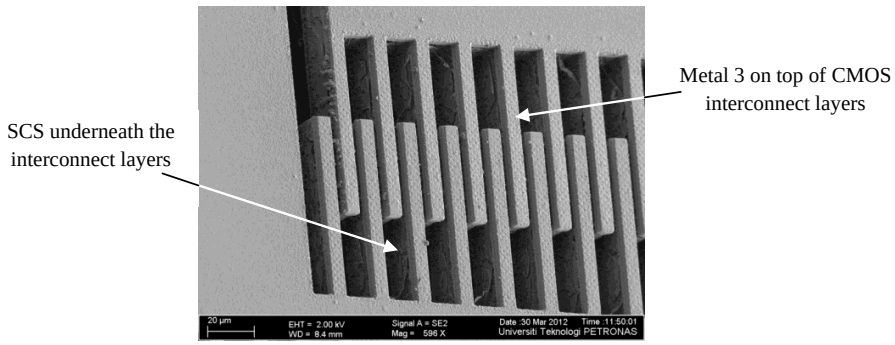

Figure 11. FESEM image showing comb fingers with thick SCS underneath

In some MEMS structures isotropic silicon etch can be added to create nice mechanical structures which only consist of CMOS thin films. A resonant magnetic field sensor fabricated under University Technology PETRONAS (UTP) MEMS Research group incorporates both CMOS thin-film layers for the beams and silicon substrate along with CMOS thin films in the side torsional coils as shown in Fig. 12.

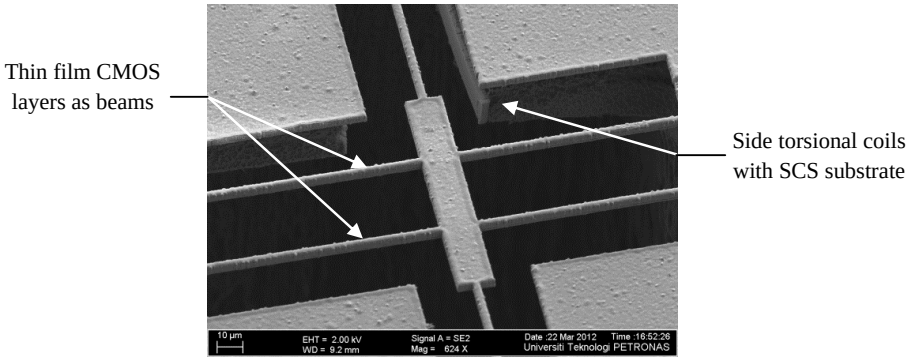

Figure 12. FESEM image of CMOS thin layers and incorporation of SCS with thin layers as MEMS structures

Double side alignment is required in the backside DRIE step to define the thickness of the MEMS structures. It is observed that normally the remaining silicon for bulk MEMS structures is on the order of tens of microns and by the substrate thinning there is no apparent circuit performance degradation. Therefore, there is no hard and fast constraints for alignment in the backside etch. A reliable sensing and actuation is achieved with the flat MEMS microstructures enabled by the DRIE CMOS MEMS technology. A resonant magnetic field sensor with piezoresistive sensing is fabricated using this technology [11]. The technology is very suitable for the fabrication of, in particular, thermally actuated micromirrors where bimorphs are used to elevate the mirror plate. Numerous resonant chemical sensors, electrothermal micromirrors and accelerometers have been fabricated using this technology [12].

2.2.2. Design rules for MEMS devices

For CMOS circuit designs, there are different ways to break up a layout into basic elements. Designers usually divide and analyze a circuit by the function of individual components, devices and interconnect. The devices may be active (e.g. transistors, diodes) or passive devices (e.g. resistors, capacitors and inductors). The interconnects include in-plane wires, pads and vias which connect multiple metal layers. The critical information on the geometric patterns includes the size of each feature, the spacing between features and the overlap of features. These geometric data, required in the design, leads to evolutions of processes and ensures successful fabrication of microelectronic circuitry. In order to fulfill the requirements of successful MEMS device designs, processing information, which quantitatively describes the capabilities and limitations of the process under predetermined processing conditions and

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parameter settings, is necessary and crucial. This information is abstracted as MEMS design rules and is verified in the design environment as illustrated in Fig. 13.

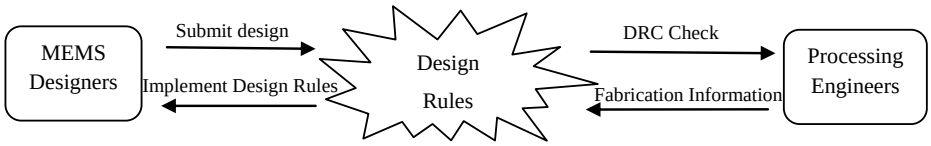

Figure 13. Design rules function between MEMS designers and MEMS fabrication engineers.

This section explains how to construct concise and conclusive design rules. We used MIMOS Berhad Malaysia standard 0.35 μm CMOS design rules for the fabrication of CMOS MEMS devices and only the design rules for mechanical structures are discussed in this section. These MEMS design rules add further constraints to layouts. Similar to CMOS design rules, a complex micromechanical layout is fragmented into small pieces, and MEMS design rules contain only fundamental geometries directly related to the post CMOS micromachining process. A set of geometric constraints and design rules are then based on the final process.

Design rules are expressed in the design-rule file used in layout tools such as Cadence Virtuoso, Magicor, Mentor Graphic, layout tool etc. After all processing completion, a post-CMOS micromachined chip can be partitioned into a released area (containing free standing parts and free moving parts) and a non-released area (anchored parts) according to the mechanical behavior. The objective of post CMOS processing is the final result of releasing microstructures and maintaining critical dimensions. There are practical difficulties in monitoring each intermediate process stages. Therefore characterization of the process to extract design rules is performed at the end of the entire process flow. An overview of a typical post CMOS MEMS magnetic sensor is shown in Fig. 14.

The anchored part is the area outside of the red dash-line box on FESEM, whereas the released part is the area inside the red border. The close-up FESEM view of circled portion is shown in Fig. 14 (b). Sufficient paths for the gas flow are required in order to allow the reactive radicals in the plasma to undercut MEMS structures. These paths can surround mechanical structures, so that the undercut can happen from the periphery of the structures. The gas flow can also pass through structures via etch release holes. Fig. 14 illustrates various situations for reactive species undercut: from one side of the structures toward the anchor region, from both sides of beam structures, or outward through etch release holes on plates.

Theoretically, any shape of the feature which opens a gas flow path from the top of the chip to the substrate is suitable for the purpose of undercut. However, currently in CMOS foundries, Manhattan layout is preferred, or at least convenient. The majority of CMOS foundries only accept patterns with edges which are parallel, perpendicular or 45° with respect to the horizontal/vertical alignment lines. Non-Manhattan features require more and smaller rectangular patterns to approximate the geometry, and therefore, require a larger data base and longer exposure time, which leads to higher cost. Today, raster-scanning mask-making

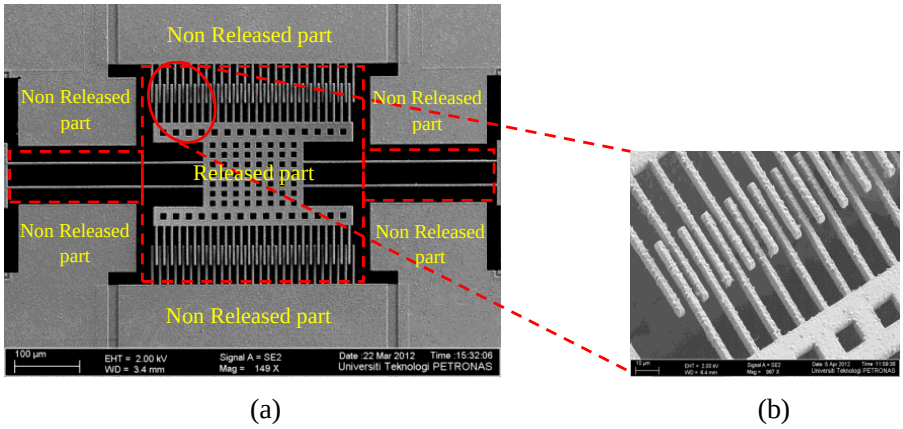

Figure 14. Partitioning of a MEMS sensor for design-rule checking

technologies such as e-beam or laser systems can overcome the difficulties mentioned above but non-Manhattan shapes approximated by a smaller raster-beam size still require more time in fabrication [13]. Following the practice of CMOS fabrication, this work only explores rectangular design rules. The major purpose of this section is to ensure the release of moving/free-standing parts and to guarantee the integration of anchor parts. Other process related rules are not included. According to situations described in Fig. 14, there have been three features encountered in the MEMS structure layout for the purpose of undercut: large openings, gaps and holes. To control the etch rates in these opening, dummy structures are used as shown in Fig.15 (a) while figure 15 (b) shows the fully released structure.

Test structures are used to extract design rules. A large opening undercut rule specifies the maximum undercut that can be achieved by the process. Any microstructure wider than this value will not be released. This rule also specifies the minimum size requirement of the anchor layout, and the skirt for bonding pads. Bonding pads are usually on the periphery of the chip for easy access during bonding and no crossing of bonding wires on the top of the chip. Therefore, at least one side of bonding pads faces large opening and is lateral undercut during the release. The sites that experience forces during wire bonding should avoid these undercut regions and bonding pads need extra area to compensate this lateral undercut. Moreover, this large opening rules specifies the minimum space required from the edge of the etch pit to preserve Si area containing circuitry during micromachining. One way to obtain this data is to use FESEM to measure the undercut from the periphery of the chip. Another way is to use an optical microscope to check which size of square pattern has been released as illustrated in Fig. 16 (a).

The undercut value is half the size of square width. A gap undercut rule is required for releasing MEMS structures such as a comb finger or a spring. The test structure for this rule is a set of cantilevers with the undercut mainly determined from the sides of the beams. To follow the situation in real layout, such as comb fingers, multiple cantilever beams with equal space

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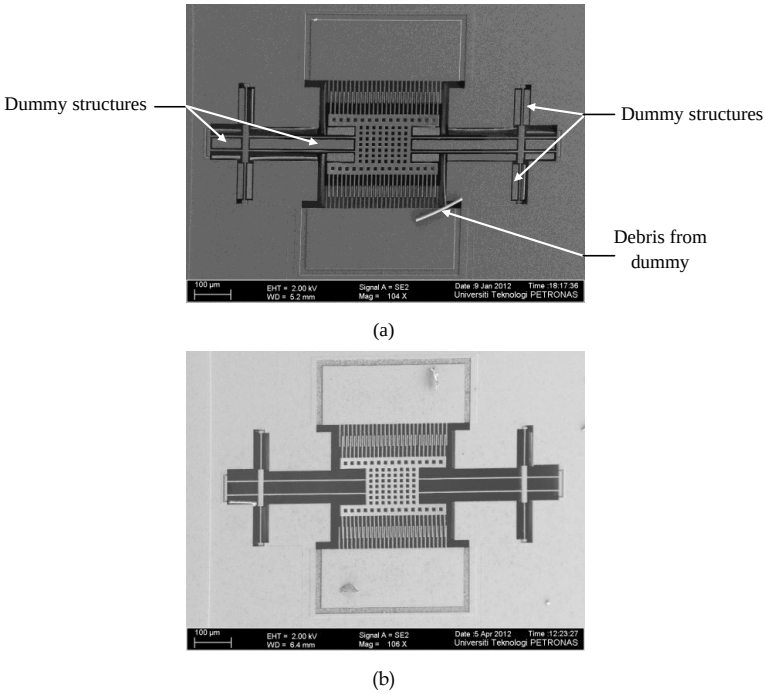
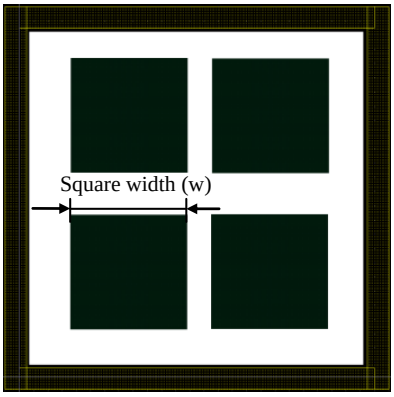


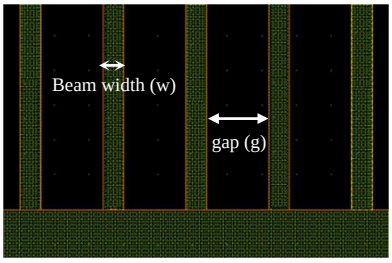
Figure 15. FESEM images of (a) unreleased device showing dummy structure at a large etch holes and (b) fully released structure.

between them are used as shown in Fig. 16 (b). The beam width (w) represents the width of the structure to be released. The gap (g) represents the separation between the structures. The beam should be long enough that the undercut from the tip of the cantilever doesn't dominate the etch. Since the residual stress induces out-of-plane curling upon release, the release can be easily detected by an interferometric measurement. A hole undercut rule is required to release plate structures. The test structure for this design rule is a set of plates with release holes. These plates are anchored by four thin beams as shown in Fig. 16 (c). Such plates should be large enough to ensure that the release of the plate is determined by the etch release holes and not from the periphery of the plate.

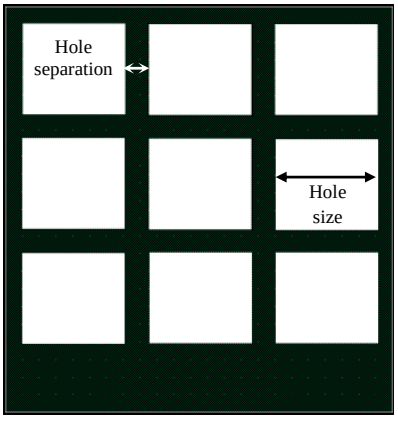
Similar to the cantilever test structures, the curling after the release of plates can be detected by the interferometric measurement. Extra processing time requires layouts to be modified such that the circuitry is far away from the edge of the mask, all the anchors are wide enough, and all bond pads have enough margins for bonding and probing. The spacing between the squares and the spacing from a square to the surrounding anchor mask area are the size of the square. This is to ensure that squares are uniformly etched from all directions. For each group of cantilever test structures, as in Fig. 16 (b), the widths of all cantilever beams are the same value. The spacing between beams and from tips of cantilever beams to anchor mask areas are the same value [14].



(a) The square structure illustrating the large opening undercut rule



(b) The cantilever structure illustrating the gap undercut rule



(c) The plate structure illustrating the hole undercut rule

Figure 16. Layout of three test structures used for extracting MEMS design rules for post-CMOS micromachining.

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3. DRIE based CMOS-MEMS devices

In this section, two devices fabricated using CMOS-MEMS bulk micromachining technology are described. The devices are a resonant MEMS magnetic field sensor and a resonant MEMS chemical sensor.

3.1. Resonant MEMS magnetic field sensor

The post-CMOS process steps of the resonant magnetic field sensor using DRIE were designed to successfully release the sensor structure. The first step in the post-CMOS process was at wafer level with the selective application of photoresist at the back-side of the 8" inch silicon wafer to etch from the back-side to produce a substrate thickness of approximately 50 μm as shown in Fig.17. DRIE was performed using SS110A Tegal plasma etcher to anisotropically etch the silicon substrate to the desired thickness.

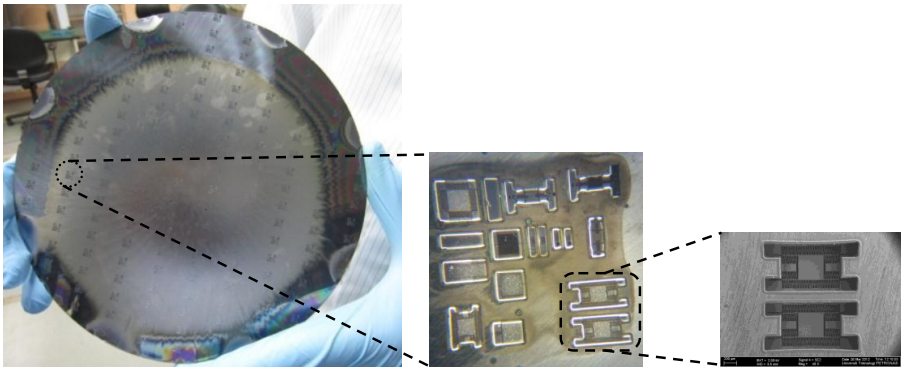

Figure 17. a) Optical image of back side Si etching at wafer level, (b) Backside optical image of a chip and (c) FESEM of backside of a sensor.

Optical microscope was used to estimate the thickness of the Si substrate during the etching process. Fig.17 (c) shows the back-side view of one of the sensors that has been successfully etched to approximately 284 μm depth leaving a about 50 μm thickness under the CMOS layers. From the back-side etching of the bulk silicon, the silicon etching rate was found to be ~3.66 μm/min. The second step was dicing the wafer as shown in Fig. 18 (a). Dicing of the wafer has to be done before the front side RIE of SiO_2 and DRIE of silicon is implemented. This sequence was followed in order to prevent the breakage of the released structures.

The third process was SiO_2 RIE on the diced chip shown in Fig. 18 (b), which was performed from the front-side of the chip using Tegal plasma etcher. Front side RIE process opened the pattern of the resonant magnetic sensor by removing the SiO_2 layer and thus exposing the silicon underneath while the MEMS sensor pattern was maintained by metal 3 acting as a mask

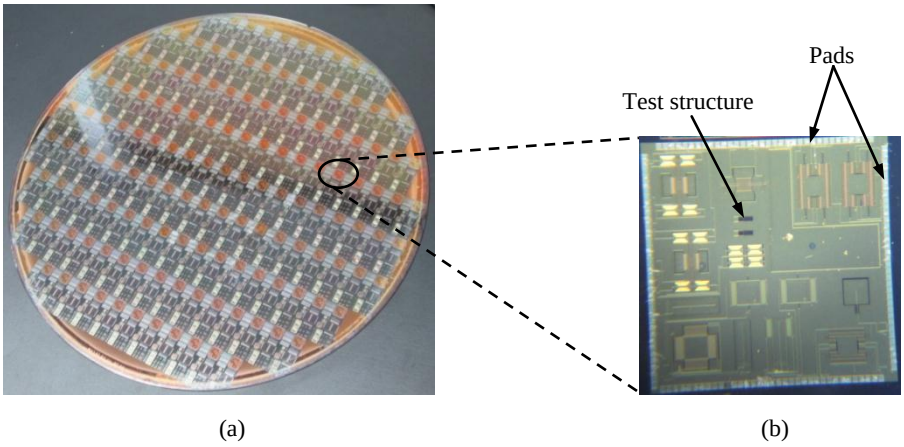

Figure 18. a) Optical image of the diced wafer and (b) optical image of front side of a 5 mm × 5 mm chip.

for the pattern. The process at chip level started by flipping over the chips such that the thin film was now on the front side. The chips were then attached to the 8" platinum coated carrier wafer using kapton tape as illustrated in Fig.19. After 13 minutes of etching, a gray colour (silicon colour) appeared in the trenches that indicated the completion of SiO_2 etching. The test structures to the right of the sensor beam were used to estimate SiO_2 etching rate and to avoid over-etch of the SiO_2 material as shown in Fig.18 (b). The total SiO_2 etching depth was approximately 5 μm.

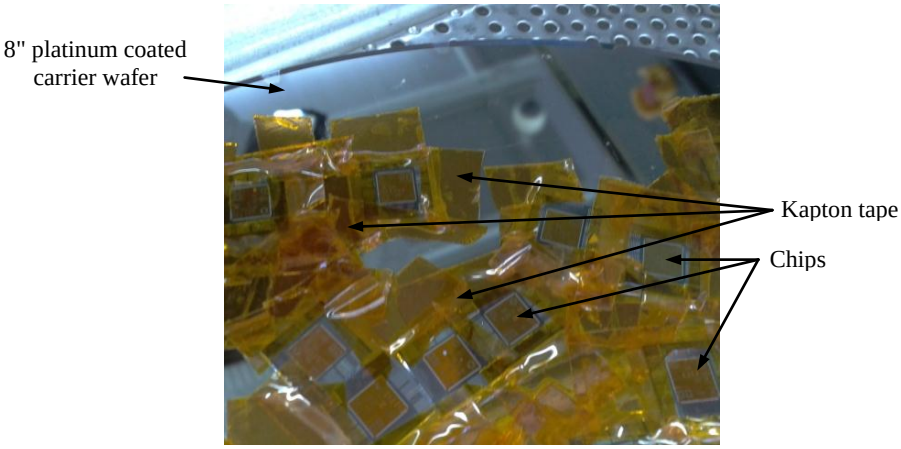

Figure 19. Sample preparation for front side etching

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Next, front-side bulk silicon DRIE process step was performed using the etching rate of 3.66 μm/min obtained from previous backside DRIE etching of silicon. The thickness of the central shuttle and long beams was approximately 50 μm, which was observed under optical microscope during back-side etching. Therefore the test structures on the chip were used as reference. Fig.20 shows FESEM micrograph of the fabricated sensor with inset showing a close-up of the comb fingers and part of dummy structure close to the beams that has fallen out while others still remain intact on the substrate [10]. Additional 3 more minutes were required to fully etch-through. This happened when all the dummy structures dropped and indicated that the etched-through process was completed.

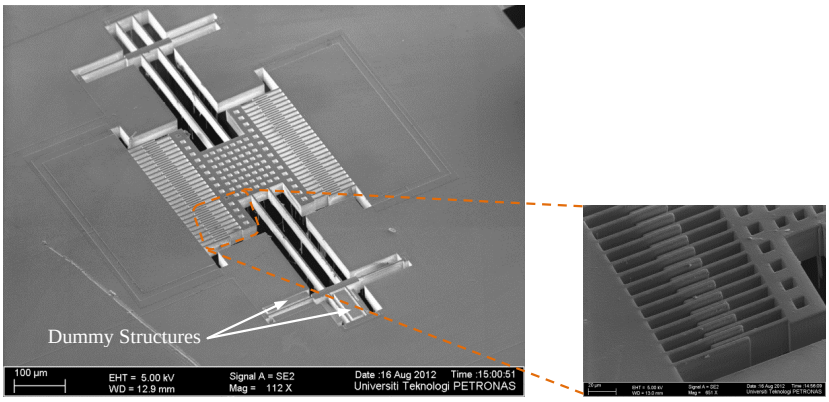

Figure 20. FESEM image of the fabricated CMOS-MEMS resonant magnetic field sensor with inset showing shuttle and stator fingers.

3.2. Resonant MEMS chemical sensor

In resonant MEMS chemical sensors, known as gravimetric sensors, the principle of detection of the gaseous species is based on the change in resonant frequency of the microresonator membrane or plate. This frequency change results from a change in the mass of the microresonator due to absorption/adsorption of an analyte molecule onto the surface of the active material deposited on it. Fig. 21 shows 2-D schematic diagram of the chemical microsensor device.

The post-CMOS micromachining process steps of the resonant MEMS chemical sensor were similar to the process steps of the resonant MEMS magnetic field sensor. The process started with the selective application of photoresist at the back-side of the die around the sensor followed by sample placement on the platinum coated carrier wafer. The second step of the process was to perform back-side silicon DRIE to achieve proof mass thickness of approximately 40 μm. The same plasma silicon etcher was used to anisotropically etch the silicon substrate to the desired thickness. Fig. 22 shows the FESEM image of the successfully released MEMS chemical sensor with the inset showing a close-up view of the perfectly flat sensing comb fingers with the SCS underneath [15].

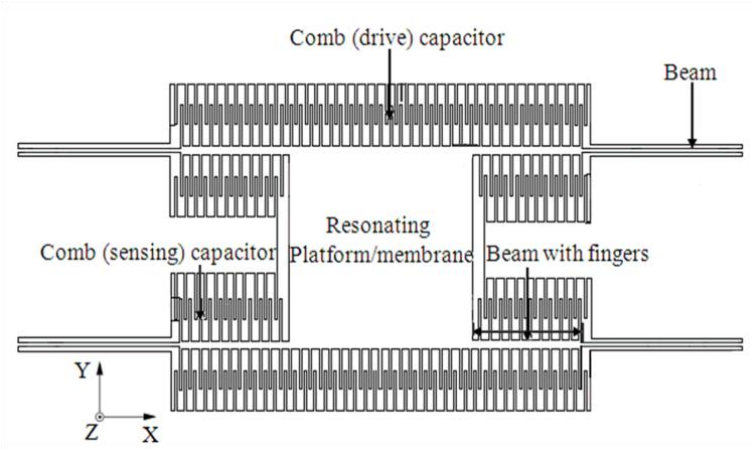

Figure 21. D Schematic of the resonant MEMS chemical sensor

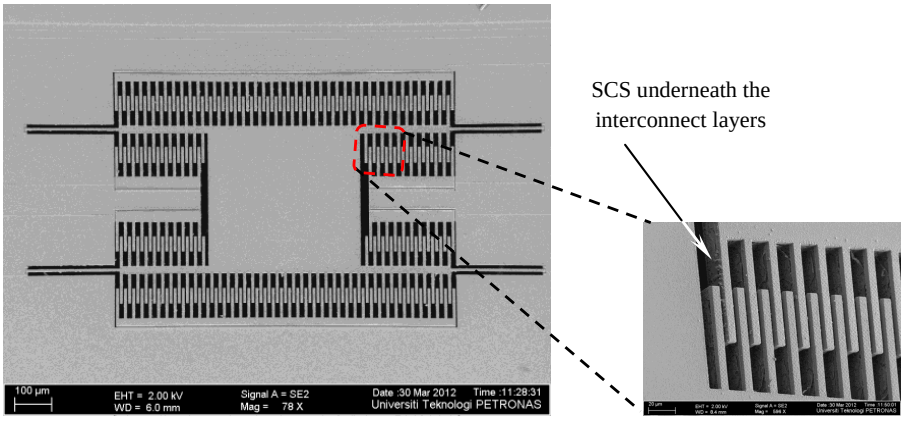

Figure 22. FESEM image of fabricated device with inset showing a close-up view of the fingers with the SCS underneath

4. Conclusion

This chapter discussed bulk micromachining technology with particular emphases on DRIE post CMOS MEMS bulk micromachining. The chapter was divided into three sections. In the first section an introduction to bulk micromachining of silicon and isotropic and anisotropic wet and dry etching was given. The second section discussed briefly DRIE post-CMOS micromachining process with particular emphasis on DRIE post-CMOS bulk micromachining process and the third and last section provides a few examples of devices fabricated by our

research group using the DRIE CMOS-MEMS process. These devices were resonant MEMS magnetic field sensor and resonant MEMS chemical sensor. The aim of the chapter was to discuss and analyze practical processes involved in the design of micromechanical devices using 0.35 μm CMOS technology.

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