CMOS Digital Circuits

- Types of Digital Circuits

Combinational

The value of the outputs at any time t depends only on the combination of the values applied at the inputs at time t (the system has no memory)

Sequential

The value of the outputs at any time t depends not only on the values applied at the inputs at time t, but also on the past sequence of inputs that have been applied (the system has memory)

Logic values and noise margins

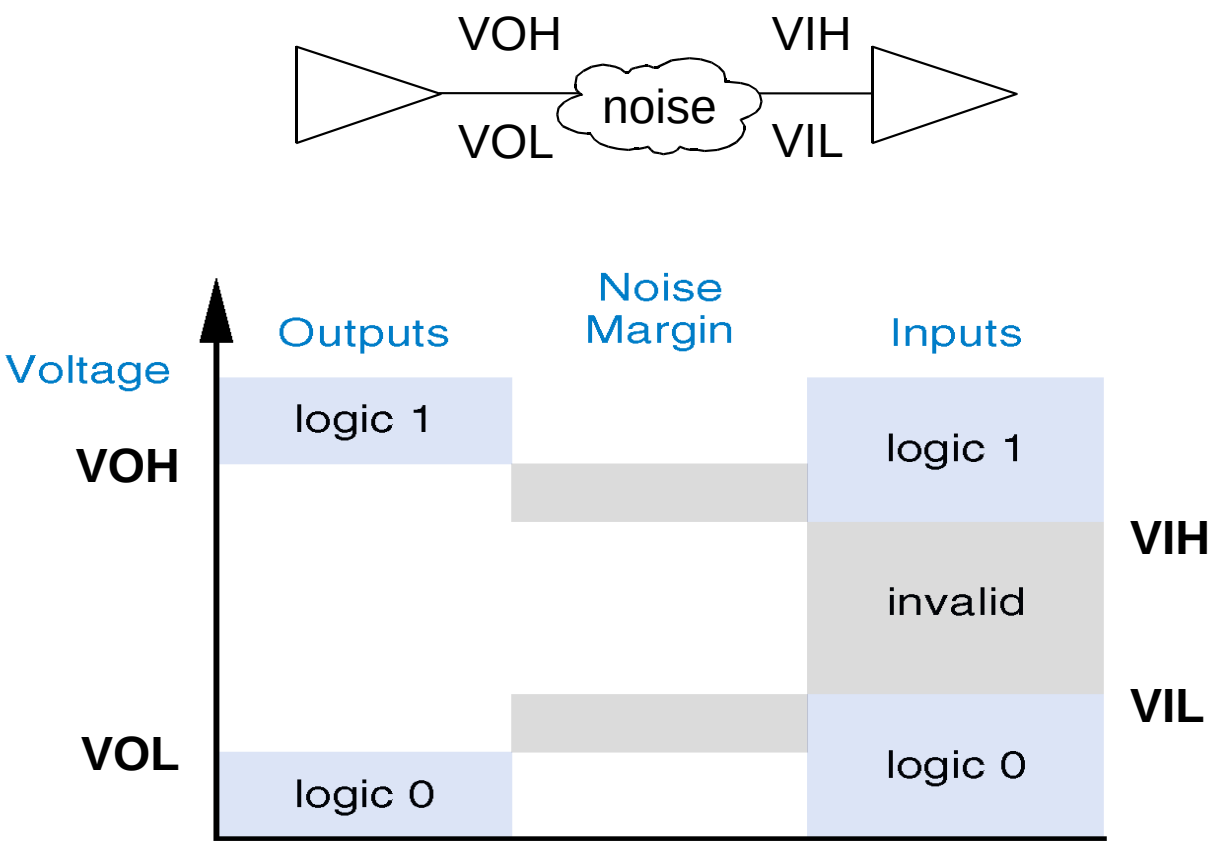


Figure 1-2
Logic values and noise margins.

MOS Transistors

- Four terminals: gate, source, drain, body (= bulk)

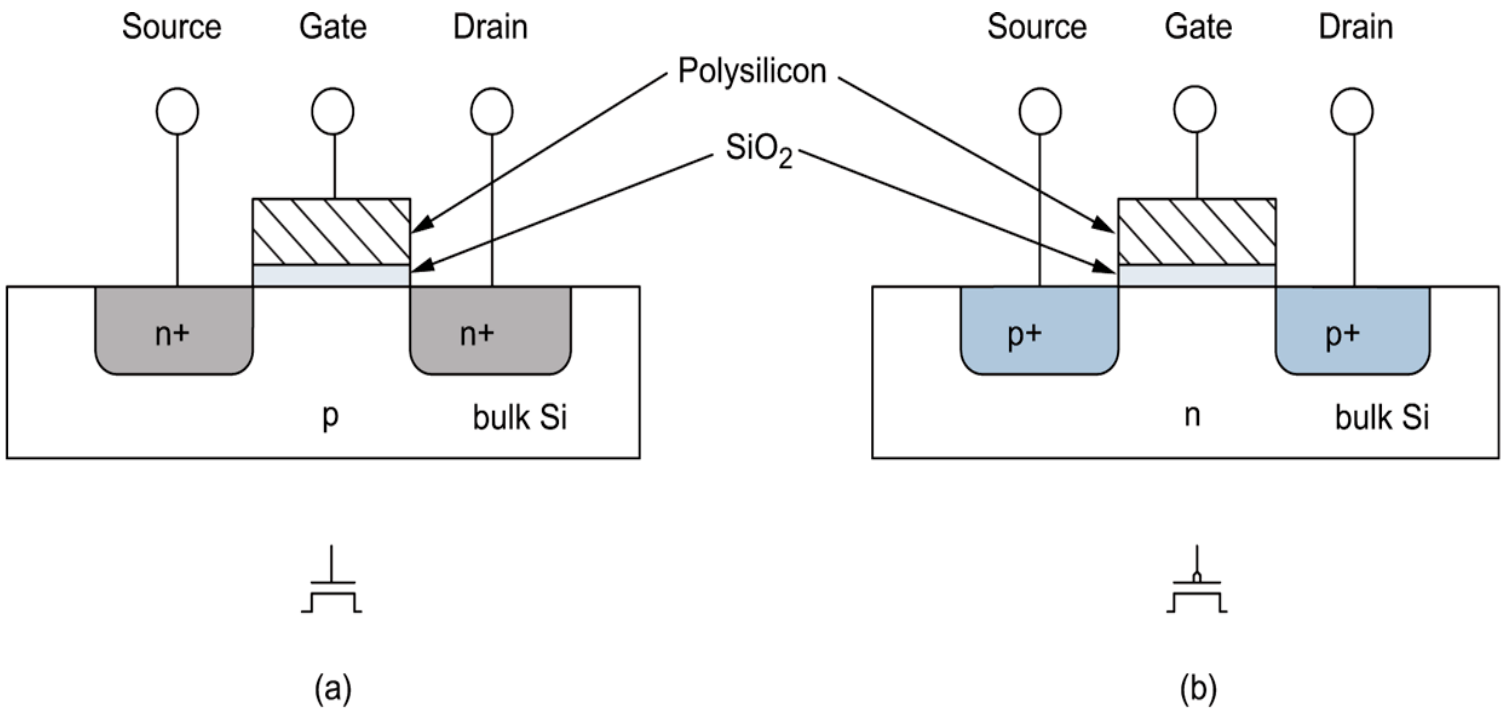


FIG 1.8 nMOS transistor (a) and pMOS transistor (b)

Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a semiconductor (Group IV material)
- Forms crystal lattice with bonds to four neighbors

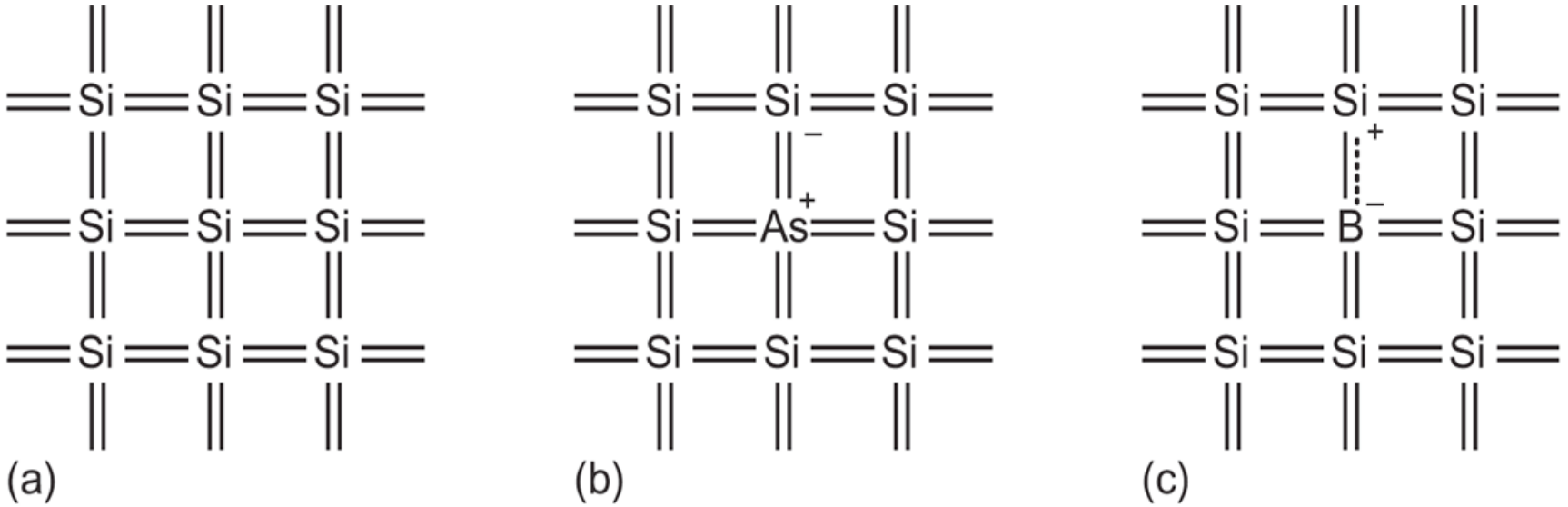
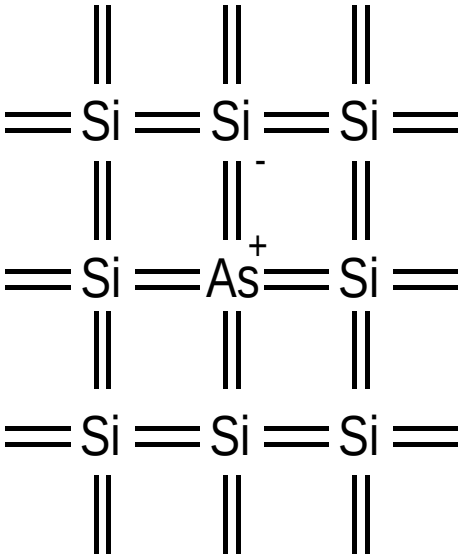
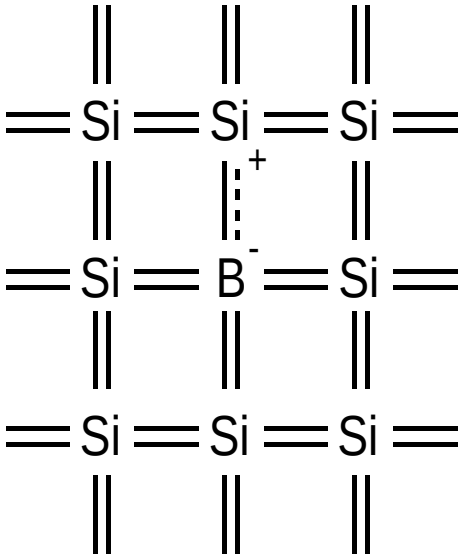


FIG 1.6 Silicon lattice and dopant atoms

Dopant atoms

- Pure silicon has no free carriers and conducts poorly.
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)

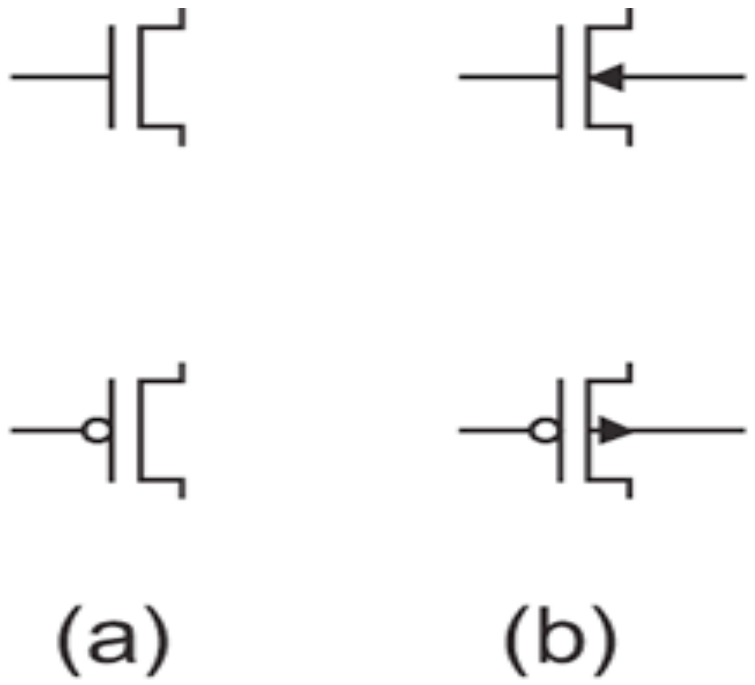




Types of Transistor

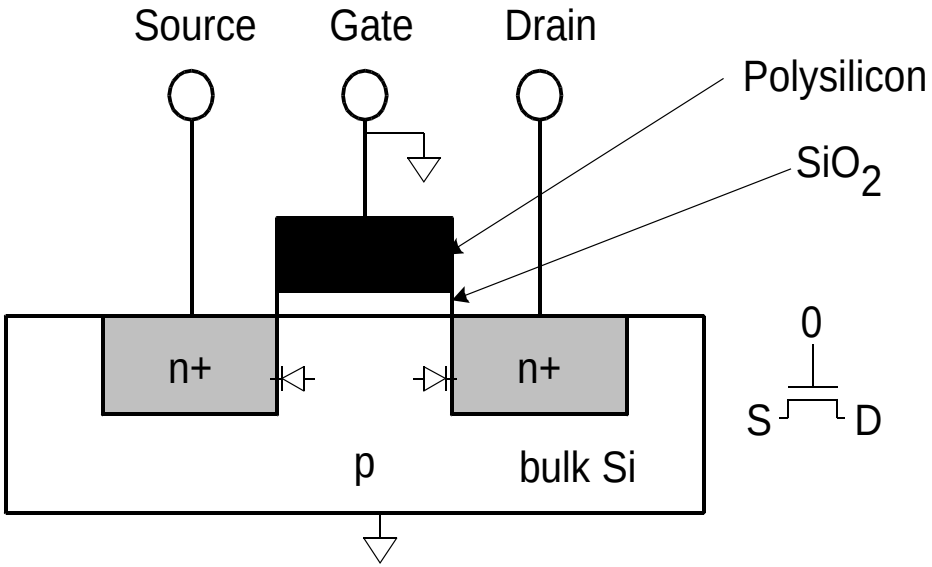
- Bipolar Junction Transistor (BJT)
  - NPN and PNP transistors
  - Small current into very thin base layer controls large current between emitter and collector
  - Base currents limit integration density
- MOS Field Effect Transistor (MOSFET)
  - NMOS and PMOS FETs
  - Voltage applied to insulated gate controls current between source and drain
  - Low power allows very high integration

MOS Transistor symbols



N-MOSFET operation (1)

- Body is commonly tied to ground (0 V)
- When the gate is at a “low” voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



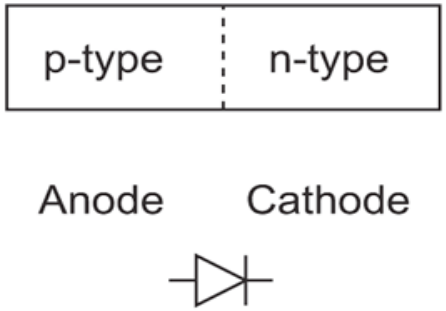
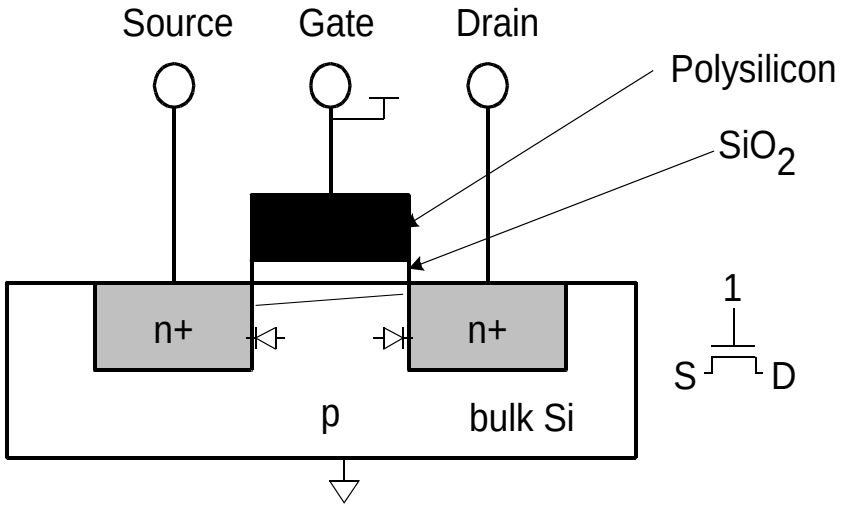


FIG 1.7 p-n junction diode structure and symbol

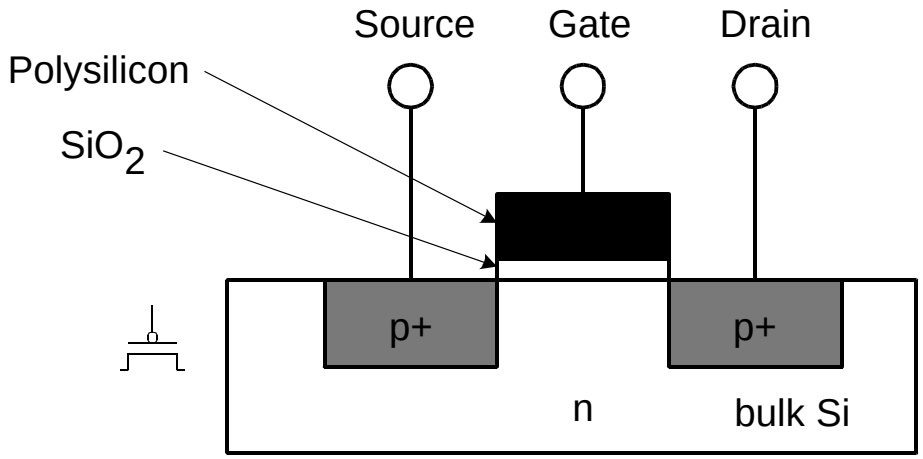
N-MOSFET operation (2)

- When the gate is at a “high” voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - channel under gate gets “inverted” to n-type
  - Now current **can** flow through n-type silicon from source through channel to drain, transistor is ON



P-MOSFET operation

- Similar BUT **doping and voltages are reversed**
- Body tied to “high” voltage (V_{DD})
- Gate “low”: transistor ON
- Gate “high”: transistor OFF
- Bubble indicates inverted behavior



What does high and low voltage really means ?

- Power Supply Voltage:
  - GND = 0 V
  - In 1980's, V_{DD} = 5V
  - V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
  - V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

MOSFETs as SWITCHES

- We can model MOS transistors as controlled switches
- Voltage at gate controls current path from source to drain

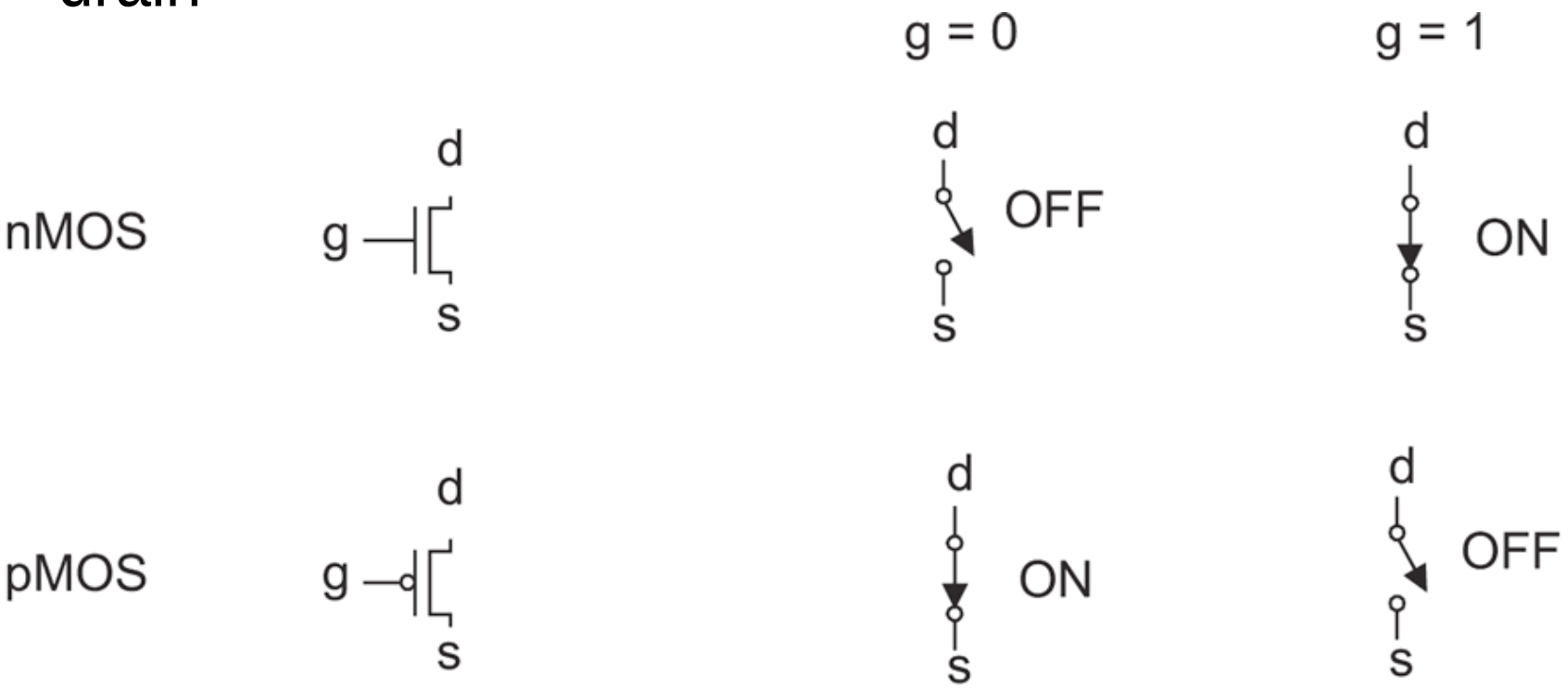
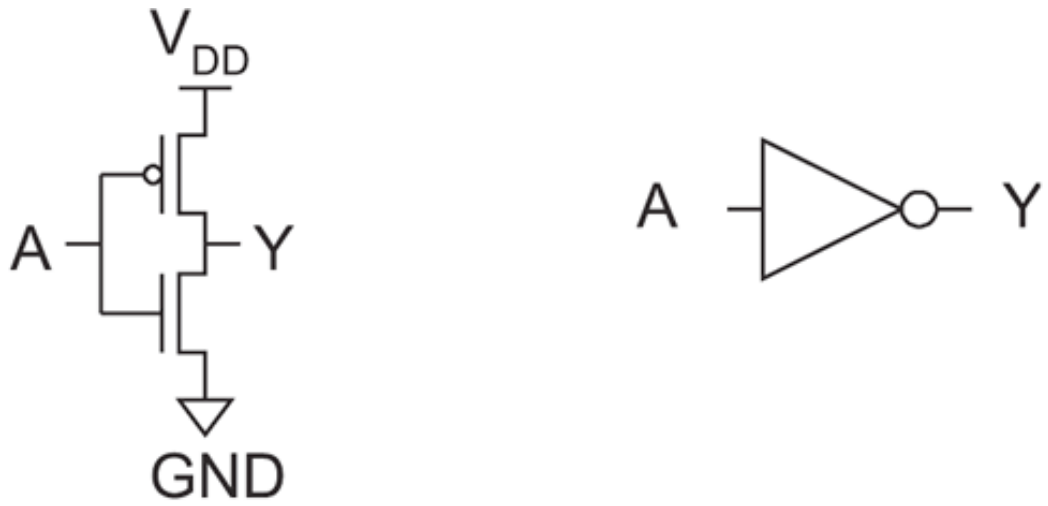


FIG 1.9 Transistor symbols and switch-level models

CMOS Inverter (= NOT gate)

Table 1.1 Inverter truth table

A	Y
0	1
1	0



(a) (b)

FIG 1.10 Inverter schematic (a) and symbol (b) $Y = \overline{A}$

CMOS Technology

- CMOS technology uses both nMOS and pMOS transistors
- The transistors are arranged in a structure formed by two complementary networks
  - Pull-up network is complement of pull-down network
  - Parallel → Series
  - Series → Parallel

CMOS Logic NAND

Table 1.2 NAND gate truth table

A	B	pull-down network	pull-up network	Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

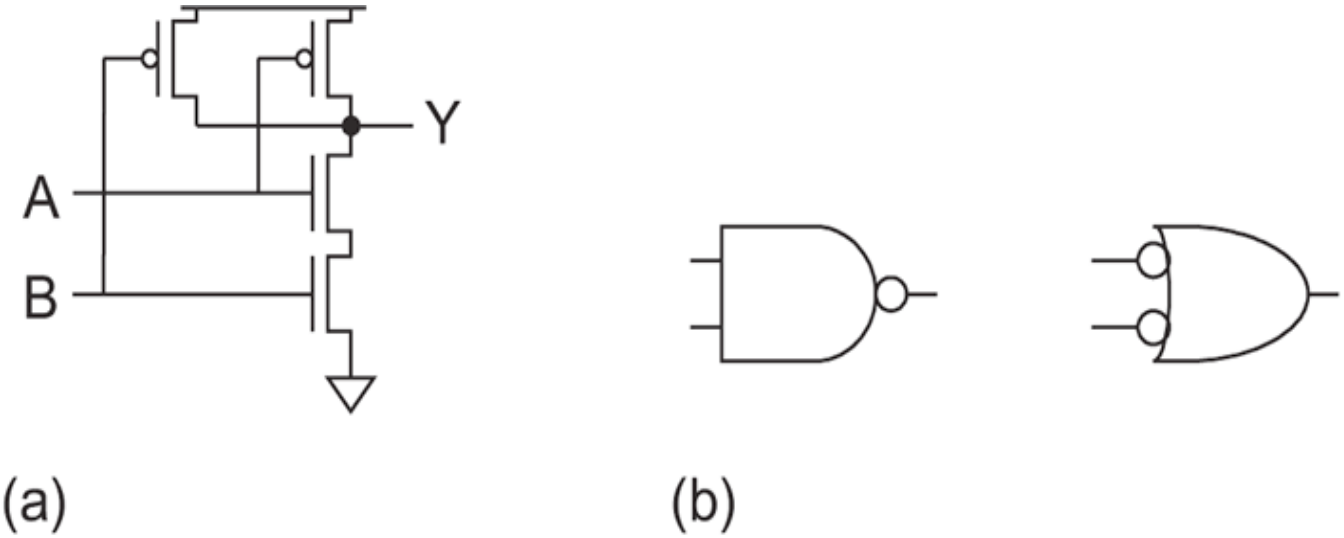


FIG 1.11 2-input NAND gate schematic (a) and symbol (b) $Y = \overline{A \bullet B}$

CMOS Logic NOR

Table 1.4 NOR gate truth table

A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	0

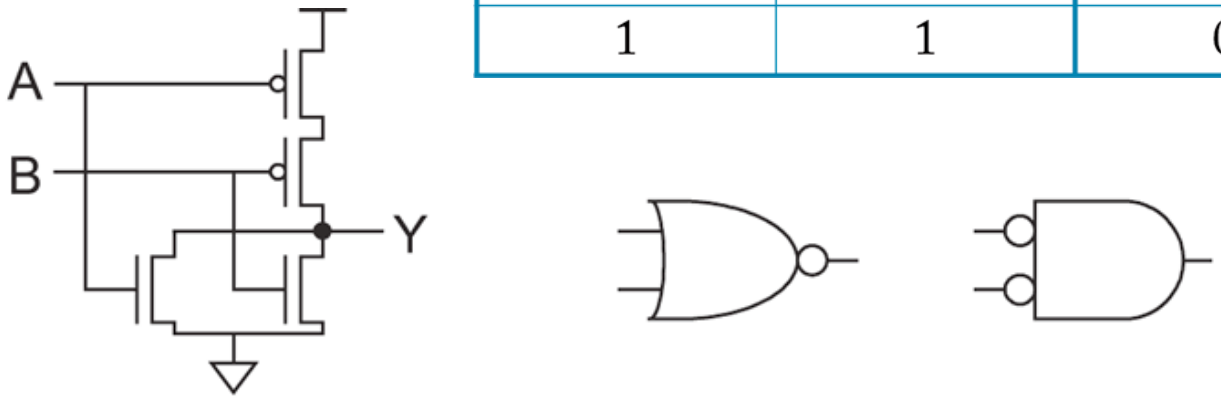
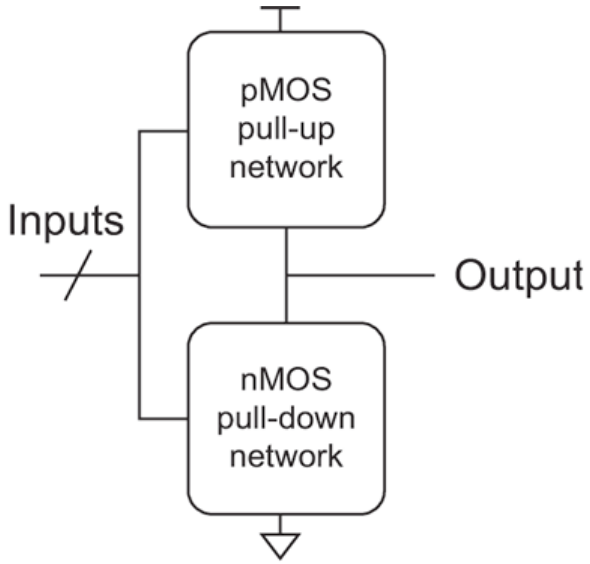


FIG 1.15 2-input NOR gate schematic (a) and symbol (b) $Y = \overline{A + B}$

CMOS logic gates (a.k.a. Static CMOS)



- Pull-up network is complement of pull-down
- Parallel → Series
- Series → Parallel

FIG 1.13 General logic gate using pull-up and pull-down networks

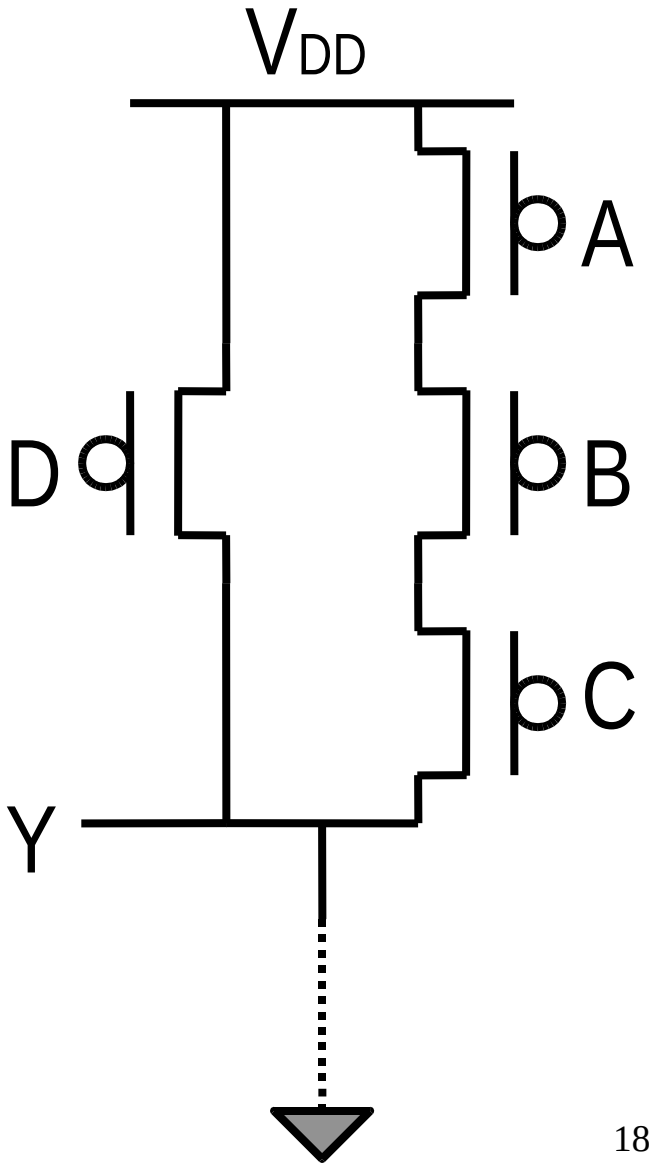
Table 1.3 Output states of CMOS logic gate

	pull-up OFF	pull-up ON
pull-down OFF	Z	1
pull-down ON	0	crowbarred (X)

Compound gates

- Example: $\overline{(A+B+C)*D}$

A	B	C	D	Y
-	-	-	0	1
0	0	0	-	1
1	-	-	1	0
-	1	–	1	0
-	-	1	1	0



Compound gates

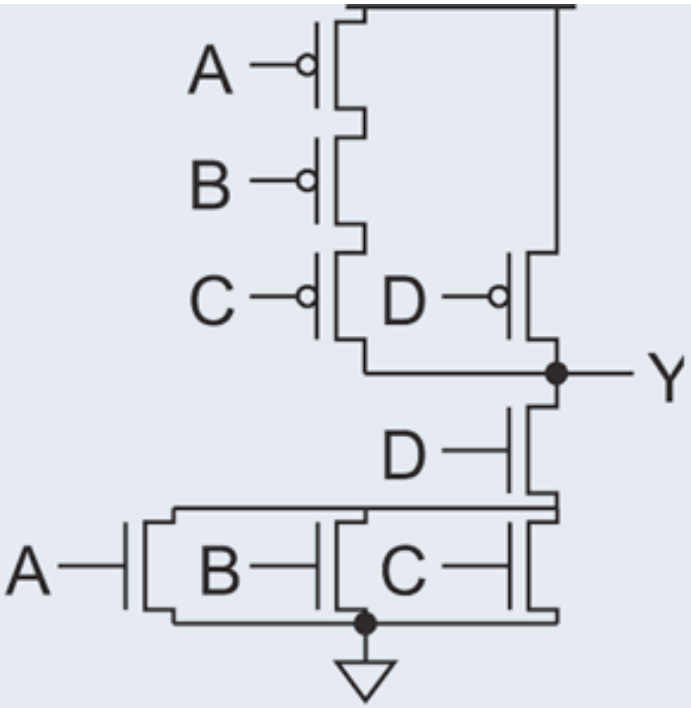


FIG 1.18 CMOS compound gate for function $Y = \overline{(A + B + C) \bullet D}$

How good is the output signal ?

- **Strength** of signal
  - How close the signal approximate ideal voltage source
- V_{DD} and GND rails are the strongest 1 and 0
- nMOS and pMOS are not ideal switches
  - pMOS passes strong 1 , but degraded (weak) 0
  - nMOS passes strong 0. but degraded (weak) 1
- THUS:
  - nMOS are best for the pull-down network
  - pMOS are best for the pull-up network

The Pass Transistor

- Transistors used as switches

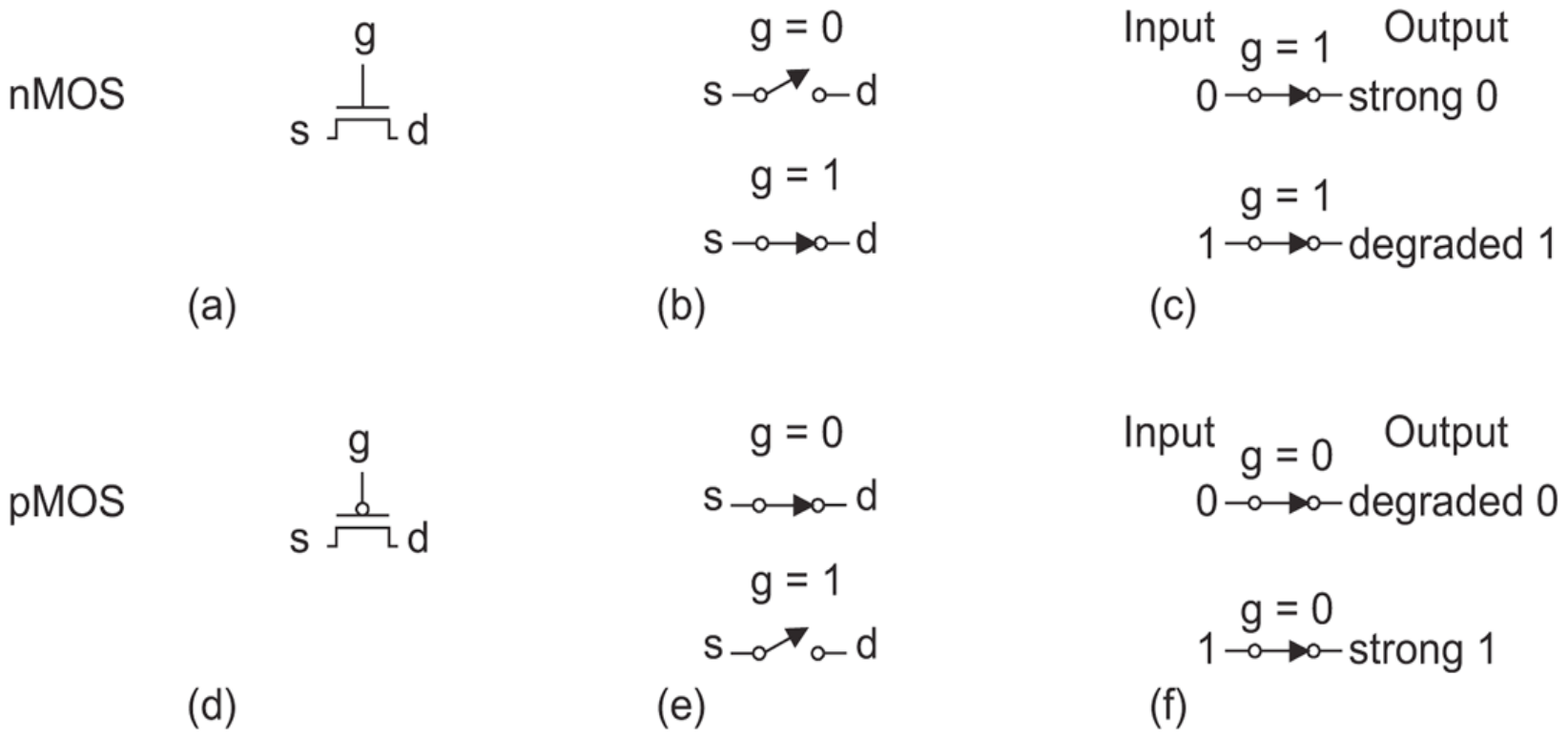


FIG 1.19 Pass transistor strong and degraded outputs

The Transmission Gate

- Pass transistors produce degraded outputs
- Transmission gates pass both 0 and 1 well

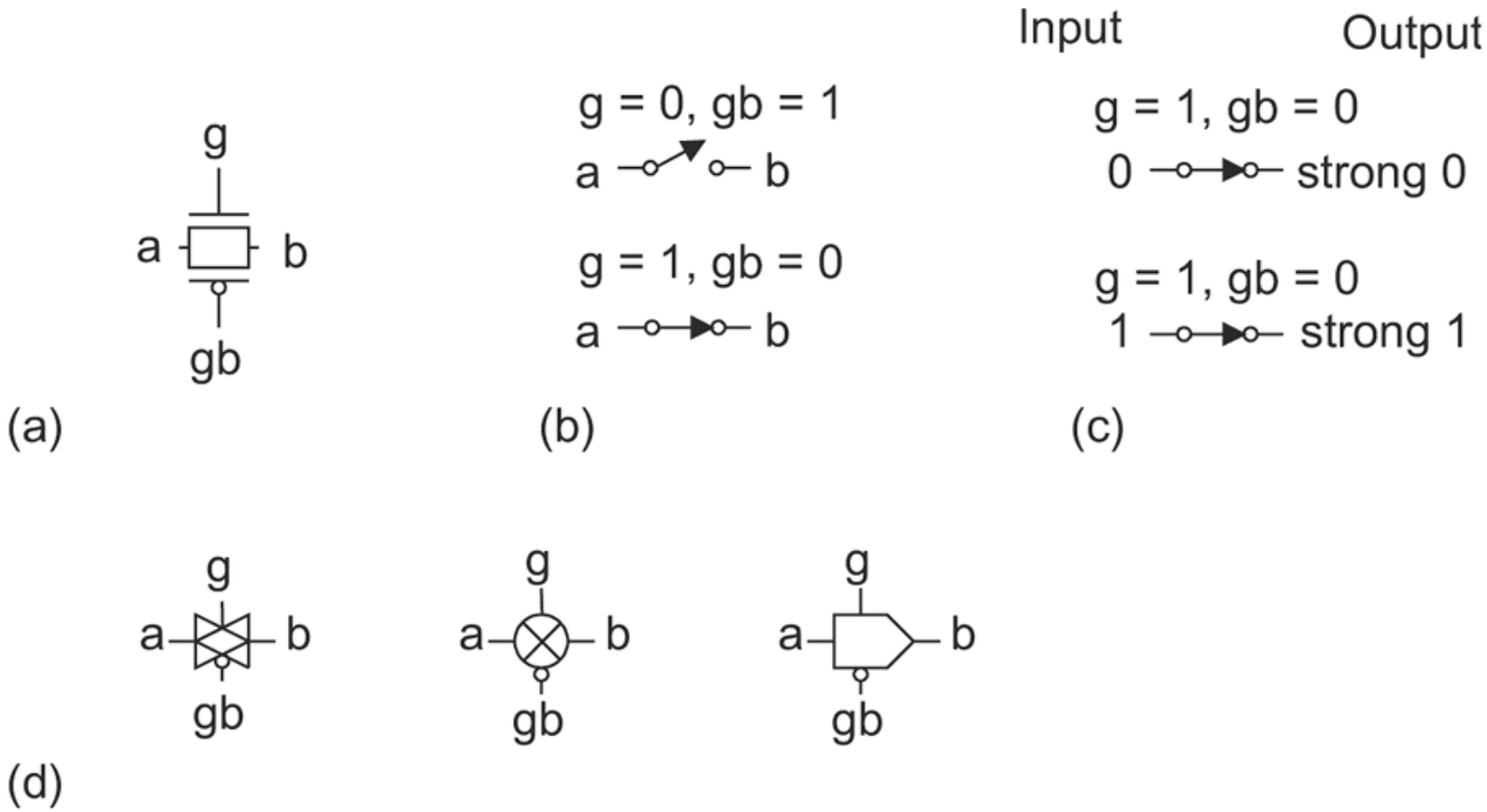


FIG 1.20 Transmission gate

Static CMOS gates are fully restoring

- In static CMOS, the nMOS transistors only need to pass 0's and the pMOS only pass 1's, so the output is always strongly driven and the levels are never degraded

- This is called a fully restoring logic gate

Static CMOS is inherently inverting

- CMOS single stage gates must be inverting
- For building non inverting functions we need multiple stages

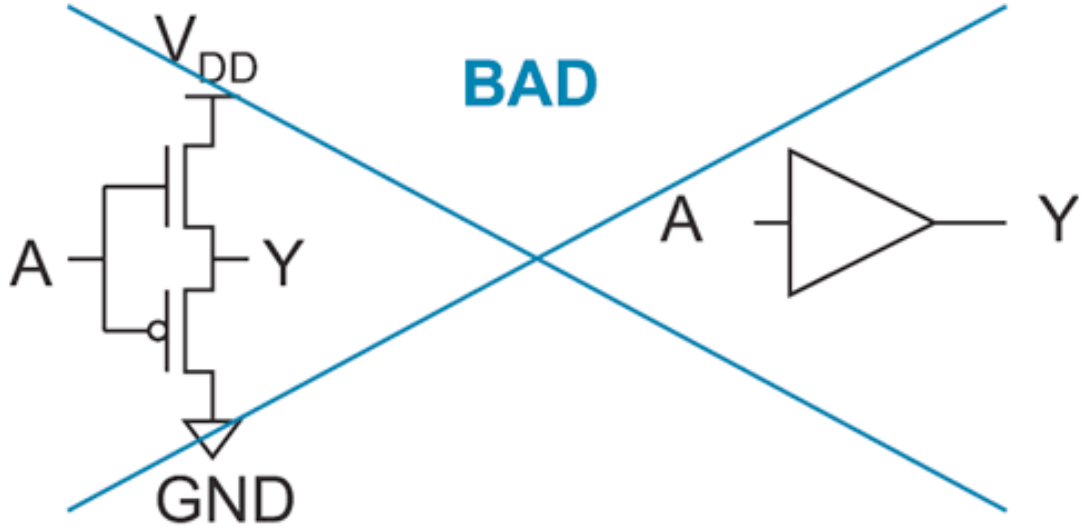


FIG 1.21 Bad noninverting buffer

Tristate Buffer

- A tristate buffer produce Z when not enabled

FIG 1.24 Tristate buffer symbol

A	EN	Y
0	0	Z
0	1	0
1	0	Z
1	1	1

Non restoring tristate

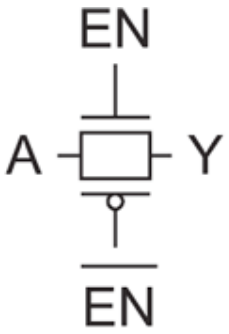


FIG 1.25 Transmission gate

- Transmission gate acts as tristate buffer
  - It takes only 2 transistors
  - **BUT** is nonrestoring
    A is passed to Y as it is
    (thus, Y is not always a strong 0 or 1)

Tristate inverter

- Tristate inverter produces restored output
- For a non inverting tristate add an inverter in front

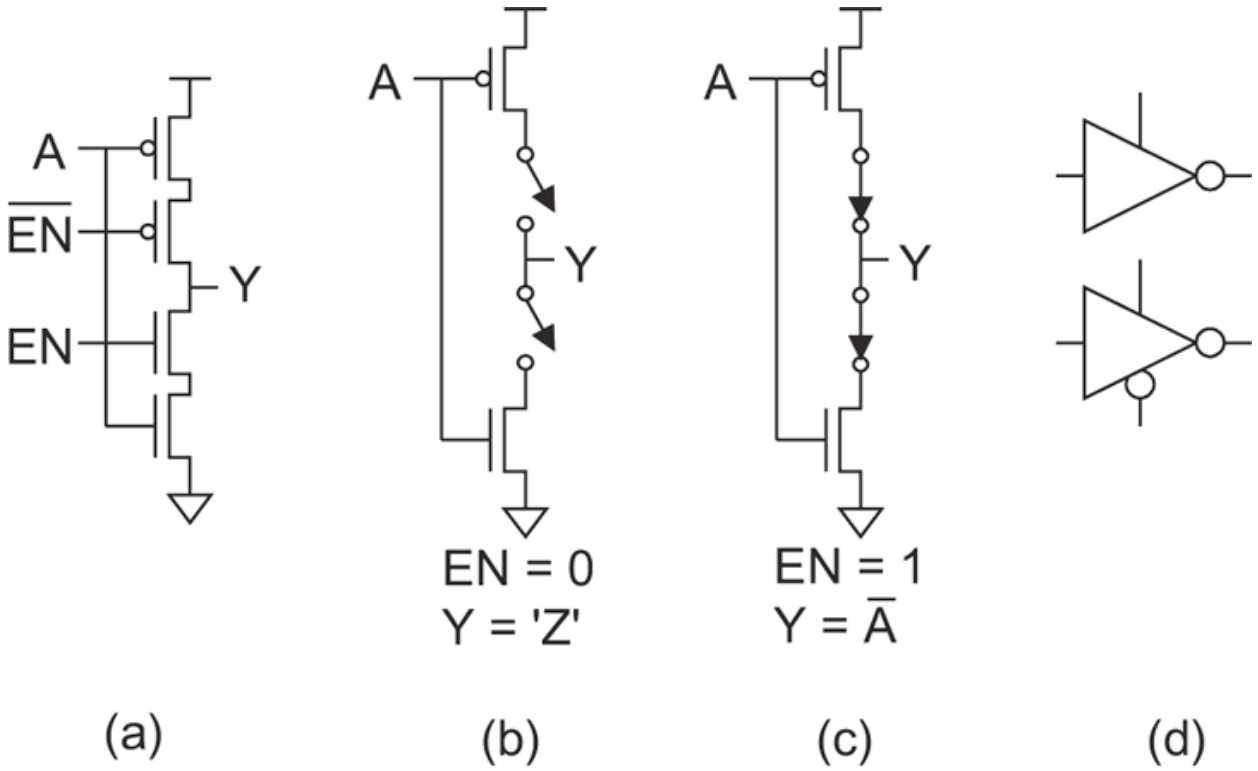
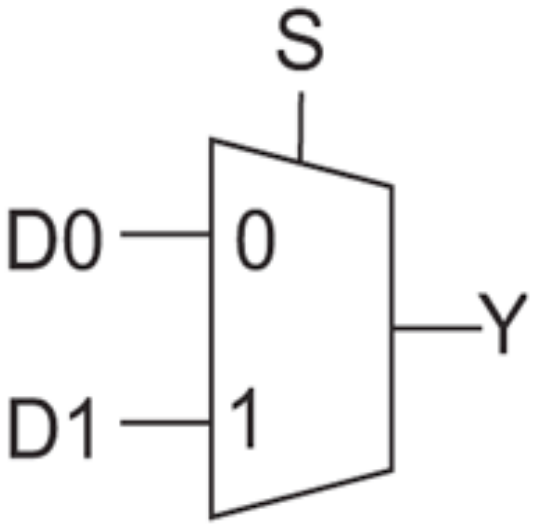


FIG 1.26 Tristate inverter

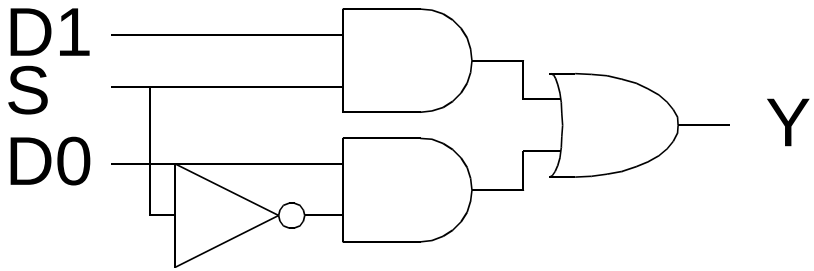
Designing a 2:1 mux

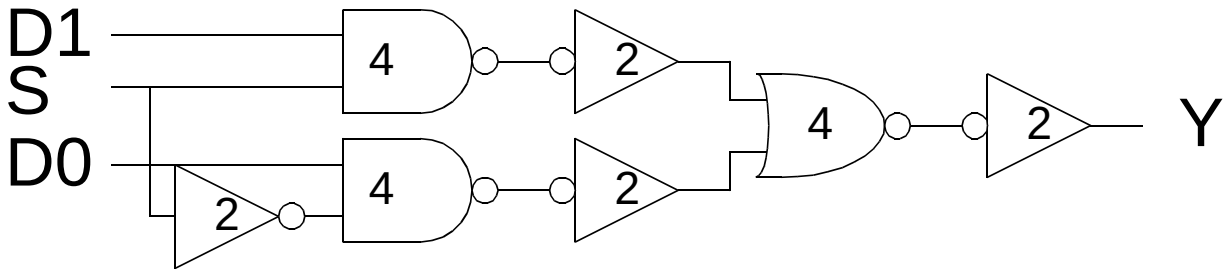


D0	D1	S	Y
0	-	0	0
1	-	0	1
-	0	1	0
-	1	1	1

2:1 mux - gate level approach

$$Y = D0 * \overline{S} + D1 * S$$





- How many transistors are needed ?
  Too Many !!! (20 transistors)

2:1 mux – TG approach

- We need only 4 transistors (6 to be honest)

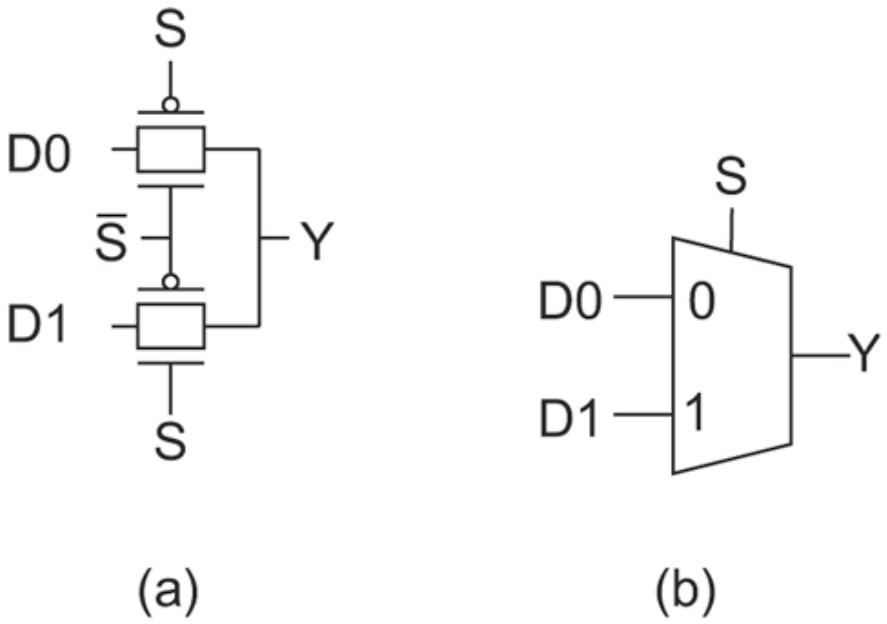
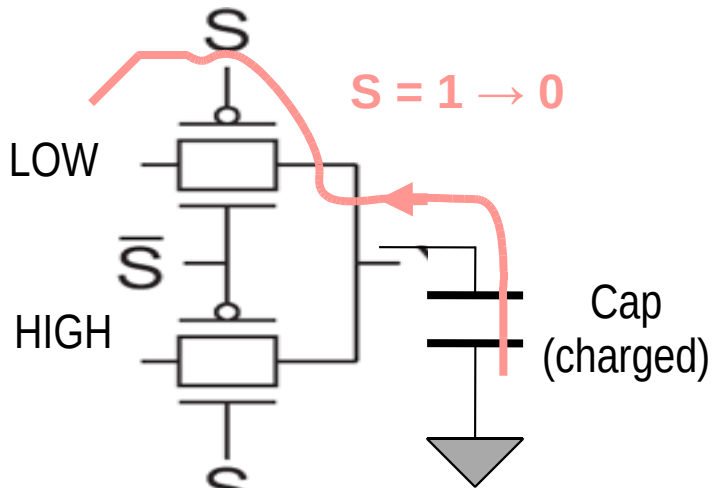


FIG 1.27 Transmission gate multiplexer

BUT it is non restoring and it has another issue called charge sharing



inverting mux

D0	D1	S	Y
0	–	0	1
–	0	1	1
1	–	0	0
–	1	1	0

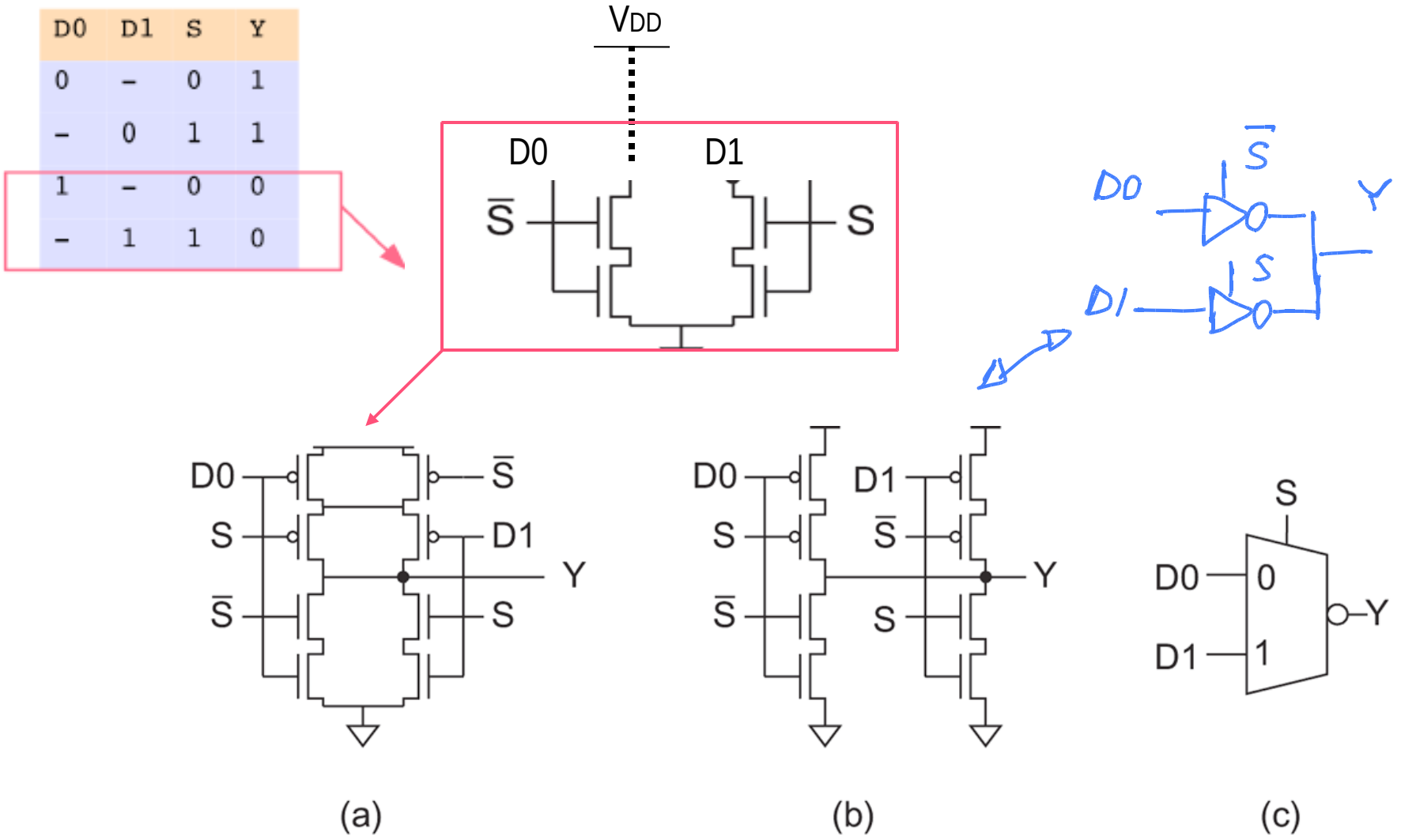


FIG 1.28 Inverting multiplexer

D Latch

- When CLK = 1, latch is *transparent*
  - D flows through to Q like a buffer
- When CLK = 0, the latch is *opaque*
  - Q holds its old value independent of D
- a.k.a. *transparent latch* or *level-sensitive latch*

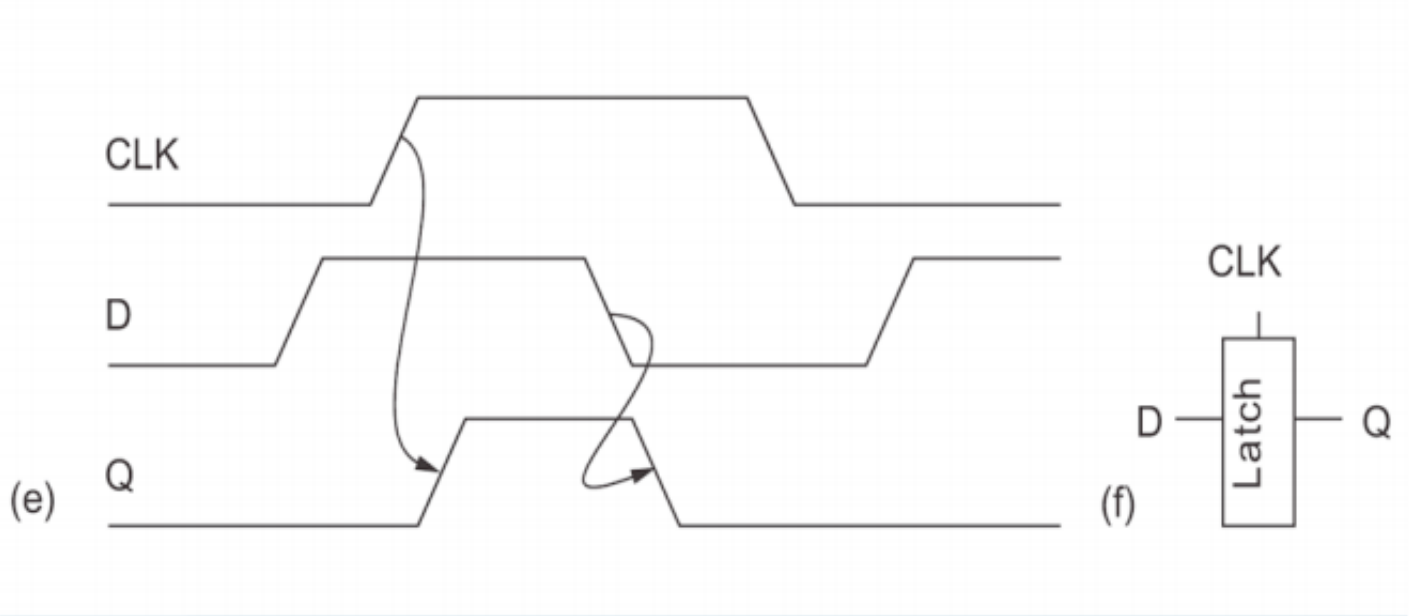


FIG 1.30 CMOS positive-level-sensitive D latch

D Latch Design and Operation

Multiplexer chooses D or hold Q

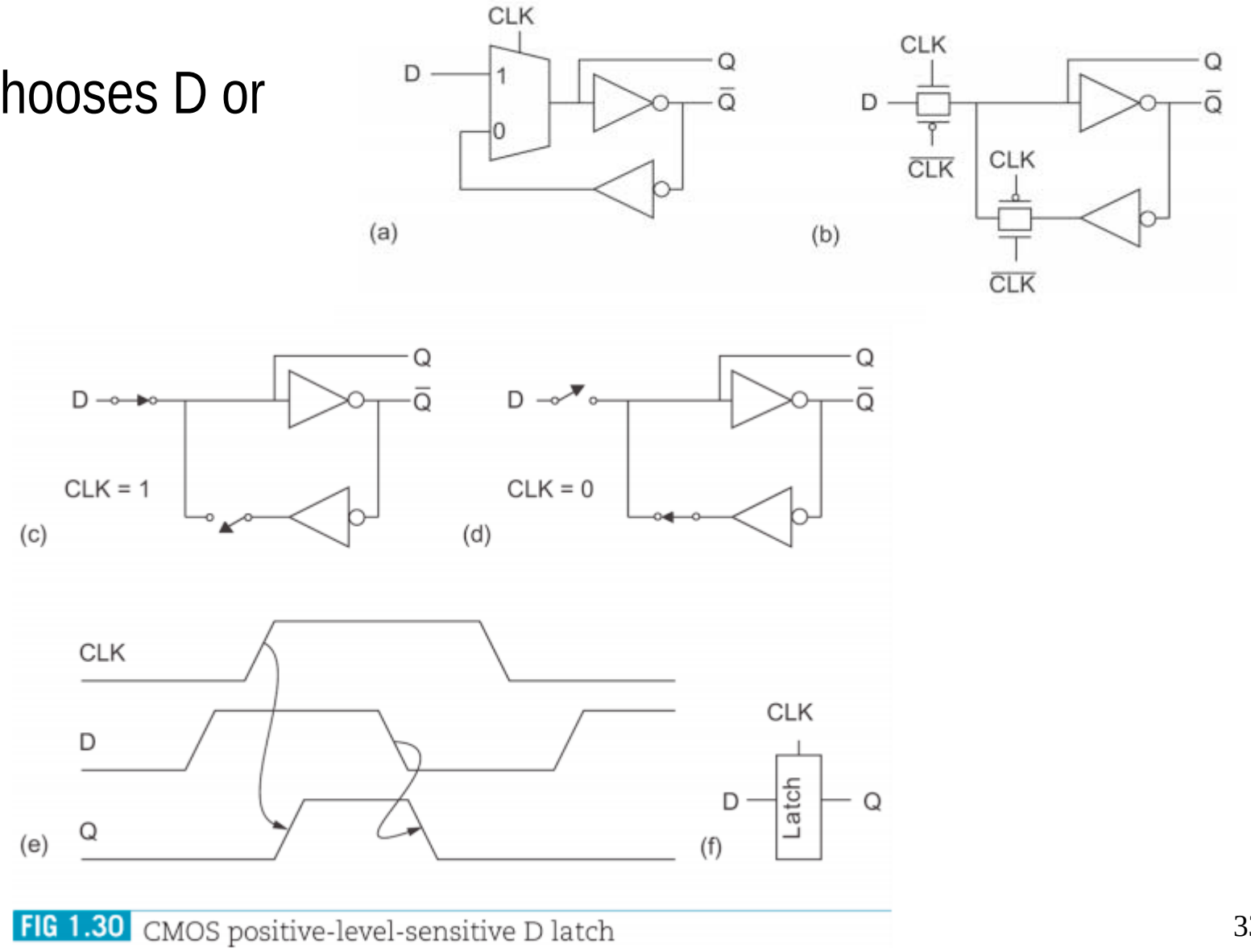


FIG 1.30 CMOS positive-level-sensitive D latch

D Flip Flop

- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- a.k.a. *positive edge-triggered flip-flop*, *master-slave flip-flop*

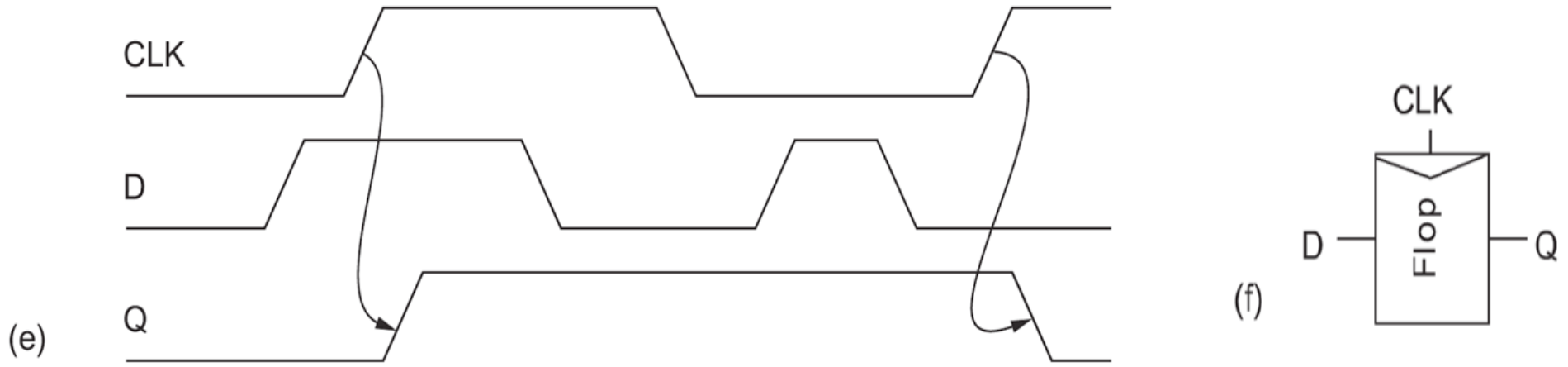
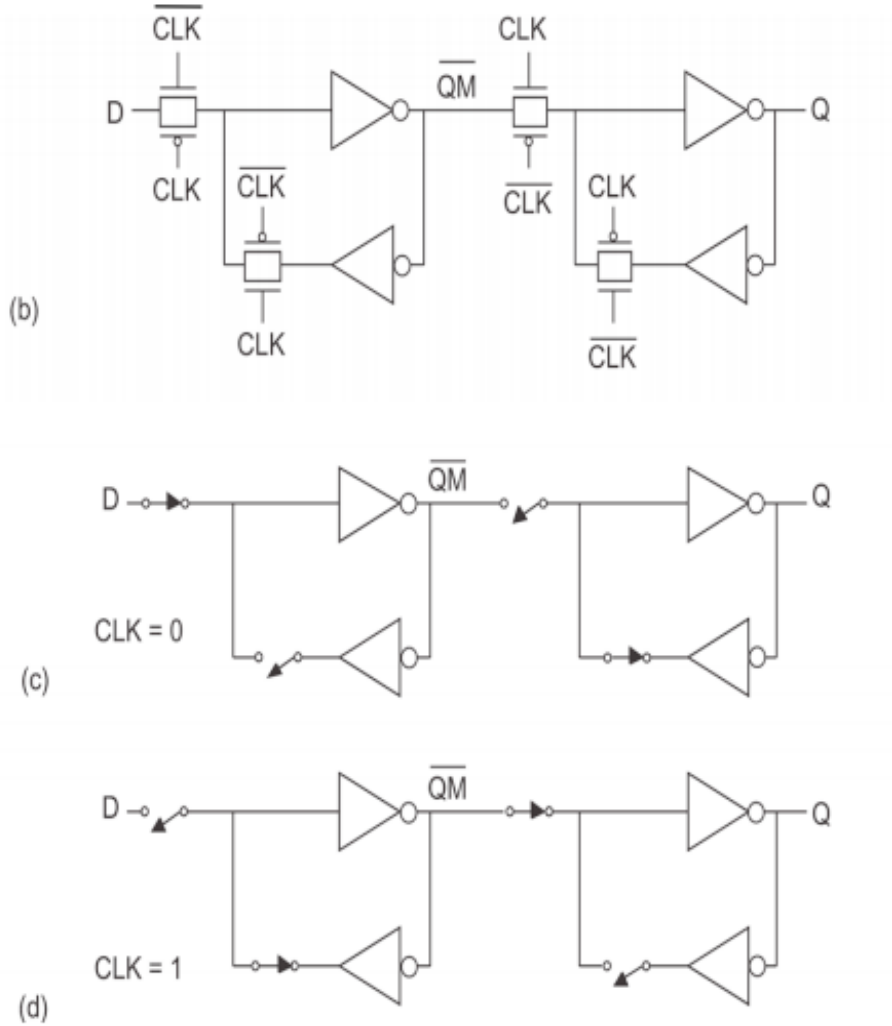
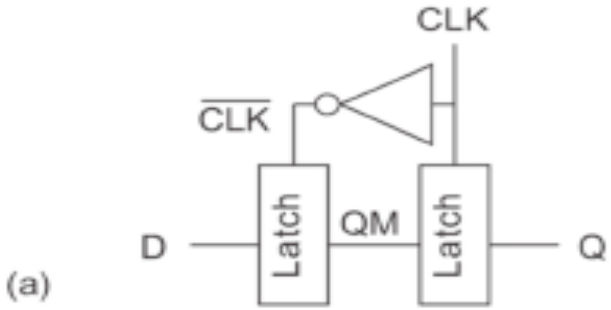


FIG 1.31 CMOS positive-edge-triggered D flip-flop

D Flip Flop Design and Operation

- Built from master and slave D Laches





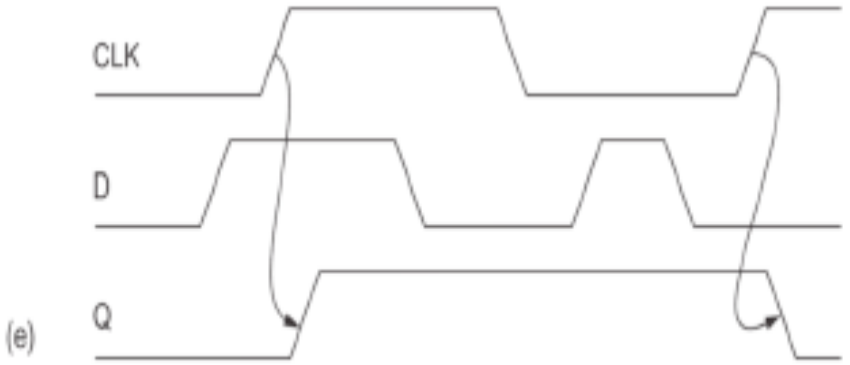


FIG 1.31 CMOS positive-edge-triggered D flip-flop