CMOS Image Sensors: Recent Innovations in Imaging Technology

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Abstract:- **Recent advances in CMOS imager technology has shown the potential to be applicable in the field of space technology, apart from its use in consumer digital camcorders, PC and cellphone cameras, machine vision, surveillance, toys, ID checks, etc. to name a few. The rapid progress has enabled the CMOS Imaging devices to compete with the well-established CCD devices. CMOS imagers has a definite edge over CCD devices vis-à-vis integration with standard CMOS operation, compact size, low cost, low power, on-chip support circuitry, random access, radiation tolerance, etc. The heart of present day CMOS digital camera is its pixel array. The Active Pixel Sensor (APS) comprises of multi-transistors (NMOS or PMOS) pixel, along with the photodiode or photogate to capture the light. The incident photons are converted into respective charge and/or voltage values. The Column Amplifier further moves this voltage to Double Correlated Sampling circuit and the resultant voltage value is converted into Digital Domain by the Analog-to-Digital converter (ADC). After this, Storing and Processing of the digital data is done by the digital block of the camera, which is considered as a relatively noise-proof operation. The major issue of various Temporal and Fixed pattern Noise, dark current etc. are inherited from the basic pixel block. Therefore, one of the most important parts of noise reduction in digital camera is to improve the noise performance of the pixel structure comprising of Photodiode/photogate and various NMOS Transistors. The present paper gives a brief insight into the development, design and working of a typical 4-Transistor (4T) APS. Various other pixel designs are also discussed briefly to bring out the 4T pixels abode in the CMOS APS device scene. A discussion on various Characterization factors to evaluate 4T APS functioning as a digital image sensing device and its Noise issues are also presented.**

Keywords: CMOS imaging, Active Pixel Sensors, 4T pixels, pixel noise, pixel characterization

I. INTRODUCTION:

The first ever metal oxide semiconductor (MOS)image sensor was suggested by Morrison in 1963 [1]. However, the first MOS image sensorin photon flux integration mode was proposed in 1967 by Weckler [2], which was a passive pixel sensor (PPS) [3]. In a typical PPS, the photons are converted into electrical charge by the photosite (photodiode), and this charge is controlled using a single pass transistor (MOS switch) to taken out of the pixel, and the signal is readout in charge sensing mode.This use of photosite for charge sensing and charge integration is the central theme in even present day complementary metal oxide semiconductor (CMOS) image sensors. Incidentally, the first MOS active pixel sensor (APS) was soon realizedin 1968 by Noble [4], which proposed the voltage sensing mode for photodiode(PD) charge by using an in-pixel buffer amplifier in Source follower mode. However, the MOS fabrication technology of that era was still under-developed for a mature image sensors technology, using a photodiode and MOS. The commercial viability and research interest took a back step for MOS image sensors, due to the excessive spatial noise (fixed pattern noise, FPN) in pixel arrays.

In 1970, Boyle and Smith invented the Charge Coupled Devices (CCDs), which originally were to be used as memory devices [5]. However, the light sensitive properties of CCDs were quickly recognized and owing to their simpler structure and much lower FPN, they almost finished any remaining interest in MOS imagers barring few [6, 7].Although, from 1970 to 1990, the commercial viability of CCD was firmly established and almost all digital imaging was done using CCDs, nevertheless the improvement in CMOS fabrication process, lead researchers to consider the CMOS image sensors as an alternative to the CCD technology in early 1990's.

The main motivation to look for CMOS image sensors came from the fact that CCDs are made using a dedicated fabrication process for photosensing elements, and it is difficult to co-integrate the functional blocks comprising of CMOS transistors with the CCD chip. On the other hand, CMOS imager showed the ability to provide the on-chip timing, control, correlated double sampling (CDS), and FPN suppressing circuitry along with the CMOS image sensor, by using the same fabrication process as standard CMOS processing [8]. Other motivations for using the CMOS APS imagers over CCDs are: low power consumption, lower cost, compactness, high speed, random access, integration with other devices, antiblooming, smearless operation etc. [9]. Nonetheless, CMOS imagers still has to compete with CCDs vis-à-vis pixel sensitivity to photon flux, dynamic range (DR), and noise issues etc [10].

II. DEVELOPMENT, DESIGN AND WORKING OF CMOS APS:

The CMOS pixel sensors use a photogate or photodiode to capture the photon flux and convert it into corresponding electrical charge. The main photodiode type MOS pixel sensors which use the photon flux integration mode can be divided into 2 basic approaches, i.e. of *passive*pixels (PPS) and *active* pixels (APS) [11]. A brief description of the photodiode type Pixel sensors is given as:

A. Passive Pixel Sensor (PPS) with photodiode

As shown in figure 1, Weckler [3] proposed the first PPS consisting of a photodiode and just one MOS transistor, which act as a switch to move the pixel signal charge on to a load resistor R_L. The integrated charge on photodiode was

read out by measuring the voltage across the load resistor, which was needed to reset the pixel. To integrate this pixel into array, he proposed the column wise load resistances, at the bottom of pixel columns.

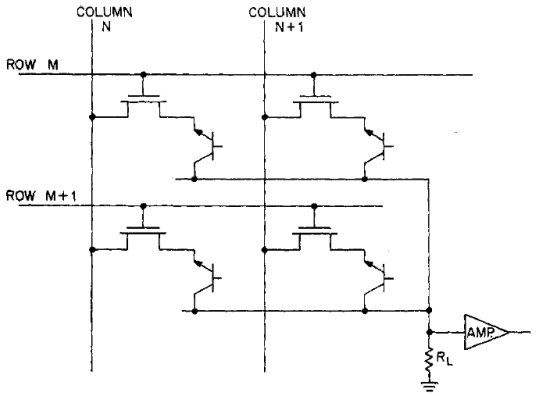

Fig. 1. Passive pixel sensor (PPS) array schematic, as proposed by Dyck and Weckler [3].

But this readout technique had limited use for large arrays due to large reset timing issues. Noble [4] proposed a one charge integration amplifier (CIA) per array for readout. But this technique suffers from large parasitic capacitance (due to all the data lines) and output signal voltage can be significantly reduced. To overcome the parasitic capacitance problem, more modern PPS use a column wise CIA at the bottom of each column bus, and uses one addressing (access) transistor, as shown in figure 2.At the start of a frame capture, the access transistor is activated such that the photodiode is connected to the vertical column bus. This resets the photodiode to a reverse bias of V_{ref}. The access transistor is then opened for the integration time (T_{int}) and photodiode is allowed to discharge at a rate approximately proportional to the incident illumination to the final value V_{diode}. Now, when the address transistor is again activated, the current flows via the resistance and capacitance of the column bus because of potential difference of V_{ref}-V_{diode}. This total charge required to reset the diode is integrated by the capacitor C_{int}, and output as a Vout. Eventually, the final bus and diode voltages are returned to V_{ref} by CIA. The address MOS is turned off and the voltage across C_{int} is removed by the reset MOS, and the next cycle ensues.

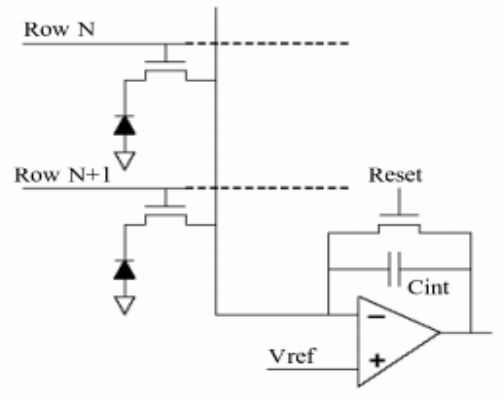

Fig. 2. Modern PPS array with column wise Charge Integration amplifier (CIA).

Although, this device still suffers from FPN (difference in CIAs), sensitivity and speed issues and used only for lower end consumer electronics, it boasts of highest design fill factor for a given pixel size. This leads to a very high Quantum efficiency (electrons collected per photon incident).

B. Active Pixel Sensor (APS) with photodiode

Noble [4] in 1968 showed the use of a MOS buffer amplifier along with a photodiode in the pixel to use the voltage sensing mode for signal readout. The buffer amplifier is used as a source follower to output the photodiode voltage as shown in figure 3.

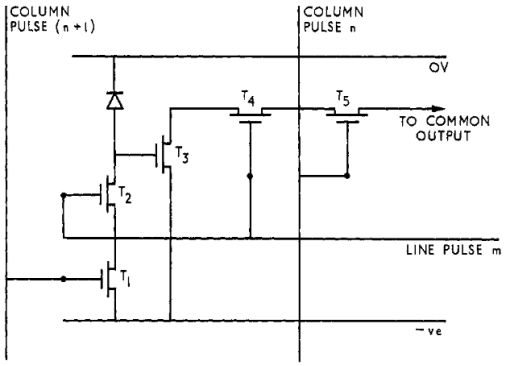

Fig. 3.First active pixel sensor (APS) with a photodiode and buffer amplifier (T3) for voltage sensing mode,as proposed by Noble [4].

The use of the buffer amplifier enables the lower noise level and higher readout speed. The power dissipation is minimal in this configuration as each amplifier is only activated during readout. In Noble's MOS APS, due to the immature fabrication technology, variations in diode dark currents, MOSFET threshold voltages and variations in leakages, capacitances etc. in circuitry lead to large FPN and very low signal to noise ratio (SNR). However, modern APS with improved CMOS fabrication process have managed to reduce the device variations and hence the FPN [12].

(a) *Three Transistor (3T) APS:* The most basic form of present day CMOS APS employs the photodiode and a readout circuit of three MOS transistors and called as 3T pixel.The three nMOS transistors are RESET transistor (M_{rst}), Source Follower (M_{sf}) and row–select (M_{sel}) transistor, as shown in figure 4.

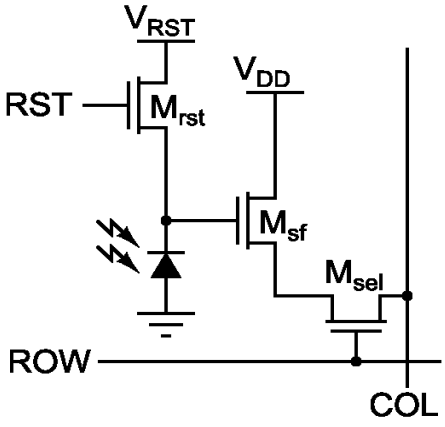

Figure 4. A Three-transistor (3T) active pixel sensor (APS)

Here, the PD capacitance is independent of the column bus capacitance and comprises only of the diode capacitance, M_{rst} source capacitance and M_{sf} gate capacitance. The p-n junction of the photodiode is used as the photon sensing node. The M_{rst}nMOS is used to reset the PD to a value equal to [reset voltage (V_{RST}) – threshold voltage (V_t)], before the integration time starts and then the M_{rst} is switched OFF during T_{int}. This sets the base voltage for the integrated signal. The integrated charge is then accumulated in the PD during T_{int} and the photodiode voltage decreases from the (V_{RST}-V_t) value due to the electron accumulation in PD. The reduced PD voltage is then sensed by the M_{sf}. The nMOS source follower transistor M_{sf} is acting as a voltage buffer to drive the output independently of the diode. The source voltage of M_{sf} is then output using the M_{sel} transistor which is acting as a switch and select transistor. There is a single active-current-source-load for each column (to keep fill factor high and FPN low) and readout timing is set such that only one row is activated at any time. The *signal voltage* is thus sampled. Now, the M_{rst} is switched ON to re-create the base voltage for PD. The double sampling circuitry in the column then subtracts the signal voltage from *reset voltage* and the light intensity is determined. The double sampling operation is supposed to negate the threshold mismatch of the M_{sf} transistors so that the pixel FPN is reduced. However, the temporal noise in the 3T pixel is rather high owing to the different reset voltages used in the signal base voltage and re-created reset level. Thus the two sampled signals in fact contain the reset noise from different reset operations. Since the Reset noise (also called as kTC noise, which originates from thermal noise of nMOS M_{rst} transistor) here is non-correlated, this double sampling operation actually increases the resulting noise power. Nonetheless, the typical fill factor for 3T APS is still reasonable (20-35%) and a major reason for its large scale commercialization in CMOS imagers.

(b) *Four Transistor (4T) APS:* In the 4T pixel, an additional nMOS transistor is used as transfer gate (TG), which separates the photodiode (PD) from the reset transistor (RG) source and floating diffusion (FD) region and hence the source follower (SF) gate, as shown in figure 5.

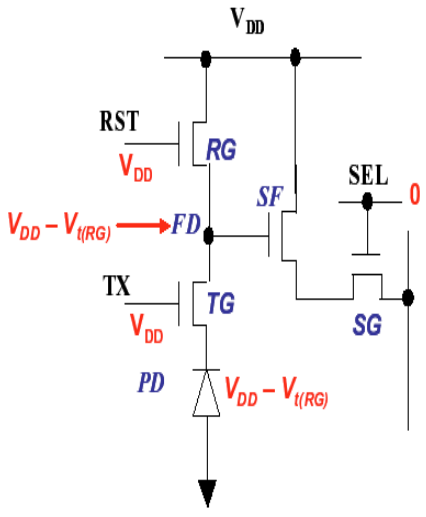

Fig. 5.A four-transistor (4T) active pixel sensor (APS)schematic during reset operation.

Row select nMOS transistor (SG) is used as switch to sample the signal voltage and reset voltage. This enables the 4T pixels to have an electronic global shutter and make use of correlated double sampling (CDS). In principle, this should remove the offset and noise due to reset signal after double sampling operation. The operation starts with a reset pulse to PD while RG and TG are switched ON. This resets the PD to a voltage of (V_{DD}-$V_{t(RG)}$). Next, the TG is switched off and PD is allowed to integrate the charge. A second reset pulse is then sampled at the end of the T_{int}, which also clears the FD off dark current charge and leakage current through TG. The TG is then switched ON and the *signal voltage* is sampled and subtracted from *reset voltage* through CDS [13]. A further improvement in 4T APS is proposed by using the pinned photodiode principle [14]. A pinned photodiode means 2 things: a diode that is fully depleted of mobile charges and one where silicon surface states are pinned to a voltage. The device uses additional implantation steps to the standard CMOS process, which implants an additional P+ surface implant on the surface of PD, as shown in figure 6.

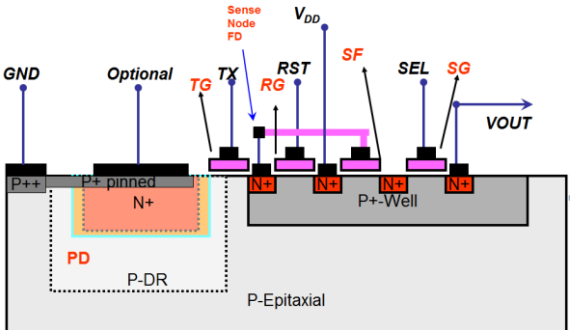

Fig. 6. A 2-D depiction of pinned photodiode (PPD) active pixel sensor (APS)

The P+ implant acts like a self-biased internal photogate. Here, the doping levels and implant depths are carefully controlled to deplete the n-region completely. The P+ implant pins the potential at the PD surface to that of the substrate,and so do not contribute to generation/recombination currents, leading to lower dark current. Moreover, a buried PD well is formed which encourages the blue electrons to move away from the surface towards the buried PD well. However, a tradeoff is there to consider a heavy doping to reduce the dark current generation at surface or to have a shallower implant to bring the electric field closer to the surface and collect more blue electrons.

III. NOISE ISSUES IN CMOS APS:

The CMOS APS are designed to maximize the sensitivity to illumination; however the overall performance of the sensor is ultimately limited by the noise that is added by the system to the signal. One of the most important figures of merit of CMOS APS is its dynamic range (DR), which is given as the ratio of saturation signal to rms noise level. The minimum resolvable signal is determined by the noise in the system, and would require a very low noise floor (also called read noise, comprising of amplifier noise, reset noise and ADC noise) to collect reasonable data at low light levels. As mentioned earlier, reset noise is thermal noise of RST

transistor and occurs due to charging of PD capacitance through the resistance of RGnMOS channel. Flicker Noise (1/f noise) is due to the conductivity fluctuations at junctions and arises mainly in amplifier circuits. At low frequency, 1/f noise can be a dominant factor. Apart from the read noise, the other two system noise components are the shot noise (due to statistical arrival of photo-generated electrons and thermal-generated electrons in depletion region) and pattern noise.

Typically, the noise in CMOS APS can be categorized as: *Random Noise*[15] and *Pattern Noise* [13]. The random noise (temporal noise) is not constant from frame to frame and so can be reduced by averaging the frames. However, the pattern noise is effectively a spatial noise and does not change from frame to frame, so cannot be removed by frame averaging. The pattern noise can be subdivided into 2 components;fixed pattern noise (FPN) and photo response non uniformity (PRNU). FPN is measured in the absence of illumination, and is mainly due to the variations in MOS characteristics (Vt, gain, W, L etc.), doping variations, dimension variations, or contamination during fabrication between pixels. More specifically, the main cause of FPN in CMOS imagers is the variation in nMOS Vt of RST and SF transistors between pixels and Vt variations between MOSFETs in column circuits.FPN can also occur due to faulty array clocking. In the late 1960's, FPN was the main reason for rejection of CMOS imagers.However, FPN is independent of the illumination level. PRNU on the other hand is illumination dependent and is caused due to variations in PD dimension, doping, topography and spectral response between pixels.A general depiction of various noise components in CMOS APS is given in figure 7.

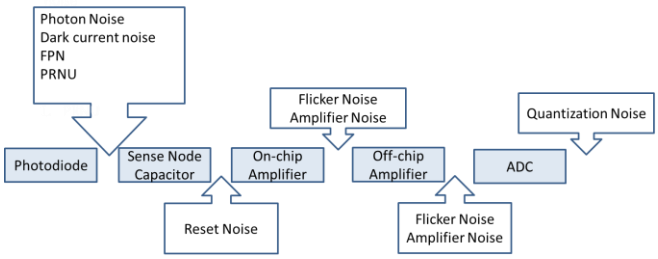

Fig. 7.Various components of CMOS APS noise and their introduction regime.

To apply the noise reduction technique, there are essentially three classes of noise; noise which cannot be reduced (shot noise), noise which can be reduced by better design of circuit components (thermal noise) and noise which can be reduced by circuit design (FPN). However, adding extra circuit to reduce FPN would increase 1/f noise and KTC noise. Photon shot noise is dependent on the illumination level and we cannot reduce it without reducing the quantum efficiency (QE) of the PD. Shot noise also arises from the pixel dark current. This again can be reduced by increasing the doping level and reducing the depletion region of PD, but will again adversely affect the QE of the diode. Fortunately, shot noise is not the usual limiting factor in CMOS APS. In general, smaller MOS channel length and an optimized channel width would reduce the thermal noise. Flicker noise arises mainly due to the trapping-detrapping of electrons at the Si-SiO2 interface. So, reducing the channel length is a viable option to reduce the device area, as channel width cannot be reduced due to adverse effect on amplifier gain. Flicker noise in CCD was reduced by using the buried channel device (BCD), however, implementing BCD in CMOS APS is a challenging task. Reset noise is difficult to design out of the CMOS APS system unless we go for lower FD node capacitance, which also increases the conversion gain. The most common solution to remove reset noise is to measure the reset noise and then subtract it from the signal as is done in correlated double sampling (CDS). In CMOS APS, we need one CDS circuit per column of the pixel array and sample and hold is carried out for all columns in parallel. However, Column wise CDS circuitry could further add the KTC noise from the sample and hold capacitors and thermal and flicker noise from its MOSFETs.Moreover, column wise FPN could also be added by the CDS circuits themselves which appears as vertical streaks in the image. But this column FPN could be removed by storing and subtracting the column reference signals off chip.Apart from the random and pattern noise sources mentioned, there could be design issues which lead to additional noise and therefore careful layout needs to be done for CMOS APS.

IV. CHARACTERIZATION FACTORS FOR CMOS APS:

The most common pixel array performance criteria are read noise (Nr), PD full well capacity (FWC), conversion gain (CG) and responsivity (Rp). FD node capacitance, maximum output voltage swing (MOVS), dynamic range (DR) and signal to noise ratio (SNR) can be calculated using this information [16, 17]. Other important pixel performance is related with dark current (DC) measurements and noise due to dark current. All the noise components related to Temporal, FPN and pixel noise are also obtained using various statistical methods during pixel sensor characterization. A brief description of various characterization parameters are given as:

A. Pixel Characteristics: The pixel characteristics are a measure of the pixels performance and can be classified as:

(a) *Dark Current (DC):* Dark current is measured as PD signal response when it is allowed to integrate the thermally generated charges under complete absence of illumination. This parameter is always reported at a particular temperature. The dark FPN becomes an important parameter under low light conditions. It is advantageous to have lower DC and DC related noise components for improved pixel performance.

(b) *Fill Factor (FF):* It is defined as the ratio of light capturing area of pixel to that of the total pixel area. CCDs has almost 100% FF [18.19], whereas, CMOS APS has 30% FF, typically. The lower FF in CMOS APS is due to the recombination of charge carrier, smaller depletion region, shadowing by metal and silicide layers etc. Various topography configuration, microlens efficiency [20], and PD dimension also decides the FF. FF is very important criteria for scalability of CMOS APS. It is advantageous to have maximum FF to improve pixel performance. Increasing PD area leads to higher FF but it also increases the PD capacitance and hence loss of pixel sensitivity [21].

(c) *Conversion Gain (CG):* It is defined as the change in pixel signal voltage as 1 electron is added to the FD sense node. It is usually measured in microvolt per electron. CG estimation is a critical factor for correctly determining the sensitivity, noise and Quantum efficiency of the pixel. A high CG is advantageous for pixel performance; however various other constraints need to be considered along with its optimization by modifying FD sense node.

(d) *Signal to Noise ratio (SNR):* Defined as the ratio of average pixel signal to that of the total noise at any particular exposure setting. A higher SNR is desirable for better pixel performance. It can be given as

$$\mathrm{SNR_{dB}} = 10\log_{10}\left(\frac{A_{\mathrm{signal}}}{A_{\mathrm{noise}}}\right)^2 = 20\log_{10}\left(\frac{A_{\mathrm{signal}}}{A_{\mathrm{noise}}}\right).$$

(e) *Read Noise (Nr):* Read noise is defined as the temporally random background noise, which is present in all pixel outputs under dark conditions. This is attributed to the temporally random reset noise, amplifier noise, ADC noise, signal chain noise, power supply coupling noise and clock coupling noise. This does not include noise due to dark current. Therefore read noise must be measured such that dark current is kept minimum in the signal output. A lower Nr would lead to better pixel performance in general and for low light conditions in particular.

(f) *Photodiode Full Well Charge Storage Capacity (FWC):* Full well capacity of PD is an important factor for pixel performance and must be optimized accordingly. FWC can be measured as number of electrons that can be stored in the PD depletion region and is calculated as ratio of the product of averaged pixel MOVS at saturation and FD node capacitance to that of an electron charge.

(g) *Responsitivity (Rp):*Pixel responsitivity is calculated by the slope of averaged pixel signal value to that of exposure. A higher Rp is advantageous for pixel performance.

(h) *Sensitivity (St):* Pixel sensitivity is defined as the average pixel signal output at the given exposure of certain wavelength. It is calculated from the Rp considering the wavelength. A higher St is advantageous for pixel performance [22].

(i) *Quantum Efficiency (QE):* Pixel QE is defined as the number of electrons generated (more accurately, collected) in the pixel when 1 photon is incident on the pixel. Together with FF, it gives an accurate measurement of the pixels electrical sensitivity to light. The energy of a photon depends on its wavelength, and hence QE is often measured over a range of different wavelengths to characterize a device's efficiency at different photon energy.

B. Array Characterization: Various characterization parameters which are used to array characterization are given as:

(a) *Fixed Pattern Noise (FPN):* FPN is defined as the spatial variations in the pixel average response under dark conditions. It is a measure of the fixed offsets present in each pixel or row or column circuitry .FPN does not include dark current contribution to fixed pixel offsets. FPN should be minimized to improve the array performance [23, 24, 25].

(b) *Image Lag (IL):*If the charges in the PD are not fully extracted, they can be visible in the next captured frame. Image lag can be present in bright-dark and dark-bright transitions. An incomplete PD charge extraction (due to large PD size or barrier in neck region between PD and TG channel) leads to bright-dark lag, often called as fat-zero. The name fat-zero comes from the fact that PD is still fat with electrons even when there is no illumination in the next frame and it will be seen in the signal output. Further, supposing that pixel is reset in dark conditions for quite some time, the thermionic emission will keep emptying the fat-zero charge. This would further lead to over-depletion of PD and would be visible as non-linearity in low light condition and as an image lag in dark-bright condition. Image lag can be measured as the ratio of residual signal in the next dark frame to that of the illuminated frame. Image lag should be minimum for better array performance [15].

(c) *Photoresponse Non Uniformity (PRNU):*PRNU is the spatial noise which does not change much from frame to frame, while the pixel is illuminated. It occurs due to the difference in average pixel response in light conditions. The measurement is almost similar to that of FPN except that light condition is used in place of dark. A lower PRNU is desired for better array performance.

(d) *Blooming:* Blooming occurs due to conditions in which the finite charge capacity of individual photodiodes is reached. Once saturation occurs at a charge collection site, accumulation of additional photo-generated charge results in overflow, or blooming, of the excess electrons into adjacent pixels. A number of potentially undesirable effects of blooming may be reflected in the sensor output, ranging from white image streaks and erroneous pixel signal values. Blooming can be removed by using an extra nMOS transistor in pixel (5T pixel).

V. INNOVATIONS IN PIXEL SIMULATIONS

At present various software tools are being used to simulate the pixel process and device characteristics. A typical 7 gate CMOS APS doping simulations is shown in figure 8. The black arrow shows the direction and position along which the 1D plot for doping concentration is extracted (in red color). Simulation of prototype pixel designs is one of the most advanced innovations in technology evolution for designing and testing the CMOS APS. Major dynamical characteristics which are investigated using pixel simulations are potential profile, electric field distribution, and electron concentration within pixel, as the various bias cycles are modified and time periods are varied. The simulations give the best insight vis-a-vis pixel performance while saving the money, time and efforts.

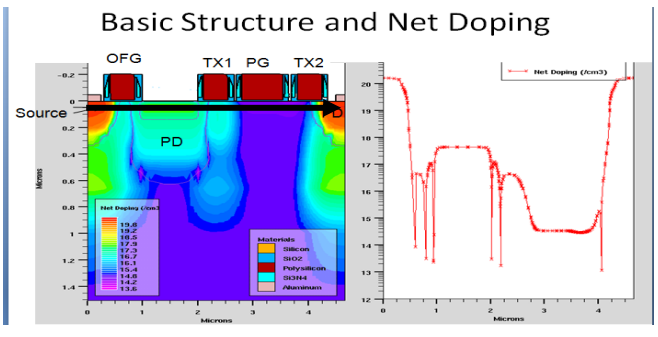

Fig. 8 Basic structure and net doping at 0.05 micron depth for a typical 7 gate CMOS APS.

VI. CONCLUSIONS

A review of the photodiode type 4T CMOS APS is presented, which is at present the most preferred choice for high performance CMOS imagers. The various issues regarding the historical origins of PPS and APS are pointed out. Although, the CCD will dominate the high performance systems such as medical imaging, astronomy for some time, nonetheless CMOS imagers will replace the CCD devices in various smart applications field [26]. The photodiode type CMOS APS clearly has the edge over CCDs vis-à-vis imager applications dedicated to portable devices [27,28], fingerprint ID, electronic toys, machine vision, security and surveillance [29], night vision, motion analysis, spectroscopy, target tracking, industrial inspection [30,31], aerospace [32-36], space technology [37,38], quality control, process control, video conferencing, internet camera, video cellphones, automotive [17] etc. High end professional CMOS video cine cameras (equivalent to 35mm film) are already in the market with 12 MP array and very high frame rates. It can be safely said that in the near future, the digital imagers' field is definitely going to be dominated by the photodiode type CMOS APS.

REFERENCES

[1] S. Morrison, Solid State Elec.5 (1963) 485-494.
[2] G. P. Weckler, IEEE J. Solid State Circ. SSC-2 (1967) 65-73.
[3] R. Dyck, G. Weckler, IEEE Trans. Electron Dev. 15-4 (1968) 196–201.
[4] Peter J. W. Noble, IEEE Trans. Electron Dev. 15-4 (1968)202–209.
[5] W. S. Boyle et al., Bell Sys. Tech. J. 49 (1970) 587-593.
[6] S. Obha et al., IEEE Trans. Electron Dev. 27 (1980) 1682-1687.
[7] K. Senda et al., IEEE Trans. Electron Dev. 13 (1984) 1324-1328.
[8] R. Nixon et al., Proceedings of SPIE. 2415 (1995) 117-123.
[9] Mendis et al., IEEE Trans. Electron Dev. 41 (1994) 452-453.
[10] A. Theuwissen, Int. Symp. VLSI Tech. Sys. App. (2001) 168-171.
[11] I. Shcherback , O. Yadid-Pecht, IEEE Trans. Electron Dev. 50 (2003) 12-18.
[12] Mendis et al., IEEE J. Solid State Circ. 32 (1997) 187-197.
[13] B. Fowler et al., Proceedings of SPIE. 4306 (2001) 68-77.
[14] T. Lule et al., IEEE Trans. Electron Dev. 47 (2000) 2110-2122.
[15] H. Tian et al., IEEE J. Solid State Circ. 36-1 (2001) 92-101.
[16] O. Schrey et al., IEEE J. Solid State Circ. 37 (2002) 911-915.
[17] M. Schanz et al., IEEE J. Solid State Circ. 35 (2000) 932-938.
[18] W. Yang et al., IEEE Int. Solid State Circ. Conf. 37 (1990) 218-219.
[19] R. Reich et al., IEDM Tech. Dig. (2001) 24.6.1-24.6.4.
[20] Y. Fan et al., Proceedings of SPIE. 4115 (2000) 263-274.
[21] S. Chamberlain, IEEE J. Solid State Circ. 4 (1969) 333-342.
[22] M. Furumiya et al., IEEE Trans. Electron Dev. 48 (2001) 2221-2227.
[23] S. Miyatake et al., IEEE Trans. Electron Dev. 50 (2003) 121-129.
[24] T. kwok et al., IEEE Elec. Lett. 38 (2002) 317-318.
[25] S. Miyatake et al., Proceedings of SPIE. 4306 (2001) 128-136.
[26] E. R. Fossum, Proceedings of IEDM. 497174(1995) 17-25.
[27] C. H. Small, Computer design, PennWell Publishing, 37-4 (1998) 37-40.
[28] K. Yoon et al., IEEE J. Solid State Circ. 37 (2002) 1839-1845.
[29] K. Cho et al., IEEE Int. Solid State Conf.. (2000) 114-115.
[30] A. Teuner et al. Int. Conf. Image Analysis Proc. (1999) 1124-1127.
[31] P. Lee, C. Anagnopoulis, IEEE Int. ASIC conf. (1998) 381-381.
[32] M. Tabet, R. Hornsey, Can. Conf. Elec. Comp. Engi. 2 (2001) 1129-1133.
[33] J. Goy et al., Proceedings of SPIE. 4019 (2000) 145-152.
[34] C. Liebe et al., IEEE Aerospace Conf. 1 (1998) 119-127.
[35] P. Holl et al., Nuclear Sci. Symp. 1 (1999) 171-175.
[36] R. Stirbl et al., Proceedings of SPIE. 4547 (2002) 1-10.
[37] E. El-Sayed, Nat. Radio Sci. Conf.17 (2000) 1-9.
[38] Woo-Tae Kim et al., Sensors 19-7 (2019) 1505.
[39] Jimin Lee et al., Sensors 19-8 (2019) 1823.