CMOS Image Sensors with Self-Power Generation Capability

Alexander Fish, Shy Hamami and Orly Yadid-Pecht, *Senior Member, IEEE*

***Abstract*— Considerations for CMOS image sensors with self-power generation capability design are presented. Design of CMOS imagers, utilizing Self-Powered Sensors (SPS) is a new approach for ultra low-power CMOS Active Pixel Sensors (APS) implementations. The SPS architecture allows generation of electric power by employing a light sensitive device, located on the same silicon die with an APS and thus reduces power dissipation from the conventional power supply. This makes image sensors using the SPS architecture very useful in applications where ultra low-power is the main demand. A detailed analysis of the SPS structure is carried out, with respect to power dissipation requirements, sensor area and power generation efficiency, showing advantages and drawbacks of the proposed concept.**

An illustrative example of CMOS imager with Self-Power generation capability in 0.18µm standard CMOS technology is discussed. Measurements from a test chip, implemented in 0.18µm CMOS process, are presented.

***Index Terms*—Active Pixel Sensor (APS), Self-Powered Sensor (SPS), Power Generated Photo Diode (PGPd), low-power sensor.**

I. INTRODUCTION

CMOS image sensors are very attractive in the field of portable battery-operated devices. CMOS imagers offer significant advantages in terms of low-cost, low-power, low-voltage and monolithic integration. Current state of the art CMOS imagers allow integration of all functions required for timing, exposure control, color processing, image enhancement, image compression and ADC on the same die, while dissipating only tens of mW of power. It is expected that the next generation of image sensors will consume less than 1mW to support the demand for continuous power reduction in mobile devices [1]-[3]. This target is usually achieved by technology scaling and aggressive supply voltage reduction. However, low-voltage power supply has an enormous impact on the imager performance, mainly due to dynamic range and signal-to-noise ratio reduction.

A comprehensive study on low-power low-voltage CMOS image sensors has been performed in the last years [1]-[14]. A number of methodologies were presented to reduce imager power dissipation while still achieving good image quality. In 2000 an CMOS Active Pixel Sensor (APS), fabricated in 0.35µm CMOS technology and operating at a supply voltage of only 1.2 V has been demonstrated by Cho [3]. In this work the bootstrapping technique was used to increase the dynamic range of the sensor. Another approach to low-voltage APS design was presented in [4],[5], where a PMOS is used as the reset transistor inside the pixel to eliminate threshold voltage drop. Low-power 1V voltage supply complementary APS architecture that removes the threshold voltage influence on the available output swing was presented by Xu in 2002 [12]. An advanced APS imager using low-power sensor design methodology was presented in 2002 [13]. In [14] an ultra-low power wide dynamic range snapshot imager with dual voltage supplies was presented. Current mode pixel architectures were also used to reduce power dissipation [15].

This paper presents considerations for CMOS image sensors with self-power generation capability design, providing both theoretical analysis and measurements from a test chip. Design of CMOS imagers, utilizing Self-Powered Sensors (SPS) is a new approach for ultra low-power CMOS Active Pixel Sensors (APS) implementations [16]. The SPS concept is based on the sensor self-power generation using an additional photo sense element, located on the same silicon die with APS. The SPS pixel architecture allows employing the energy of incident light to produce power for the APS reset operation and in-pixel amplifier, hence reducing the sensor power dissipation from the regular power supply. One of the well known methods, having a similar concept of power production is a solar cell. However, the advantage of the proposed SPS technique over solar cells is that it can be easily integrated with a CMOS imager in a standard fabrication process.

Section II describes the SPS architecture and explains its principles of operation. A detailed analysis with reference to power dissipation requirements, sensor area and power generation efficiency is presented in Section III. Section IV shows an illustrative example of an SPS structure in 0.18um standard CMOS technology. Test chip design and measurements from the prototype, fabricated in a standard 0.18µm CMOS technology are described in Section V. Conclusion and future research are outlined in Section VI.

Manuscript received Mar 9, 2004.

A. Fish is with the VLSI Systems Center, POB 653, Beer-Sheva 84105, Israel (e-mail: afish@ee.bgu.ac.il).

V. Milrud is with the VLSI Systems Center, POB 653, Beer-Sheva 84105, Israel (e-mail: milrud@ee.bgu.ac.il).

O. Yadid-Pecht is with VLSI Systems Center, POB 653, Beer-Sheva 84105, Israel (phone: 972-8646-1512; fax: 972-8647-7620; e-mail: oyp@ee.bgu.ac.il) and with Dept of Electrical and Computer Engineering, University of Calgary, Alberta, Canada T2N1N4.

II. SPS CONCEPT, ARCHITECTURE AND PRINCIPLE OF OPERATION

A. SPS concept

Fig.1 shows an example of a possible implementation of the basic SPS structure in conjunction with a 3-T photodiode CMOS APS employing a PMOS reset transistor [4],[5]. This structure implements the basic APS elements and **P**ower **G**eneration

Photo**d**iodes (PGPd), used for self-power generation. These PGPds are inverse-biased using a conventional power supply (V_{DD}). According to this proposed design, the V_{DD}' line is common to all pixels and is connected to the PGPd elements, which can be located inside each pixel or alternatively, in the sensor periphery. The SPS operates as follows: under illumination conditions, the voltage at node V_{DD}' is increased to V_{DD} by the photocurrent which discharges the PGPd space-charge capacitance. This photo-electric process is comparable to the regular photodiode (Pd) operation, where the voltage across the junction decays proportionally to the illumination level. Note, the PGPd is connected in an open-circuit configuration, as long as the reset and the RS transistors are off, which is similar to the Pd integration mode. The photo-electric charge, induced by PGPd element is used for Pd reset during the reset stage and for readout operation, as will be described in sub-section B.

Fig. 2 depicts a possible SPS implementation in a standard n-well CMOS process. The PGPd element is formed by the p+-Nwell junction, while the Pd is implemented by the n+-Psub junction.

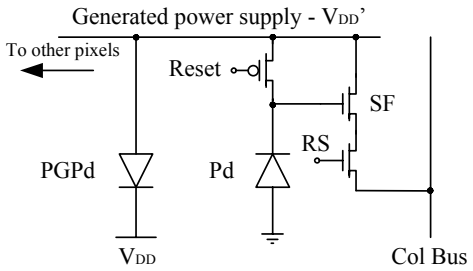

Figure 1. Possible implementation of SPS.

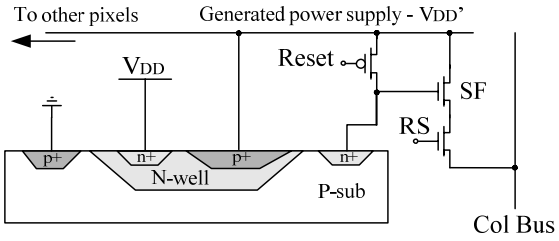

Figure 2. Possible SPS implementation in a standard N-well CMOS process.

As previously noted, the PGPd elements can be located inside each pixel (as shown in Fig. 2), which has an advantage of robustness in scene contrast because it is able to receive scene illuminance averagely by the overall focal plane. However, this approach degrades the sensor fill factor and spatial resolution. Thus, locating PGPd elements in the array periphery can be preferred in some cases.

B. SPS architecture and principle of operation

Fig. 3 shows the general architecture of the proposed SPS structure, operating in the rolling shutter readout mode [17]. The structure consists of (a) a single SPS pixel, as presented in Fig. 1, (b) VLN transistor, which acts as a current source, (c) Enable transistor for leakage current reduction due to the stack effect [18], (d) two analog switches for signal and reset signals selection, (e) two capacitors for reset and signal voltage storage, C_R and C_S, respectively.

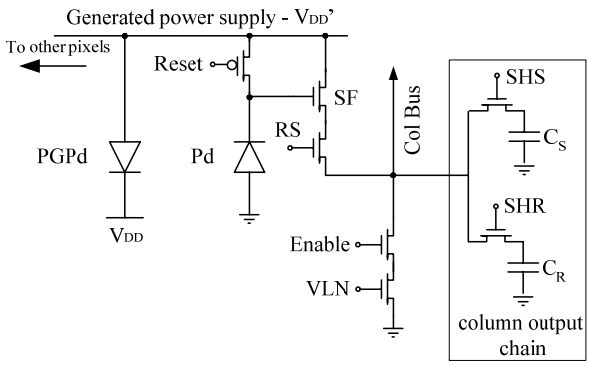

Figure 3. SPS general architecture.

From a power dissipation point of view, the SPS operation, with reference to Fig. 3 and Fig. 4, can be divided into two main phases, (a) Enable transistor is on and (b) Enable transistor is off ("power-off" phase). The first phase ($T_{readout}$ in Fig. 4) consists of the Pd reset stage, the reset value readout stage (SHR) and the photo-generated signal readout stage (SHS). During this stage, the circuit is powered by the PGPd elements. However, the phase (b) can be considered as non-power consumer phase, where the PGPd element can be charged by the photo-electric charge in open circuit configuration.

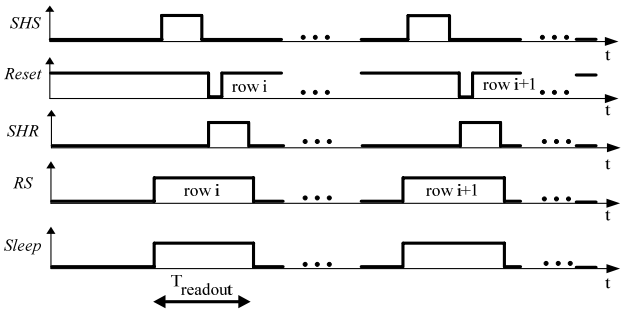

Figure 4. SPS timing waveform

In the rolling readout technique the Correlated Double Sampling (CDS) circuit is usually used to reduce the Fixed Pattern Noise (FPN) by subtracting the signal pixel value from the reset value of the next frame. Because CDS is not truly correlated without frame memory, the read noise is limited not only by the reset noise on the photodiode, but also by the voltage variations on the PGPd elements (V_{DD}'). The V_{DD}' variations are due to charge pumping during $T_{readout}$ phase and illumination level deviations between two sequential readouts. The above flaws can be overcome by the use of truly CDS, which requires 4-T transistors APS architecture [17],[19].

As mentioned above, the V_{DD}' voltage depends on illumination levels. Thus, the SPS reliability can be undermined in low illumination levels. To overcome this possible problem, a backup circuit should be used. Fig. 5 shows a possible implementation of such a type of a circuit.

The backup circuit operates as follows: before each Treadout phase, the comparator samples the VDD' voltage and compares it with appropriate reference voltage Vref. In case where the VDD'< Vref, meaning that PGPd element voltage did not recover during the "power-off" phase, the PMOS transistor is on and VDD' node

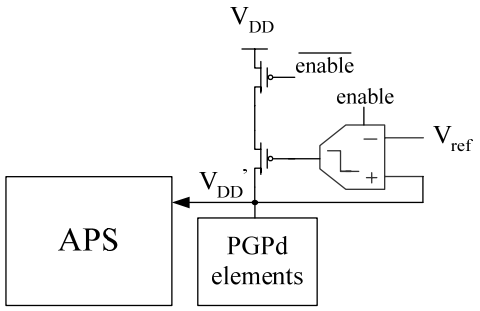

Figure 5. Possible implementation of a backup circuit.

is charged to V_{DD}. The V_{ref} voltage is defined as $V_{ref}=V_{DD}- \Delta V_{max}$, where ΔV_{max} is the maximum allowed voltage drop in power supply, which ensures a proper operation of APS. A brief ΔV_{max} determination is discussed in the next Section. Note, the comparator used in this backup circuit should be power efficient and is activated only for very small periods of time employing the enable input.

III. SPS Analysis and Constraints

A. APS Power Dissipation Pattern

APS power dissipation during the $T_{readout}$ phase can be divided into the following components: (a) the power dissipated by the VLN transistor, (b) the power dissipated to charge the storage capacitors C_S and C_R and (c) the power dissipated through reset operation of the pixel photodiode. Equations (1) - (3) describe the charge pumping of components (a) to (c), respectively.

$$\Delta Q_{V_{LN}} = T_{readout} \cdot N_{col} \cdot I_{LN} \tag{1}$$

$$\Delta Q_C = \left(C_S + C_R\right) \cdot V_{swing} \cdot N_{col} \tag{2}$$

$$\Delta Q_{reset} = C_{pd} \cdot V_{swing} \cdot N_{col} \tag{3}$$

where N_{col} is the number of pixels in the row, I_{LN} is the current flowing through the VLN transistor, V_{swing} is the maximum swing value on the C_S and C_R capacitor, C_{pd} is the pixel photodiode capacitance. The predominant power consumers are the current source I_{LN} and the C_S and C_R capacitors charging, while the ΔQ_{reset} component can be neglected, resulting in:

$$\Delta Q_{TOT} = \Delta Q_{V_{LN}} + \Delta Q_C \tag{4}$$

where ΔQ_{TOT} is the total charge dissipated during the $T_{readout}$ phase.

B. PGPd power generation efficiency

Power generation efficiency of SPS structure is defined by the photo-electric conversion efficiency of the PGPd element. The photocurrent, produced in PGPd may be considered as a current source and is given as follows:

$$I_{ph} = q \cdot \Phi \cdot \eta \cdot A \tag{5}$$

where q is the electron charge, Φ is the photon flux, η is the quantum efficiency and A is the photosensitive area.
The total photo-electric charge, generated in the PGPd element can be approximated as:

$$Q_{gen} = I_{ph} \cdot T_{gen} = I_{ph} \cdot \left(T_{frame} / N_{row} - T_{readout}\right) \tag{6}$$

where T_{frame} is the frame time and N_{row} is the number of rows in the APS array.

For proper SPS operation, ΔQ_{TOT}, required during the $T_{readout}$ phase, should be smaller than Q_{gen}. Equating (4) and (6) leads to the expression for PGPd required area, A:

$$A \geq \frac{\Delta Q_{V_{LN}} + \Delta Q_C}{q \cdot \Phi \cdot \eta \cdot \left(T_{frame} / N_{row} - T_{readout}\right)} \tag{7}$$

The drop in the V_{DD}' during the $T_{readout}$ phase is given by:

$$V_{drop} = \frac{\Delta Q_{V_{LN}} + \Delta Q_C}{A \cdot C_j(V_{DD}')} \tag{8}$$

where $C_j(V_{DD}')$ is the space-charge capacitance of the PGPd elements and in case of abrupt junction is defined as:

$$C_j(V_{DD}') = \sqrt{\frac{q\varepsilon_s}{2\left(V_{bi} - \left[V_{DD}' - V_{DD}\right]\right)} \frac{N_A N_D}{N_A + N_D}} \tag{9}$$

where ε_s is the permittivity of silicon, V_{bi} is the built-in voltage, N_D and N_D are the acceptors and donors concentrations, respectively.

Assuming the equality in (7), the equation (8) is reduced to:

$$V_{drop} = \frac{q \cdot \Phi \cdot \eta \cdot \left(T_{frame} / N_{row} - T_{readout}\right)}{C_j(V_{DD}')} = J_{ph} \frac{\left(T_{frame} / N_{row} - T_{readout}\right)}{C_j(V_{DD}')} \tag{10}$$

where J_{ph} is the photocurrent density.

As mentioned in Section II (see Fig. 2), the PGPd element is formed by the p+-Nwell junction. In a standard CMOS process, this structure provides relatively high depletion capacitance due to the high N_D concentration, resulting in smaller V_{drop}. Note, that there is no straightforward relation between V_{drop} and ΔV_{max}. While V_{drop} is defined by (8), ΔV_{max} is determined by the acceptable output swing of the APS.

IV. Illustrative Example in 0.18μm Process

An illustrative example of the SPS structure in 0.18μm process is depicted herein, based on the analysis presented in the previous Section. The QCIF APS array (176x120) operating at 30 frames per second at 1.8V is assumed. The parameter values listed in this sub-section are typical to 0.18μm process and will be utilized to illustrate the relevant expressions.

The total charge ΔQ_{TOT} dissipated during the $T_{readout}$ phase is obtained using (4) and is given by:

$$\Delta Q_{tot} = \Delta Q_C + \Delta Q_{V_{LN}} = 96p\ [Col] + 23p\ [Col] \cong 120p\ [Col] \tag{11}$$

assuming $T_{readout}$ = 250nsec, I_{LN} = 0.75uA, where $C_S = C_R$ = 0.4pF and V_{swing}=1V.

The photocurrent density is calculated using (5):

$$J_{ph} = q \cdot \Phi \cdot \eta \cong 2\mu\left[A/cm^2\right] \tag{12}$$

where η=0.3 for typical p^+/n-well junction and Φ=4x10^{13} [ph/cm^{2}sec]. Note, room light flux and clear sky flux correspond to Φ=4x10^{12} and Φ=4x10^{15}, respectively.
The required area of the PGPd element according to (7) is:

$$A \geq \frac{\Delta Q_{V_{LN}} + \Delta Q_C}{q \cdot \Phi \cdot \eta \cdot \left(T_{frame} / N_{row} - T_{readout}\right)} = 0.35 \left[cm^2\right] \quad (13)$$

According to (8) and (9) the V_{drop} voltage is:

$$V_{drop} = J_{ph} \frac{\left(T_{frame} / N_{row} - T_{readout}\right)}{C_j(V_{DD}')} \cong 7.9m \left[V\right] \quad (14)$$

where C_j=43n [F/cm^2] and V_{bi}≈0.9V were obtained using N_A=2x10^{18} [cm^{-3}] and N_D=2x10^{16} [cm^{-3}] which are typical values for 0.18μm process (the reversed voltage was neglected). Note, the edge capacitance of the PGPd element can be neglectible, relatively to $A \cdot C_j$.

According to (13) the active area required for a proper operation of the whole QCIF SPS structure and the readout circuitry at the given illumination level and without need in a conventional power supply is 0.35 cm^2. As mentioned in [16], this can be significantly reduced in applications, where small regions of interests are processed. In these applications the required area of the PGPd element is reduced by factor of M, showed in the following expression:

$$M = \frac{N_{row} \cdot N_{col}}{X \cdot Y} \quad (15)$$

where X and Y are the number of rows and columns in the region of interest, respectively. For example, for the region of 10x15 the required area is only 0.24mm^2.

V. Test Chip Measurements

A test chip, consisting of 7x7 SPS array, was implemented in a standard TSMC 0.18μm CMOS technology. Figure 6 shows the layout of 14μmx14μm single SPS pixel with an in-pixel PGPd. The pixel employs a standard n^+/p-sub photodiode, as a sensing element, similarly to the pixel shown in Fig. 1. The sizes of the photodiode and each PGPd element are approximately 14 μm^2 and 60 μm^2, respectively.

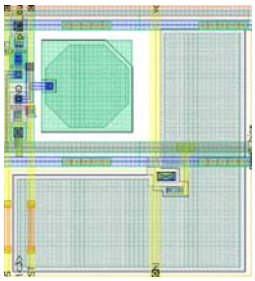

Figure 6. Layout of a single SPS pixel

A variety of tests were carried out to prove the SPS concept. The electrical scheme of the fabricated circuit, including additional elements for testing is shown Fig. 7. This figure shows the pixels 1, *k* and 7 (out of 7) of a single row. As mentioned before, all PGPd elements are connected to the power generated V_{DD}' line. The 'Reset' and 'RS' lines are common for each row. The PGPd elements can be reset to ground using the 'PGPd reset' line via NMOS transistor. Because of relatively large capacitance of all PGPd elements, the 'PGPd reset' transistor is implemented using a number of transistors, connected in parallel, to allow fast reset of PGPd element. The voltage value on the PGPd elements is buffered using four simple source follower amplifiers. That is, the signal value on the PGPd element is represented by two output voltages: V_{out1} and V_{out2}. While the output swing of V_{out1} is limited to the range of approximately 0.7V to 1.8V, the voltage value of V_{out2} is varying between 0V to 1V. These two output chains allow the representation of the full swing of the output voltage. The reason to use these two source amplifiers instead of one rail-to-rail amplifier was due to their simplicity and thus risk of fault reduction. The first two amplifiers (employing V_{bias1} and V_{bias2}) have very low input capacitances to reduce the influence of the test circuitry on the SPS operation. The other two buffers (employing V_{bias3} and V_{bias4}) are sized to drive the off-chip loads.

Fig. 8 shows the measurements of PGPd elements charge at low illumination conditions. In this test, all pixels were disconnected from the V_{DD}' line. As can be seen, after the PGPd elements are reset to ground (the reset operation is performed every 30msec), all PGPd elements are situated in the open circuits configuration and linearly charged. As expected, the PGPd voltage value is increased from 0V to 1.8V in 30msec (can be observed in Fig. 8 by the combination of V_{out1} and V_{out2}.), providing charge for SPS self-power capability. The same test was also applied at different illumination levels (e.g. room light, clear sky and laser beam) and as expected, the time required to charge the PGPd elements to V_{DD} was decreased linearly with the increasing of illumination level.

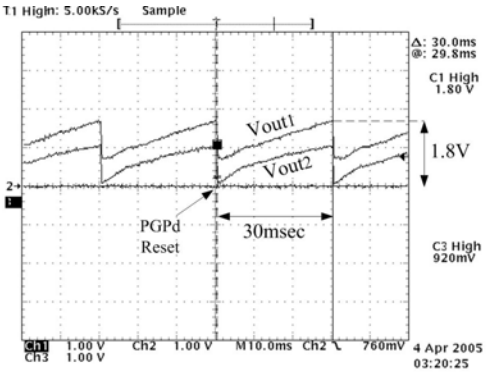

Figure 8. Measurement of the PGPd elements charging at low illumination conditions.

An additional test, examining SPS operation, is presented in Fig. 9. In this test two phases can be clearly distinguished, i.e. T_1 and T_2. During the first phase (T_1), both PGPd and photodiodes are disconnected each from other (all Reset transistors from Fig. 7 are off) and exposed to incident illumination. During T_1, the PGPd elements are charged to V_{DD} (V_{out1} in Fig. 9) and on the other hand, the voltage value of the APS photodiodes is zero. From the beginning of the T_2, the SPS array is situated in dark conditions and the Reset transistors turn on in the rolling shutter fashion [17]. As can be observed, the voltage on the PGPd elements is declined according to charge sharing between the PGPd overall capacitance and the total capacitance of the APS *i* row (including the photodiodes capacitance and the parasitics associated with that node). The total voltage drop in the PGPd elements is 450mV (out of 1.8V) which is approximately the relation between the APS photodiodes and PGPd capacitances.

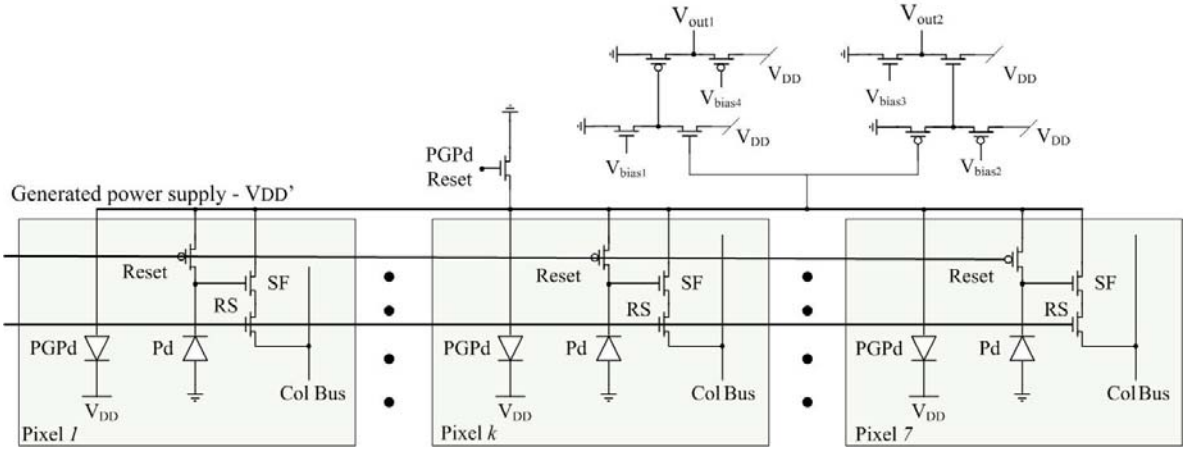

Figure 7. The electrical scheme of the fabricated circuit, including additional elements for testing.

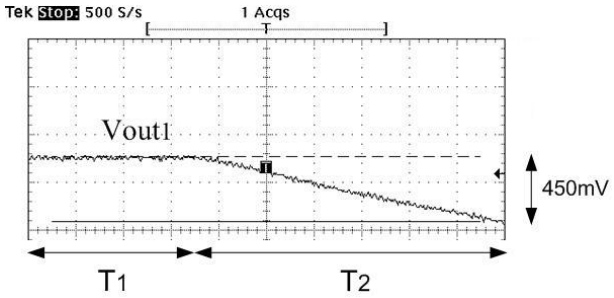

Figure 9. Measurement of the charge sharing between the PGPd overall capacitance and the total capacitance of the APS *i-th* row

VI. Conclusions and Further Research

Considerations for CMOS image sensors with self-power generation capability design were presented. A detailed quantitative and qualitative discussion was carried out successfully demonstrated, that the proposed SPS architecture allows generation of electric power for the whole APS array and signal readout circuitry operation. This makes image sensors using the SPS architecture very useful in applications where ultra low-power is the main demand. A test chip, consisting of 7x7 SPS array, was designed in a standard TSMC 0.18µm CMOS and the measurements results support the SPS concept and the theoretical analysis.

Further work should be concentrated on the improving of the PGPd elements efficiency in order to reduce the demand for die area. In addition, large APS array with full self-power generation capability will be designed.

References

[1] C. Xu, W. Zhang, W. Ki and M. Chan, "A 1.0-V VDD CMOS Active-Pixel Sensor With Complementary Pixel Architecture and Pulsewidth Modulation Fabricated With a 0.25µm CMOS Process", IEEE Journal of Solid State Circuits, Vol. 37, NO. 12, June 2002.

[2] H. S. Wong, R. T. Chang, E. Crabbé, and P. D. Agneelo, "CMOS active pixel image sensors fabricated using a 1.8V, 0.25µm CMOS technology," IEEE Trans. Electron Device, vol. 45, pp. 889–894, 1998.

[3] K. B. Cho, A. Krymski, and E. R. Fossum, "A 1.2V micropower CMOS active pixel image sensor for portable applications," in IEEE Int. Solid state Circuit Conf., Dig., Feb. 2000, pp. 114–115.

[4] C. Xu, W. Zhang, and M. Chan, "A low voltage hybrid bulk/SOI CMOS active pixel image sensor," IEEE Electron Device Lett., vol. 22, pp. 248–250, 2001.

[5] S. Y. Ma and L.-G. Chen, "A single-chip CMOS APS camera with direct frame difference output," IEEE J. Solid-State Circuits, vol. 34, pp. 1415–1418, Oct. 1999.

[6] M. Ansorge, S. Tanner, X. Shi, J. Bracamonte, J. L. Nagel, P. Stadelmann, F. Pellandini, P. Seitz, N. Blanc, "Smart Low-Power CMOS Cameras for 3G Mobile Communicators", Invited paper, IEEE International Conf. on Circuits and Systems for Communications (ICCSC 2002), June 26-28, 2002, St-Petersburg, Russia.

[7] C. Shen, C. Xu, W. Zhang, R. Huang, and M. Chan, "Low Voltage CMOS Active Pixel Sensor Design Methodology With Device Scaling Considerations", IEEE Hong Kong Electron Devices Meeting Proceedings, pp. 21-24, June 30, 2001, Hong Kong.

[8] X. Zheng, G. Yang, C. Wrigley, and B. Pain, "High responsivity CMOS imager pixel implemented in SOI technology," Proc. 2000 IEEE Int. SOI Conf., pp. 138–139, Oct. 2–5, 2000.

[9] G. Shahidi, A. Ajmera, F. Assaderaghi, R. Bolam, A. Bryant, M. Coffey, H. Hovel, J. Lasky, E. Leobandung, H.-S. Lo, M. Maloney, D. Moy, W. Rausch, D. Sadana, D. Schepis, M. Sherony, J.W. Sleight, L. F.Wagner, K. Wu, B. Davari, and T. C. Chen, "Mainstreaming of the SOI technology," in Proc. IEEE Int. SOI Conf., Oct. 1999, pp. 1–4.

[10] W. Fang, G. Yang, B, Pain and B. J. Sheu, "A Low Power Smart Vision System Based on Active Pixel Sensor Integrated with Programmable Neural Processor", Proc. ICCD, pp. 429-434, 1997.

[11] L. G. McIlrath, "A Low-Power Low-Noise Ultrawide-Dynamic-Range CMOS Imager with Pixel-Parallel A/D Conversion", IEEE J. Solid-State Circuits, vol. 36, no.5, pp.846-853, May. 2001.

[12] C. Xu, W. Ki and M. Chan, "A Low-Voltage CMOS Complementary Active Pixel Sensor (CAPS) Fabricated Using a 0.25µm CMOS Technology", IEEE Trans. on Electron Devices, Special Issue on Image Sensors, vol. 23, no. 7, pp.398-400, July 2002.

[13] K. Cho, A. I. Krymski, and E.R. Fossum, "A 1.5-V 550µW 176 x 144 autonomous CMOS active pixel image sensor", IEEE Trans. on Electron Devices, Special Issue on Image Sensors, vol. 50, pp.96-105, January, 2003.

[14] A. Fish, A. Belenky and O. Yadid-Pecht, "Low Power Global Shutter CMOS Active Pixel Image Sensor with Ultra-High Dynamic Range", submitted to IEEE Journal on Circuits and Systems II, October 2004.

[15] R. M. Philipp and R. Etienne-Cummings, "A 1V Current-Mode CMOS Active Pixel Sensor," Proc. IEEE ISCAS'05, pp. 4771-4773, Kobe, Japan, May 2005.

[16] A. Fish, S. Hamami and O. Yadid-Pecht, "Self-Powered Active Pixel Sensors for Ultra Low-Power Applications", Proc. IEEE ISCAS'05, pp. 5310-5313, Kobe, Japan, May 2005.

[17] O. Yadid-Pecht and R. Etienne-Cummings, " CMOS imagers: from phototransduction to image processing", Kluwer Academic Publishers

[18] Z. Chen, L. Wei, K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks, " Proceedings of the International Symposium on Low Power Electronics and Design, pp. 239-244, 1998.

[19] S. Mendis, S. Kemeny, R Gee, B. Pain, C. Staller, Q. Kim and E. Fossum, "CMOS active pixel image sensors for highly integrated imaging systems," IEEE J. Solid State Circuits, vol. 32, pp. 187-197, Feb. 1997.