B. P. PODDAR INSTITUTE OF MANAGEMENT & TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
ACADEMIC YEAR: 2018-2019 ODD SEMESTER
Analog and Digital Electronics (CS301)
COURSE OUTCOME

	Course Outcomes	Cognitive Level
CO1	**Explain** the difference between analog and digital systems, logic gates and number representations, different weighted and non weighted codes	Understand
CO2	**Describe** and **illustrate** the basic postulates of Boolean algebra and simplification of K maps and solve related problems	apply
CO3	**Define** the outline of formal procedures and **compare** different digital components like multiplexers, flip flops, decoders, adders.	Analyze
CO4	**Discuss** the difference between combinational and sequential circuits and **Design** registers and counters.	create
CO5	**Recall** transistors, basic OPAMP circuits and **explain** the concept of feedback, logic families and A/D, D/A converter.	Understand
CO6	**Evaluate** AND, OR, XOR gates in different sequential and combinational circuits to get minimum number of gate delays.	evaluate

CO-PO-PSO Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CS301.CO1	1		2									1		1
CS301.CO2	2	2	3	2								2		2
CS301.CO3	2	2	3	2								3		2
CS301.CO4	2	3	3	2								3		2
CS301.CO5	2	2	3	2								2		2
CS301.CO6	2	3	3	3								3		2
CS301	1.8	2	2.8	1.8								2.33		1.8

Prepared by

Ayesha Ali

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LESSON PLAN

Lecture No.	Topics to be covered	Teaching Aids	Books
1	Binary Number System & Boolean Algebra (recapitulation)	BB	T1
2	BCD, ASCII, EBDIC, Gray codes and their conversions .	BB	T1
3.	Signed binary number representation with 1's and 2's complement methods	BB	R1
4.	Binary arithmetic, Venn diagram, Boolean algebra (recapitulation)	BB	R1
5.	Representation in SOP and POS forms	BB	T1
6.	Minimization of logic expressions by algebraic method.	BB	T1
7.	Minimization of logic expressions by algebraic method continued	BB	T1
8.	K Map method to simplify expressions	PPT	R1,W1
9.	Solving problems on K Map technique	BB	R1,W1
10	Adder and Subtractor circuits (half & full adder)	BB PPT	T1
11	Adder and Subtractor circuits (half & full subtractor) continued	BB	T1
12	Encoder, Decoder, Comparator, Multiplexer	BB	T1
13	De-Multiplexer and Parity Generator, Hamming code	PPT	T1
14	Basic Flip-flop & Latch	BB	T1
15	Flip-flops -SR, JK	BB	T1
17	Flip-flops -Master-slave Flip Flops, Mealy and Moore state machine	PPT	T1,R1
18	Registers (SISO,SIPO)	BB	T1
19	Registers (PIPO,PISO)	BB	T1,R1
20	Ring counter,Johnson counter	PPT, BB	T1,R1
21	Universal shift register	PPT, BB	T1
22	Basic concept of Synchronous and Asynchronous counters	BB	T1,R1
23	Basic concept of Synchronous and Asynchronous counters continued	BB	T1,R1
24	Design of Mod N Counter	BB	T1,R1
25	Design of Mod N Counter continued	BB	T1,R1

26	A/D and D/A conversion techniques – Basic concepts	BB	T1,R1
27	D/A :R-2-R only A/D	BB	W1,T1
28	Successive approximation	BB	W1,T1
29	Logic families- TTL, ECL - basic concepts.	PPT	T1,W2
30	Logic families- MOS and CMOS - basic concepts.	PPT	T1,W2
31	Different Classes of Amplifiers - (Class-A, B, AB and C)	PPT	T2
32	basic concepts, power, efficiency of different amplifiers	PPT	T2
33	Recapitulation of basic concepts of Feedback and Oscillation	BB	T2
34	Phase Shift	BB	T2
35	Wein Bridge oscillators	PPT	T2
36	Astable & Monostable Multivibrators	BB PPT	T2
37	Schimtt Trigger circuits	BB	T2
38	555 Timer	BB	T2
39	Solving questions on amplifier	BB	Illustration by example, Problem Solving
40	Discussions on last year question papers	BB	Problem Solving

Required Text Books:

T1.S.Salivahanan, A.Arivaszhagan- Digital Circuit design

T2.D.Chattopadhyay,P.C.Rakshit-Electronics Fundamental and application

Required Reference Books:

R1.Morris M.Mano- Digital Logic and Computer design

Web resources

W1.http://nptel.ac.in/courses/117103064/

W2.https://www.slideshare.net/dheeruee/analog-and-digital-electronics-by-u-a-bakshi

W3.https://www.tutorialspoint.com/digital_circuits/index.htm

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GAP IN AND BEYOND SYLLABUS

Gap in the Syllabus

Sl. No	Course Code	Course Name	Faculty Name	**Topic**	**PO**	**CO**	**PSO**
1	**CS 301**	Analog and Digital Electronics	Ayesha Ali	**Universal Shift register**	**PO1, PO2 PO3**	**CO1,CO3**	**PSO2**

Gap beyond the Syllabus

Sl. No	Course Code	Course Name	Faculty Name	**Topic**	**PO**	**PSO**
1	**CS 301**	Analog and Digital Electronics	Ayesha Ali	**Hamming code(error detection)**	**PO1, PO2, PO3**	**PSO2**

Gap beyond syllabus:

- https://www.slideshare.net/ibrar562/error-correction-and-hamming-code-ibrar
- https://www.tutorialspoint.com/digital_electronics/error_correction_in_hamming_code.asp
- https://nptel.ac.in/courses/106105080/pdf/M3L2.pdf
- https://users.math.msu.edu/users/jhall/classes/codenotes/Hamming.pdf

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Gaps addressed by a resource person/Teaching Methodology - document

Gaps	Resource Person	Document
Gaps within the syllabus	Ayesha Ali	Gaps included in COs (CS301.1, CS301.3) Lecture 21 included in Lesson Plan to address relevant teaching learning and assessed through Assignments towards fulfilment of Gaps within the syllabus Document addressing gaps is included in Lesson Plan w.r.t Textbooks/References: 1.S.Salivahanan, A.Arivaszhagan- Digital Circuit design 2.Morris M.Mano- Digital Logic and Computer design Available at- http://nptel.ac.in/courses/117103064/
Gaps outside the syllabus	Not Applicable (Addressed via web resources)	https://www.slideshare.net/ibrar562/error-correction-and-hamming-code-ibrar https://www.tutorialspoint.com/digital_electronics/error_correction_in_hamming_code.asp Data Communication and Networking by Behrouz A. Forouzan Error Detection and Correction in the International Standard Book Number by Peter Waweru Kamaku

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ACADEMIC YEAR: 2018-2019 ODD SEMESTER
BRIGHT Students SUMMARY

Course Name: ANALOG AND DIGITAL ELECTRONICS (CS 301)
Course code: CS301
Academic year: 2018-2019
Program: CSE Section: B Year: 2nd

Name of the faculty: Ayesha Ali

LIST OF BRIGHT STUDENTS [1ST LIST].

Serial Number	Roll Number	Name
1	11500117028	Trisha Maji
2	11500117032	Supriti Atha
3	11500117044	Soumyadeep Paul
4	11500117047	Shreyasi Ghosh
5	11500117055	Satyaki Sen
6	11500117060	Sanah Asgar
7	11500117061	Samyadeep Bhowmick
8	11500117062	Samidha Singhi
9	11500117076	Rahul Lohia
10	11500117080	Preeti Jha

% of students : 17%

Parameter-1: SGPA above 8.0

Parameter-2: Class performance

Parameter 3: Class test mark

Bright student engagement plan :

1.Sharing the question bank and study material for GATE and other competitive exams.

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BRIGHT Students SUMMARY

Course Name: ANALOG AND DIGITAL ELECTRONICS (CS 301)
Course code: CS301
Academic year: 2018-2019
Program: CSE Section: B Year: 2nd

Name of the faculty: Ayesha Ali
LIST OF BRIGHT STUDENTS [2ND LIST].

**Parameter selection: Considering performance in class and attendance, students have been put in this list.

Serial Number	Roll Number	Name
1	11500117030	Tathagata Jana
2	11500117061	Samyadeep Bhowmick
3	11500117062	Samidha Singhi
4	11500117038	Subhadeep Bandyopadhyay
5	11500117044	Soumyadeep Paul
6	11500117077	Punit Khandelwal
7	11500117026	Upasana Bit
8	11500117047	Shreyasi Ghosh
9	11500117073	Rajsekhar Roy Chowdhury
10	11500117057	Saronee Das
11	11500117032	Supriti Atha

% of students : 19%

Bright student engagement plan :

1. Giving some advanced level problems to solve.
2.Sharing the question bank and study material for GATE and other competitive example

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BRIGHT Students SUMMARY

Course Name: ANALOG AND DIGITAL ELECTRONICS (CS 301)
Course code: CS301
Academic year: 2018-2019
Program: CSE Section: B Year: 2nd

Name of the faculty: Ayesha Ali

LIST OF BRIGHT STUDENTS [3RD LIST].

**Parameter selection: 1st internal Test Result

Serial Number	Roll Number	Name
1	11500117030	Tathagata Jana
2	11500117041	Sreeja Paul
3	11500117061	Samyadeep Bhowmick
4	11500117044	Soumyadeep Paul
5	11500117060	Sanah Asgar
6	11500117062	Samidha Singhi
7	11500117034	Sudip Kumar Jha
8	11500117057	Saronee Das
9	11500117026	Upasana Bit
10	11500117032	Supriti Atha
11	11500117052	Sayantan Singha
12	11500117047	Shreyasi Ghosh

% of students : 20%

Prepared by

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ASSIGNMENT CS301

OUTCOME BASED EDUCATION (OBE)

Question No.	Knowledge Domain	COs
1,3,	Create	CO 3
2,7	Apply	CO 2
4	Analyze	CO 1, CO 3
5,6,8	Create	CO 2,CO 4
9,10	Analyze	CO 2,CO 3

1. Design a SR flip flop using a NAND gate, and construct the corresponding characteristic and excitation table.
2. Minimize the function:

   f (A,B,C,D) = ∑m(4,8,10,11,12,15) + Ɛ(9,14)

3. Design a JK flip flop using a NOR gate, and find the expression of J and K respectively.
4. Design an OR and a XOR gate from 2:1 MUX
5. Design a circuit to generate odd parity if the data is represented with 4 bits and construct the corresponding K-Map to obtain the simplified expression.
6. Design a 1-bit full adder with two half adders and minimum number of additional gates
7. Use Boolean Algebra to show that A'BC'+AB'C'+AB'C+ABC'+ ABC = A+BC'
8. Implement a Full Subtractor using a 3 to 8 Decoder
9. Implement the following function with 8x1 multiplexer. F(A,B,C,D) = Σ(0,1,3,4,8,9,15) with A,B,C connected to S0, S1, S2 respectively.
10. Find the Boolean function that a 8x1 multiplexer implement with A,B,C connected to select lines S2,S1,S0 respectively, if I0=0, I1=D, I2=0, I3=D‟, I4=I5=D, I6=0, I7=1

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ASSIGNMENT CS301

OUTCOME BASED EDUCATION (OBE)

Question No.	Knowledge Domain	COs
1,4,8	Understand	CO 5
2	Understand	CO 1
3,6,7,9	Analyze	CO 2, CO 3
5	Create	CO 4
10	Evaluate	CO 6

1. What do you mean by power amplifier? Explain the working of Class B push pull amplifier ?
2. Explain grey code. Why is grey code called reflected code?
3. Implement the following Boolean function using a single 4 to 1 Multiplexer.
   F (A,B,C,D) = Σ m (0, 1, 2, 4, 6, 9, 12, 14)
4. Explain A/D converter. What is the advantage of R-2R type D/A converter over any other type of D/A converter.
5. Explain the working of a ring counter with timing diagram.
6. Design and implement a comparator circuit that compares 3 two bit binary numbers.
7. Derive SR flip flop from JK flip flop. Construct the master-slave flip flop. Why is it so called ?
8. Explain and draw the Schmitt trigger circuit.
9. Write a short note on Priority encoder and parity generator.
10. Design a 1-bit full adder with two half adders and minimum number of additional gates

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QUIZ

OUTCOME BASED EDUCATION (OBE)

Question No.	Knowledge Domain	COs
1,5	Create	CO 4, CO 1
2	Analyze	CO 3, CO 2
3	Create	CO 4
4	Evaluate	CO 6

1. The terminal count of a modulus-11 binary counter is _____. 1

A. 1010

B. 1000

C. 1001

D. 1100

2. Convert SR Flip flop to T flip flop. Show proper steps and the final circuit diagram. 3
3. Construct the block diagram and timing diagram of a 3-bit up Ripple counter. 2

4. How many flip-flops are required to make a MOD-32 binary counter? 1

A. 3

B. 45

C. 5

D. 6

5. Construct a MOD-12 counter from MOD-16 counter. 3