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Final Year Projects Handbook

(An easy guide to understanding projects)

You learn more quickly under the guidance of experienced teachers. You waste a lot of time going down blind alleys if you have no one to lead you.
- W. Somerset Maugham

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IEEE

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About CodeBytes

CodeBytes is the profit based Research & Development Company, catering to the development and research for wide range of computational applications in the field of business solutions, embedded developments, technology developments, entertainment software, retail and transport , construction, telecom & satellite. Having an experienced manpower, who have an expertise in respective fields, CodeBytes provides the consultancy in technology based solutions in order to achieve automated , unbiased , reliable processes.

Academic Project Consultancy

CodeBytes offers consultancy in academic projects for the advanced topics. Research and industrial projects available for B.E. ,B.Tech, M.E. ,M.Tech, Ph.D, M.Phil ,Msc, MCA, BSc and Polytechnic students of Computer, Electrical ,Electronics, IT, Telecom, Instrumentation branches.Some of the areas in which we provide projects are:

* Image Processing & computer vision
* Multimedia Codec, Processing & Transmission
* Neural Network, Fuzzy Logic , AI and GA
* Web-Technology
* Embedded applications: VLSI, RTOS, DSP Processor
* Network and Security,Sensor Network, Ad-hoc Network
* Communication and Wireless Technologies
* Instrumentation, Virtual Instrumentation & Data Acquisition
* Digital Signal Processing, Speech Coding and Recognition
* Data Warehousing and Data Mining
* Hardware, Firmware, PCB based Implementation
* Electrical & Power Electronics
* Robotics and Imaging
* Java Technologies (J2SE,J2EE ,J2ME,AJAX,JSP, Servlets,etc)
* VLSI- VHDL, NS2 ,RTOS
* VC++, COM, DCOM
* VB .NET, C#.NET, ASP.NET

We provide implementation of research papers from reputed journals and conference proceedings like IEEE, EURASIP , IEE etc.

CODE	IEEE TRANSACTION ON VLSI	YEAR	E09VL32	VLSI Design & Implementation of Encryption & Decryption using VHDL	2009
E09VL01	Low-Power Programmable FPGA Routing Circuitry	2009	E09VL33	VLSI Design & Implementation of Bus Arbiter using VHDL	2009
E09VL02	Predictive-Flow-Queue-Based Energy Optimization for Gigabit Ethernet Controllers	2009	E09VL34	VLSI Design & Implementation of Data Routing Multiplexer using VHDL	2009
E09VL03	Design and Implementation of a Field Programmable CRC Circuit Architecture	2009	E09VL35	VLSI Design & Implementation of DMA using VHDL	2009
E09VL04	A Low Power JPEG2000 Encoder With Iterative and Fault Tolerant Error Concealment	2009	E09VL36	VLSI Design & Implementation of Water Pump Controller using VHDL	2009
E09VL05	An Area-Efficient Universal Cryptography Processor for Smart Cards	2009	E09VL37	VLSI Design & Implementation of Associate Memory using VHDL	2009
E09VL06	The CSI Multimedia Architecture	2009	E09VL38	VLSI Design & Implementation of I2c Controller Core	2009
E09VL07	FPGA Based Power Efficient Channelizer for Software Defined Radio	2009	E09VL39	VLSI Design & Implementation of Stepper Motor Controller	2009
E09VL08	Improvement of the Orthogonal Code Convolution Capabilities using FPGA	2009	E09VL40	VLSI Design & Implementation of Basic RSA Encryption Engine	2009
E09VL09	A VHDL Model of a IEEE1451.2 Smart Sensor: Characterization and Applications	2008	E09VL41	VLSI Design & Implementation of Basic Des Crypto Core	2009
E09VL10	Fuzzy based PID Controller using VHDL/VERILOG for Transportation Application	2008	E09VL42	VLSI Design & Implementation of Fuzzy Controller Design	2009
E09VL11	Implementation of IEEE 802.11 a WLAN baseband Processor	2008	E09VL43	Optimized Software Implementation of a Full-Rate IEEE 802.11a	2009
E09VL12	A Lossless Data Compression and Decompression Algorithm and its Hardware	2008	E09VL44	VLSI Design & Implementation of Fir & Lir Designing	2009
E09VL13	A Verilog Implementation of UART Design with Bist Capability	2008	E09VL45	VLSI Design & Implementation of Home Appliances Control Designing	2009
E09VL14	A Robust Uart Architecture based on Recursive Running Sum Filter for Better Noise	2008	E09VL46	VLSI Design & Implementation of Electronic Voting Machine	2009
E09VL15	FPGA Implementation of USB Transceiver Macrocell Interface with Usb2.0 Specifications	2009	E09VL47	VLSI Design & Implementation of Security System	2009
E09VL16	A VLSI Architecture for Visible Watermarking In A Secure Still Digital Camera (S2dc) Design	2009	E09VL48	VLSI Design & Implementation of Robot Controller	2009
E09VL17	A Low-Power Multiplier with the Spurious Power Suppression Technique	2009	E09VL49	VLSI Design & Implementation of Solar Panel Control	2009
E09VL18	Design of Reconfigurable Coprocessor for Communication Systems	2009	E09VL50	VLSI Based Temperature Controller Implementation	2009
E09VL19	Block-Based Multiperiod Dynamic Memory Design for Low Data- Retention Power	2009	E09VL51	VLSI Based Motor Speed Controller	2009
E09VL20	A Symbol-Rate Timing Synchronization Method for Low Power Wireless OFDM Systems	2009	E09VL52	Designing of Risc Controller using Verilog Hdl	2009
E09VL21	On the Design of a Multi-Mode Receive Digital-Front-End for Cellular Terminal RFICS	2009	E09VL53	Designing of I2c Master Core / Spi Master Core using Verilog Hdl	2009
E09VL22	Design Exploration of a Spurious Power Suppression Technique (SPST) and its	2009	E09VL54	Designing of Pc Printer Port / Serial Port using Verilog Hdl	2009
E09VL23	Implementation of a Multi-Channel UART Controller based on FIFO Technique and FPGA	2009	E09VL55	Designing of Programmable Peripheral Interface (Ppi) using Verilog Hdl	2009
E09VL24	Compliant Digital Baseband Transmitter on a Digital Signal Processor	2009	E09VL56	Designing of Programmable Timer Interface (Pti) using Verilog Hdl	2009
E09VL25	An FPGA-Based Architecture for Real Time Image Feature Extraction	2009	E09VL57	Designing of Universal Sync / Async Receiver and Transmitter (Usart)	2009
E09VL26	FPGA based Generation of High Frequency Carrier for Pulse Compression Using Cordic	2009	E09VL58	Design of Industrial PLC	2009
E09VL27	VLSI Architecture and FPGA Prototyping of a Digital Camera for Image Security and	2009	E09VL59	Design of Industrial Robot	2009
E09VL28	VLSI Design & Implementation of Cellphone Controller using VHDL	2009	E09VL60	Design and Implementation of Elevator Controller	2009
E09VL29	VLSI Design & Implementation of Code Converters using VHDL	2009	E09VL61	Design and Implementation of Traffic Light Controller	2009
E09VL30	VLSI Design & Implementation of Electronic Automation using VHDL	2009	E09VL62	Implementation of Data Link Layer Receiver in PCI Express	2009
E09VL31	VLSI Design & Implementation of Arithmetic Logic Unit using VHDL	2009	E09VL63	Implementation of Data Link Layer Transmitter in PCI Express	2009

E09VL64	Matrix Multiplication Synthesis	2009	E09VL96	Hardware Algorithm for Variable Precision Multiplication on FPGA	2009
E09VL65	Implementation of a Multi-Coder Processor for the WTLS with High Compression Ratio	2009	E09VL97	Superscalar Power Efficient Fast Fourier Transform FFT Architecture	2009
E09VL66	VHDL Implementation of Cordic Algorithm for Wireless LAN	2009	E09VL98	A New High-Speed Architecture for Reed-Solomon Decoder	2009
E09VL67	Design and Simulation of Synchronization Unit for Wcdma Uplink Receiver	2009	E09VL99	Low-Power Leading-Zero Counting and Anticipation Logic for High-Speed Floating Point	2009
E09VL68	Design of a Simulator Tool for a Channel with Rayleigh Fading and Awgn Communication	2009	E09VL100	Cost-Efficient SHA Hardware Accelerators	2009
E09VL69	Emotion Recognition using Facial Expressions	2009	E09VL101	A Framework for Correction of Multi-Bit Soft Errors in L2 Caches based on Redundancy	2009
E09VL70	Design and Implementation of Arithmetic Logic Unit using VHDL	2009	E09VL102	Soft-Error Tolerance and Mitigation in Asynchronous Burst-Mode Circuits	2009
E09VL71	VLSI Design and Implementation of Associate Memory using VHDL	2009	E09VL103	Tag Overflow Buffering: Reducing Total Memory Energy by Reduced-Tag Matching	2009
E09VL72	VLSI Design and Implementation of Encoder & Decoder using VHDL	2009	E09VL104	On the Exploitation of Narrow-Width Values for Improving Register File Reliability	2009
E09VL73	VLSI Design and Implementation of Data Routing Multiplexer using VHDL	2009	E09VL105	Behavioral Synthesis of Asynchronous Circuits using Syntax Directed Translation as Backend	2009
E09VL74	VLSI Design and Implementation of Bus Arbiter using VHDL	2009	E09VL106	Fault Secure Encoder and Decoder for Nano-Memory Applications	2009
E09VL75	VLSI Design and Implementation of Code Convertors using VHDL	2009	E09VL107	Novel Area-Efficient FPGA Architectures for Fir Filtering With Symmetric Signal	2009
E09VL76	VLSI Design & Implementation of Electronic Automation using VHDL	2009	E09VL108	Custom Floating-Point Unit Generation for Embedded Systems	2009
E09VL77	VLSI Design and Implementation of Encryption & Decryption using VHDL	2009	E09VL109	Design and Synthesis of Programmable Logic Block with Mixed Lut and Macrogate	2009
E09VL78	VLSI Design and Implementation of Water Pump Controller using VHDL	2009	E09VL110	Improving Error Tolerance for Multithreaded Register Files	2008
E09VL79	VLSI Design and Implementation of Cellphone Controller using VHDL	2009	E09VL111	Area-Efficient Arithmetic Expression Evaluation using Deeply Pipelined Floating Point Cores	2008
E09VL80	A Fast Hardware Approach for Approximate, Efficient Logarithm and Antilogarithm	2009	E09VL112	Design Of Reversible Finite Field Arithmetic Circuits with Error Detection	2008
E09VL81	VLSI Design of Diminished-One Modulo 2n + 1 Adder using Circular Carry Selection	2009	E09VL113	BZ-Fad: A Low-Power Low-Area Multiplier Based on Shift-and-Add Architecture	2009
E09VL82	The Design and FPGA Implementation of Gf(2^128) Multiplier for Ghash	2009	E09VL114	The Arise Approach for Extending Embedded Processors with Arbitrary Hardware Accelerators	2009
E09VL83	Bz-Fad: A Low-Power Low-Area Multiplier Based On Shift-and-Add Architecture	2009	E09VL115	Variation-Aware Low-Power Synthesis Methodology for Fixed-Point Fir Filters	2009
E09VL84	Novel Area-Efficient FPGA Architectures for Fir Filtering with Symmetric Signal Extension	2009	E09VL116	Low Power Design of Precomputation-Based Content-Addressable Memory	2008
E09VL85	Spread Spectrum Image Watermarking with Digital Design	2009	E09VL117	L-Cbf: A Low-Power, Fast Counting Bloom Filter Architecture using VHDL	2008
E09VL86	A Generalization of a Fast RNS Conversion for a New 4-Modulus Base	2009	E09VL118	Low-Power Leading-Zero Counting and Anticipation Logic for High-Speed Floating Point	2008
E09VL87	Left to Right Serial Multiplier for Large Numbers on FPGA	2009	E09VL119	Low Power Hardware Architecture for Vbsme using Pixel Truncation	2009
E09VL88	A Compact AES Encryption Core on Xilinx FPGA	2009	E09VL120	Asynchronous Protocol Converters for Two-Phase Delay-Insensitive Global Communication	2009
E09VL89	A Fast VLSI Design of Sms4 Cipher Based On Twisted BDD S-Box Architecture	2009	E09VL121	FPGA Implementation(S) of a Scalable Encryption Algorithm	2008
E09VL90	An improved RC6 algorithm with the same structure of encryption and decryption	2009	E09VL122	Design Of Advanced Encryption Standard Using VHDL	2008
E09VL91	A Novel Multiplexer Based Truncated Array Multiplier	2009	E09VL123	Bit-Swapping LFSR and Scan-Chain Ordering: A Novel Technique for Peak- and Average-Power	2009
E09VL92	A New Low Power Test Pattern Generator using A Variable-Length Ring Counter	2009	E09VL124	Low-Power Scan Testing for Test Data Compression Using A Routing-Driven Scan	2009
E09VL93	Power optimization of linear feedback shift Register (LFSR) for low power BIST	2009	E09VL125	Enhancement Of Fault Injection Techniques Based On The Modification Of VHDL Code	2008
E09VL94	Deviation-Based LFSR Reseeding for Test-Data Compression	2009	E09VL126	A Full-Adder-Based Methodology for the Design of Scaling Operation In Residue Number System	2008
E09VL95	Fault Secure Encoder and Decoder for Nano-memory Applications	2009	E09VL127	FPGA Implementation of Low Power Parallel Multiplier	2008

E09VL128	Designing Efficient Online Testable Reversible Adders with New Reversible Gate	2008	E09VL160	Compact Hardware Design Of Whirlpool Hashing Core	2006
E09VL129	Cost-Efficient SHA Hardware Accelerators	2008	E09VL161	Novel Technique For Peak- And Average-Power Reduction In Scan-Based Bist	2009
E09VL130	System Architecture and Implementation of MIMO Sphere Decoders On FPGA	2008	E09VL162	Compression Using A Routing-Driven Scan Architecture	2009
E09VL131	Design of Gps-Gsm Mobile Navigator	2009	E09VL163	Enhancement Of Fault Injection Techniques Based On The Modification Of Vhdl Code	2008
E09VL132	VISI Design of Des(Data Encryption Standard) Algorithm	2009	E09VL164	High Speed and Low Power FPGA Implementation of FIR Filter for DSP	IEEE 2009
E09VL133	Implementation Five - Stage Pipelined RISC Processor for Parallel Processing	2009	E09VL165	An Asynchronous Field-Programmable VLSI using LEDR/4-Phase-Dual-Rail Protocol	IEEE 2009
E09VL134	Design of MPLS Router and Opitmization of MPLS Path Restoration Technique using VLSI	2009	E09VL166	Design and FPGA Implementation of High Speed, Low Power Digital Up Converter for	IEEE 2009
E09VL135	Implementation Huffman Coding For Bit Stream Compression In Mpeg - 2	2009	E09VL167	Variation-Aware Low-Power Synthesis Methodology for Fixed-Point FIR Filters	IEEE 2009
E09VL136	Implementation of Hash Algorithm Used for Cryptography And Security	2009	E09VL168	A Fast Hardware Approach for Approximate, Efficient Logarithm and Antilogarithm	IEEE 2009
E09VL137	Implementation of Content Addressable Memory for Atm Applications	2009	E09VL169	Efficient Asynchronous Protocol Efficient Asynchronous Protocol Converters for Two	IEEE 2009
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E09VL140	VLSI Design Of Two Wire Serial EEPROM for Embedded Microcontrollers Specification	2009	E09VL172	81.6 GOPS Object Recognition Processor Based on a Memory-Centric NOC	IEEE 2009
E09VL141	High Definition (Hd) Tv Data Encoding and Decoding using Reed Solomon Code	2009	E09VL173	Low-Power, High-Speed Transceivers for Network-on-Chip Communication	IEEE 2009
E09VL142	Total Power Modeling in FPGAs Under Spatial Correlation	2009	E09VL174	Low-Power Programmable FPGA Routing Circuitry	IEEE 2009
E09VL143	Design And Synthesis Of Programmable Logic Block With Mixed Lut And Macrogate	2009	E09VL175	Design and Implementation of a Field Programmable CRC Circuit Architecture	IEEE 2009
E09VL144	Improving Error Tolerance For Multithreaded Register Files	2008	E09VL176	Scalable Multi-Input–Multi-Output Queues With Application to Variation-Tolerant Architectures	IEEE 2009
E09VL145	Design Of Reversible Finite Field Arithmetic Circuits With Error Detection	2008	E09VL177	Fault Secure Encoder and Decoder for Nano Memory Applications	IEEE 2009
E09VL146	Register For Phase Difference Based Logic	2007	E09VL178	A Low Power JPEG2000 Encoder With Iterative and Fault Tolerant Error Concealment	IEEE 2009
E09VL147	Designing Efficient Online Testable Reversible Adder With New Reversible Gate	2007	E09VL179	Multi-Gb/s LDPC Code Design and Implementation	IEEE 2009
E09VL148	Bz-Fad: A Low-Power Low-Area Multiplier Based On Shift-And-Add Architecture	2009	E09VL180	High-Throughput Layered LDPC Decoding Architecture	IEEE 2009
E09VL149	Processors With Arbitrary Hardware Accelerators	2009	E09VL181	Custom Floating-Point Unit Generation for Embedded Systems	IEEE 2009
E09VL150	Low Power Design Of Precomputation-Based Content-Addressable Memory	2008	E09VL182	An improved RC6 algorithm with the same structure of encryption and decryption	IEEE 2009
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E09VL152	Fpga Implementation Of Low Power Parallel Multiplier	2007	E09VL184	Superscalar Power Efficient Fast Fourier Transform FFT Architecture	IEEE 2009
E09VL153	A Low-Power Multiplier With The Spurious Power Suppression Technique	2007	E09VL185	A New High-Speed Architecture for Reed-Solomon Decoder	IEEE 2009
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E09VL158	Fpga Implementation(S) Of A Scalable Encryption Algorithm	2008	E09VL190	Research on Image Median Filtering Algorithm and Its FPGA Implementation	
E09VL159	Design Of Advanced Encryption Standard Using Vhdl	2008	E09VL191	FPGA/Soft-Processor Based Real-Time Object Tracking System	

E09VL192	Research on Image Median Filtering Algorithm and Its FPGA Implementation	
E09VL193	FPGA/Soft-Processor Based Real-Time Object Tracking System	
E09VL194	Fpga Implementation Of Low Power Parallel Multiplier	2007
E09VL195	Fpga Implementation(S) Of A Scalable Encryption Algorithm Using Vhdl	2008
E09VL196	Design And Implementation Of Aes Using Vhdl	2008
E09VL197	Rtl Design And Simulation Of Micro Controller In Hdl	
E09VL198	Hdl Implementation Of Error Detection And Correction Circuit	

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We at CodeBytes have evolved a unique practical methodology to give a real project experience to the students. CodeBytes with its understanding of the academic requirement and the expertise gained though implementing the projects over last six years offers industry relevant real time projects to the final year students in IT field, which are executed in the simulated development environment of CodeBytes. The availability of essential tools, software and hardware combined with the able guidance gives the learners all the confidence and capabilities required to execute the projects in the industries in which they get employed.

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