fedora ELECTRONIC LAB

The Fedora Project is out front for you, leading the advancement of free, open software and content.

Community Leader in opensource EDA deployment.

# Empowers you with an advanced hardware design and simulation platform for micro-nano electronics engineering.

| Design/Model | Simulate | ASICs | Evaluation Boards |
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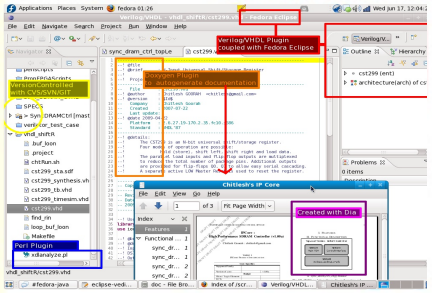
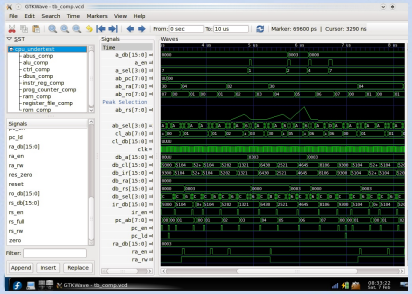
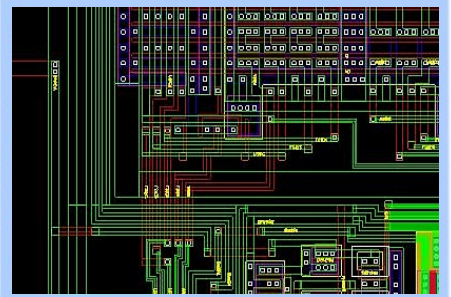
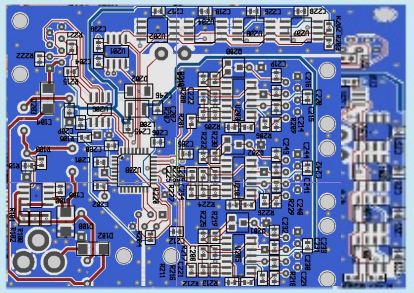
|  |  |  |  |

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fedora™
ELECTRONIC LAB

fedora

Proven community Leader in innovative opensource software development

FEL empowers you with a quality-class Linux distribution, coupled a matured EDA platform for your advanced electronic hardware design and simulation !

- Design tools for Application-Specific Integrated Circuit (ASIC) design flows.
- Extra standard cell libraries supporting upto a feature size of 0.13um.
- Interoperability between EDA packages to achieve different design flows.
- Collection of Perl modules is offered to extend Verilog and VHDL support.
- Collaborative development and code review methodologies.
- Tools for embedded/ARM design.

## History

Initiated 3 years ago by providing a handful set of design tools, now Fedora Electronic Lab is a matured design and simulation platform for Micro-Nano Electronics Engineering and Embedded Systems.

Fedora Electronic Lab, a subset of Fedora (with 15 million users around the world), is also available for free. FEL has already been adopted by many universities, engineers and startups.

## Design Tools

The software provided benefits both EDA engineers and ASIC designers engaged in chip design.

- Analog/Digital Circuit design and simulation
- Perl modules for CAD engineers
- Verification and Documentation
- Eclipse IDE for Embedded Systems Development
- Micro Controller Programming and Simulation

FEL also empowers your entreprise Linux distributions(CentOS-5/RHEL-5) with EPEL-5 repository.

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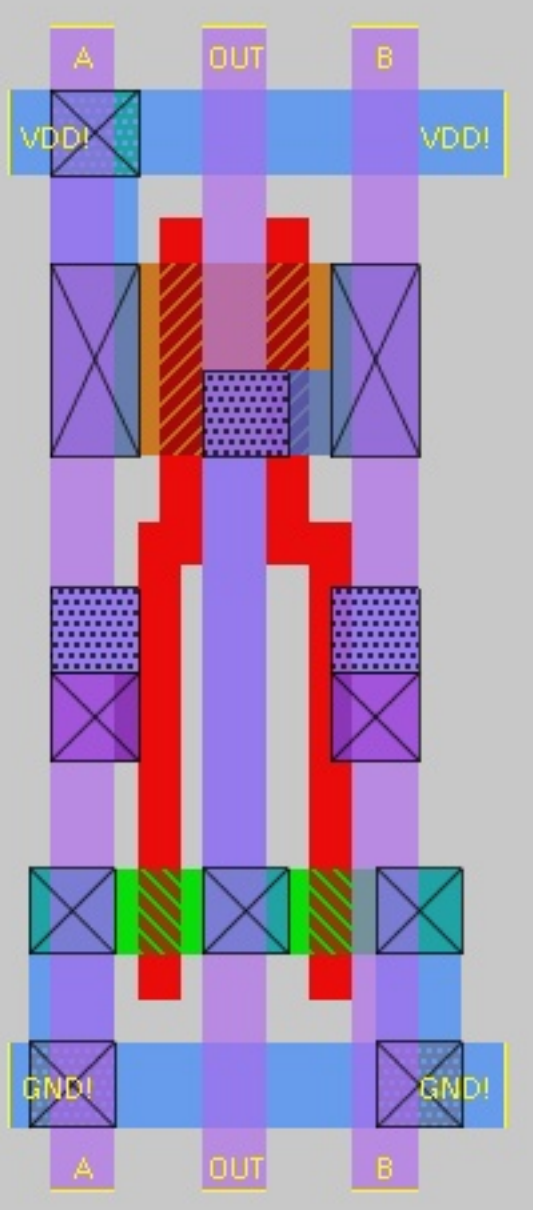



# VLSI Design Layout & Checks

Includes
- A continuous DRC that operates in background and maintains an up-to-date picture of violations.
- A hierarchical circuit extractor that only re-extracts portions of the circuit that have changed.
- Plowing that permits interactive stretching and compaction.
- Routing tools that work under and around existing connections.
- Logs and corner stitching to achieve efficient implementations.

Dedicated to training in sub-micron CMOS VLSI design with full editing facilities.

Supports technology files by the MOSIS foundry service.

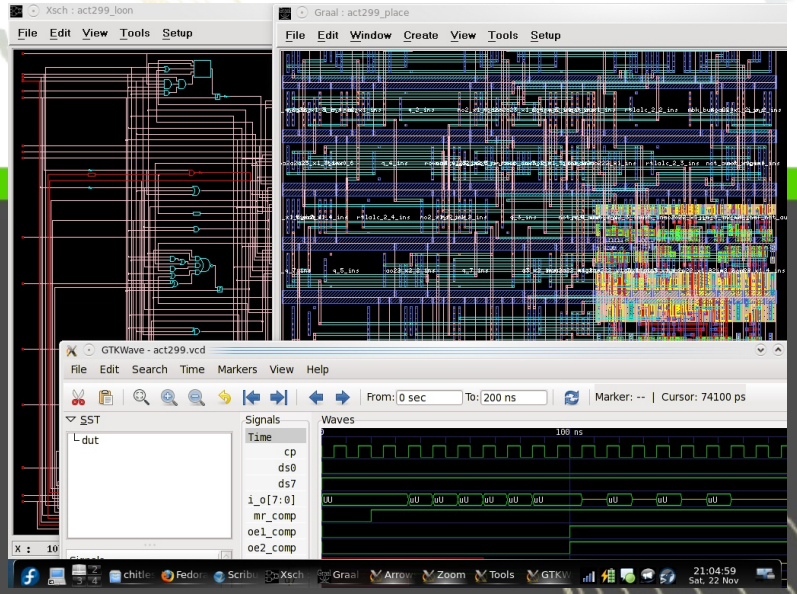
Switch-level simulation of the layout,
by considering transistors as ideal switches,
or using RC time constants to predict the relative timing of events through extracted capacitance and lumped resistance values.

Ensures that layout connectivity matches the logical design represented by the schematic or netlist before tapeout by automatically
- extracting devices and nets formed across layout hierarchy and,
- comparing them to the schematic netlist. (LVS)

Generates GDS II stream format and Caltech Intermediate Form (CIF) from a given layout.

**Achievement :** Thick-film circuit layout using the Magic layout editor.

# Digital Design




## Key Features:

Supports both VHDL and Verilog designs.
Implementation of the VHDL language
- o IEEE 1076-1987 standard
- o IEEE 1076-1993 standard
- o the protected types of VHDL00 (aka IEEE 1076a or IEEE 1076-2000)
- o and non-standard third party libraries.

VPI functionality and PLA capabilities.
Pretty printing or cross references generation in HTML.
Makefile generation for any component in a design.
A graphical waveform viewer with TCL support.
A Verilog simulator and synthesis tool for IEEE 1364-2001 standard.
Logic optimizations with espresso.

Fedora Electronic Lab was designed to help you create a chip (mixed-signal supported) from specification, simulate the HDL designs, conduct functional verification, do physical design and finally handoff your chip for manufacturing.

FEL also includes tools to help you create evaluation boards for your chips.

Fedora's HDL simulation environment enables you to verify the functional and timing models of your design.

Automatic layout generation from HDL files and standard cell libraries up to a feature size of 0.13µm can be carried out on Fedora 12.

Focus on your complex designs and users should not compile EDA software but use them out of the box.

# Extra hardware modelling capabilities

## Fedora Electronic Lab 12

**Eclipse setup for reusable Embedded/VHDL/Verilog IP modules**

DESIGN

Design VHDL/Verilog modules
eclipse-veditor

Design Embedded C code
eclipse-cdt

Autogenerate documentation from IP
eclipse-eclox

DOCS

Customize autogenerated docs
eclipse-texlipse

Maintain Perl scripts
eclipse-epic

EDA

Maintain TCL scripts
eclipse-dltk-tcl

Version Control (CVS/GIT/SVN)
eclipse-subclipse
eclipse-egit

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**Make full use of Parametrized-based design with Perl modules for both Verilog and VHDL**

The Perl modules being shipped with Fedora Electronic Lab empower digital designers and CAD engineers with methodologies to:

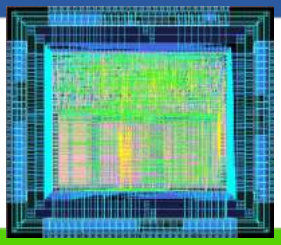
- Extend home grown design flow methodology for professional use.
- Take full advantage of the existing EDA tools on Fedora (both frontend and backend)
- Have a quick grip on the gate count and static timing analysis.
- Reduce the gap between proprietary EDA tool and opensource EDA tool
- Spin one's own home grown IP core portfolio. (DDS,SPI controller, I2C controller...)
- Auto-generate code, e.g. testbenches, stimulus/ATPG vectors, code wrappers, etc
- Execute various operations from a multi-tool environment in a design flow.
- Analyze large quantities of output data quickly and efficiently.

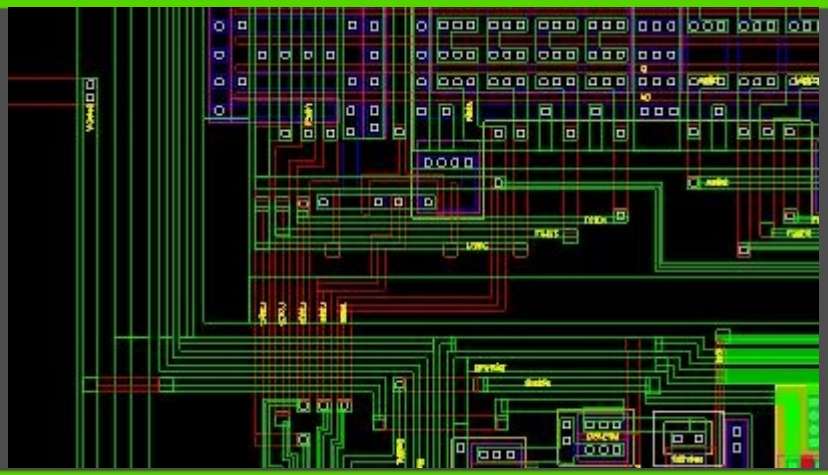
**Reduce Verilog Coding time with Emacs**

(Context-sensitive highlighting, Auto-Indenting, Macro expansion, ...) capabilities

Verilog-mode is being used by thousands of engineers world wide. The Verilog AUTOS are in use by many of the leading IP providers, including IP processor cores sold by MIPS and ARM.

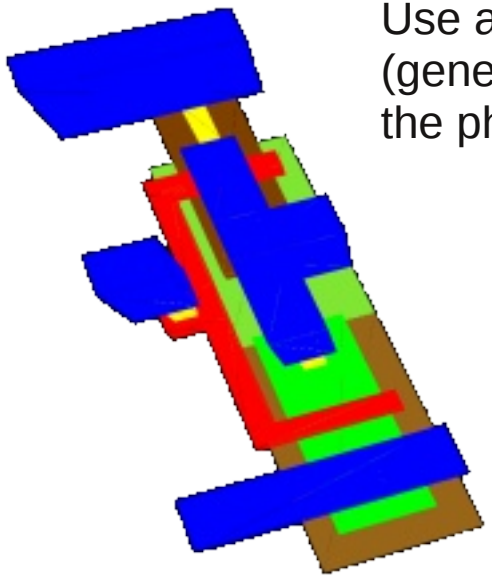
# Frontend to Backend ASIC design flows





From project definition via Synthesis, physical optimization and layout design flows till CIF/GDSII handoff, Fedora ensures that with the 7 extra standard cells (up to a feature size of 0.13µm), designers have adequate design tools.

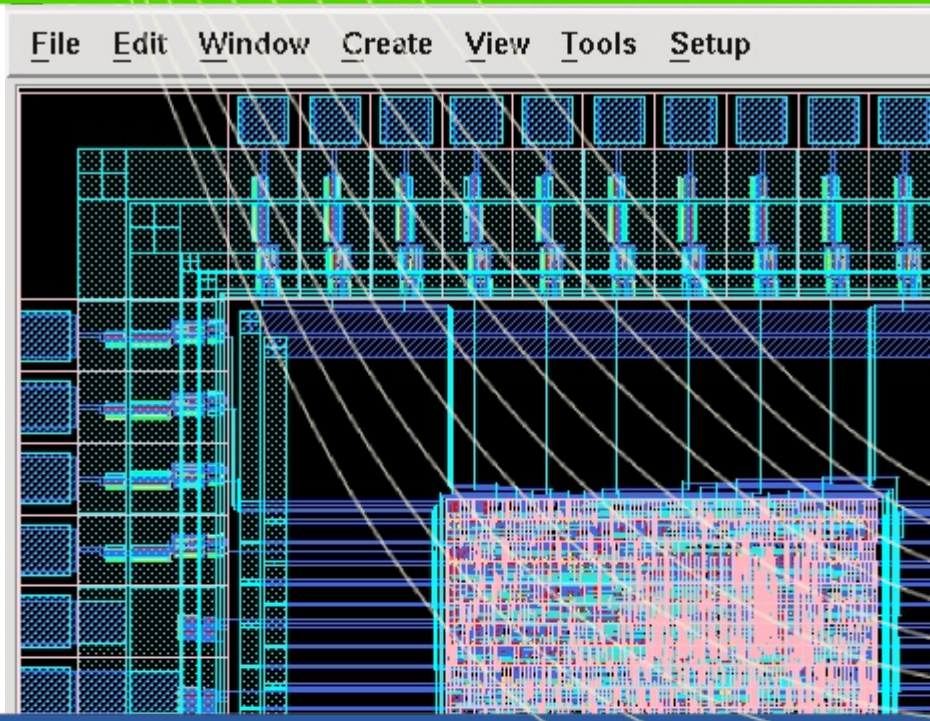
GDSII files created can even be used on analog layout editors to benefit with Analog/Mixed signal capabilities.



Use a 3D view representation (generated from GDSII data) of the physical layout in teaching.

PCB layout editors are provided to help you create evaluation boards of your chips.

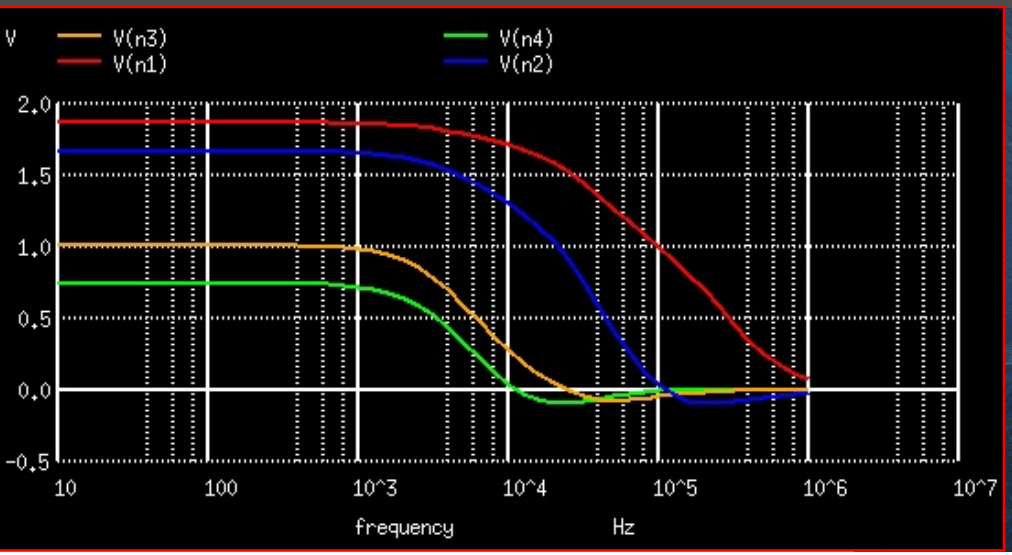
Prototyping can be automated with the wide collection of Perl modules, provided under the Fedora umbrella.



# Circuit Simulation

Build interactive schematics for your custom designs.
Various types of netlists can be extracted, simulated or used for PCB layout.

All spice simulators included possess mixed-mode capabilities.



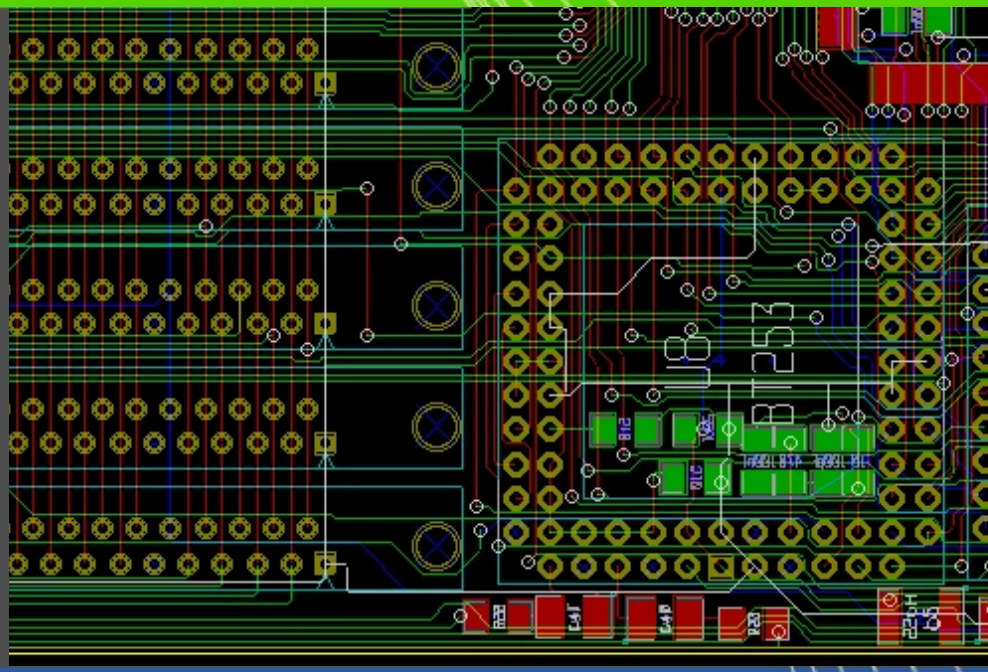

– General Purpose Circuit Simulators
  - Nonlinear AC/DC analysis
  - Transient, Fourier analysis
  - S-parameter and harmonic balance analysis
– Beyond Spice capabilities:
  Level 49, BSIMv4 and EKV implementations
– Multi-lingual, ablilty to mimic different variants of spice, and also supporting the newer languages like Verilog-AMS

– Draws publishable-quality electrical circuit schematic diagrams.
– Circuit components can be retrieved from libraries which are fully editable.
– Easy-to-use GUI with TCL interface or GTK interface.
– Coupled with espresso and eqntott, tclspice can be used for mixed signal simulations.

# PCB Layout Design

A professional-quality **printed circuit board design environment** along with :
- schematic capture, simulation, prototyping attribute management,
- bill of materials (BOM) generation and netlisting into over 20 netlist formats.

Footprints can be generated by simple Perl scripts. These Perl scripts can be maintained under a revision control sytem with Eclipse IDE.



Includes a rats nest feature, design rule checking, and can provide industry standard RS-274-X (Gerber), NC drill, and centroid data (X-Y data) output for use in the board fabrication and assembly process.

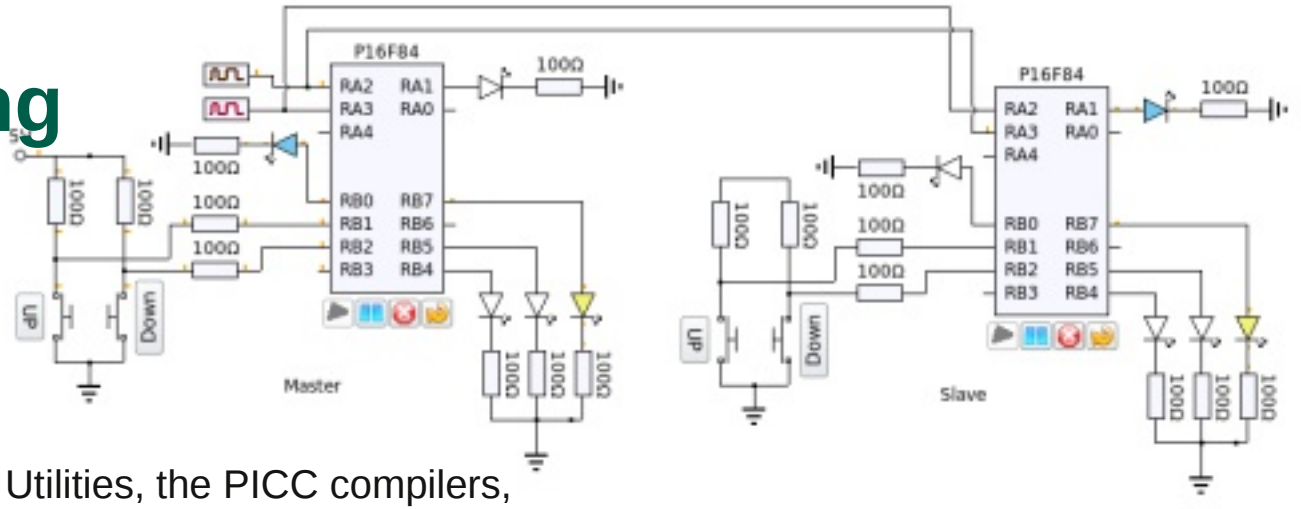
Offers high end features such as an autorouter and trace optimizer, which can tremendously reduce layout time.

Creates PCB of up to 8 layers with an unlimited number of components and nets.

Includes a viewer for Gerber files (RS274X), which supports NC-drill and Excellon formats.

Fedora also ships the kicad version and fped which are required for OpenMoko's (an opensource smartphone) development.

# µController Programming




Supported compilers :

the Small Device C Compiler, the GNU PIC Utilities, the PICC compilers, the PIC30 toolchain, the C18 compiler, the JAL and JALV2 compilers, the CSC compiler, and the Boost compilers.

Ease to use IDEs for microcontrollers circuit design, simulation and programmation to serial, parallel and USB ports. IDE includes an oscilloscope and a flowchart integration.

Supported debuggers : ICD2 and GPSim.
Supported programmers : ICD2, PICkit1,PICkit2 & PicStart+ programmers.

Supports 8051 and AVR and Binutils for SPU on IBM Cell processors.

Includes 8051 and 8085 simulators.

# Embedded Systems Development

## ARM and AVR Development System

Supports the Atmel's STK500 and the PPI (parallel port interface) programmer types.

Includes

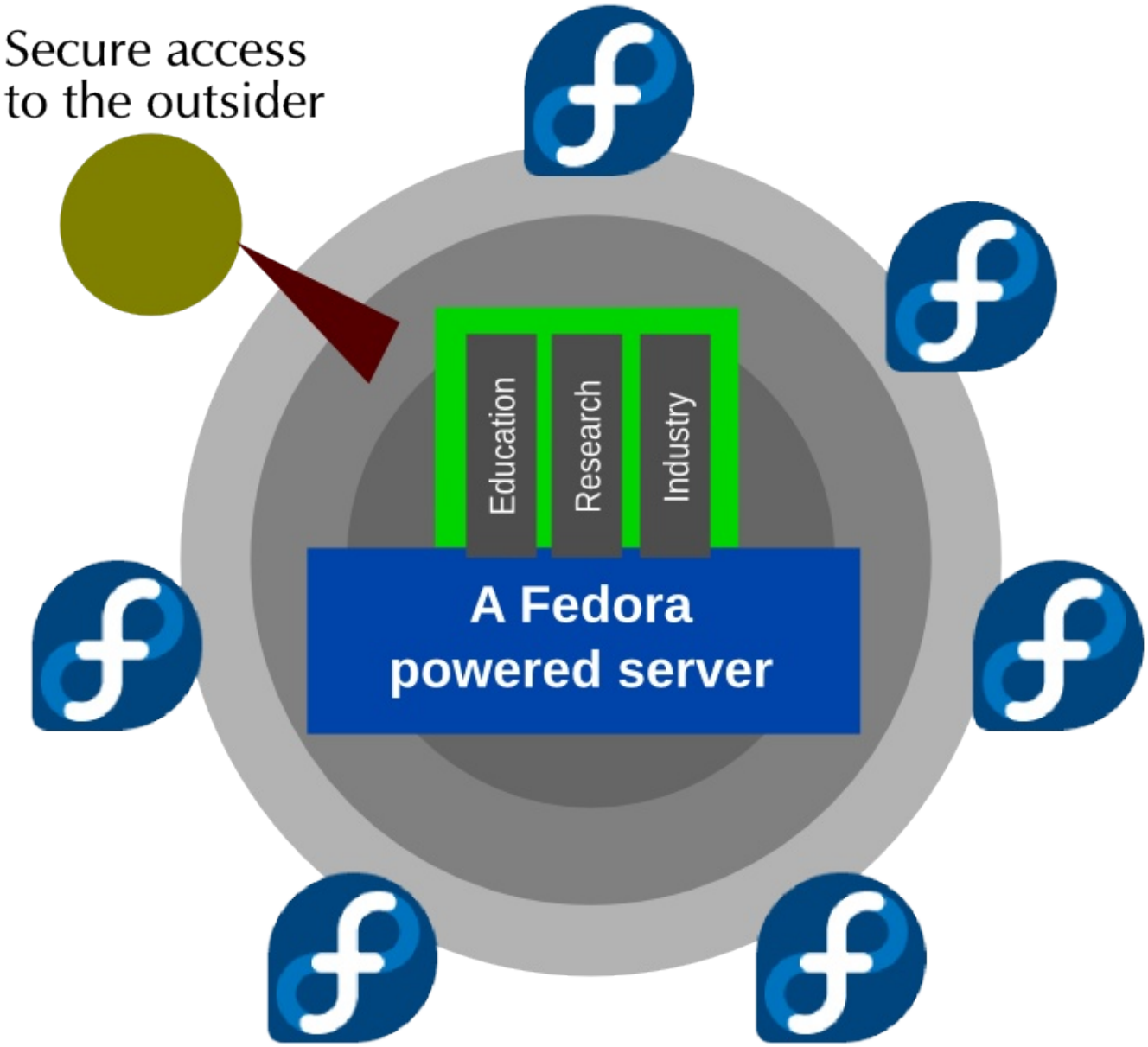
- Cross compilers and Programmers
- a Universal In-System Programmer for Atmel AVR and 8051
- a Program for interfacing the Atmel JTAG ICE to GDB

Small Device C Compiler

Includes openocd (On Chip JTAG Debugger for arm processors)

# Fedora : Collaborative hardware development

Fedora Electronic Lab




Deployment of a simple Code Review Solution for
- digital IC design
- FPGA design
- embedded design

A Fedora powered server hosting a wiki, web-based version control, progress tracking feature, ticketing service and peer review feature.

Fedora desktops with electronic design and simulation tools coupled with Fedora Eclipse and its plugins.

From Fedora Eclipse, easy and simple HDL code management along with code review via a browser.

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# OVERVIEW : FEDORA'S HIGH END HARDWARE DESIGN PLATFORM

## Fedora Electronic Lab

Fedora Electronic Lab improves hardware design experience with free and opensource software.

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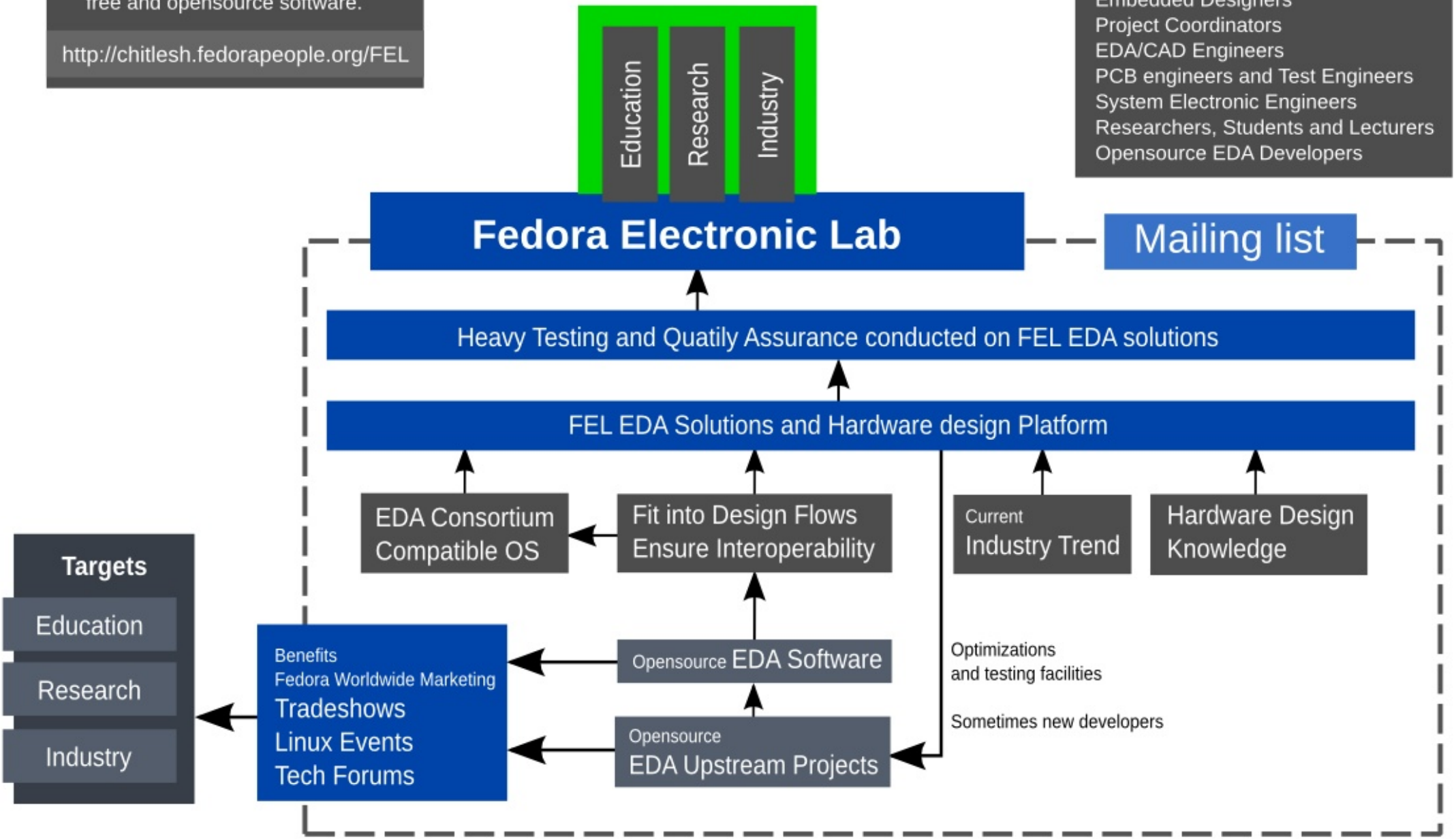
## Benefits

Analog/Digital/Mixed Designers
Verification solutions
Embedded Designers
Project Coordinators
EDA/CAD Engineers
PCB engineers and Test Engineers
System Electronic Engineers
Researchers, Students and Lecturers
Opensource EDA Developers



fedora


# About

fedora™ ELECTRONIC LAB

Fedora Electronic Lab is a subproject of the Fedora Project dedicated to EDA tools and open hardware content. We develop and provide each 6 months a new version release for free. Our goal is not only package those tools for you, but shape those tools to satisfy design methodologies.

It can be downloaded freely as a LiveDVD.

## Download the latest version 12.

All Fedora Electronic Lab packages can be freely installed via yum from official repositories.

Website :
http://chitlesh.fedorapeople.org/FEL

technical support :
Fedora Electronic Lab Mailing List