AMD

COMPUTER ARCHITECTURE AND FEEDBACK CONTROL

CHALLENGES AND OPPORTUNITIES

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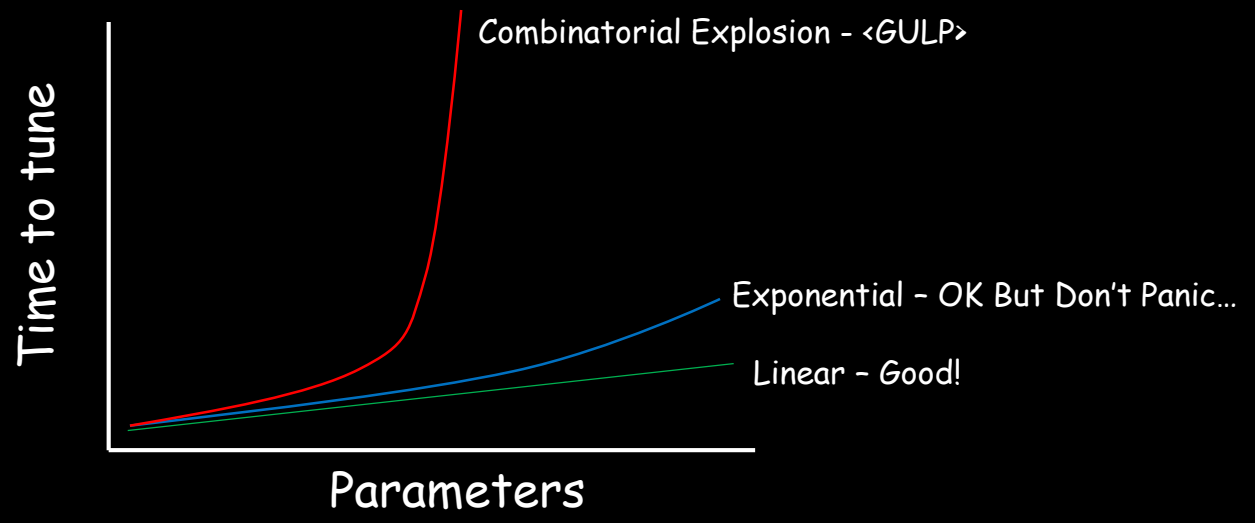
OUTLINE

- “Simple yet effective”
  - Trade-off between software and firmware
  - Code reusability
- Tuning multiple parameters
- Safety controllers
- Machine Learning Solutions
  - Data
  - Security and privacy
  - Time to market
- Designing for heterogeneous systems
  - Controller composability across internal IPs
  - Controller composability between vendors



FEEDBACK CONTROL: STATE-OF-THE-ART

HEURISTICS-BASED DESIGNS

- If (A < Threshold) do B else do C
- Simple and easy to implement
- Lots of parameters. Hence hard to tune
- Verifying correctness is expensive for complex systems
- Examples
  - CoScale (2012) [1]
  - Crank It Up or Dial It Down (2013) [2]
  - Harmonia (2015) [3]

PID AND ADAPTIVE CONTROLLERS

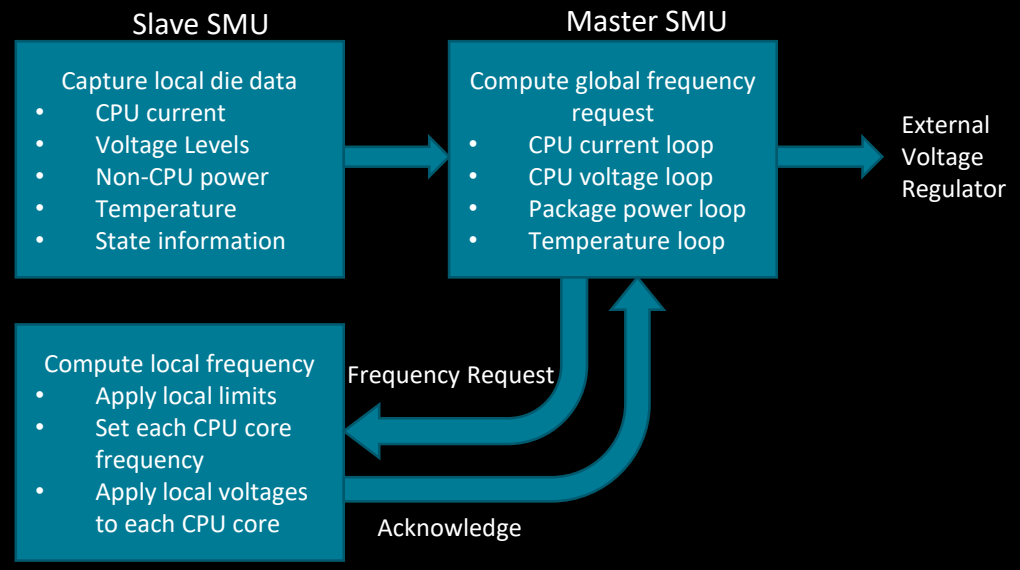
- PID is simple. Hence a popular choice
- Single Input Single Output (SISO)
- PID is great for Newtonian systems
- Computers are inherently non-linear
  - Adaptive gain controllers address some non-linearities
- Examples:
  - Temperature Aware Microarchitecture [4]
  - Adaptive Gain Power Regulator [5]

ADVANCED CONTROL THEORY

- Mathematically rigorous
- Multi – Objective optimization
- Linear Quadratic Gaussian regulator (LQG), Model Predictive Control (MPC)
- Multiple Input Multiple Output (MIMO)
- Examples:
  - DTM with MPC (2009) [6]
  - DTM with Convex Optimization (2008) [7]
  - MIMO and LQG [8]

HEURISTICS-BASED DESIGNS
SIMPLE YET EFFECTIVE

- Heuristics-Based and PID controllers are great candidates for simple designs
- Thresholds in heuristics and Gains in PID require tuning
  - Time consuming process
- Software implementation (e.g., `cpufreq`)
- Suits firmware implementation as well! (e.g., System Management Unit (SMU) [9])
  - Faster response times compared to software
  - Small code size
  - Meets real-time constraints
- Core reusability is very important
  - Must be applicable across products with “minimal” tuning
  - Time to market
- Basically, works like a charm! Until…



MULTI – PARAMETER TUNING

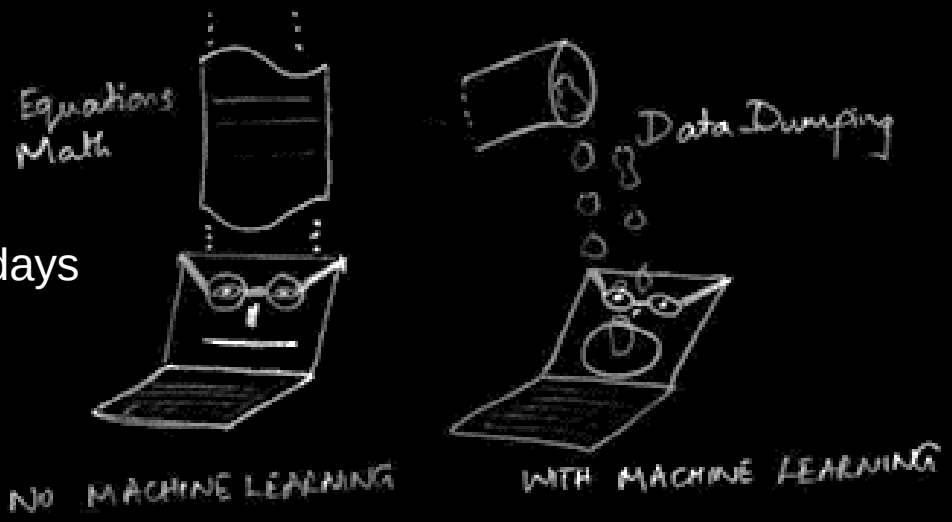
- Performance, Power, Temperature and Energy (PPTE) – high-level outcomes
- Parameters affecting PPTE
  - Cache sizes, associativity, issue width
  - Capacitance, frequency, voltage, leakage current
  - Application behavior: compute vs. memory, bursty vs. steady, CPU vs. GPU
- Ideal situation: PPTE = *f* (All possible parameters) and sensitivity of PPTE w.r.t. each parameter is well understood
- Reality: The model *f* is hard to characterize. *Shmoo*–ing each parameter is practically infeasible
  - Cache size affects performance and power and hence temperature which in turn affects leakage currents
  - Power dissipated in GPU reduces boost clock frequency of CPU (Cooperative Boosting 2013 [10])
- The BIG UNKNOWN: Application behavior
  - Characterize the system and tune for a generic set of applications (3DMark®, PCMark®, Cinebench®, SPEC Power®, etc.)
- Heuristics-based methods and PID controllers begin to show their limitations in such complex environments
- CHALLENGES: What is the best approach to handling multiple parameters?
  - Smaller, simplified piece-wise linearized models? If yes, what determines the metric “simplified”?

SAFETY CONTROLLERS

- Potential Hazards on a typical processor
  - Over heating (> T_j), Thermal Design Power (TDP), Thermal Design Current (TDC), Electrical Design Current (EDC), Current spikes (dI/dt)
- SMU firmware monitors each individual hazard at fine granularity
- Academic proposals do not always consider them
  - Designing within TDP and temperature limits as constraints is only the first step
- A well-rounded, practical power management solution MUST address these critical hazards swiftly and effectively
- Control theory (e.g., Robust control) provides some guarantees on PPTE
- But without explicitly addressing safety hazards can render them practically unsuitable
- CHALLENGES: How should we integrate safety controllers alongside PPTE optimization controllers?
  - Softmax?
  - Use Machine Learning to classify hazard scenarios?
  - Composability (will talk about it in a few slides)

USING MACHINE LEARNING

- "New kid on the block" challenging traditional PID and heuristics-based techniques
- Hank will give an in-depth review later
- Seems to work great when there is lots and lots of training data
  - But how much data is "sufficient"? Does it cover all possible use-cases?
  - Should we simply let ML handle everything?
- User Data Collection: Not the most popular set of three words these days
  - AMD cares about security and privacy
  - Cannot necessarily train on user-specific data (could cause overfitting)
- Model Training Time
  - ML training is time consuming
  - Product shipping deadlines are tight: Time to market is extremely critical
- CHALLENGES: If we decide to take the ML route,
  - Which ML algorithm is best suited for practical implementation? (Recall: Firmware has tight real-time and space constraints)
  - Do we know if applications X, Y and Z represent the full spectrum?
  - What about code reusability?



HETEROGENEOUS SYSTEMS

Cores + Cache

DSP, Network

GPU

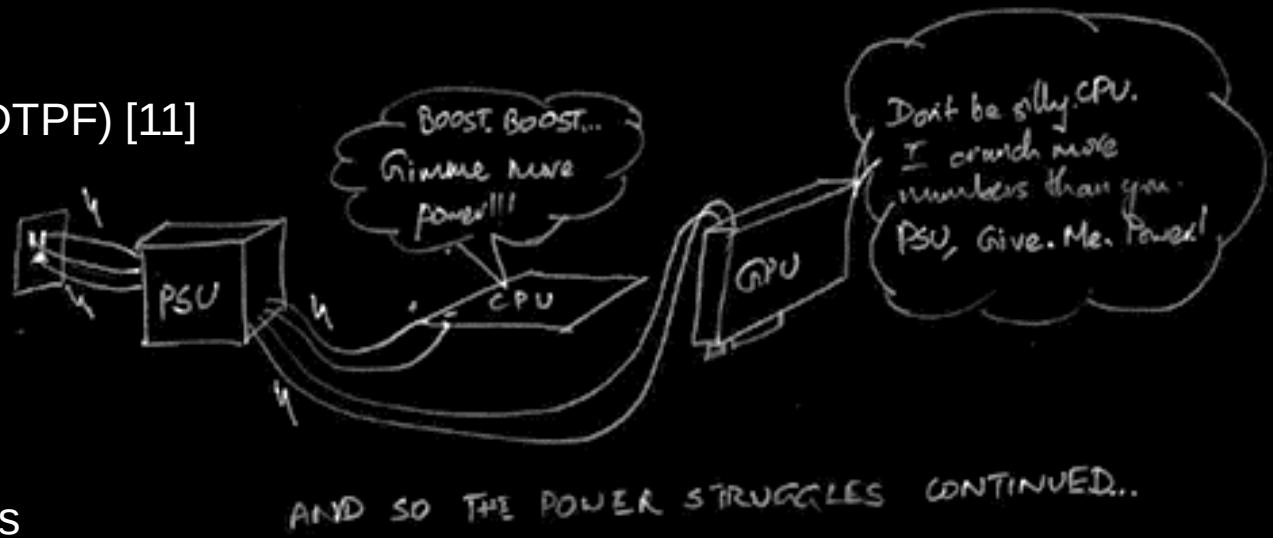
Mem Ctrl + IO

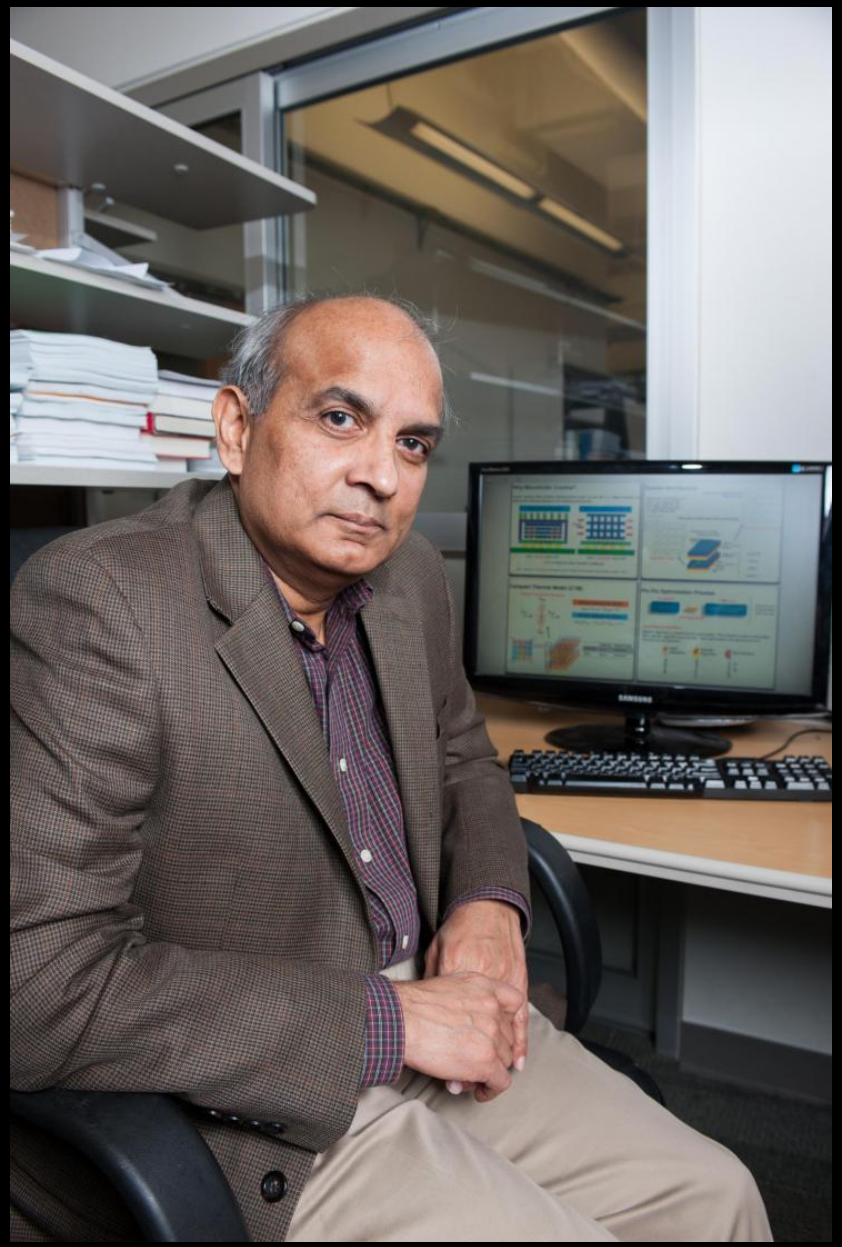
HETEROGENEITY WITHIN A PROCESSOR

- AMD's Accelerated Processing Unit (APU): Heterogeneity in processor types
  - AMD Ryzen™ 7 3750H Mobile Processor with Radeon™ RX Vega 10 Graphics
- Arm® big.LITTLE: Heterogeneity in CPU types
- Power management is a challenge, but all IPs are "in-house"
- Power and thermal models are well understood
- Application characteristics driven power sharing between CPU and GPU (between big and LITTLE cores)
- Chiplet based architecture
  - Great for performance scaling
  - Challenging for power management

SYSTEM–WIDE HETEROGENEITY

- Intel uses Dynamic Power and Thermal Framework (DTPF) [11]
  - Centralized Kernel driver
  - Each chip exposes sensor data
  - DTPF controls the chip inputs
- IBM POWER9 uses On Chip Controller (OCC) [12]
  - Centralized hardware controller
  - Master – Slave strategy for 2 – socket configurations
- Composability of controllers in heterogeneous systems
  - Each vendor optimizes its IP “locally”. Does it imply “global” optimality as well?
  - Will locally stable controllers work harmoniously when composed together in a large system?
  - Centralized controllers do not scale
  - What is the right granularity for de-centralizing individual controllers?
- Computing systems can be assembled with parts from multiple vendors (AMD, Intel , NVIDIA etc.)
- How should we separate power control between OS and FW?
- Control theory could shed some light on these questions: Raghav will talk in detail next





IN MEMORY OF MY ADVISOR

DR. SUDHAKAR YALAMANCHILI

THANK YOU !
QUESTIONS?

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