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Computer Organization

Part 41 – Superscalar Architecture

UNIT – VI

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Superscalar Architecture

- Microprocessors such as the PowerPC reach performance levels greater than one instruction per cycle by fetching, decoding and executing several instructions concurrently. This mode of operation is known as Superscalar.
- A superscalar processor has multiple execution units, each of which is usually pipelined so that they constitute a set of independent instruction pipelines.
- Its program control unit is capable of fetching several instructions concurrently.

Issues in superscalar architecture

- Instruction types
- E-unit availability
- True data dependency
- Procedural dependency
- Resource conflicts
- Output dependency
- Antidependency

Instruction types

- Floating point instructions fetched to floating point unit only.
- Integer arithmetic instructions are fetched to integer unit only.

E-unit availability

- An instruction can be issued to a pipelined E-unit only if no collision will result, as determined by the pipeline's reservation table.

True data dependency

- For example:

  SUB R_1, R_2

  MOV R_3, R_1

Procedural Dependency

- We can not execute the instruction until the branch operation is completed.

Resource conflicts

- While executing number of instructions in parallel, the situation may occur that two or more instructions require same resource at the same time.
- For example, two or more instructions may require references to memories, caches, buses register-file ports and functional units at the same time.

Output dependency

- For example:

R3 = R3 + R5 ← L1

R4 = R3 + 1 ← L2

R3 = R5 + 1 ← L3

R6 = R3 + R4 ← L4

Antidependency

- For example:

R3 = R3 + R5 ← L1

R4 = R3 + 1 ← L2

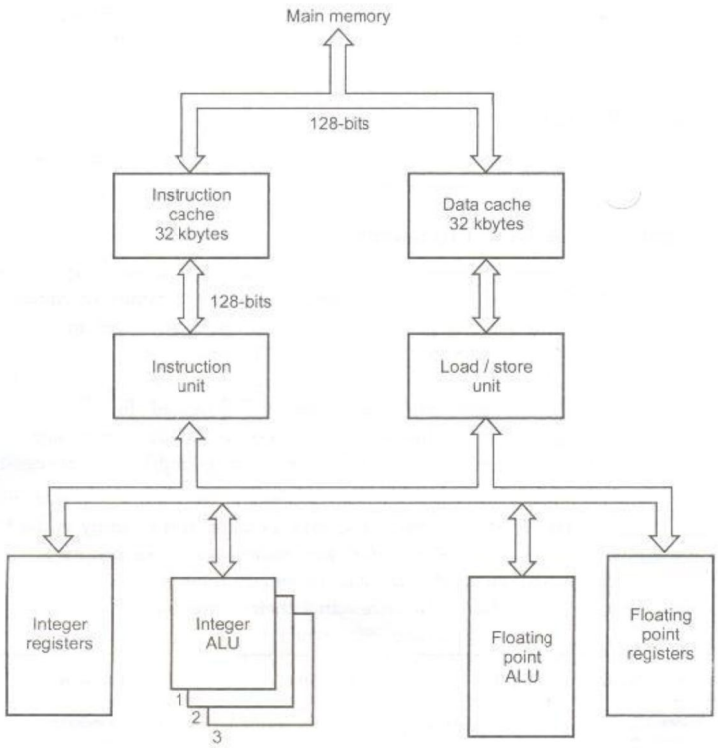
R3 = R5 + 1 ← L3

R6 = R3 + R4 ← L4

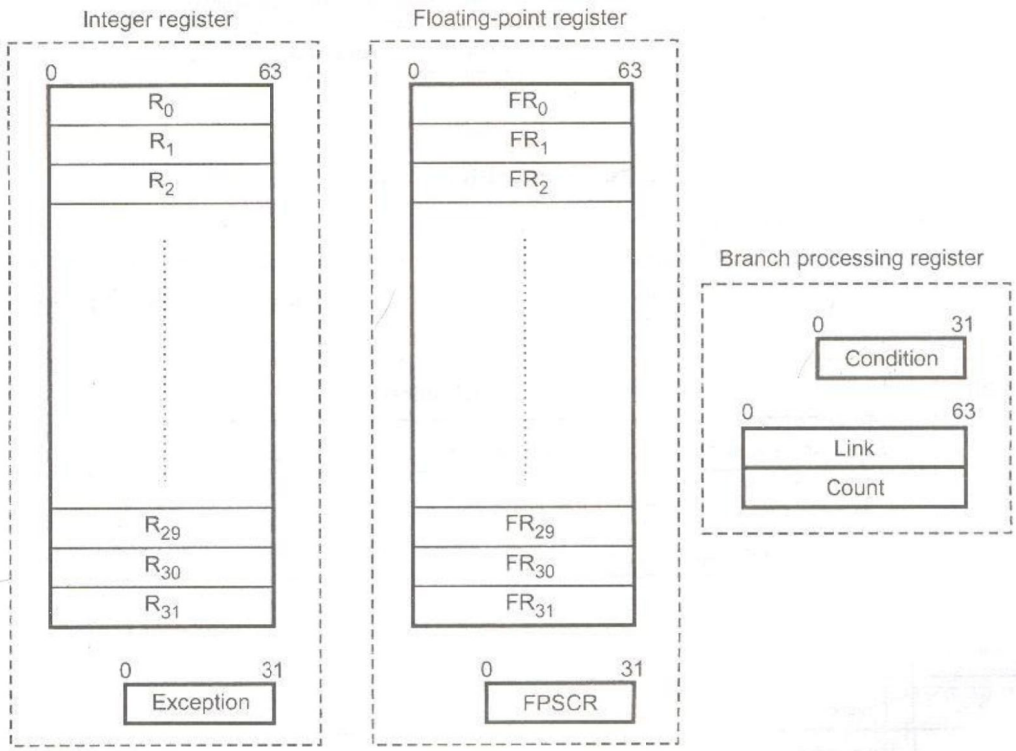
Example: PowerPC

- Developed jointly by Motorola, IBM, and Apple Computer
- It is based on Power architecture implemented by RS/6000 family of computers.
- It takes advantages of recent technology advances in areas such as process technology, compiler design and RISC.

Architecture of PowerPC



PowerPC register organization



Registers

- Exception register
  - It is used to indicate exceptions in integer arithmetic operations and to store byte count field.
- FPSCR Floating Point Status and Control Register
  - It contains control bits as well as status bits.
- Link Register
  - It is used for call/return operations.

Registers

- Count Register
  - Used as the count for iteration loop.
- Condition Register
  - It consists of eight 4-bit condition code field. These are used for showing different conditions.

Machine Status Register

- When the program is interrupted, it is necessary to store the current state of the processor or machine. So that after the interrupt is over it is possible to recover the state of the processor at the time of the interrupt.
- The state of the processor not only includes the contents of the register but also the contents of various control conditions related to execution.
- The MSR is used to store the state of the processor.

Data Types of PowerPC

- Byte (8-bits)
- Halfword (16-bits)
- Word (32-bits)
- Doubleword (64-bits)

PowerPC Addressing Modes

- Register direct
- Immediate
- Register indirect
- Register indirect with immediate index
- Register indirect with index
- Link register direct
- Count register direct

PowerPC instruction set

- Integer arithmetic
- Logical and shift
- Floating point
- Load / store
- Flow control
- Memory control
- Processor control
- External control

Features of PowerPC

- Separate 32-entry register files for integer and floating point instructions.
- FPR and GPR
- Uniform length instructions
- Nondestructive use of registers for arithmetic instructions.
- A precise exception model.
- IEEE-754 floating point operations.
- Single and double precision floating point arithmetic.
- User level instructions for cache.
- Separate instruction and data cache.
- Support for big and little endian system.
- Support for 64-bit addressing.

References

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  - *By A. P. Godse* (from books.google.com)
- Computer Organization
  - *By Hamacher and Zaky*
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