2

Cost Per Wafer

2 Cost Per Wafer

Cost per wafer is perhaps the most widely used cost metric in the semiconductor industry. Its value lies in the ability to combine large quantities of cost data and obtain one indicator of operating cost that can be used to compare different pieces of equipment, different processes, alternative materials, etc. Cost per wafer can also be used as a benchmarking metric (see Chapter 4, Fab Benchmarking). It can further be used to estimate a fair price for foundry-produced wafers.

Information from the Semiconductor Industry Association in the U.S. indicates that average cost per wafer has increased by 3X over the last 15 years (Figure 2-1). Although the cost of labor, materials and capital expenditures per wafer have increased, the real cost of manufacturing semiconductor chips continues to decrease because the number of transistors that can be placed on a wafer has grown faster than manufacturing costs, as shown in Figure 2-2.

As discussed in Chapter 1, this ever-increasing cost per wafer is offset by the ability to shrink feature size by 30 percent each device generation, thereby decreasing the manufacturing cost per transistor. The effective price of DRAMs, measured in cost per bit, falls by 30 percent per year. Rising manufacturing cost is further offset by manufacturers' ability to continually increase device yields, transition to larger wafers sizes and increase the productivity of fab equipment and operations. By continually decreasing or controlling cost per wafer, IC manufacturers can increase profitability.

Cost per wafer at the fab level can be simply computed using the total cost of manufacturing divided by the total number of yielded wafers produced. Cost per wafer at the equipment level is typically computed "from the ground-up" using the cost of equipment depreciation, cost of direct labor, maintenance and materials, cost of energy and other facilities as well as building depreciation costs.

Cost per wafer first enjoyed widespread use several years following the introduction of cost-of-ownership modeling by SEMATECH, the consortium of semiconductor manufacturers in the U.S. Cost per wafer is often used to compare the cost-of-ownership performance of competing pieces of equipment. It is also used by semiconductor manufacturers for benchmarking purposes, and to assess the cost of making process modifications and adopting new processes. Importantly, however, one of the most critical components in cost-of-ownership calculations is the yield of the given process step. Because yield influences cost so dramatically and because yield is very difficult to determine on a step-by-step basis, most COO calculations assume identical yields from one process tool to another. For more discussion on COO see Chapter 4, Fab Benchmarking.

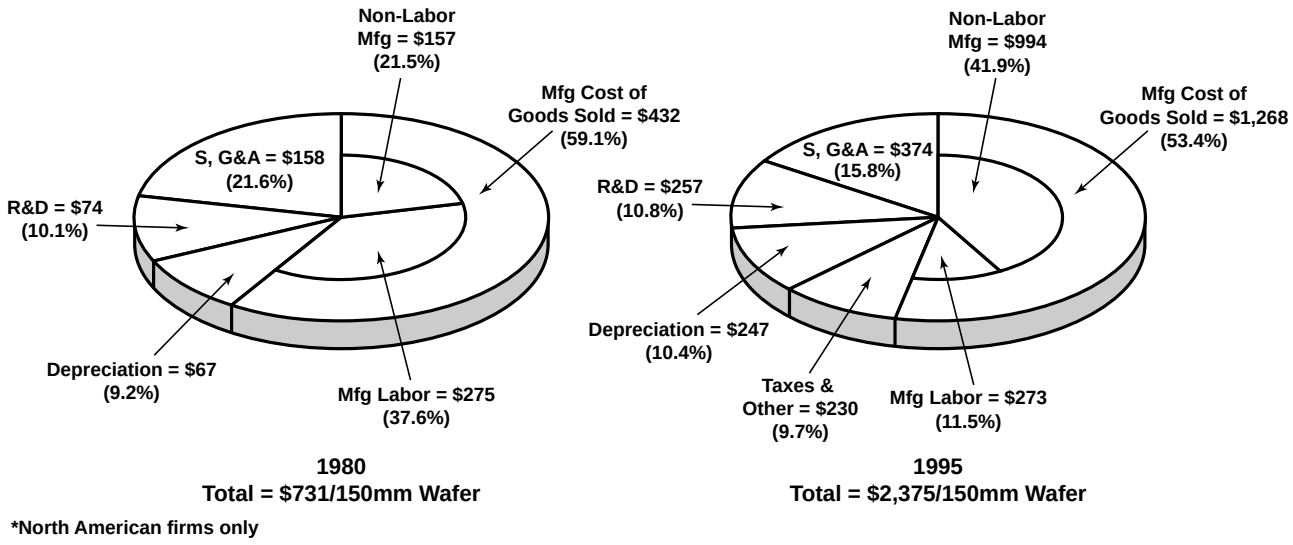


Figure 2-1. Total Cost Per Wafer Start (1980 Versus 1995)*

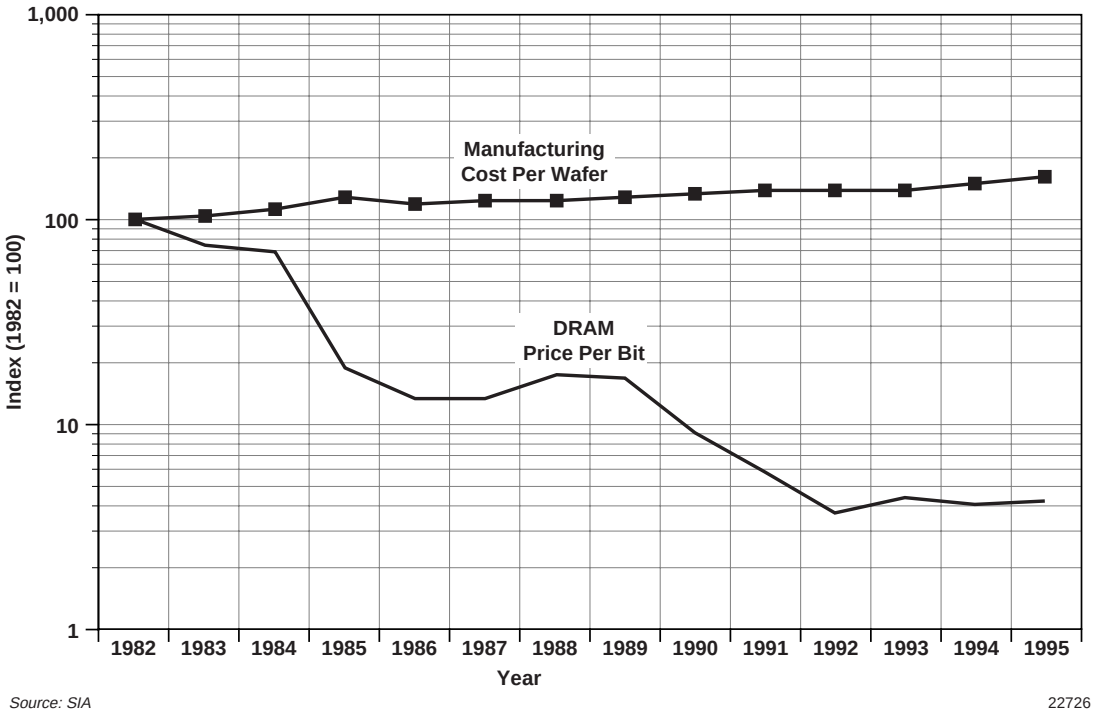


Figure 2-2. How Decreasing Cost Per Bit Compensates for Increasing Manufacturing Cost

Operating Costs

Fab operating costs can be divided into fixed costs and variable costs. Fixed costs include equipment depreciation, R&D, overhead, and general and administrative costs. The most important variable cost is the cost of sales (manufacturing cost of goods sold), which includes the cost of consumables, spare parts, materials (including cleanroom garments, etc.), labor, production control, and facilities (operating power for the plant, deionized water systems, etc.). The trend of increasing manufacturing cost of goods sold is shown in Figure 2-3. This cost of manufacturing wafers, without considering increasing depreciation costs, rises at an average rate of 5-6 percent per year.

Operating costs are often defined for wafer processing alone as assembly and final testing of devices are commonly performed at a different manufacturing sites, often in Southeast Asian countries where labor costs are low by North American, Japanese, and European standards. In rough terms, IC manufacturing costs can be divided into three categories consisting of:

- 10-15 percent due to labor cost,
- 35-40 percent due to materials costs (including starting wafer cost), and
- 40-50 percent for capital costs[1]

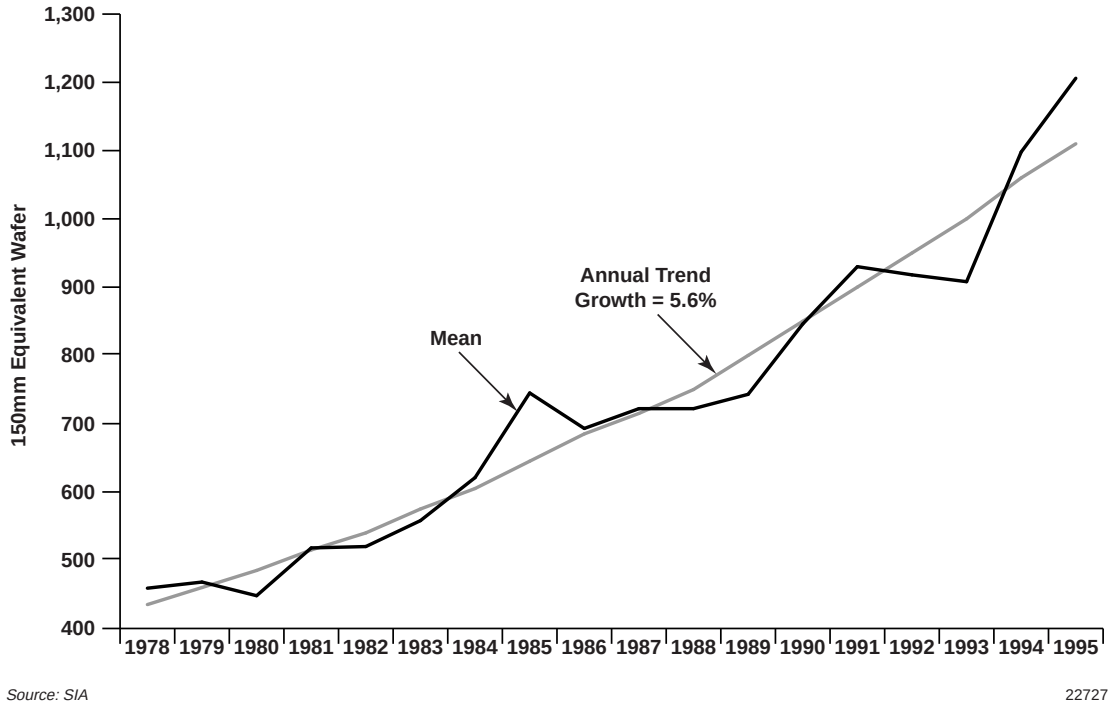


Figure 2-3. Manufacturing Cost of Goods Sold (Less Depreciation) Per Wafer Start

Beyond these broad categories, operating costs are typically broken down into four main components:

- Manufacturing cost of devices sold (all costs directly allocated to production, less depreciation),
- Selling, general and administrative expenses,
- Research and development costs, and
- Depreciation expenses.

As shown in Figure 2-1, manufacturing cost of goods sold in 1995 accounted for over 53 percent of the total cost per wafer start for merchant IC producers in the U.S.[2] Cost per wafer for IC manufacturers has increased from 1980's level of around $730 per 150mm equivalent wafer to 1995's level of nearly $2,400 per 150mm wafer. In other words, the cost per wafer has risen by over a factor of three in a fifteen year period. In addition, the portion of manufacturing costs due to labor expenses has dropped dramatically. Interestingly, the dollar amount companies had to devote to labor was almost exactly the same in 1995 as it was in 1980.

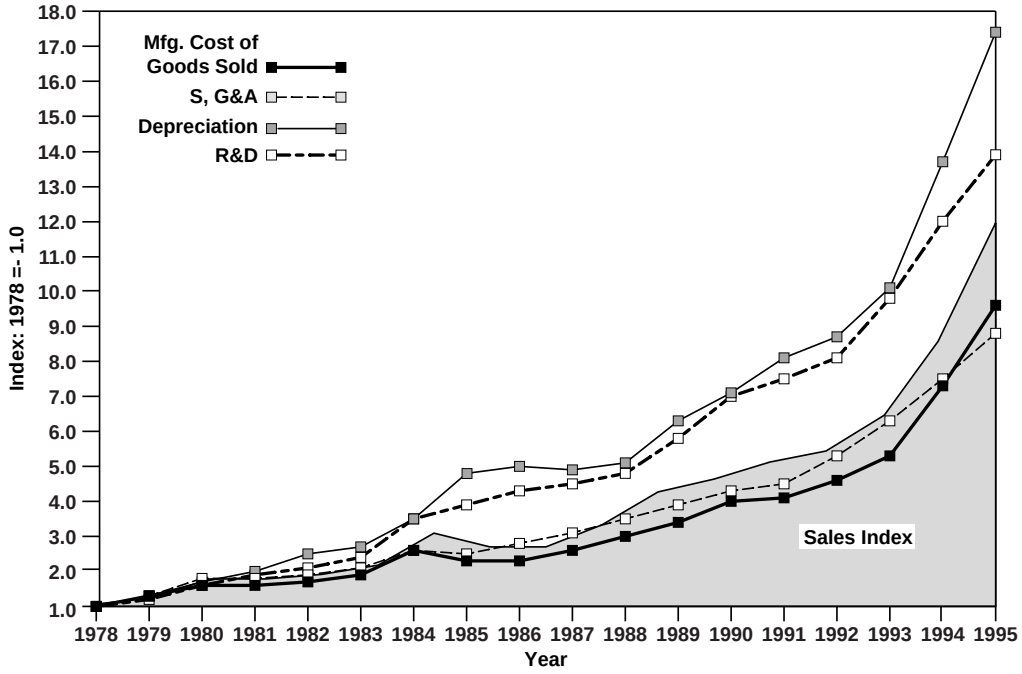
These expenditures can also be viewed relative to annual semiconductor industry sales. In other words, the rates of increase in expenditures for manufacturing, R&D, depreciation, and S, G&A expenses can be compared to the rate of annual increases in overall semiconductor industry revenues. Shown in Figure 2-4 are year-to-year values for R&D, depreciation expenses, manufacturing costs, S, G&A costs, and semiconductor sales, normalized to 1978 values. Long term, depreciation and R&D costs have risen much more dramatically than manufacturing costs, semiconductor sales, and S, G&A expenditures. Between 1978 and 1995, depreciation outlays increased by a factor of 17; R&D costs increased by a factor of 14; manufacturing costs and S, G&A costs increased by almost a factor of 9 each; and sales by U.S.-based merchant semiconductor firms increased by a factor of 12. As can be gleaned from this illustration, during the industry's most difficult period in the mid-1980s, R&D and depreciation expenditures remained high while the sales index (annual semiconductor sales) dipped too low to support these expenditures.

In the most recent expansionary cycle between 1993 and 1996, the focus on increasing expenditures for equipment and new fabs has increased dramatically. However, as shown in Figure 2-5, depreciation expenses as a percent of sales appear to be stabilizing, despite a long-term average increase of 10-15 percent per year.

The following sections briefly discusses the cost components for manufacturing costs, depreciation, and R&D costs. Selling, general and administrative costs will not be covered as these expenditures vary a great deal from one company to the next, and vary little from year to year for a given company.

R&D and Depreciation Costs

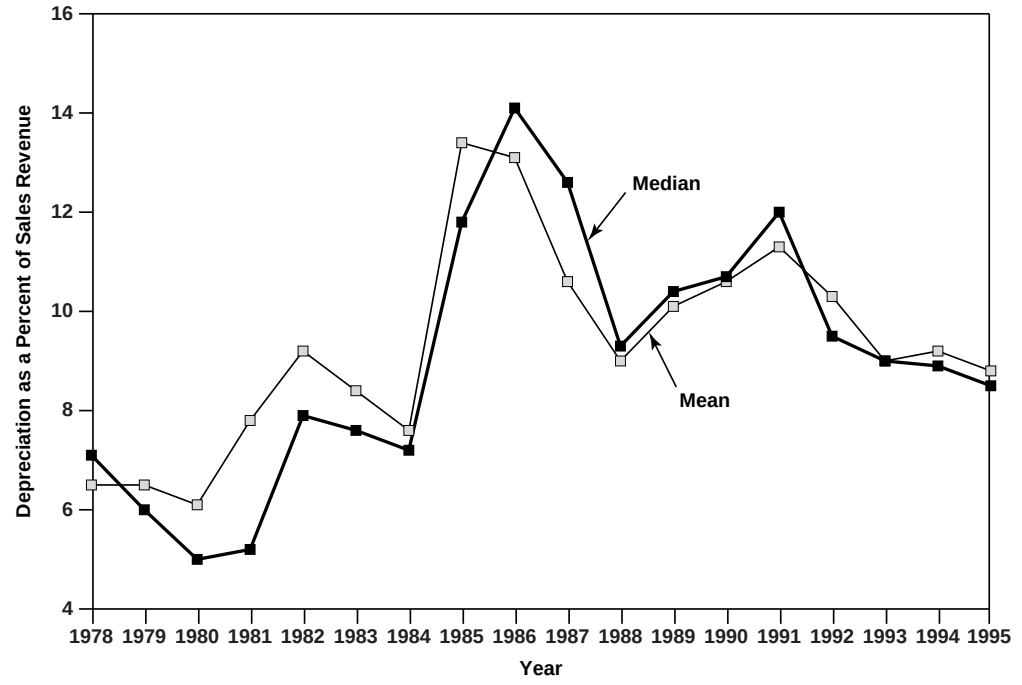
As mentioned previously, due to the extremely high pace of technological innovation in this industry, necessary investment for R&D, new fabs, and equipment can be as high as 25-30 percent of sales. In fact, the percentage of sales that must be reinvested for R&D in the semiconductor industry surpasses that needed in nearly every other high technology industry (Figure 2-6). Interestingly enough, the key industries that semiconductors feed—computers, consumer electronics, communications, and automotive—each requires lower investment to develop than the chips that run them.



Note: U.S. merchant semiconductor manufacturers only.

Source: SIA 19783B

Figure 2-4. Annual Expenditures for Major Cost Components



Note: U.S. merchant semiconductor manufacturers only.

Source: SIA 19784B

Figure 2-5. Depreciation Expenses Rise More Rapidly Than IC Revenues

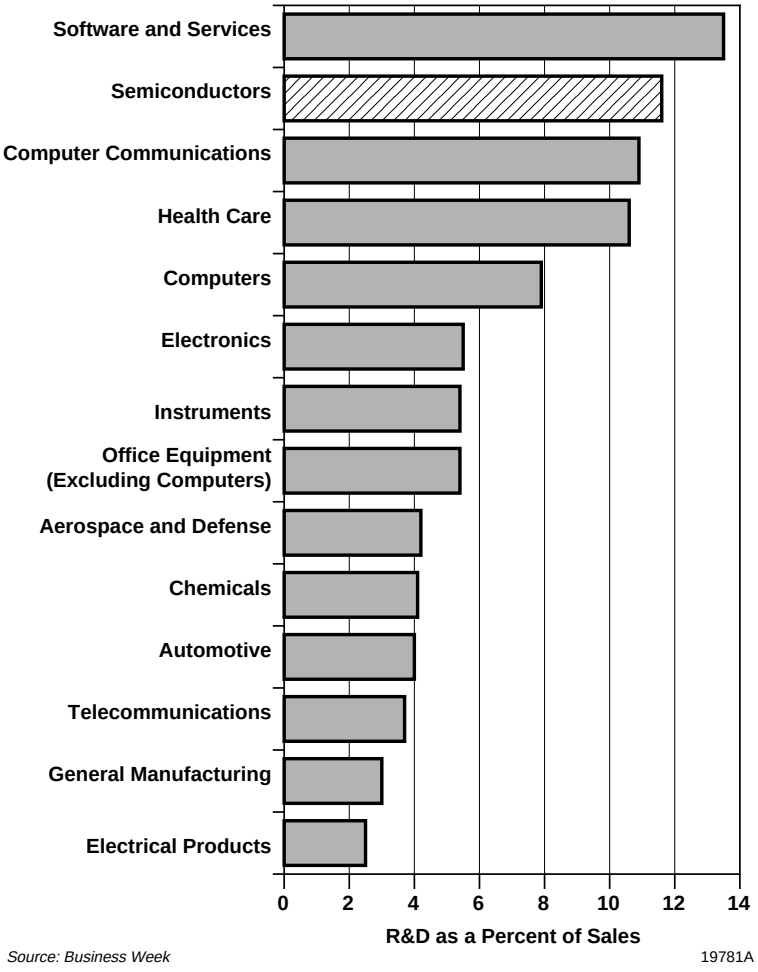


Figure 2-6. R&D For Semiconductors Exceed Most Other High Technology Industries

In addition, as technology development becomes more expensive, it becomes more difficult to get a timely return on investment. Generally, IC manufacturers invest 10-15 percent of sales each year in R&D. Figure 2-7 shows R&D expenditures both in billions of dollars and as a percentage of sales revenues for merchant IC manufacturers in the US. While this percentage appears to have declined over the 1992-1995 period, R&D outlays rose dramatically at an average annual rate of 18 percent over the period.

The most important components in development costs are equipment costs and labor, as illustrated in Figure 2-8. One of the most important strategies used by semiconductor companies to control these costs is the formation of strategic partnerships for both technology development and in some cases, fab ownership.

Also shown back in Chapter 1, the top 10 companies accounted for 55 percent of all capital spending in the semiconductor

industry in 1996, and 83 percent of all spending is performed by 25 companies. Worldwide, SEMI and SEAJ estimate that 63.5 percent of capital spending goes toward wafer processing equipment, 21 percent toward testing equipment, nearly 10 percent to assembly equipment and nearly 6 percent to facility related equipment (i.e., computers, automation, etc.). These numbers equate to 1996 market sizes of $26.6 billion for wafer processing equipment, $8.8 billion for testing equipment, $4 billion for assembly equipment and $2.5 billion for facility equipment.

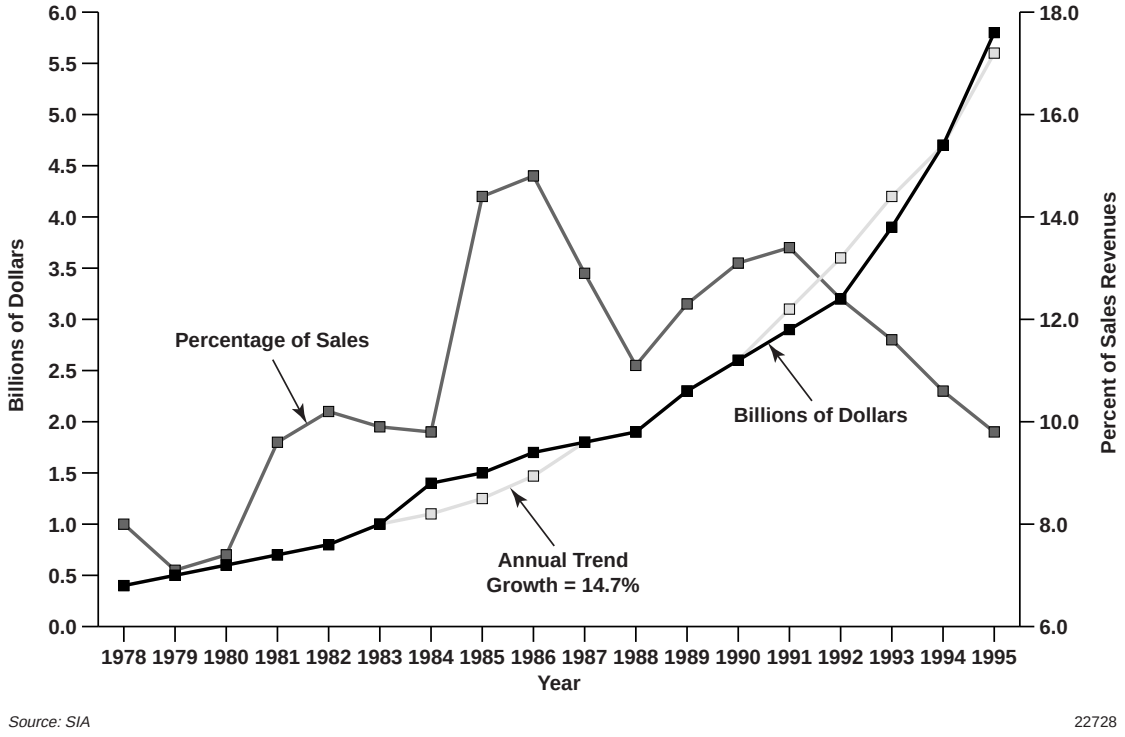


Figure 2-7. Semiconductor R&D Expenditures

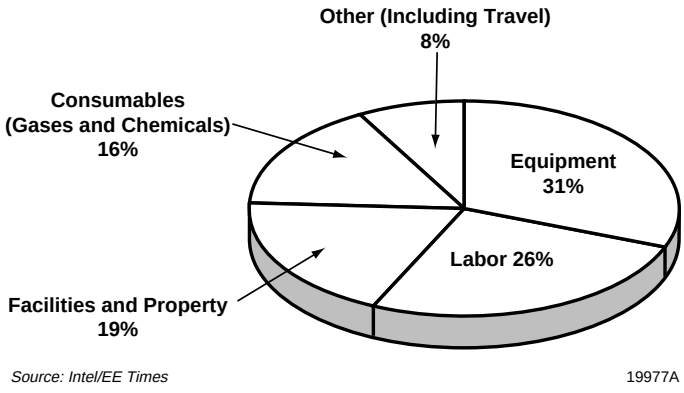


Figure 2-8. Breakdown of Semiconductor Technology Development Costs

Depreciation schedules vary from one country to another. Semiconductor firms in the U.S. have attempted to change 5-year depreciation schedules on semiconductor processing equipment to 3 years to better reflect the rapid rate of technological obsolescence in fabs today. Despite bipartisan support in the U.S. House of Representatives and Senate, the bill to change these depreciation schedules did not pass. However, some progress was made in 1997 as a bill was passed to raise R&D tax credit for basic research from 8 percent to 11 percent. The bill also allows a 6 percent manufacturers investment credit for cleanrooms built by IC manufacturers and semiconductor equipment companies. Figure 2-9 shows depreciation schedules for a fab facility in the U.S.

Within the fab area, the photolithography cell is the most expensive (Figure 2-10), as leading-edge steppers and step-and-scan machines for 0.25um processing are priced between $5-$7 million each. In addition, the investment for advanced reticles is rising rapidly (Figure 2-11). Beyond lithography costs, the next most expensive is diffusion processes, followed by etching, thin film deposition, and ion implantation. Trends indicate a long-term increase in number of CVD, sputtering, and etching tools in the fab, principally driven by an increasing number of metal layers in advanced logic devices (currently at 5-6 levels for 64-bit MPUs), and the introduction of chemical mechanical polishing tools for global planarization. Many sources estimate that back-end wafer processing (all processing of films above the substrate level) accounts for more than 50 percent of overall cost per wafer.

Year in Service	Land	Fab Building	Cleanroom Equipment	Wafer Processing Equipment	Office and Utility
1	100%	98%	89%	67%	98%
2	104%	97%	79%	46%	94%
3	108%	97%	70%	29%	90%
4	112%	97%	62%	16%	86%
5	117%	97%	55%	10%	82%
6	122%	96%	49%	10%	79%
7	127%	95%	44%	10%	76%
8	132%	94%	39%	10%	74%
9	137%	93%	35%	10%	72%
10	142%	91%	31%	10%	69%
11	148%	90%	28%	10%	67%
12	154%	89%	25%	10%	65%
13	160%	87%	22%	10%	64%
14	167%	85%	20%	10%	62%
15	173%	83%	20%	10%	61%
16	180%	81%	20%	10%	60%

Source: Oregon Department of Revenue 1994-1995 Electronics Trend and Depreciation Schedules 22729

Figure 2-9. Depreciation Schedules Projected Appraised Value of Investment as Percentage of Original Cost

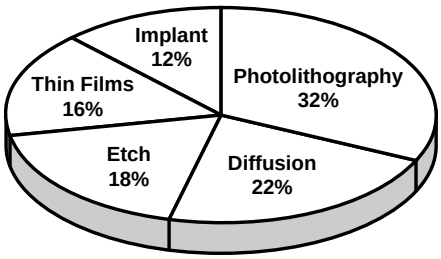


Figure 2-10. Relative Costs of Semiconductor Manufacturing Areas

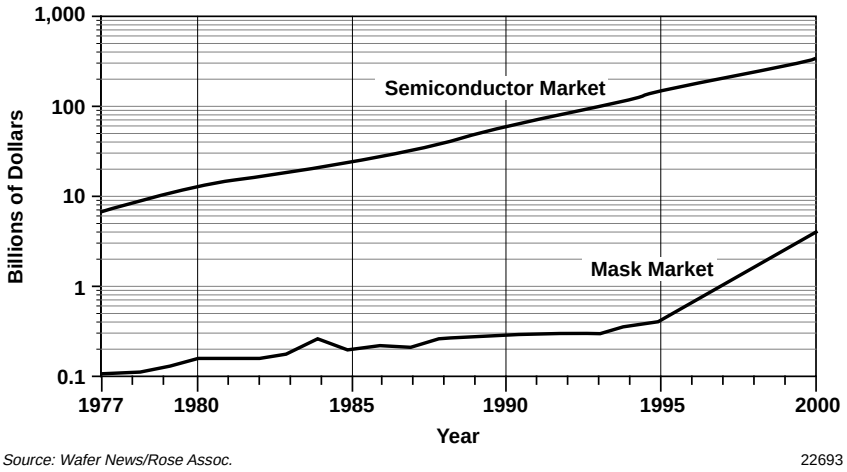


Figure 2-11. Growing Investment in Reticles and Masks

Long-term increases in depreciation and R&D expenditures continually challenge the cost-effectiveness of IC manufacturing. One metric used to examine overall cost effectiveness is asset turnover rate. Figure 2-12 shows that in the years preceding 1980, every dollar of net fixed assets generated greater than $3.00 in sales revenue. By 1987, asset turnover rate had fallen by 50 percent. However, recent trends indicate that asset turnover rates are stabilizing. However, further deterioration in the rate may affect the financial future of the industry. Once again, by making facilities and operations more cost effective, margins can be preserved and the rate of technological advancement can continue at its rapid pace. Astoundingly, the average employee of a merchant IC manufacturer in the U.S. is supported by $120,000 in net fixed assets (Figure 2-13).

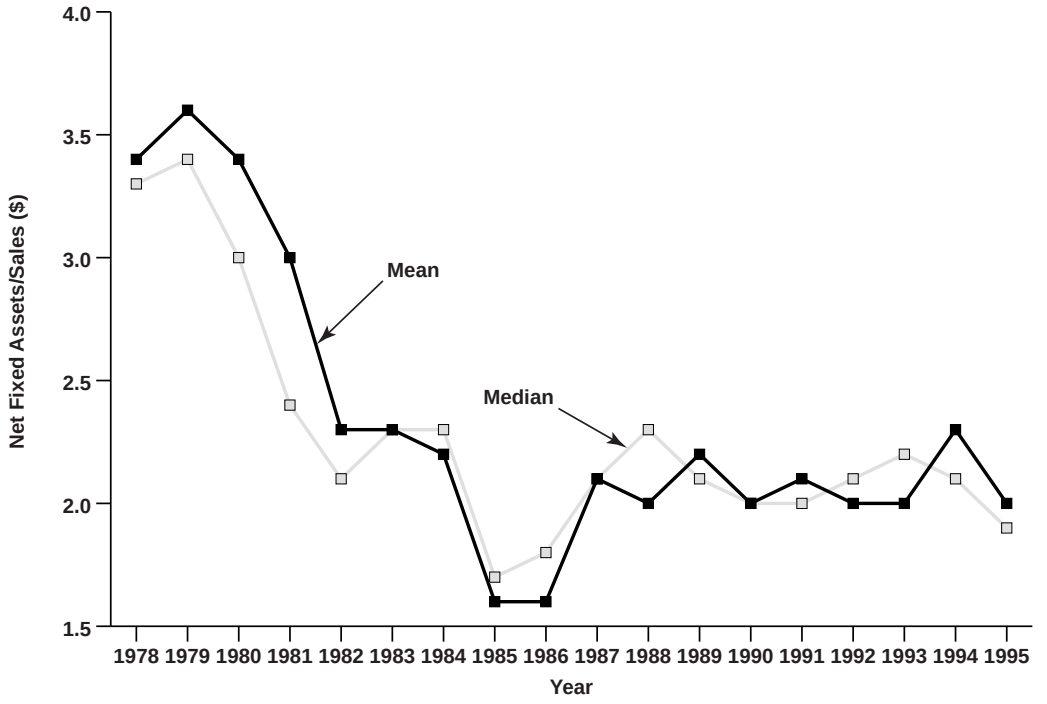


Figure 2-12. Net Fixed Assets Rise Faster Than Industry Revenues

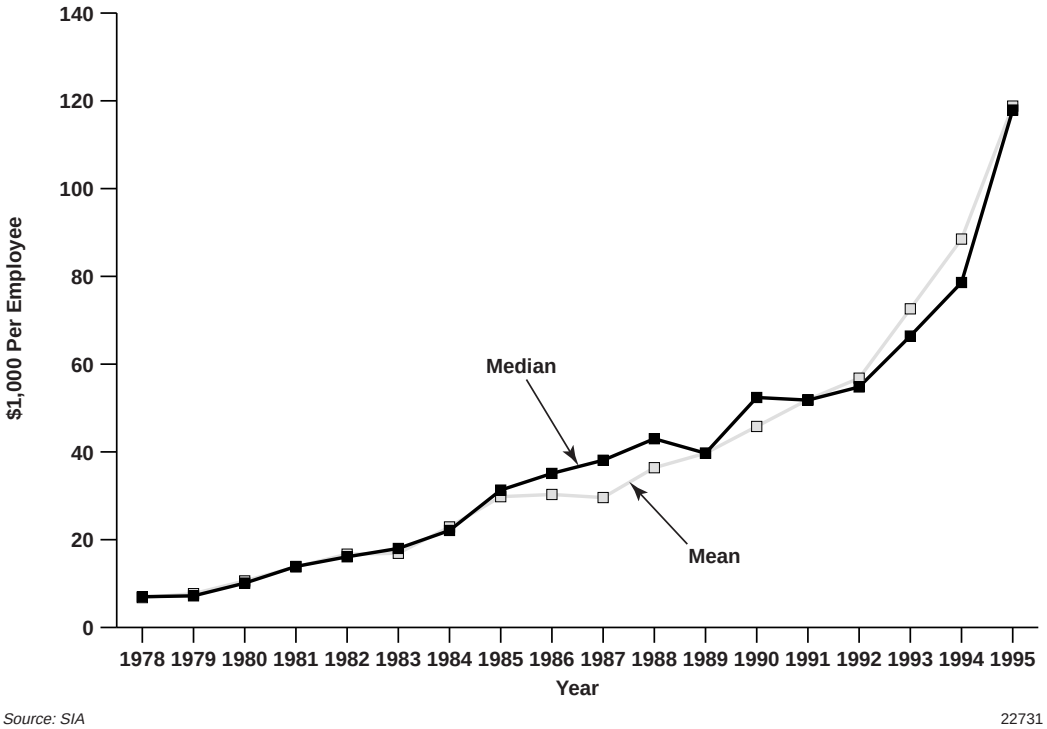
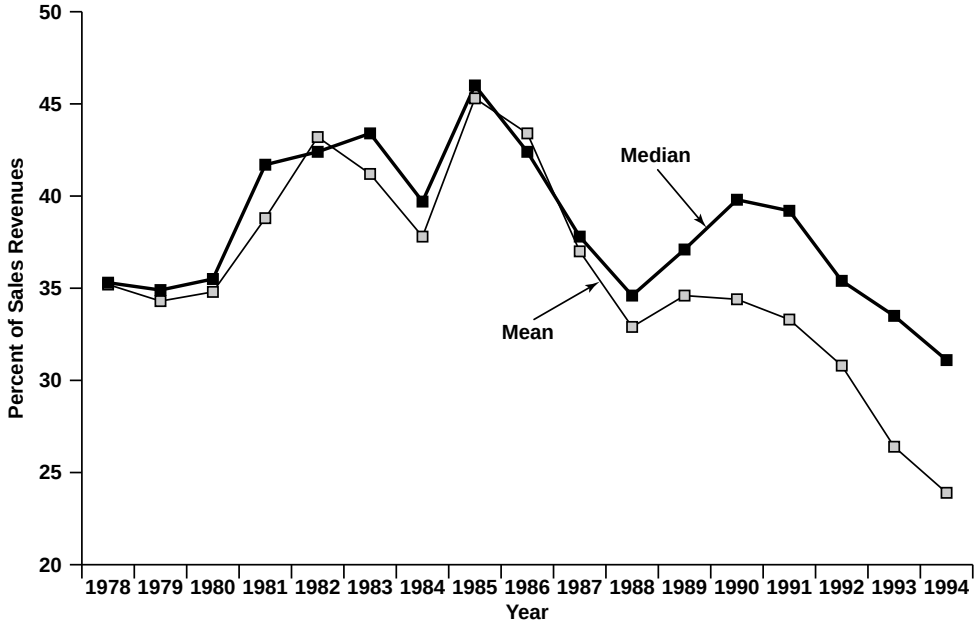


Figure 2-13. Net Fixed Assets Per Employee

The Cost of Labor

As semiconductor fabs become more automated and reliable, labor costs typically represent a smaller portion of total wafer processing costs. As shown back in Figure 2-1, total labor costs typically constitute 11.5 percent of overall cost per wafer for U.S. firms. Figure 2-14 shows how the total labor rate (including wages, salaries, payroll taxes, etc.) as a percent of sales for U.S. firms has dropped dramatically over the last several years and the divergence between the mean and median lines indicates that larger firms spend much less on labor than smaller IC manufacturers, which is expected. Figure 2-15 gives a sampling of salaries and wages earned by different individuals working in or around the fab.

By 1996, labor rate differences between the U.S. and Japan had diminished due to changing standards in Japan and the changing value of the yen (Figure 2-16). The semiconductor industry has become a truly global industry with fabs now emerging in all regions of the world. Regions that have recently attracted fabs include China, Malaysia, Thailand, India, and Eastern Europe. These countries offer the labor cost advantages that Japan once enjoyed over the U.S. It comes as no surprise that these regions, home to many assembly houses, are now being used for wafer processing. Such developing regions offer enormous growth potential, as evidenced in the growth of exports in developing regions relative to export growth in developed regions (Figure 2-17).



***Includes wages, salaries, retirement expenses, incentive compensation, payroll taxes**
****North American firms only**

Source: SIA 21072

Figure 2-14. Total Labor Expenses* as a Percent of Sales Revenues**

	Minimum 50th Percentile	Maximum Average
Semiconductor (Dollars/Hour)		
Operator Wafer Fab I	6.30	9.98
Operator Wafer Fab II	7.24	10.55
Operator Wafer Fab III	8.24	12.69
Semiconductor Specialist	9.49	14.78
Semiconductor Line Mech.	13.72	19.72
Semiconductor (Thousands of Dollars/Year)		
Process Engineer I	30.8	47.5
Process Engineer II	35.8	56.1
Process Engineer III	44.3	68.7
Process Technician	20.3	31.4
Sr. Process Technician	25.5	38.7
QA Technician I	18.2	27.1
QA Technician II	20.6	30.9
QA Technician III	24.3	36.7
QA Engineer	33.8	51.0
Elec. Management (Thousands of Dollars/Year)		
Process Development Manager	53.6	81.6
QA Manager	47.4	74.4
MIS Manager	49.6	78.4
R & D Manager	60.1	94.8
HR Manager	43.6	68.2
Compensation Manager	47.4	71.6
Emp. Relations Manager	50.4	80.8
Gen. Accounting Manager	43.4	68.2
Facilities Manager	43.2	68.6
Office Manager	31.0	47.4
Production Manager	41.1	64.7
Other Technical (Thousands of Dollars/Year)		
Test Engineer	34.5	52.8
CAD Operator I	20.5	30.5
Clerical (Thousands of Dollars/Year)		
Accounting Clerk I	15.7	23.4
Receptionist	16.6	23.9
Secretary	21.5	31.6
Executive Secretary	24.9	36.9
Administrative Assistant	24.8	37.3
Data Entry Operator	17.0	24.3

Definitions – Minimum 50th Percentile: The minimum salary range which is higher than 50% of all minimum ranges.
Maximum Average: The average of the maximum salary ranges reported.

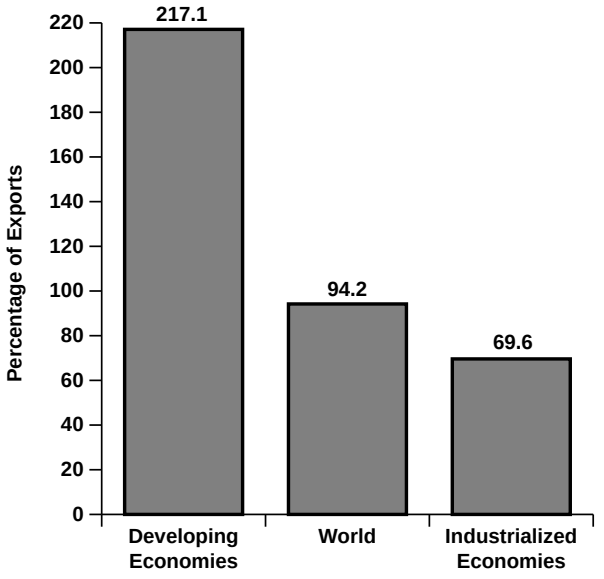
Source: American Electronics Assoc. 21076

Figure 2-15. Typical Industry Salary Ranges in U.S., West Coast

COST FACTOR	1996 U.S. WAFER FAB DIRECT LABOR RATE	JAPANESE WAFER FAB DIRECT LABOR RATE	
		1985 - 1986*	1996**
HOURLY RATE	$11.80	$5.50	$11.21
FRINGE RATE	35%	40%	40%
TOTAL	$15.93	$7.70	$15.69
LABOR COST PER WAFER TO PROBE (1.5 HOURS)	$23.90	$11.55	$23.54

*** 205 ¥ = $1.00**
****108¥ = $1.00**
Source: ICE
12030J

Figure 2-16. U.S. and Japanese 1995 IC Facility Direct Labor Costs



Source: Wall Street Journal/DRI/McGraw Hill
22701

Figure 2-17. Real Growth of Exports in the World, 1995-1996

Worldwide, the semiconductor industry employs roughly between 750,000 and a million people (Figure 2-18). Of these, approximately 260,000 are employed by North American merchant semiconductor manufacturers. Figure 2-19 shows the cyclical patterns in North American on-shore and off-shore employment levels in response to changing market condition. As shown, employment levels have increased significantly between 1992 and 1995, despite continual advances in labor productivity. In 1995, approximately 70 percent of the North American wages were disbursed to employees in North America, and the off-shore employee earns approximately one-third the salary of the employee based in North America, reflecting the semi-skilled labor at off-shore assembly operations as opposed to the base of highly-skilled and professional workers at North American facilities. This pay differential is narrowing slowly (Figure 2-20) as off-shore wages steadily increase.

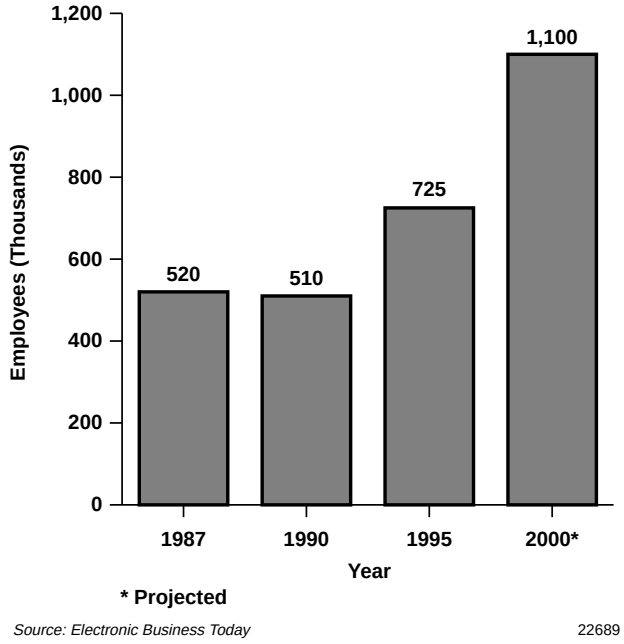


Figure 2-18. Worldwide Semiconductor Employment

Device Cost Modeling

Several years ago ICE developed a simplified cost model to examine manufacturing costs. The model estimate a company's gross margin and revenues for a given device based on the ASP for the devices at the time, and a calculation of device factory cost based on design rules, type of device, equipment cost, wafer size used, defect density estimates, etc. Among these assumptions, defect density is the most critical. Through fab benchmarking studies and cost modeling, ICE developed the wafer cost estimates shown in Figure 2-21.

Figures 2-22 and 2-23 show cost model results for a Pentium microprocessor and 16M and 64M DRAM devices in first quarter 1997. As shown, the advanced-generation Pentium device yields a significant gross margin as little competition exists in this marketplace. As the advanced-generation Pentiums mature and are replaced by the Pentium Pro device, Intel will continue to lower the price of this processor more dramatically and improve yields more quickly to preserve margins.

The margins on DRAM devices, however, have dramatically declined in the past year, forcing important changes in the 16M DRAM market and the adoption of 64M technology. At least some DRAM manufacturers are accelerating their transition to 64M production due to the slim profit margins of 16M devices, as illustrated in Figure 2-23. At the same time, manufacturers are rapidly shrinking the die size of 16M devices from typical levels of 80mm2 to as small as 60mm2 to preserve yields and margins.

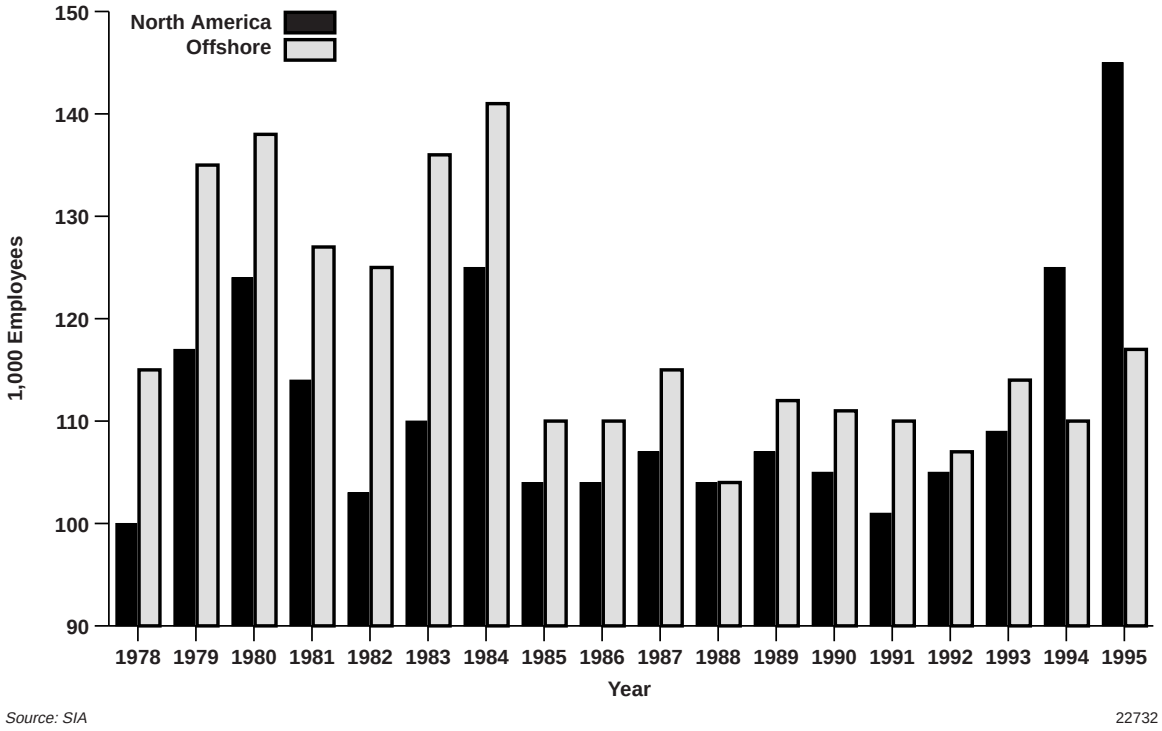


Figure 2-19. North America and Offshore Employment Levels

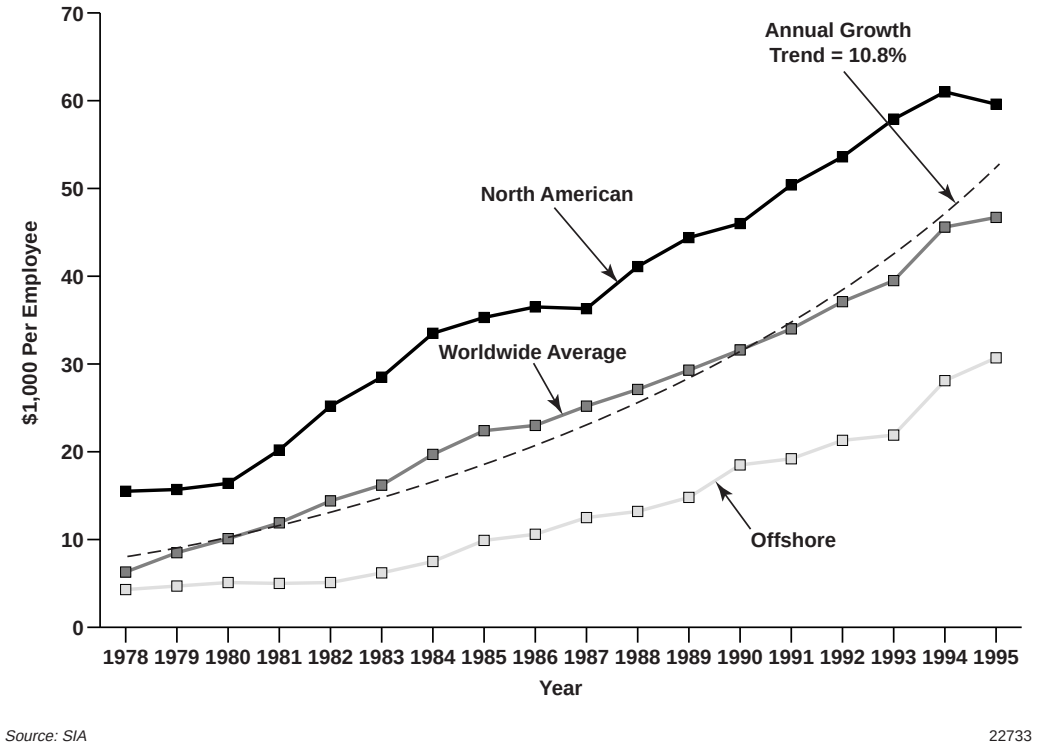


Figure 2-20. Labor Expenses Per Employee

Feature Size (μm)	Wafer Size (mm)	Process Technology					
		CMOS 14-16 Masks	Advanced CMOS 18-20 Masks	Advanced BiCMOS 22 Masks	Bipolar 8-10 Masks	Bipolar 14-16 Masks	Advanced Bipolar 22 Masks
1.5	125	170	—	360	210	245	360
1.0	125/150	—/310	—	—/575	—	270/—	—/575
0.8	150/200	390/—	600/990	660/—	—	—	660/—
0.5	150/200	525/—	700/1,140	900/1,400	—	—	900/—
0.35	200	—	1,415	1,800	—	—	—

Source: ICE 20279A

Figure 2-21. Whole Wafer Cost Before Probe ($)

	BiCMOS MPU (0.35μ)
Tested Wafer Cost	$1,890 (200mm epi wafer)
Die Size	135,000 sq mils (90mm^2)
Total Dice Available	292
Probe Yield	37% (at 1.2 defects/cm^2)
Number Of Good Dice	108
Package Cost	$25.75 (296-pin CPGA)
Assembly Yield	99%
Final Test Cost	$35.00
Final Test Yield	70%
Factory Cost	$112.41
ASP (1,000)	$350
Approx. Revenue/Wafer Start	$26,195
Revenue/Sq In. Started	$542
Gross Margin	68%

Source: ICE 14448G

Figure 2-22. Pentium (166MHz P54CS) Cost Analysis (3Q96)

DRAM, MPU and ASIC Manufacturing Costs

The semiconductor industry has traditionally been driven by the needs of the DRAM manufacturers because these companies are the single largest consumers of semiconductor equipment and materials, and because DRAM devices, until recently, were the technology drivers. In recent years, microprocessors have become the technology driver as Intel has speeded its transitions to smaller feature sizes faster than the transitions in the DRAM device sector. In addition, the manufacturing technology using multilevel metalization designs of 5 layers or more is driven by needs of the microprocessor supplier. The industry therefore has two very strong segments, DRAMs and microprocessors, driving the designs of process equipment, facilities, automation and factory management.

DRAM manufacturers produce ICs in high volume, thereby driving the development of equipment that delivers the highest throughput possible, while meeting processing

requirements that vary little within a given facility. For instance, a fab may be producing 1M DRAMs and 4M DRAMs, while running pilot line production and design of 16M and 64M DRAMs, respectively. In addition, different versions of the same generation may be produced, for instance, for 3.3V and 5.0V operation, or 4x4 and 1x16 bit cell configurations. Due to the small differences in processing requirements for these devices, generally two generations of equipment are found in DRAM fabs. High-volume production also means that production lots of 24 wafers at a time are almost always run, and engineers have the luxury of dedicating process tools to certain processes, thereby improving processing results.

At the other extreme are ASIC manufacturers. ASIC production means that lot sizes vary from one to twenty-four wafers; every lot has a different mask set; wafers are produced in small volume; the product line contains several generations of equipment; and the fab must be constructed to be very responsive to changes. ASICs are also more difficult to analyze than memory devices. Memories are highly testable structures and yield learning is only performed once for a product that will be manufactured for 8-10 years. ROI typically takes 2-3 years for each new generation of DRAMs. For ASICs, there is very little time for yield learning and reliability studies. The delivered design must be "fool-proof," negating the need for failure analysis and yield analysis. Acceptable yield from the time manufacturing is started is a prerequisite for ROI over a few months, and the guarantee that delivery dates are met. For these reasons, simulation plays a large role in device and process development for ASICs, whereas process simulation for memories is not traditionally performed, and pilot runs suffice. In general, ASIC manufacturing also drives the development of computer aided design and factory control software, and packaging technology, due to larger chip sizes of varying dimensions.

	16M DRAM (0.35μ)	64M DRAM (0.35μ)
Tested Wafer Cost	$1,180 (200mm)	$1,485 (200mm)
Die Size	84,000 sq mils (54mm^2)	232,500 sq mils (150mm^2)
Total Dice Available	476	162
Probe Yield	80% (at 0.5 defects/cm^2)	40% (at 0.7 defects/cm^2)
Number Of Good Dice	380	65
Package Cost	$0.40	$0.50
Assembly Yield	99%	99%
Final Test Cost	$0.60	$1.20
Final Test Yield	95%	85%
Factory Cost	$4.36	$29.15
ASP	$7.75	$55.00
Approx. Revenue/Wafer Start	$2,770	$3,008
Revenue/Sq In. Started	$55	$60
Gross Margin	44%	47%

Source: ICE 16912G

Figure 2-23. 16M and 64M DRAM Cost Analysis

Figure 2-24 shows further differences between DRAM and ASIC manufacturing. The high-volume DRAM manufacturing lines suffer little from reconfiguration and capacity additions relative to ASIC fabs. The cost benefits due to automated scheduling, and wafer and mask tracking for ASICs outweigh the same benefits to the DRAM manufacturer. However, too much automation can inhibit flexibility. In addition, equipment reliability, mean time to repair (MTTR), and the importance of being able to quickly make real-time process changes, are much more important to the ASIC manufacturer. Development equipment must be extremely comparable to manufacturing equipment as yield ramp-up for ASICs must be minimized.

As far as manufacturing cycle time and work in process (WIP) are concerned, the fab with a greater number of different products being processed at once (greater variability) will reach higher levels of WIP and longer cycle times, faster (Figure 2-25). Achieving low cycle time in the presence of variability requires either flexible equipment or idle time.

Other Key Cost Trends

In addition to product yield, cycle time, labor costs, and equipment productivity, important components in cost per wafer include the cost of equipment maintenance, test wafers, and consumables. Although discussing every cost components in detail is beyond the scope of this book, some highlights provides insight into their importance:

- Contracted maintenance costs vary between nothing ($0) for the first two years, to up to $400,000 per tool per year, depending on the equipment supplier and terms of the contract.

- Equipment installation, including tool hook-up and the running of test wafers to full qualification, typically adds 35 percent to the price of the tool.

- The cost of cleaning gases for single-wafer tools is significantly higher than for batch tools. In-situ cleaning procedures also contribute significantly to tool downtime.

Issues	Measure	ASIC	DRAM
Modularity	Cost of Reconfiguration	High	Low
	Cost of Capacity Additions	High	Medium
Benefits Due to Computer Integrated Manufacturing	Automated Downloading	High	Low
	Wafer/Mask Tracking	High	Low
	Scheduling	High	Low
Important Equipment Characteristics	Reliability	High	Medium
	MTTR	High	Medium
	Defect Free	Medium	High
	Real Time Process Change	High	Medium
	Dev. Eqpt. = Mfg. Eqpt.	High	Medium

Source: Motorola 19775

Figure 2-24. Relative Fab Characteristics

- Test wafer cost rises dramatically at the 200mm level as manufacturers use prime polished wafers, rather than reclaimed wafers, for process monitoring.

- Studies indicate that some fabs are spending $1 million or more a month on test wafers, which does not include the cost of lost productivity when tools are running these wafers[3].

Conclusions

A company's ability to drive down cost per wafer requires an understanding of the cost components. Cost competitiveness is absolutely essential regardless of device market due to the true globalization of today's semiconductor market.

References

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2. 1978-1995 Industry Data Book, *Semiconductor Industry Association*
3. S. Billat, "Process Control: Covering All of the Bases," *Semiconductor International*, Sept. 1993, p. 78.

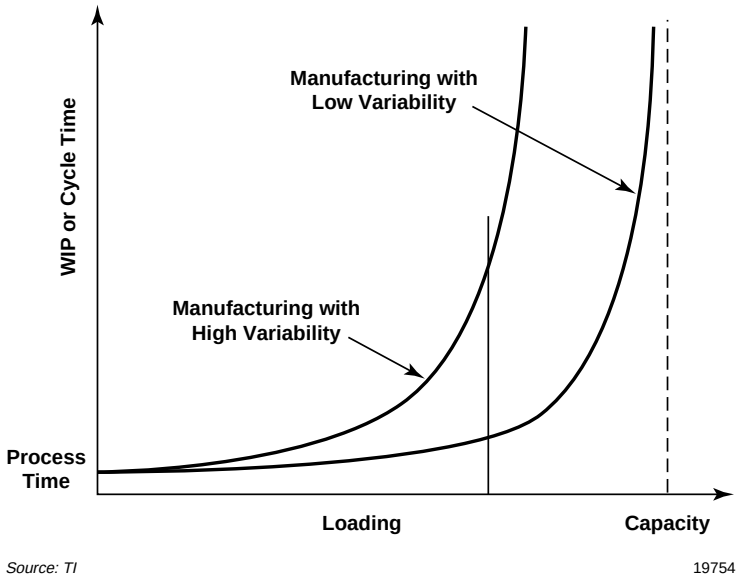

Figure 2-25. The Effect of Variability on WIP and Cycle Time