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# *Cree's SiC Power MOSFET Technology: Present Status and Future Perspective*

**Lin Cheng and John W. Palmour**

***Cree, Inc.***

***August 14, 2014***

**9th Annual SiC MOS Workshop, UMD, USA, Aug 14-15, 2014**

# Outline

- The last frontier for SiC Power MOSFETs
- Breakthrough in SiC MOS Stability & Reliability
- Next-Generation SiC Power MOSFETs
- Future Perspective

# The Last Frontier for SiC - Cost

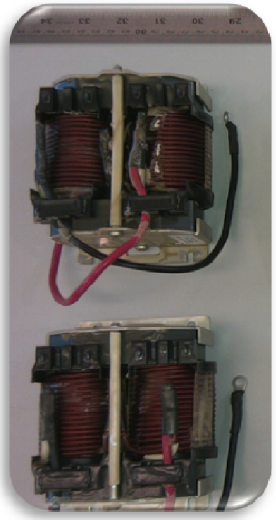
**Performance** ✓

**Reliability** ✓

**Cost:**

- ✓ by optimal chip design
- ✓ by improved Fab yield
- ✓ by robust reliability

- SiC solution is 60% smaller at ≥ 20% lower cost than Si solution.

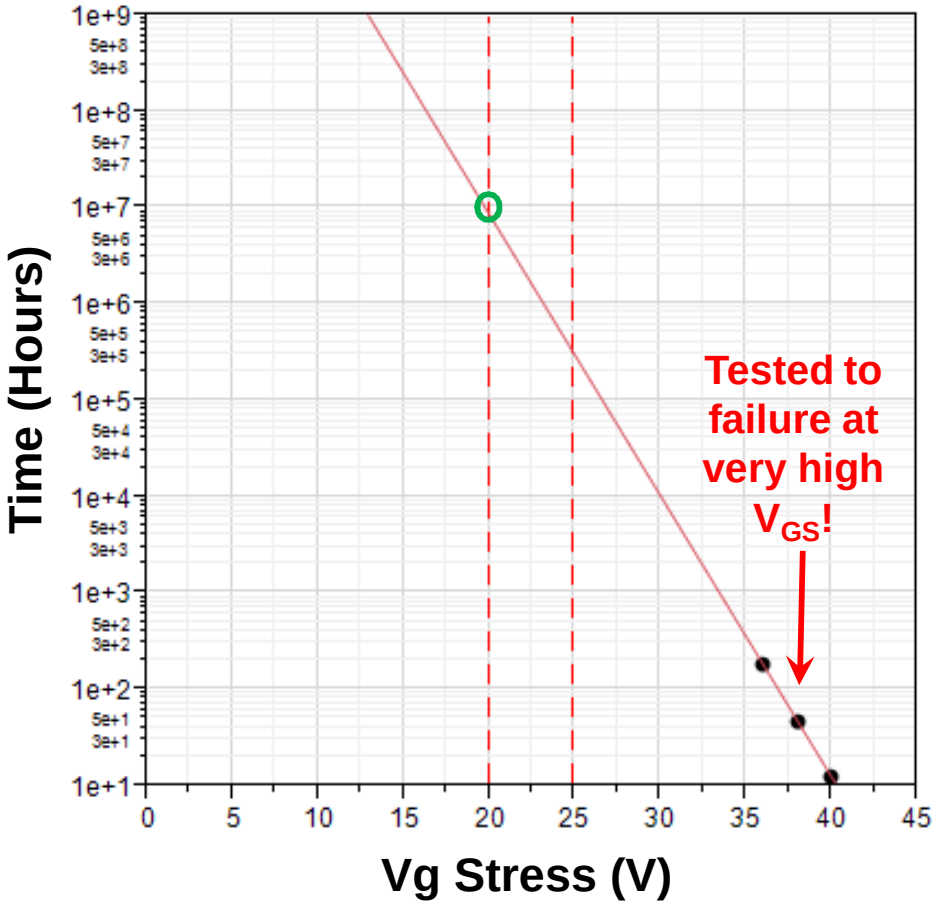


Transformer at 20 kHz


Transformer at 100 kHz

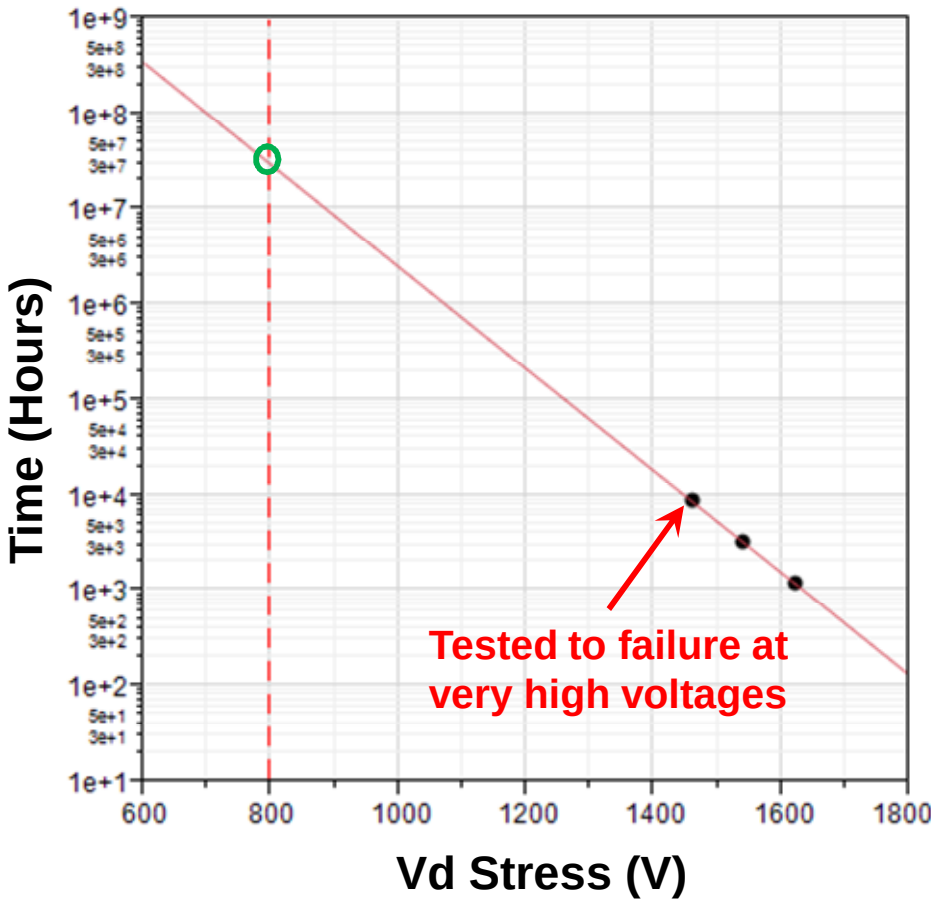
# Long-term Reliability

**Extrapolated MTTF of**
**~ $10^7$ hours at $V_{GS}$ = 20V**




**TDDB of Gate Oxide on 1200 V/80 mΩ Gen 2 MOSFETs at 150°C**

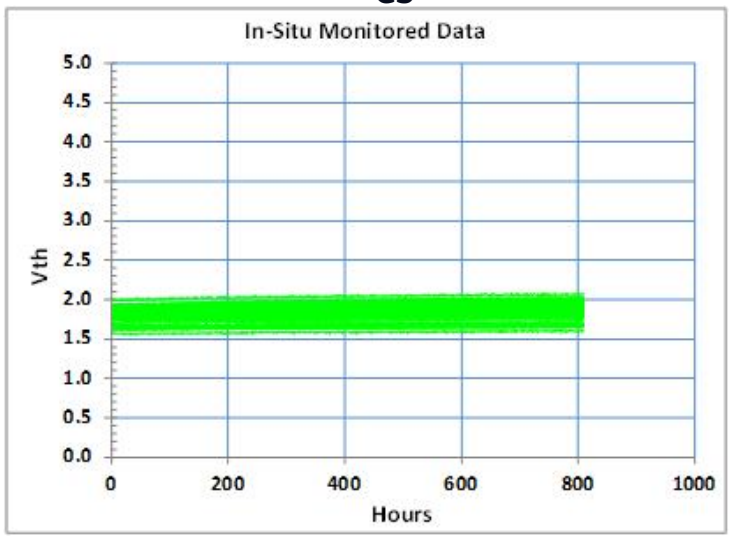
**Extrapolated MTTF of**
**~ 3 x $10^7$ hours at $V_{DS}$ = 800 V**



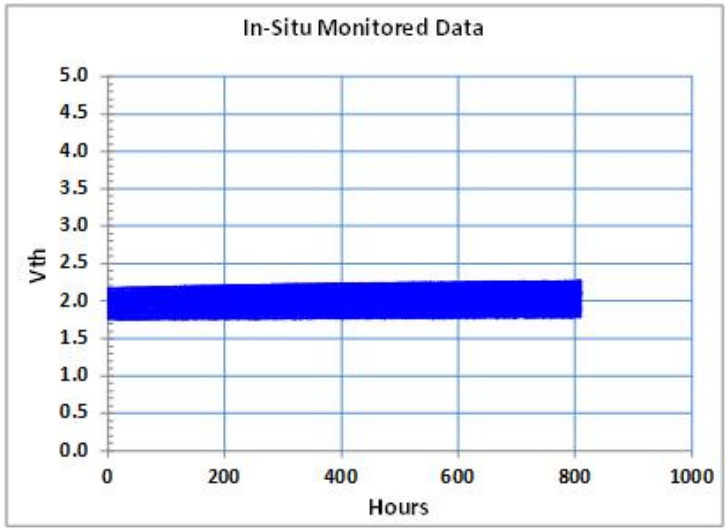

**Accelerated HTRB Testing at 150°C**

# Qualification Data for NBTS at 150°C: 3 Lots x 75 Parts

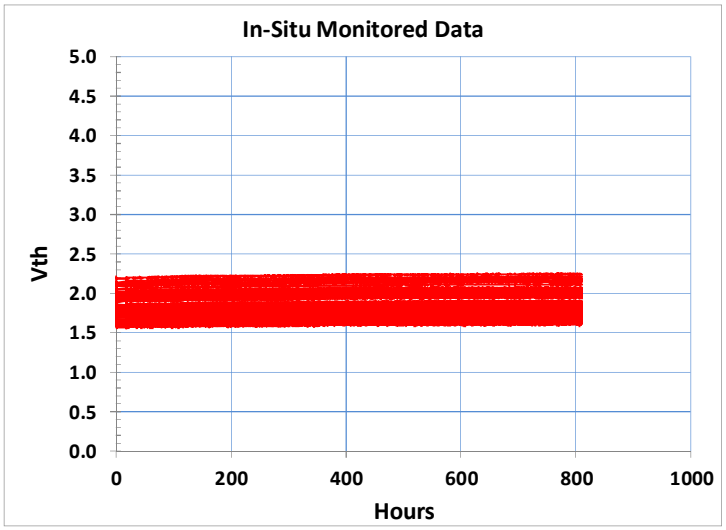
**HTGB at 150°C $V_{GS}$ =-10 V Lot 1**




**HTGB at 150°C $V_{GS}$ =-10 V Lot 2**



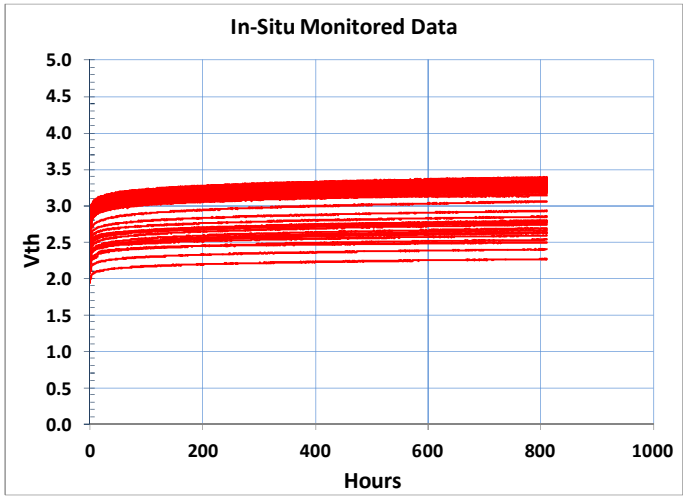

**HTGB at 150°C $V_{GS}$ =-10 V Lot 3**



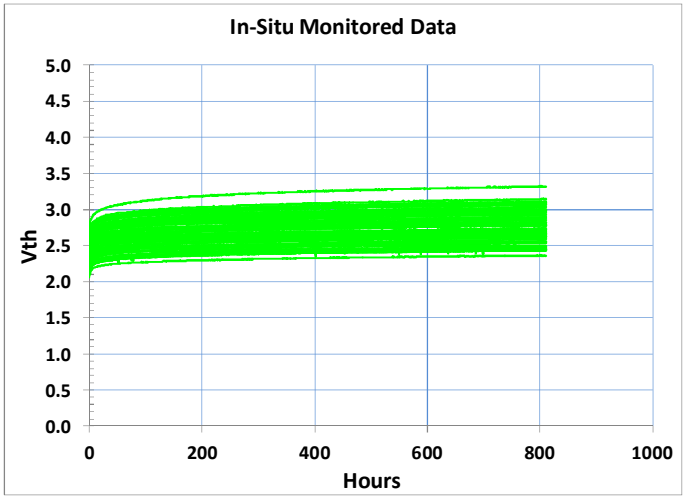

- **C2M (1200 V/80 mΩ) SiC MOSFETs rated for Max. $V_{GS}$ of -10 V.**
- **Full automotive qualification running to demonstrate 1,000 hours of $V_{TH}$ stability at 150°C**
- **New process started shipping into distribution in April 2014**

# Qualification Data for PBTS at 150°C: 3 Lots x 75 Parts

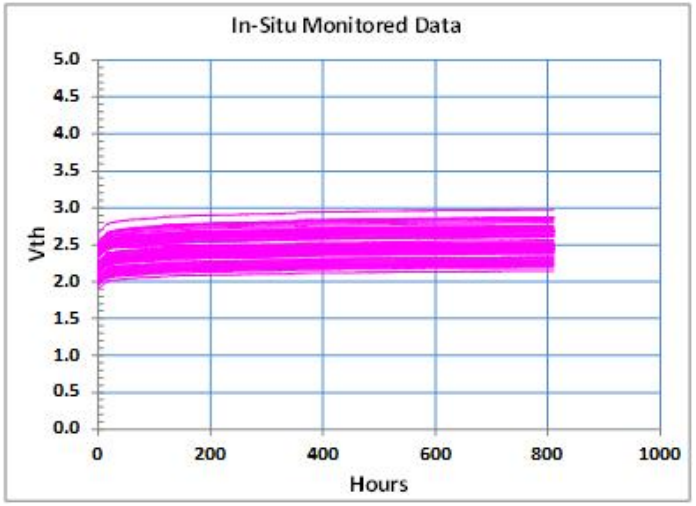
**HTGB at 150°C $V_{GS}$ =25 V Lot 1**




**HTGB at 150°C $V_{GS}$ =25 V Lot 2**



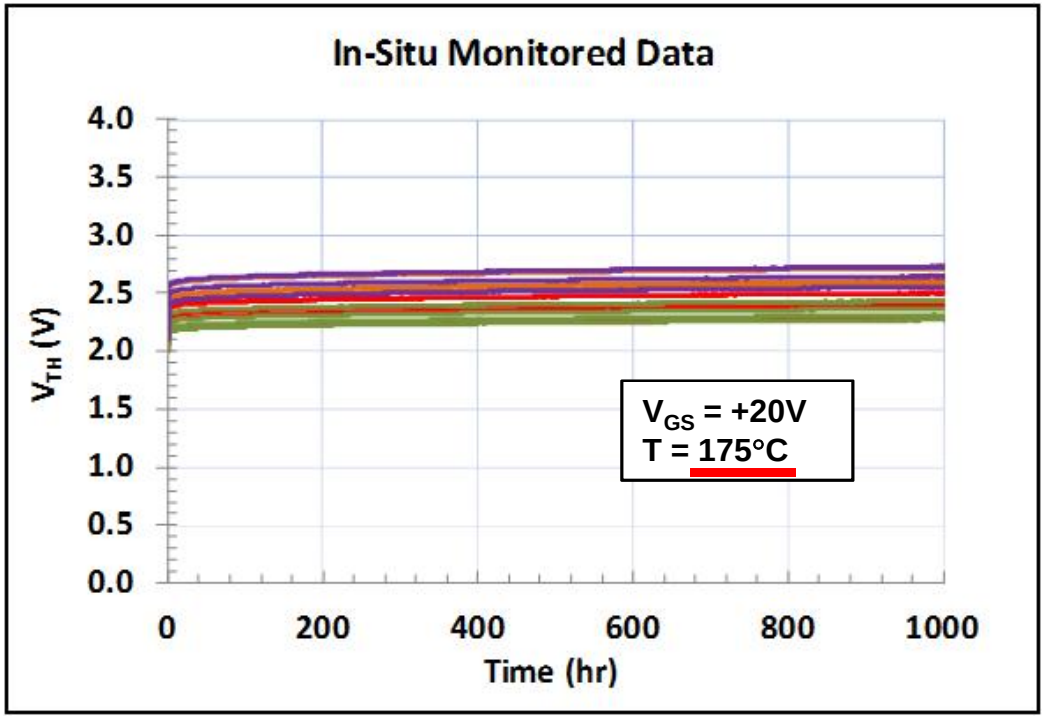

**HTGB at 150°C $V_{GS}$ =25 V Lot 3**



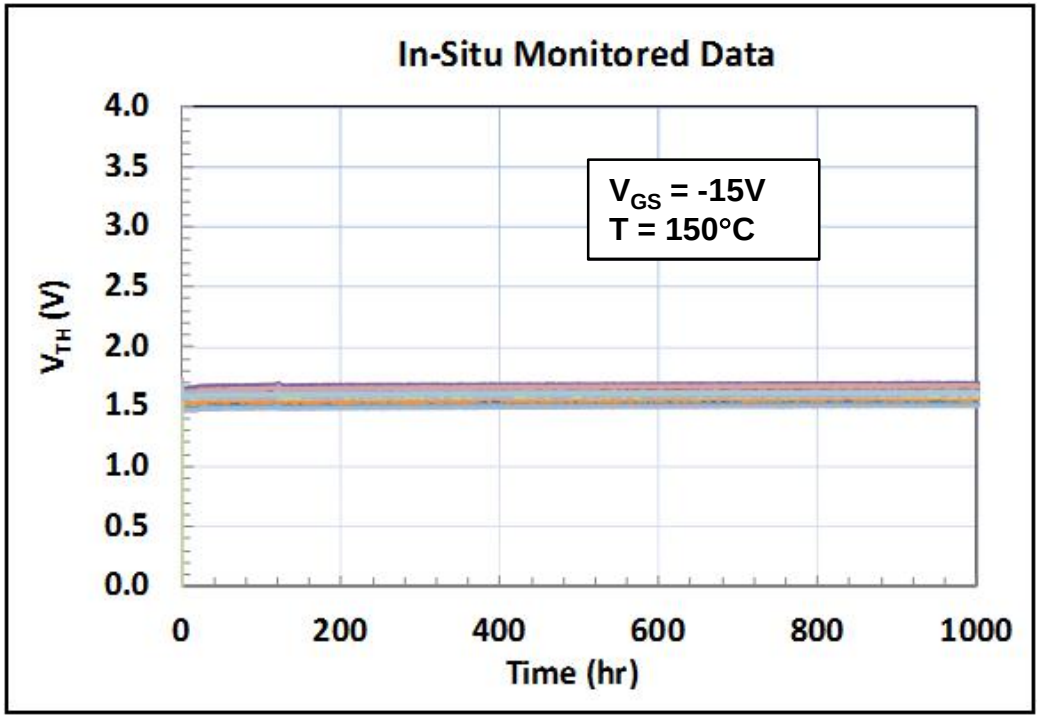

- **C2M (1200 V/80 mΩ) SiC MOSFETs rated for Max. $V_{GS}$ of +25 V.**
- **Full automotive qualification running to demonstrate 1,000 hours of $V_{TH}$ stability at 150°C**
- **New process started shipping into distribution in April 2014**

# C2M $V_{TH}$ Stability Under ± BTS Beyond Datasheet Specs

**Positive Bias (PBTS) Accelerated at 175°C**

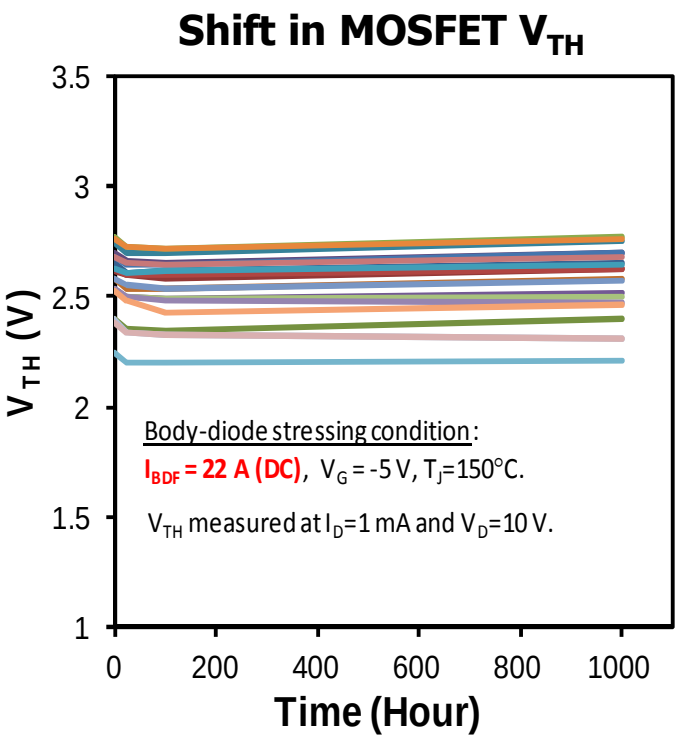


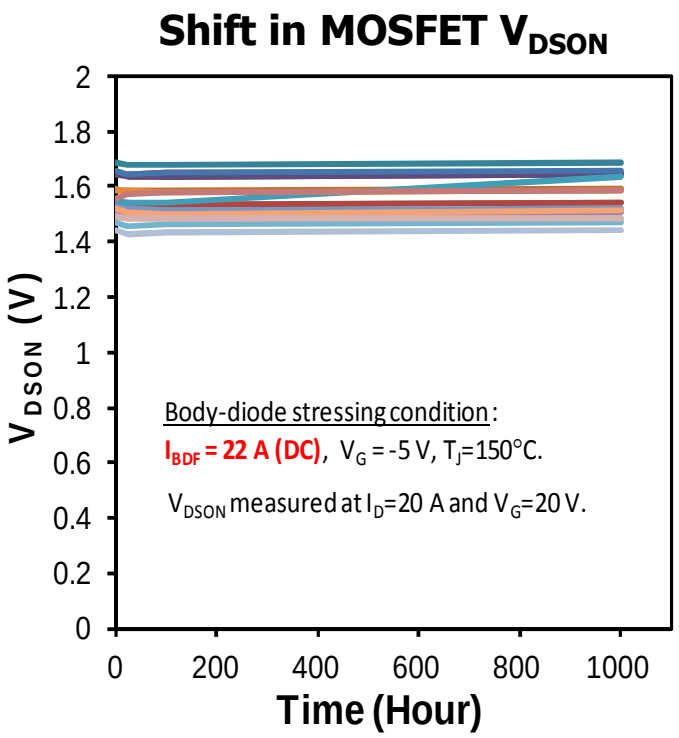

**Negative Bias (NBTS) Accelerated at -15 V**

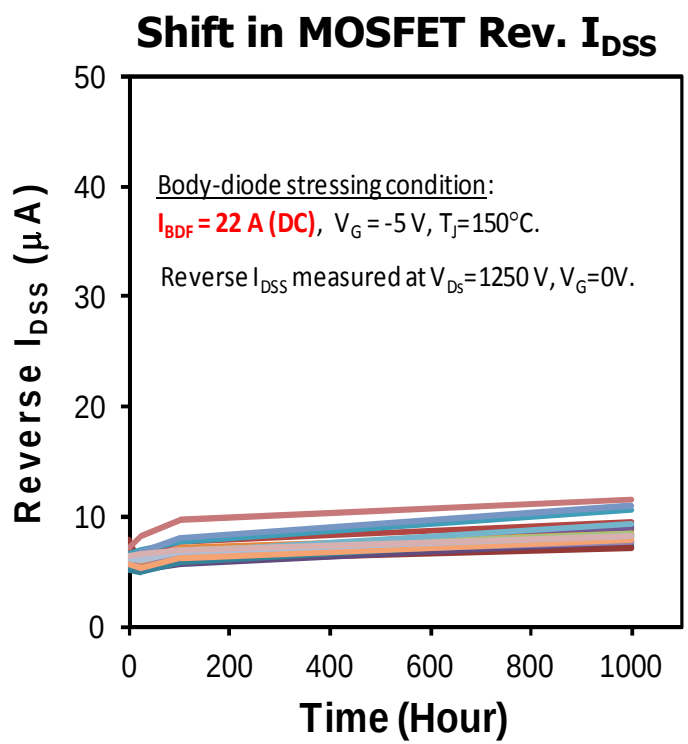



- **Extremely stable for 1,000 hours under ± BTS at elevated temp.**
  - **Accelerated beyond data sheet to see any measurable change**
  - **Average shift under positive bias: $\Delta V_{TH}$ = 0.06 V**
  - **Average shift under negative bias: $\Delta V_{TH}$ = 0.01 V**

# C2M Body Diode Stress @ 110% Rated $I_{DS}$(DC), 150°C



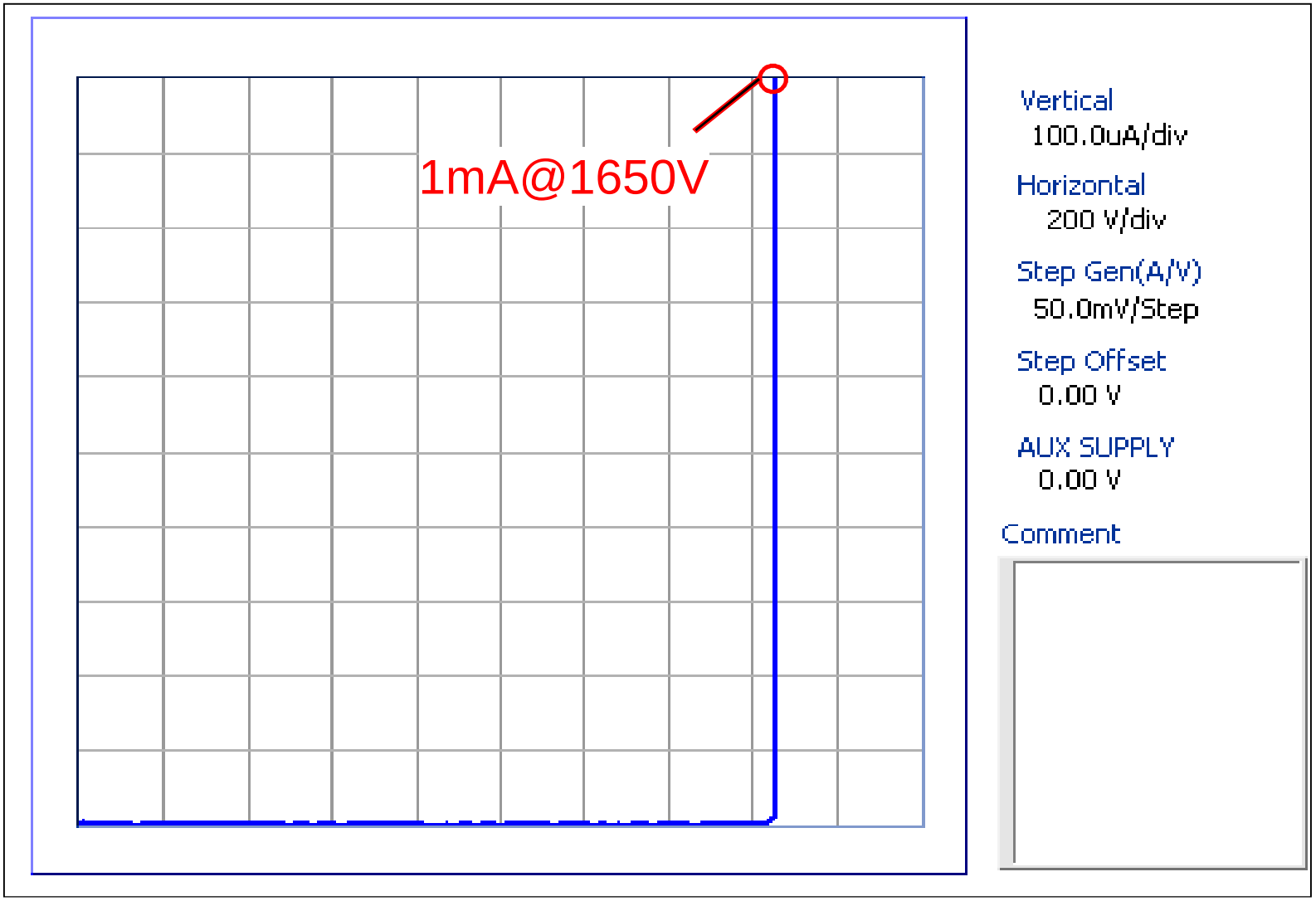




- **Negligible shifts in MOSFET $V_{TH}$, $V_{DSON}$, $I_R$ after 1,000 hrs body diode stress at $I_{DS}$ = 22 A (DC), $V_{GS}$ = -5 V, 150°C:**
  - 20 x C2M0080120D (1200 V/80 mΩ) SiC MOSFEFTs
  - Max. $\Delta V_{TH}$ of MOSFET < 0.02 V, average $\Delta V_{TH}$ ~ 0.002 V.
  - Max. $\Delta V_{DSON}$ of MOSFET < 0.09 V, average $\Delta V_{DSON}$ ~ 0.01 V.
  - Max. $\Delta I_{DSS}$ of MOSFET < 5 μA, average $\Delta I_{DSS}$ ~ 2.8 μA.

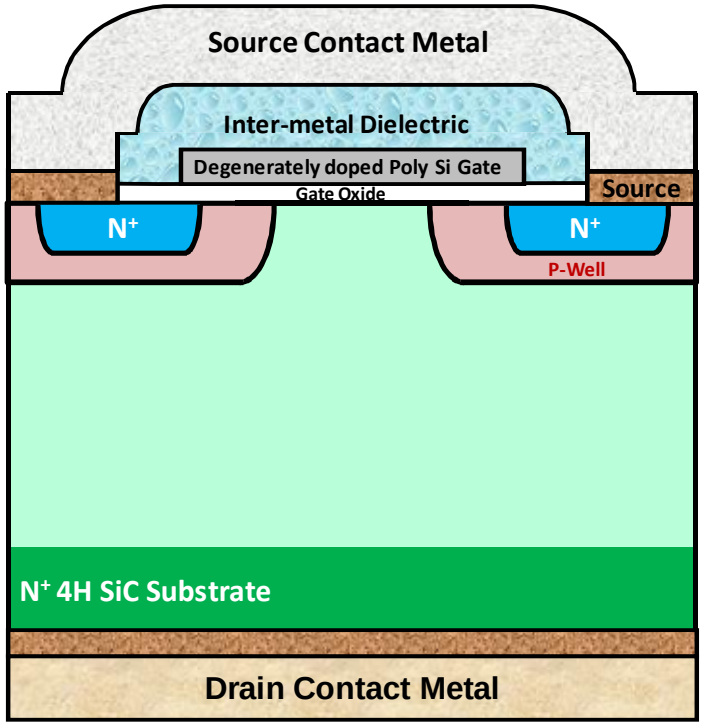
# Avalanche Ruggedness of C2M SiC MOSFETs

## Unclamped Inductive Switching (UIS) Testing

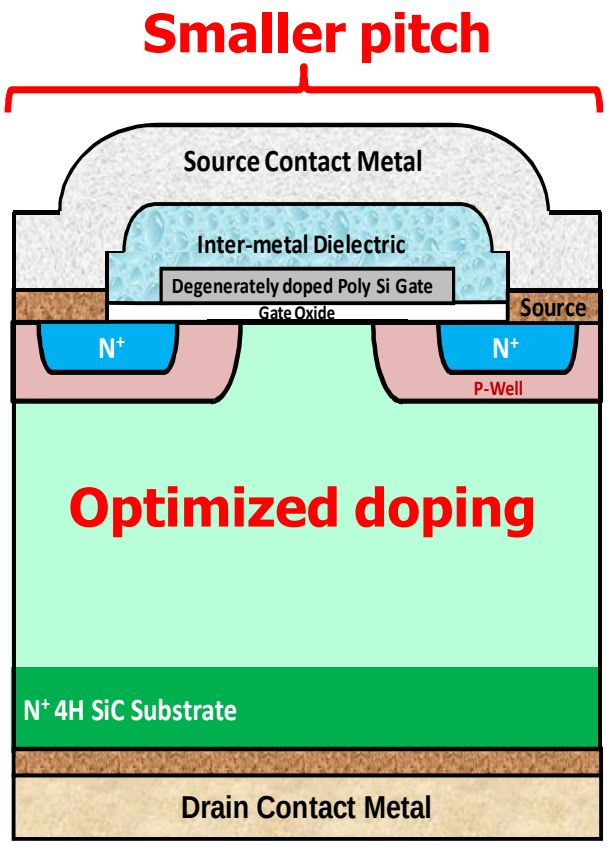


# Further reduction in $R_{ON,SP}$ of Cree's 3rd Generation SiC Power MOSFETs since last MOS Workshop in August, 2013

# 3rd Generation (Gen-3) SiC MOSFETs




Gen-2 DMOS




Gen-3 DMOS

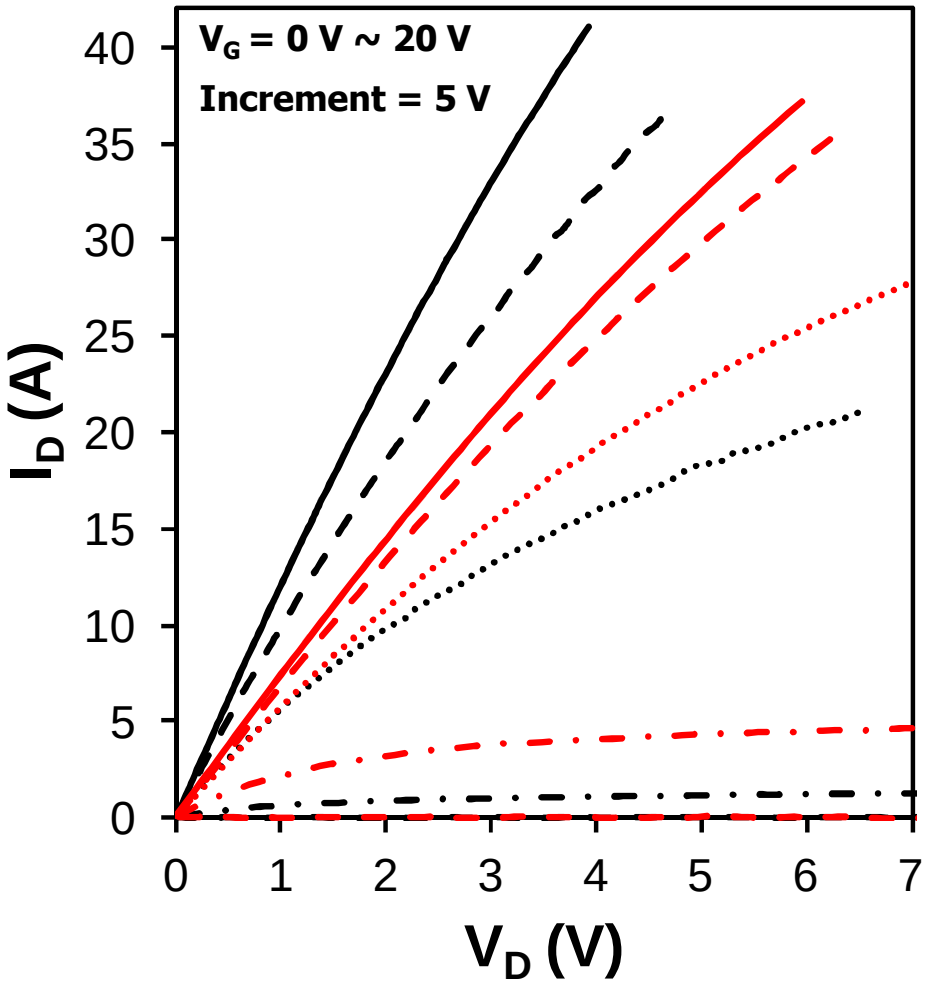
**Same high-reliability DMOSFET Structure, but optimized to dramatically reduce die size.**

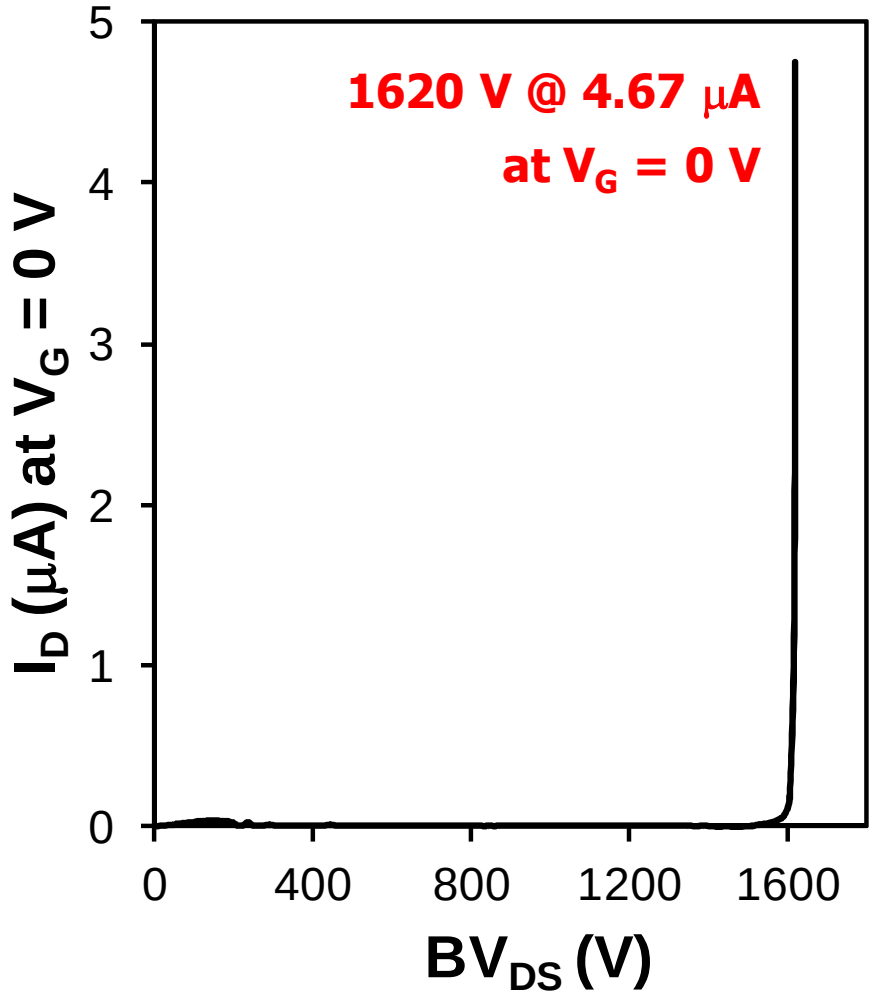
# 1200 V/80 mΩ, Gen-3 MOSFETs: 2.7 mΩ.cm² in R&D, 2014

**At $V_G$ = 20 V, $I_D$ = 15 A:**

- $R_{ON,SP}$ (25°C) = 2.7 mΩ·cm²
- $R_{ON,SP}$ (150°C) = 4.9 mΩ·cm²

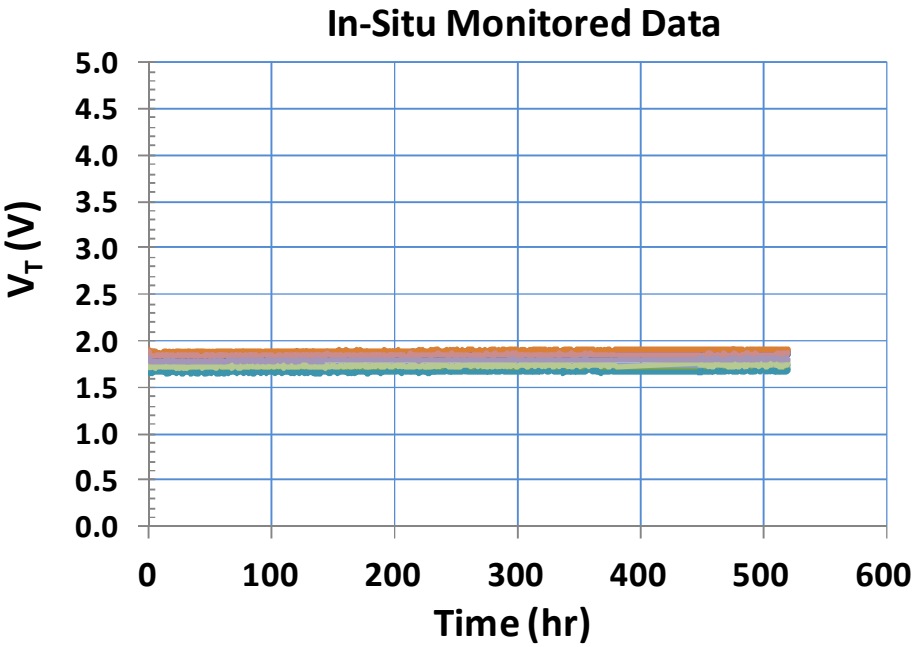
- $A_{die}$ = 6.82 mm² (2.35 x 2.9)
- Active area: 3.41 mm²



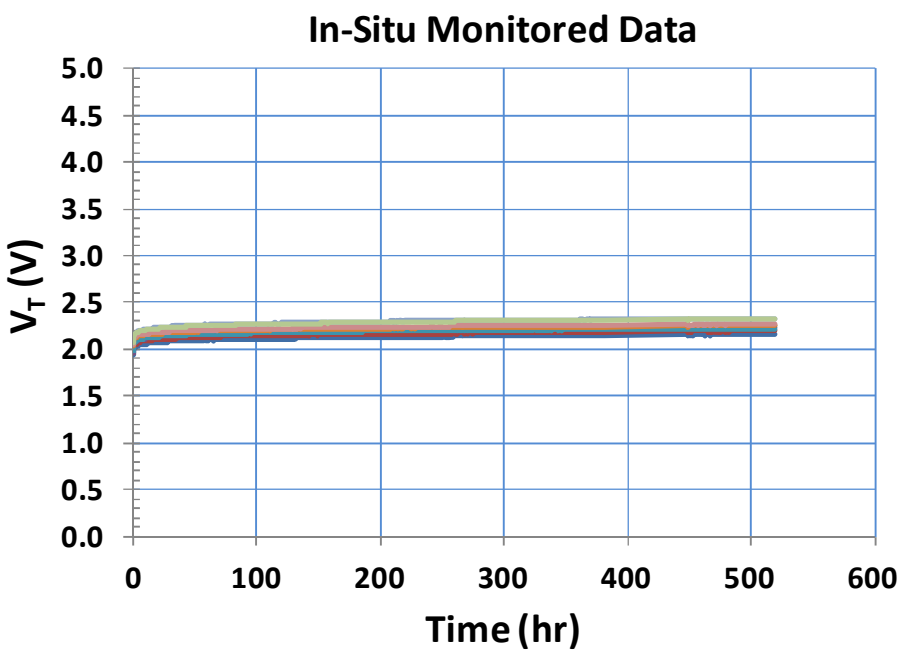



# Negligible ± BTS $V_{TH}$ shifts for Gen-3 MOSFET at 175°C

## NBTS at 175°C, $V_{GS}$ = -10V



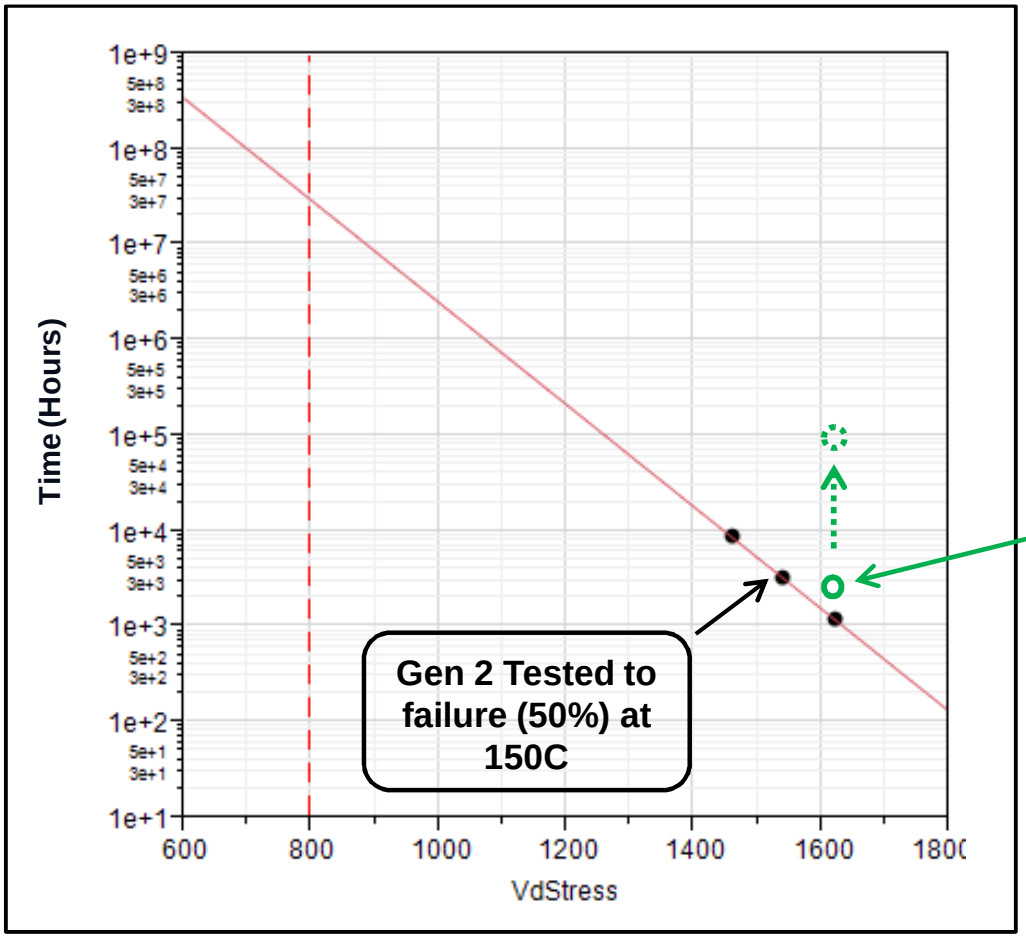

## PBTS at 175°C, $V_{GS}$ =+20V




- Excellent $V_{TH}$ stability is demonstrated repeatedly at 175°C
- Same excellent gate yield and repeatability as Gen-2 MOSFET in volume production

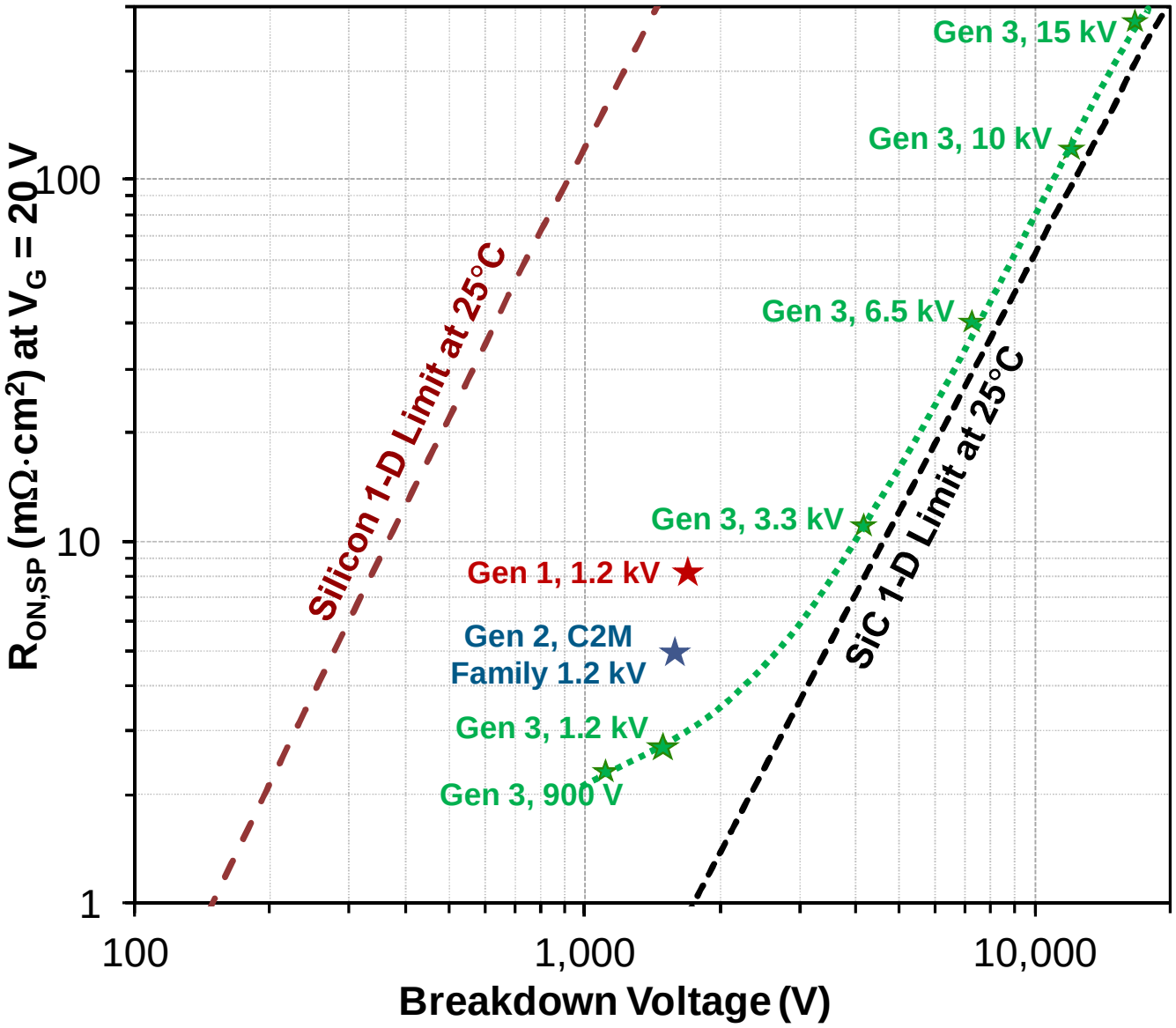
# Gen-3 MTTF Lifetime Higher Than Gen-2 MOSFETs

## MTTF Prediction from Accelerated Field Testing




- Gen 2 Extrapolated MTTF of 3E7 hours at $V_{DS}$ = 800 V and 150C
- Gen 3 lifetimes are higher than Gen 2 at 175°C

# Scaling of State-of-Art Gen-3 SiC Power MOSFETs in R&D




- $R_{Ch}/R_{ON}$ becomes larger for lower-V MOSFETs.
- For Gen-3 1200V MOSFET, $R_{Ch}$ > 40% of total $R_{ON}$.

**Future Prospective**

- Reduce $R_{Ch}/R_{ON}$ by:
  - Improving MOS $\mu_{INV}$
  - Higher packing density

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# *High-mobility 4H-SiC (0001) MOSFETs with Chemically Modified MOS-Interface*

**Daniel J. Lichtenwalner, Lin Cheng, & John W. Palmour**

*Jointly funded by Cree IR&D and Army HEPS Programs*

***Cree, Inc.***

***August 14, 2014***

**9th Annual SiC MOS Workshop, UMD, USA, Aug 14-15, 2014**

# OUTLINE

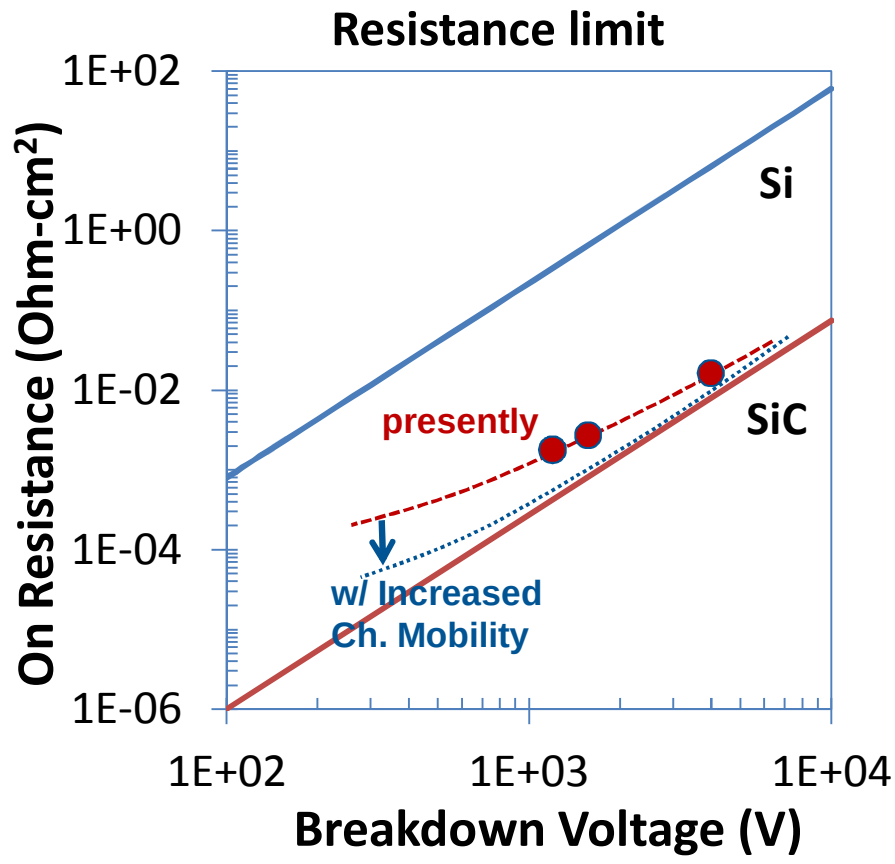
1. Motivation
    1. Channel resistance
    2. MOS interface passivation
2. Experimental: interface modification
    1. Device Fabrication
    2. Measurements
3. MOSFET channel properties (All data reserved to be published later)
    1. Field-Effect Mobility
    2. MOS Interface charge
4. MOSFET gate oxide properties (All data reserved to be published later)
    1. Material characterization
    2. Electrical properties
5. Summary

# 1.1 MOSFET channel resistance

- Graph shows resistance limits due to drift layer.
- For low voltage devices, channel resistance becomes a large % of total device resistance.

**Ways to lower $R_{chan}$:**

- Increase channel packing density
- **improve channel mobility**



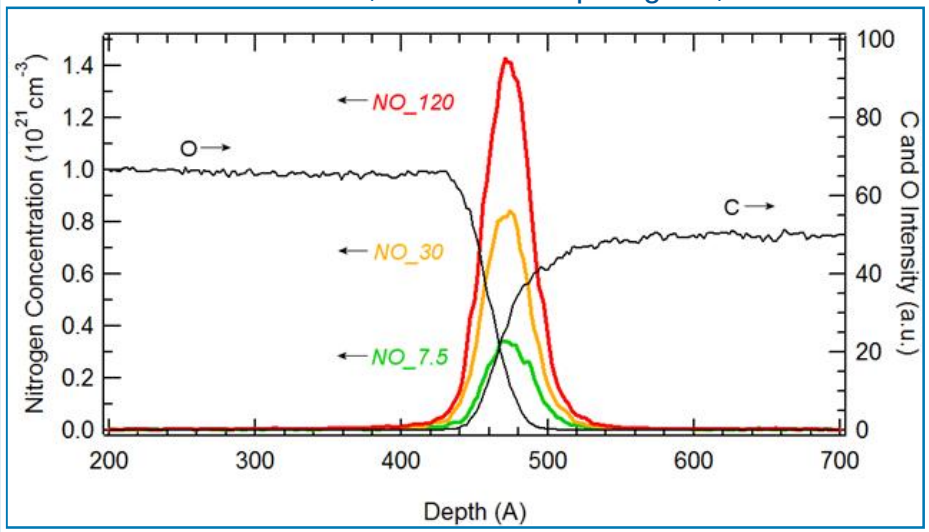

e.g., 1700$V_{BD}$: $R_{ch}$ ~25% of $R_{on}$
600$V_{BD}$: $R_{ch}$ ~40% of $R_{on}$

# 1.2 MOS interface passivation (Group V)

## NO, $N_2O$ anneal:

- **FE Mobility ~35 $cm^2/V{\cdot}s$ (Si-face)
  ~85 $cm^2/V{\cdot}s$ (A-face)
- *Interface N ~$5 \times 10^{14}$ $cm^{-2}$ (Si-face)
  N ~$9 \times 10^{14}$ $cm^{-2}$ (A-face)
- **~ideal $SiO_2$ oxide quality**

Data: Yi Xu et al., ARL workshop Aug. 22, 2013.




*,**G. Lui et al., EDL **34** (2013).
**Lichtenwalner et al., MRS spring meeting (2013, 2014).

## Phosphorous processing:

- *FE Mobility ~85 $cm^2/V{\cdot}s$ (Si-face)
  ~125 $cm^2/V{\cdot}s$ (A-face)
- *Interface P ~$1.8 \times 10^{14}$ $cm^{-2}$ (Si-face)
  P ~$1.6 \times 10^{14}$ $cm^{-2}$ (A-face)
- **~Poor oxide quality/stability; Phos typically throughout oxide**

S. Kotake et al., Mat. Sci. Forum 679-680 (2011).

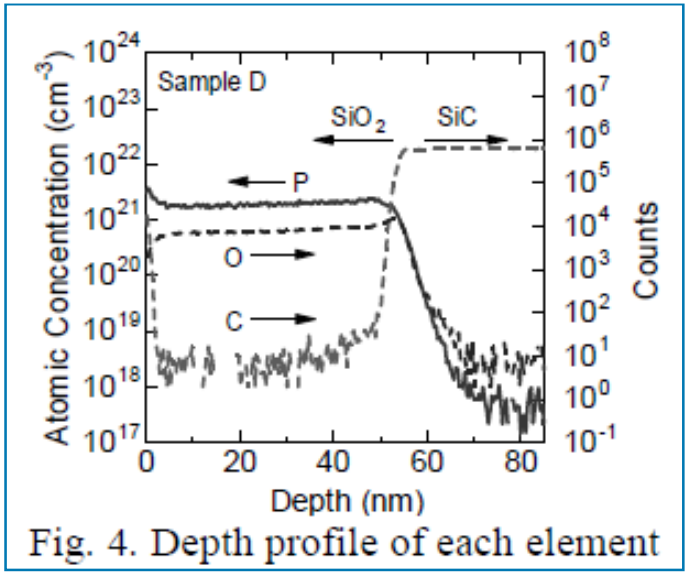


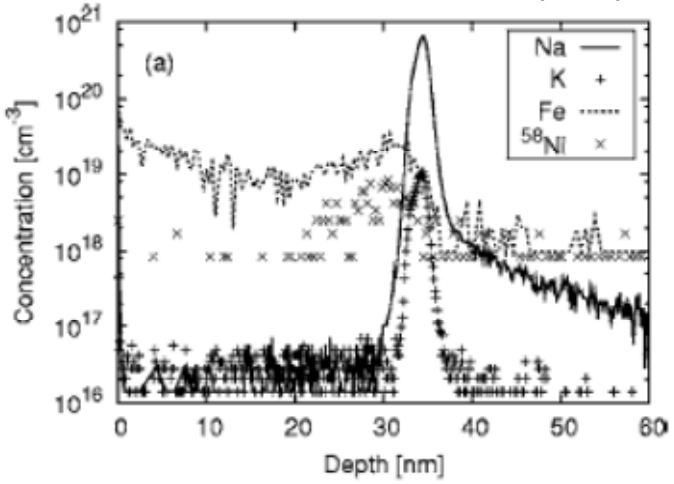

Fig. 4. Depth profile of each element

# 1.2 MOS interface passivation (Group I)

**Sodium effects:**

- *FE Mobility to 220 $cm^2/V{\cdot}s$ (Si-face)
- **Interface Na ~$1 \times 10^{14}$ $cm^{-2}$ (Si-face)
- **Device μ, $V_T$ unstable, mobile ions**

F. Allerstam et al., JAP **101** (2007).



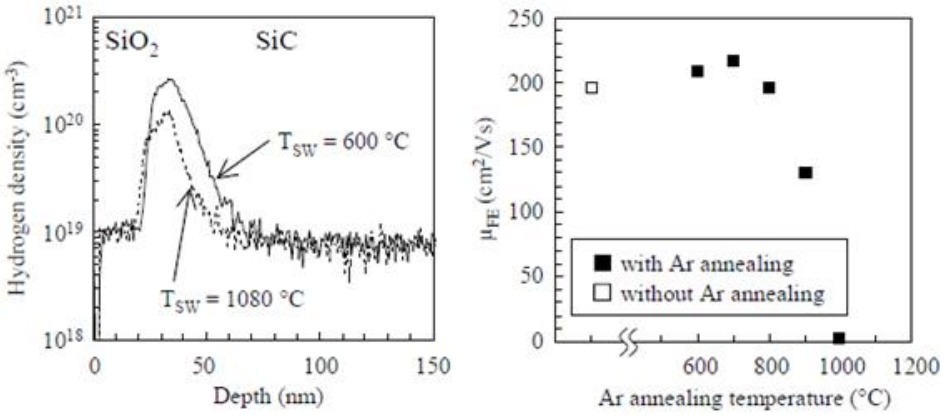

* B. Tuttle et al., JAP **109** (2011).

** F. Allerstam et al., JAP **101** (2007).

**Hydrogen anneals:**

- *FE Mobility ~5 $cm^2/V{\cdot}s$ (Si-face) to 200 $cm^2/V{\cdot}s$ (A-face)
- **Interface H ~$6 \times 10^{13}$ $cm^{-2}$ (A-face)
- **Hydrogen doesn't benefit Si-face; weakly bonded, MOS instability**

T. Endo et al., Mat. Sci. Forum **600-603** (2009).




* H. Yano et al., APL 78 (2001).

** T. Endo et al., Mat. Sci. Forum **600-603** (2009).

# 1.2 MOS interface passivation: approach

**The Ideal Passivation:**

- Interface concentrations >1 × $10^{13}$ $cm^{-2}$ needed to passivate thermal oxide/SiC $N_{IT}$ states.
- All concentrated at interface.
- Strongly bonded, stable interface.

**Our Approach:**

- Investigate effects of Group I & Group II elements.
- Utilize deposited $SiO_2$ as the gate oxide.

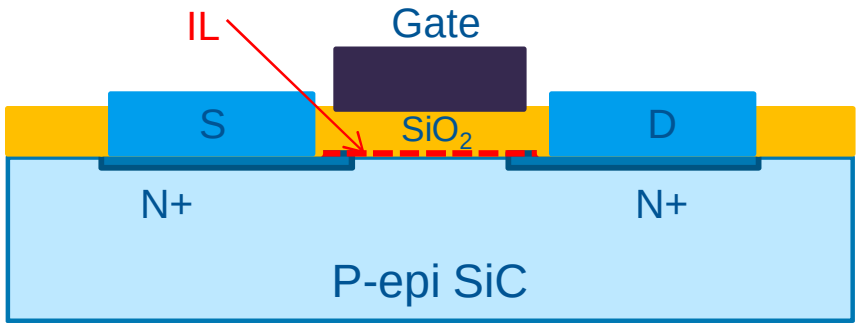
Project initiated by A. Agarwal, J. Palmour at Cree and initially funded by Cree IR&D in 2010.

**U.S. Patent applications:** 20120326163 Dec 2012
20120329216 Dec 2012
20130034941 Feb 2013

# 2. Experimental: Si-face SiC lateral MOSFETs

Lateral MOSFET Fabrication:

- $Al^+$ doped p-type SiC (0001) channel
- Deposited passivation layer
- Deposited $SiO_2$ gate oxide
- Poly-Si gate




Measurements: Lateral MOSFET:

- $I_D$-$V_D$
- $I_D$-$V_g$ vs Temp
  ($V_T$, F.E. mobility)
- Quasi-static gate C-V
  ($T_{ox}$, $V_{fb}$, $V_T$, $Q_f$)
- Gate $I_g$-$V_g$
  (CB, VB F-N barrier height, $E_{BD}$)

(All data reserved to be published later)

# Thank you!

# Question?