Chip-package interaction and interfacial delamination

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Abstract:

In flip-chip package, the mismatch of thermal expansion coefficients between the silicon die and packaging substrate induces concentrated stress field around the edges and corners of silicon die during assembly, testing and services. The concentrated stresses result in delamination on many interfaces on several levels of structures, in various length scales from tens of nanometers to hundreds of micrometers. A major challenge to model flip-chip packages is the huge variation of length scales, the complexity of microstructures, and diverse materials properties. In this paper, we simplify the structure to be silicon/substrate with wedge configuration, and neglect the small local features of integrated circuits. This macroscopic analysis on package level is generic with whatever small local features, as long as the physical processes of interest occur in the region where the concentrated stress field due to chip-packaging interaction dominates. Because it is the same driving force that motivates all of the flaws. Therefore, the different interface cracks with same size and same orientation but on different interfaces should have similar energy release rates provided that the cracks are much smaller than the macroscopic length. We calculate the energy release rate and the mode angle of crack on the chip-package interface based on the asymptotic linear elastic stress field. In a large range of crack length, the asymptotic solution agrees with finite element calculation very

well. We discuss the simplified model and results in context of real applications. In addition, we find that the relation of energy release rate G and crack length a is not power-law since local mode mixity η is dependent of crack length a. Therefore, the curve of G~a can be wavy and hardly goes to zero even if crack length a goes to atomically small. The local mode mixity plays an important role in crack behavior.

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1. Introduction

After integration of billions of transistors, capacitors, resistors, inductors, etc. on its surface, the silicon die is flipped over facedown and connected to substrate by solder joints array, with the gap filled by underfill. This is so called "flip-chip package", as shown in Figure 1(a). In this package, the length scale of functional electronic components varies from centimeters to nanometers. The packaging substrate is several centimeters wide and about 1 mm thick. The silicon die is about 1 cm wide and 0.8 mm thick. The size of solder joints and the thickness of underfill are about tens of microns in the current technology and will be smaller in the future [Figure 1(b)]. If we look into the interconnects on the silicon die, the width and thickness of copper line is about tens of nanometers [Figure 1(c)]. The smallest transistor channel length can be several nanometers.

As the market demands on maximum performance and minimum cost, new designs, materials and processes are employed from transistor level to package level in the length scale from nanometer to centimeter. For example, the source/drain channel in silicon is strained to increase the mobility of electrons or holes (Ieong et al., 2004). The Al/SiO_2 interconnects with shunt layer has been replaced by Cu/low-permittivity dielectrics dual-damascene interconnects to reduce the Resistance-Capacitance delay (Murarka, 1997). The number of silicon-to-package interconnects have increased more than six times over the past 5 years. The scaling demands are driving the size and pitch of solder joints to the limits of current technologies, shrinking from hundreds of microns to tens of microns. The packaging substrate changed from ceramic to organic laminates in the mid of 1990s for better performance at a lower cost because organic substrates are of

lower dielectric constant and easy to process metallization (Atluri et al., 2003). In addition, the mismatch in coefficient of thermal expansion (CTE) between organic substrate and plastic motherboard is also reduced. More information can be found in a multi-author review of the microelectronics packaging and integration in MRS bulletin, edited by Reuss and Chalamala (2003).

However, as new technologies advance, new reliability challenges appear. On the package level, the large CTE mismatch between silicon die and organic substrate can induce bending or warping of the package during thermal excursion from packaging temperature (about 165^{o}C) to room temperature. Also huge stresses concentrate around the edges and corners of silicon die during packaging assembly, thermal cyclic testing and services. The huge stresses result in many failure modes as shown in Figure 1(b), such as the debonding of the interfaces of die/underfill, underfill/substrate or underfill/solder joints (Semmens et al., 1998; Rzepka et al., 1998; Chen et al., 2001; Fan et al., 2001; Hirohata et al., 2002; Zhai et al., 2004); solder joints detachment or cracking (Zhang et al 2000; Chen et al., 2001; Zhai et al, 2003; Tummala et al., 2004); dielectric cracking, copper trace cracking, and die cracking (Tummala et al., 2004). On the interconnects level, as shown in Figure 1(c), the interfacial delamination of back-end-of-line (BEoL) (Mercado et al., 2003; Wang et al., 2003; Liu et al., 2007) become serious. On one hand, this is because the global CTE mismatch between silicon die and organic substrate on package level becomes larger, meanwhile the local CTE mismatch between Cu and low-permittivity dielectrics on interconnects level also becomes larger. On the other hand, the low-permittivity dielectrics (e.g. CDO) is of low cohesive and adhesive energy, and so more susceptible to cracking and debonding.

A major challenge to model or simulate flip-chip packages is the huge variation in length scales, from several centimeters to tens of nanometers, with five or six orders of magnitude difference. Besides, the complication of structures and diverse materials interaction makes the modeling and simulation even harder. To overcome these difficulties, multi-scale FEM simulation or so-called global-local submodeling approach is adopted by many researchers to reconcile the huge length scale variation, such as Gu et al (2001), Mercado et al. (2003), Wang et al. (2003). However, the simulation itself is hard and expensive.

As well known, the failure modes mentioned above become serious or more critical after packaging (Wang et al., 2003), especially with the use of organic substrate. The concentrated stresses around the edges and corners of silicon die due to die-package mismatch are the *global* driving force; the stresses arising due to the local mismatch of materials' properties are *local* driving force (e.g. the stresses in stand-alone wafer before packaging). The local driving force is usually much smaller than global driving force (Wang et al., 2003). Hence, in this paper, we will study the interfacial delamination by analyzing the relation between the interface crack and the asymptotic singular stress field around the edges or corners of silicon die on package level. The delamination can occur at any possible site in this domain, including the examples shown in Figure 1(b) and 1(c). The relation is quite generic in the following sense. The linear elastic asymptotic singular stress solution matches the exact solution in a zone about one fifth or one quarter of the die thickness, i.e., the length scale is about 0.2mm. The flaw size in this zone can be as big as the size of solder joints, or can be as small as the width of Cu lines in interconnects. That is, the flaw size varies from tens of microns to nanometers, but is

small compared to the singular stress region. So the physical processes of interest occur in the region where asymptotic singular stress solution applies. It is the same driving force that motivates all of the flaws to grow. The different interface cracks with same orientation should have similar energy release rates but different fracture toughness. Hence, we adopt the simplified model as shown in Figure 2 to consider the interfacial delamination on package level. This macroscopic analysis is generic and the results are able to characterize chip-package interaction with whatever local features, such as solder joints, underfill, interconnects, as long as they are small.

Following the introduction section, Section 2 briefly recaps the singularity features of bimaterial wedge and mode mixity. Section 3 investigates the interface delamination driven by the singular stress field due to chip-package interaction under thermal excursion. In Section 4, we compare with three-dimensional multi-level submodeling calculation by others, and discuss the validity of the simplified model and other related issues. Section 5 summarizes the main points.

2. Split singularities and local mode mixity

Figure 2(b) illustrates an edge of the silicon die on the substrate, along with a system of polar coordinates (r,θ). In the view of the root of the edge, the die takes the quarter space, $0^0 \le \theta \le 90^0$, and the substrate takes the half space, $-180^0 \le \theta \le 0^0$. The two materials are bonded along the interface, $\theta = 0^0$. Both materials are taken to be elastic and isotropic. Similar split singularities are studied by Liu et al. (1999), Zhang and Suo (2007), and Feron et al. (2007), here we just recap the main features.

For problems of this type Dundurs (1969) showed that the stress field depends on elastic constants through two dimensionless parameters:

$$\alpha = \frac{\mu_1(1-\nu_2)-\mu_2(1-\nu_1)}{\mu_1(1-\nu_2)+\mu_2(1-\nu_1)} \tag{1}$$

$$\beta = \frac{1}{2}\left[\frac{\mu_1(1-2\nu_2)-\mu_2(1-2\nu_1)}{\mu_1(1-\nu_2)+\mu_2(1-\nu_1)}\right] \tag{2}$$

where μ is the shear modulus, and ν Poisson's ratio. The subscripts 1 and 2 refer to the silicon die and the packaging substrate, respectively. By requiring $0 \le \nu \le 0.5$ and $\mu > 0$, the Dundurs parameters are confined within a parallelogram in the (α, β) plane, with vertices at $(1, 0)$, $(1, 0.5)$, $(-1, 0)$ and $(-1, -0.5)$.

For the singular field around the root of the edge, each component of the stress tensor, say $\sigma_{\theta\theta}$, takes the form of $\sigma_{\theta\theta} \sim r^{-\lambda}$. This singular stress field is determined by an eigenvalue problem, resulting a transcendental equation that determines the exponent λ (Bogy 1971; Liu et al 1999; Feron et al., 2007). The exponent is restricted as $0 < \mathrm{Re}(\lambda) < 1$, a restriction commonly adopted, with justifications critiqued by Hui and Ruina (1995) and Dunn et al (2001). For the specific geometry illustrated in the inset, Figure 3 plots the contours of the exponents on the (α, β) plane. The parallelogram is divided into two regions by a dark curve. In the lower-left region, the exponents are two unequal real numbers, one stronger (λ_1) and the other weaker (λ_2). The values for λ_1 are labeled horizontally, and those for λ_2 are labeled vertically. In the whole region, $\lambda_2 < \lambda_1 \le 0.5$. In the upper-right region, the exponents are a pair of complex conjugates, $\lambda_{1,2} = \xi \pm i\varepsilon$. The real part is depicted by solid lines and labeled horizontally, while the imaginary part is depicted by dashed lines and labeled vertically. At each point on the

boundary (i.e., the dark curve), the two exponents degenerate to one number: when the point is approached from a region of real exponents, the two real exponents become identical; when the point is approached from a region of complex-conjugate exponents, the imaginary part vanishes.

As noted in Liu et al (1999), when the two materials have similar elastic constants ($\alpha = \beta = 0$ denotes the homogeneous case), i.e., when $\alpha = \beta = 0$, the two modes of singular fields can be interpreted readily. In this case, the line bisecting the angle of the wedge is a line of symmetry. The stronger mode corresponds to a stress field symmetric about this line (i.e., the tensile mode). The weaker mode corresponds to a stress field anti-symmetric about this line (i.e., the shearing mode). When the two materials have dissimilar elastic constants, however, the symmetry is broken, and we do not have such a simple interpretation for the two modes.

We next paraphrase fundamental ideas in fracture mechanics. Once we retain the two unequal real exponents, the stress field around the root of the wedge is a linear superposition of the two modes:

$$\sigma_{ij}(r,\theta) = \frac{k_1}{(2\pi r)^{\lambda_1}} \Sigma_{ij}^1(\theta) + \frac{k_2}{(2\pi r)^{\lambda_2}} \Sigma_{ij}^2(\theta). \qquad (3)$$

The angular functions $\Sigma_{ij}^1(\theta)$ and $\Sigma_{ij}^2(\theta)$ are normalized such that $\Sigma_{r\theta}^1(0) = \Sigma_{r\theta}^2(0) = 1$, and their full expressions are listed in Appendix A. The stress intensity factors, k_1 and k_2, are determined by the external boundary conditions, as described in Section 3.

The singular stress field (3) is obtained by assuming that the materials are elastic, and the edge is perfectly sharp. Such assumptions are invalid in a process zone around the root of the edge. Let Λ be the size of the process zone, within which the singular

stress field (4) is invalid. Also, the singular stress field (3) is invalid at size scale h, where the external boundary conditions will change the stress distribution. However, provided the process zone is significantly smaller than the macroscopic length, $\Lambda << h$, the singular stress field Eq. (3) prevails within an annulus, known as the *k*-annulus, of some radii bounded between Λ and *h*.

The two stress intensity factors, k_1 and k_2, have different dimensions, being $(\text{stress})(\text{lengh})^{\lambda_1}$ and $(\text{stress})(\text{lengh})^{\lambda_2}$, respectively. As discussed in Zhang and Suo (2007), Eq. (3) suggests that, as the distance *r* from the edge varies, the proportion of the two modes also varies and can be specified by the dimensionless parameter $(k_2/k_1)r^{\lambda_1-\lambda_2}$ (Liu et al., 1999). This parameter is suitable to describe the mode mixity of the singular stress field, so long as an arbitrary length *r* is chosen, in the same spirit as Rice's (1988) suggestion for a crack lying on a bimaterial interface. Indeed, Labossiere et al. (2002) have used this mode mixity in describing their experimental data.

The microscopic processes of fracture occur within the process zone, but are driven by the singular stress field in the *k*-annulus. In discussing the effect of the mode mixity on failure processes, it is intuitive to select the length characterizing the size of the process zone, i.e., setting $r = \Lambda$. Thus, we specify a dimensionless parameter (Zhang and Suo, 2007):

$$\eta = (k_2/k_1)\Lambda^{\lambda_1-\lambda_2}. \tag{4}$$

This parameter, to be called the *local mode mixity*, measures the relative contribution of the two modes to the stress field at length scale Λ.

3. Interfacial delamination due to chip-package interaction

We now analyze the delamination of chip-package interface. Consider two kinds of packages: flip-chip on ceramic substrate, and flip-chip on organic substrate. The typical organic substrate is epoxy-based laminates, such as FR4 or BT. However, the organic packages have fundamental limits, and so novel ceramic substrates are demanded (Tummala et al., 2004). Low Temperature Co-fired Ceramic (LTCC), a ceramic-glass composite with small CTE mismatch with silicon die, is the potential choice of package substrate (Frear and Thomas, 2003). LTCC is fired at sufficiently low temperature that Cu can be used in the metallization; and it offers the hermeticity and mechanical stability. We will use chip/FR4 and chip/LTCC packages as two typical examples to study the interfacial delamination due to chip-package interaction under thermal excursion from 165^0C to 25^0C. The material properties used in calculation are listed in Table 1. The geometric parameters are specified as $h = 0.7$ mm, $H = 1.65$ mm, $L = 10$ mm and $S = 20$ mm, as shown in Figure 2(a).

For either chip/FR4 package or chip/LTCC package, we calculate the full stress field in the structure, i.e. Figure 2(a), by using the finite element code ABAQUS6.6, then fit the interfacial shear stress close to the root, say $10^{-3} < r/h < 10^{-2}$, to the equation

$$\sigma_{r\theta}(\theta = 0) = \frac{k_1}{(2\pi r)^{\lambda_1}} + \frac{k_2}{(2\pi r)^{\lambda_2}}. \tag{5}$$

with k_1 and k_2 as fitting parameters.

For this chip-package structure under thermal excursion, the bi-axial stress state in the silicon die away from the edges is $\sigma = E_{Si}\Delta\alpha\Delta T/(1-\nu_{Si})$, where $\Delta\alpha = \alpha_{sub} - \alpha_{Si}$, and $\Delta T = 140\ ^0$C. Linearity and dimensional considerations dictate that the two stress intensity factors should take the form

$$k_1 = \kappa_1 \sigma h^{\lambda_1}, \quad k_2 = \kappa_2 \sigma h^{\lambda_2}. \tag{6}$$

where κ_1 and κ_2 are dimensionless coefficients, *h* the silicon die thickness.

Assume an interfacial flaw preexists, as shown in Figure 2(c). The crack length *a* is much smaller than die thickness *h*, i.e., $a << h$. The length Λ now is identified with the length *a* of the small crack, so that the local mode mixity is

$$\eta = (k_2 / k_1) a^{\lambda_1 - \lambda_2} = (\kappa_2 / \kappa_1)(a / h)^{\lambda_1 - \lambda_2}. \tag{7}$$

which describes the relative contribution of two modes at the length scale of crack size.

The stress field at the interfacial crack tip is characterized by the complex stress intensity factor K, which is related to the stress intensity factors of the wedge (k_1, k_2) linearly as follows:

$$\frac{\mathrm{Re}\left(K a^{i\varepsilon}\right)}{\sqrt{a}} = c_{11} \cdot \frac{k_1}{a^{\lambda_1}} + c_{12} \cdot \frac{k_2}{a^{\lambda_2}}. \tag{8}$$

$$\frac{\mathrm{Im}\left(K a^{i\varepsilon}\right)}{\sqrt{a}} = c_{21} \cdot \frac{k_1}{a^{\lambda_1}} + c_{22} \cdot \frac{k_2}{a^{\lambda_2}}. \tag{9}$$

where $\varepsilon = 1/(2\pi) \ln\left[(1-\beta)/(1+\beta)\right]$. The coefficients c_{11}, c_{12}, c_{21} and c_{22} only depend on material combination (α, β) and wedge angle (90^o in this study), and are tabulated in Table 2. The determination of the coefficients is stated in Appendix B.

For such a bimaterial wedge configuration, the coefficients c_{11}, c_{12}, c_{21} and c_{22} are generic for any macroscopic structure, external loading, and boundary condition. Once we obtain them for the specific material combination (e.g., silicon/FR4 or silicon/LTCC), we can use them for different geometric parameters (e.g., die thickness) and loadings (e.g. thermal excursion, bending, etc.). This is an advantage compared to

multi-scale submodeling approach, in which we have to recalculate again and again in order to study the parameter dependence.

From Eqs. (6) to (9), the energy release rate *G* and the mode angle ψ of interfacial delaminated crack are:

$$G = \frac{1-\beta^2}{1-\alpha}\frac{\kappa_1^2\sigma^2 h}{\bar{E}_{Si}}\left(\frac{a}{h}\right)^{1-2\lambda_1}\left[\left(c_{11}+c_{12}\eta\right)^2+\left(c_{21}+c_{22}\eta\right)^2\right]. \tag{10}$$

and

$$\tan\psi = \frac{\mathrm{Im}\left(Ka^{i\varepsilon}\right)}{\mathrm{Re}\left(Ka^{i\varepsilon}\right)} = \frac{c_{21}+c_{22}\eta}{c_{11}+c_{12}\eta}. \tag{11}$$

To obtain *G* and ψ under any loading case, we just need to find out two stress intensity factors, k_1 and k_2. Then plug into Eqs.(10) and (11), we have *G* and ψ for any arbitrary interfacial flaw size *a*, only if $a << h$. In order to verify the relations given by Eqs.(10) and (11), we use finite element method (FEM) to directly calculate *G* and ψ of interfacial crack with different crack length *a* in the range of $10^{-4} < a/h < 10^{0}$ for both chip/FR4 and chip/LTCC packages under the thermal excursion from 165^0C to 25^0C. In order to plot Eqs.(10) and (11), we use FEM to calculate the stress field under the same thermal excursion of the full structure without crack [Figure 2(a)], and obtain κ_1 and κ_2 by curve fitting Eq.(5) with dimensional consideration of Eq.(6). For chip/FR4 package, $\kappa_1 = -0.05$ and $\kappa_2 = -0.06$; for chip/LTCC package, $\kappa_1 = -0.23$ and $\kappa_2 = -0.11$.

In Figure 4, energy release rate *G* and mode angle ψ of interfacial crack are plotted as a function of normalized crack length *a/h* for both chip/FR4 and chip/LTCC packages under thermal excursion from 165^0C to 25^0C. The curves are plotted from Eqs.(10) and (11), and the data points with markers are from finite element calculation in

ABAQUS6.6 by contour integral. For both packages, the FEM data and Eqs.(8) and (9) agree with each other very well when $a/h < 0.1 \sim 0.2$, i.e. the *k*-annulus regime, within which the asymptotic solution Eq.(3) applies. For chip/FR4 package, the shear mode dominates in the range of crack length, while for chi/LTCC package, the opening mode plays more role. As we know, the driving force is due to CTE mismatch of die-package. Hence, the energy release rate of interface flaws in chip/FR4 package is much larger than that in chip/LTCC package.

4. Discussion

4.1 Global driving force and local driving force

In our model, we neglect the small local features, such as solder joints, underfill, Cu/low-*k* interconnects, etc., and also we neglect the elastic or CTE mismatch among them, since these small features and the associated local mismatch make less contribution to interfacial delamination provided that the global driving force dominates. For example, both Wang et al. (2003) and Liu et al. (2007) shown that the energy release rate of horizontal interfacial flaws within the Cu/low-*k* interconnects are about 1 J/m^2 or less under the typical thermal loading condition if the silicon die is standing alone. On the contrary, the energy release rate increases one order of magnitude larger after being packaged to the organic substrate. Therefore, neglecting the small features and local mismatch in interconnects, we can still obtain an accurate value by doing a macroscopic analysis on package level. Let us consider the following case. The flaws in interconnects are about 100 nm or less, the die thickness is about 1 mm, i.e. $a/h \sim 10^{-4}$, so the energy

release rate is around 10 J/m^2 for chip/FR4 package, which is close to the values given by 3D multi-level submodeling technique in Wang et al. (2003).

Length scale varies five to six order of magnitude from interconnects level to package level. So does the size of the interfacial flaws. Our model supplies a reasonable estimate of energy release rates of interfacial flaws with huge variation in length scale without complexity of microstructures and diverse materials. This is based on the following argument. From the perspective of package level, asymptotic singular stress field (3) arises due to the CTE mismatch of silicon die and package substrate. The stress intensity factors, k_1 and k_2, carrying information of macroscopic structure and loading condition, are independent of microstructures. As long as the crack growth under the global driving force is concerned, the energy release rates of interfacial cracks with same size and same orientation but on different interfaces have similar values only if they are much smaller than macroscopic length.

In order to improve the reliability of interconnects, the reduction of global driving force is one big gain. As shown in Figure 4(a), the replacement of compliant organic substrate (e.g., FR4) by stiff ceramic with small CTE (e.g. LTCC) decreases the energy release rate multiple-fold.

4.2 Underfill effect

In our model, we neglect the underfill effect. However, this effect could be significant (Suryanarayana et al., 1991; Rzepka et al., 1998; Chen et al., 2001; Zhai et al., 2004). Because in the previous technology, the size of solder joints and the thickness of underfill are over 100μm and the thickness of silicon die is about 700μm, therefore the underfill acts as a thick buffer to alleviate the concentrated stresses. From Figure 4, for

chip/FR4 package, the energy release rate is about $20J/m^2$ if the crack length is about $0.1h$, which represents a typical crack along the die/underfill interface. However, this value could be reduced five-fold if underfill is considered (Zhai et al., 2004). In this case, we have to include underfill in our model to study such a wedge configuration that two-layered materials sit on substrate.

However, this buffer effect is tapering. Because the technology demands denser solder joints with smaller pitch and smaller size on the similar size of silicon die, and results in the decrease of the underfill thickness, which will be the case as our model represents. Finally, this trend increases the global driving force.

The fillet height of underfill around the die corner can affect the reliability of the crack along the die/underfill interface (Zhai et al., 2004). This phenomenon can be explained qualitatively in the following, and more details can be found in Yoon et al. (2007). Physically the stress concentration around the wedge is due to the elastic mismatch and geometric discontinuity in this domain. If we use a fillet, the bimaterial wedge becomes a tri-material junction, the singularity exponent λ becomes usually much smaller (Pageau et al., 1994).

In order to address our idea clearly, we do not use fillet. Therefore, the crack is edge crack. If fillet is considered, the crack is fully embedded. So the energy release rate should be smaller. More detailed study of fillet effect is beyond the scope of this chapter.

4.3 Relation of k-field and K-field

Eqs. (10) and (11) agree with FEM data very well when crack size a is less than $0.2h$, as shown in Figure 4. If the crack becomes longer, Eqs. (10) and (11) goes away from FEM data. It can be understood as follows. The singular stress field of interfacial

crack tip, characterized by complex stress intensity factor *K*, scales with the crack size. The singular stress field of 90^0 wedge, characterized by stress intensity factors k_1 and k_2, scales with the die thickness. When the crack is small, the *K*-field is embedded in the *k*-field, and so the linear relations (8) and (9) apply. When the crack has comparable size as the die thickness, the *K*-field goes beyond the *k*-field, and so the linear relations (8) and (9) break down. Meanwhile, the breakdown point in Figure 4 shows that the asymptotic stress field (3) is accurate within one fifth or one quarter of macroscopic length, similar to the solution of a finite crack in a homogeneous infinite sheet in the classic linear elastic fracture mechanics.

4.4 Length dependent of local mode mixity and breakdown of power-law relation of G~a

It is well known that for such a structure that a thin film is bonded on substrate with interfacial crack [Figure 2], $G=0$ if $a=0$. When $0<a<h$, G depends on a; when $a>>h$, G attains steady state and so is independent of a. Therefore, the energy release rate should start from zero and increase monotonically to the steady-state value (Yu et al., 2001). However, from Figure 4, the energy release rate is far away from zero when $a/h=10^{-4}$. Even if we extend the plot to $a/h=10^{-7}$ that corresponds to a crack with atomic length, the energy release rate is still far from zero. The energy release rate *G* could go to zero unless we would let crack length *a* go to zero mathematically, but it is out of interest.

Eq.(10) also shows that the relation of *G* and *a* is not power-law since η is dependent of crack length *a*. And also the power $1-2\lambda_1 \approx 0$, so $(a/h)^{1-2\lambda_1} \to 1$ except

$a = 0$ exactly. Therefore, the curve of G~a can be wavy as shown in Figure 4(a) for the case of chip/LTCC package, and hardly goes to zero even if crack length a goes to atomically small.

5. Summary

The singular stress field around the edges and corners of flip-chip package arises due to the CTE mismatch of silicon die and packaging substrate. On package level, the small features within the interconnects can be neglected. The cracks with same size and same orientation but on different interfaces should have similar energy release rates but different fracture toughness provided that the cracks are much smaller than the macroscopic length. We take delamination of chip-package interface as an example. We calculate the energy release rate of interface crack both from FEM and from asymptotic relations. The results show that the asymptotic relations agree with FEM data very well within a large range of crack length. From our results and others work, we can clearly see that the simplified model catch the essence without the complexity of 3D microstructure and diverse materials in the integrated circuits.

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Appendix A: Stress components in polar coordinates

The singular stress field Eq.(3) is solved by the methods outlined in Bogy (1971) and Liu et al. (1999). The eigenfunctions $\Sigma_{ij}(\theta)$ associated with the eigenvalue λ are expressed in polar coordinates (r,θ,z) as

$$\Sigma_{rr}(\theta) = -(\lambda-1)\{(\lambda-2)[A\sin(\lambda-2)\theta + B\cos(\lambda-2)\theta] + (\lambda+2)[C\sin\lambda\theta + D\cos\lambda\theta]\}, \quad \text{(A.1)}$$

$$\Sigma_{\theta\theta}(\theta) = (\lambda-1)(\lambda-2)[A\sin(\lambda-2)\theta + B\cos(\lambda-2)\theta + C\sin\lambda\theta + D\cos\lambda\theta], \quad \text{(A.2)}$$

$$\Sigma_{r\theta}(\theta) = (\lambda-1)\{(\lambda-2)[A\cos(\lambda-2)\theta - B\sin(\lambda-2)\theta] + \lambda[C\cos\lambda\theta - D\sin\lambda\theta]\}, \quad \text{(A.3)}$$

$$\Sigma_{zz}(\theta) = -4\nu(\lambda-1)[C\sin\lambda\theta + D\cos\lambda\theta], \quad \text{(A.4)}$$

$$\Sigma_{rz} = \Sigma_{\theta z} = 0. \quad \text{(A.5)}$$

The eigenvalue λ and its associated coefficients *A*, *B*, *C* and *D* in both film and substrate are solved by the boundary value problems.

Appendix B: Determination of coefficients by stretching and bending

We solve four boundary value problems sketched in Figure 5 and Figure 6, using the finite element code ABAQUS6.6. Let's consider two loading conditions for the flip-chip package: stretching and bending. Let *P* be the stretching force per unit thickness and *M* the bending moment per unit thickness. Plane strain conditions are assumed. The stress intensity factors of the bimaterial wedge of silicon chip on substrate, k_1 and k_2, are obtained by fitting Eq. (3) with the stresses calculated for problems in Figure 5, along $\theta = 0$ within $10^{-3} < r/h < 10^{-2}$. For the problems in Figure 6, the size of the interfacial crack *a* is set to be 0.01*h*. The complex stress intensity factor of the interfacial crack, $K = K_I + iK_{II}$, is read out from the outputs of contour integrals. Using the linear relations (6) and (7), we obtain the coefficients c_{11}, c_{12}, c_{21} and c_{22} for both chip/FR4 and chip/LTCC packages.

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Table 1: Materials properties used in calculation.

	E (GPa)	ν	α (10^{-6} / ^{o}C)
Silicon	130	0.28	3.3
FR4 or BT [a)]	23	0.3	15
LTCC [b)]	120	0.3	5.8
Underfill	6	0.32	36
Solder	26	0.35	24

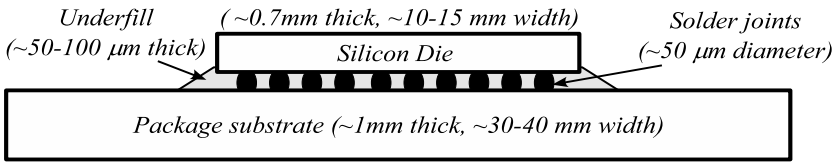
a) Both FR4 and BT are epoxy-based organic substrates.

b) Low Temperature Co-fired Ceramic.

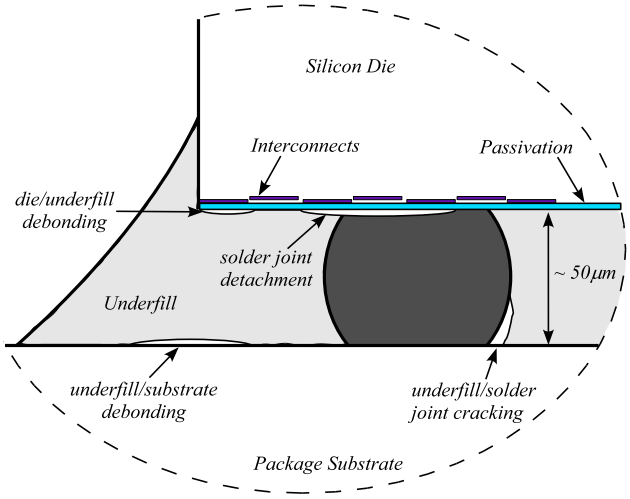
Table 2: Coefficients c_{11}, c_{12}, c_{21} and c_{22} for two types of flip-chip packages.

Flip-chip package	α	β	λ_1	λ_2	c_{11}	c_{12}	c_{21}	c_{22}
Chip/FR4	0.696	0.196	0.499	0.318	0.951	-1.206	0.922	1.443
Chip/LTCC	0.034	0	0.457	0.100	1.965	-5.418	0.870	2.270

(a)



(b)



(c)

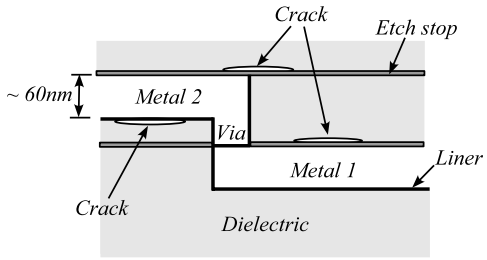


Figure 1:(a) Typical structure of flip-chip package. The Cu/low-*k* interconnects are integrated on the silicon die and passivated, then silicon die is flipped upside down and bonded to substrate by solder joints array, with the gap filled by underfill material. (b) Magnified view of chip-package corner with typical failures phenomena is illustrated. The flaw size is about tens of microns. (c) Magnified view of Cu/low-*k* interconnects around the die corner with typical interfacial delamination is depicted. The flaw size is about tens of nanometers.

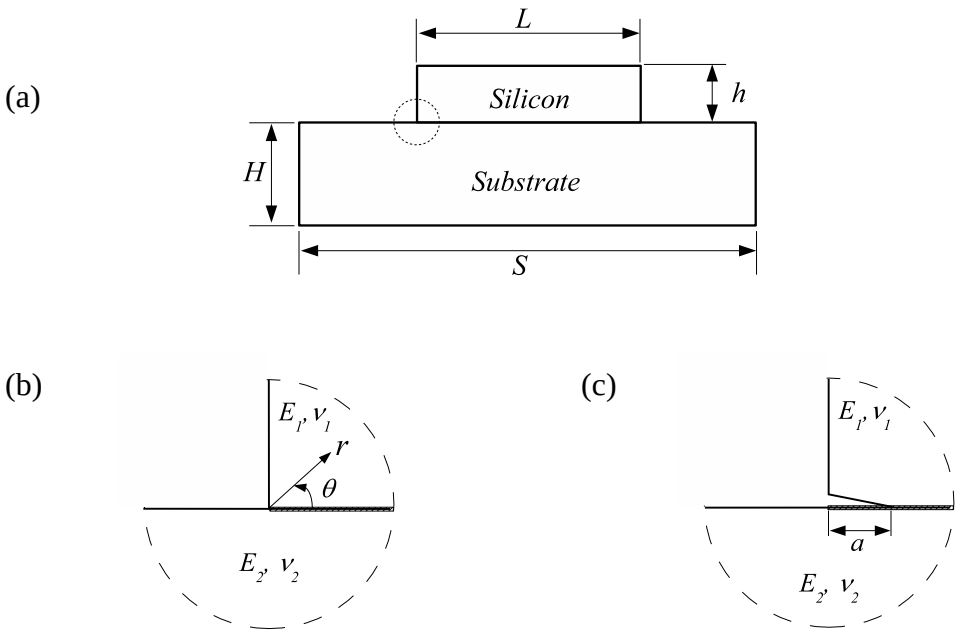


Figure 2:Geometry used in calculations: (a) Silicon die on package substrate; (b) Geometry near the die edge. (c) A preexisting small interface crack in the corner.

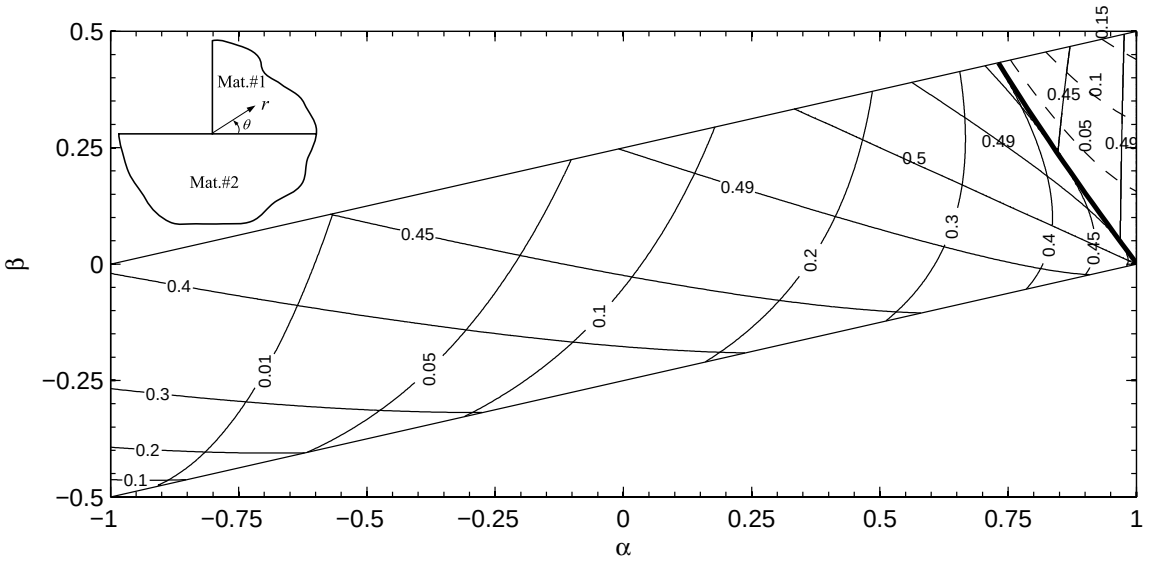
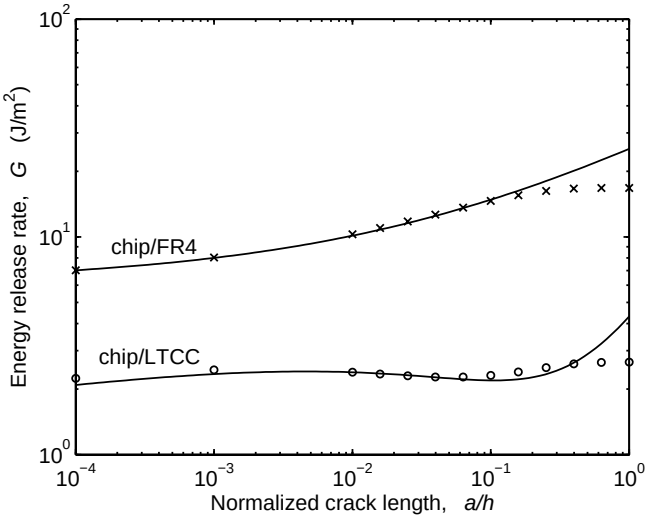


Figure 3:The inset shows the root of an edge of silicon die bonded on a substrate. Contours of the singular exponents are plotted on the plane of Dundurs parameters (α, β). The parallelogram is divided into two regions by a dark curve. In the lower-left region, the exponents are two unequal real numbers, with the larger one labeled horizontally, and the smaller one labeled vertically. In the upper-right region, the exponents are a pair of complex conjugates, with real part depicted by solid lines and labeled horizontally, and the imaginary part depicted by dashed line and labeled vertically.

(a)



(b)

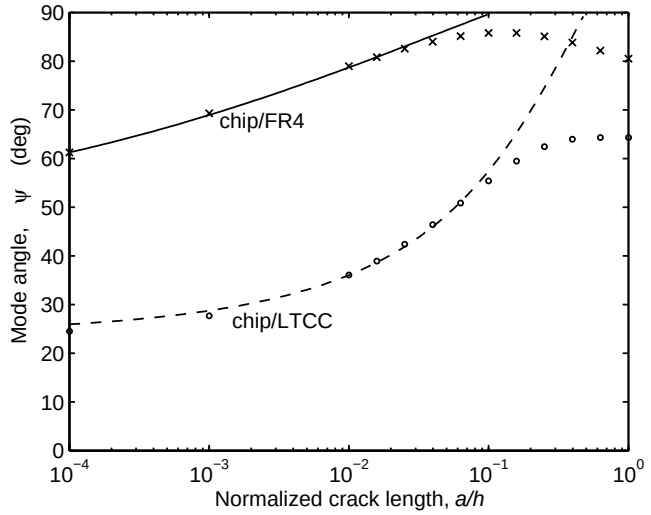


Figure 4:Energy release rate (a) and mode angle (b) of interfacial crack are plotted as a function of normalized crack length *a/h* for both chip/FR4 and chip/LTCC packages under thermal excursion from 165^0C to 25^0C. The curves are plotted from Eqs.(4.10) and (4.11), and the data points with markers are read out from finite element calculation in ABAQUS by contour integral.

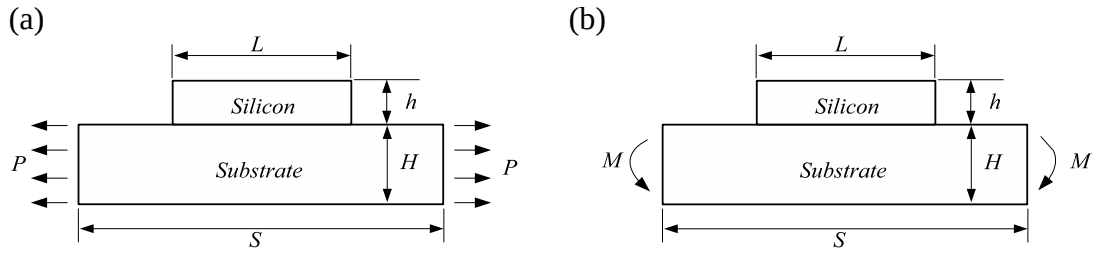


Figure 5:The flip-chip package *without crack* is under two loading conditions: stretching (a) and bending (b).

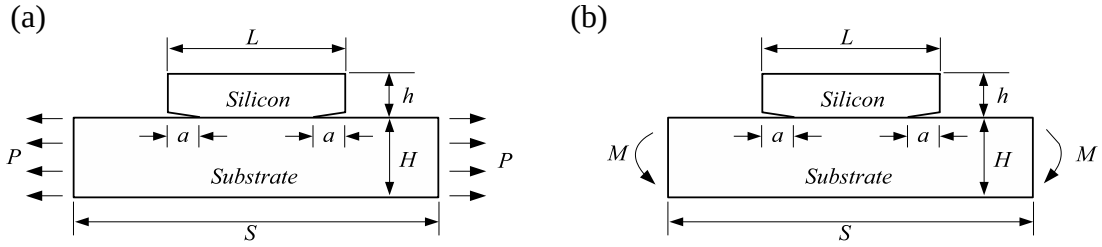


Figure 6:The flip-chip package *with interfacial crack* is under two loading conditions: stretching (a) and bending (b).