Current-Transformer Based Gate-Drive Power Supply with Reinforced Isolation

Jiewen Hu

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

Rolando Burgos
Dushan Boroyevich
Steve C. Southward

05/04/2018
Blacksburg, VA

Keywords: Gate driver power supply, resonant current bus, inductor/capacitor/capacitor/inductor (LCCL), electro-magnetic interference (EMI)

Current-Transformer Based Gate-Drive Power Supply with Reinforced Isolation

Jiewen Hu

ABSTRACT

In recent years, there is a clear trend toward increasing the demand for electric power in high-power applications. High-power converters are making major impacts on these high-power applications. Recent breakthroughs in Silicon Carbide (SiC) materials and fabrication techniques have led to the development of high-voltage, high-frequency power devices, which are at the heart of high-power converters. SiC metal-oxide semiconductor field-effect transistors (MOSFETs) have advantages over silicon (Si) devices due to their higher breakdown voltage, higher thermal capability, and lower on-state resistance.

However, their fast switching frequency and high blocking voltage bring challenges to the gate-drive circuit design. The gate driver of SiC-MOSFETs requires a power supply that provides a high-voltage, high-density design, a low input-output capacitance ($C_{I/O}$) transformer design, good voltage regulation, as well as good resilience to faults to enable safe and fast operation.

In this thesis, a power supply that supplies multiple gate drivers for 10 kV SiC MOSFETs is presented. A transformer design approach with a single turn at the primary side is proposed. A 20 kV insulation is achieved by the primary HV cable insulation across a toroid transformer core. The $C_{I/O}$ is designed less than 2 pF to mitigate the Common-Mode (CM) noise. A circuit topology analysis is performed and the

inductor/capacitor/capacitor/inductor (LCCL) – inductor/capacitor (LC) circuit is selected. This circuit allows Zero-Voltage Switching (ZVS) at full operation range. A Resonant-Current-Bus (RCB) is built at the transformer primary side to achieve load-independence.

Current-transformer Based Gate-drive Power Supply with Reinforced Isolation

Jiewen Hu

GENERAL AUDIENCE ABSTRACT

Wide-bandgap semiconductor devices have attracted widespread attention due to their superior performance compared to their silicon devices counterpart. To utilize its full benefits, this thesis presents a complete design and optimization of a gate-drive power supply that supplies multiple gate drivers for high-voltage, high-speed semiconductor devices. Four objectives, including high density at high voltage, good noise mitigation, fair voltage regulation, resilience to faults have been achieved.

During the design procedure, different topology candidates are introduced and compared, after which a resonant topology is selected. The wide-bandgap semiconductor devices are utilized to reduce the size and losses. Hardware assembly is shown and experimental testing results are provided in the end to verify the design.

Table of Contents

List of Figures

List of Tables

Chapter 1: Introduction

1.1 Overview

In recent years, there is a clear trend toward increasing the demand of electric power in high-power applications, widely used in transportation, power, and energy industries. These high-power applications, such as those used in ships, airplanes, and wind turbines shown in Fig. 1, require innovative power converters to meet stringent requirements of cost, size, weight, power-density, and reliability. When the converter voltage rating is increased, it becomes a common practice to utilize multilevel topologies such as 3-level, 5-level, and other hybrid topologies due to the devices' limited voltage and current ratings. Using these approaches, the complexity of the system design is increased, and reliability becomes a concern.

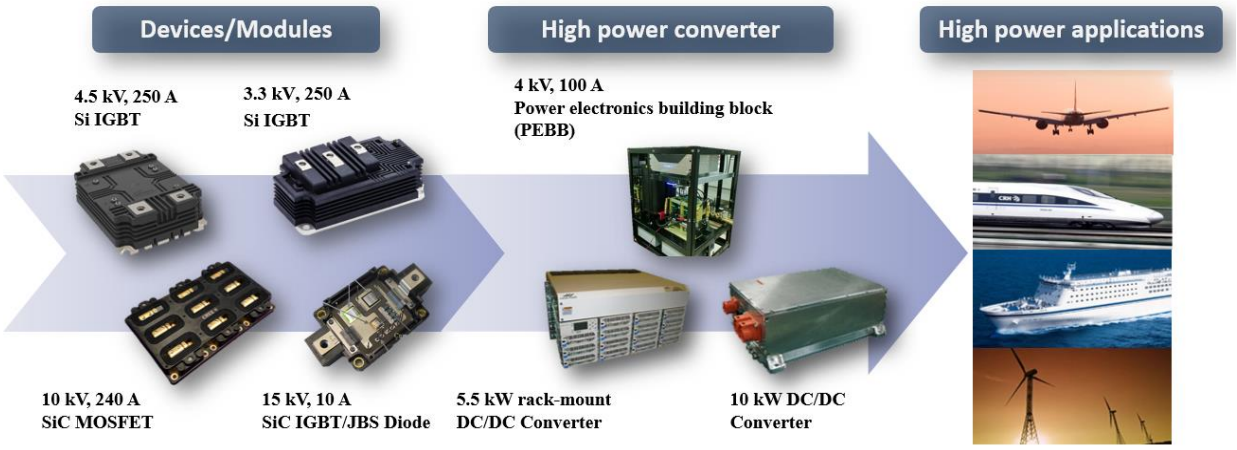


Fig. 1. Background and Motivation

Due to the recent breakthroughs in Silicon Carbide (SiC) materials and fabrication techniques, power devices can now achieve higher blocking voltage and faster speed due to their higher breakdown voltage, higher thermal capability, and lower on-state resistance, compared to their Silicon (Si) counterpart [1]. The high blocking voltage enables simpler topologies while a higher switching frequency maintains the overall harmonic performance despite reduced voltage

levels. TABLE 1 shows the comparison between two designs using a 3.3 kV Si insulated gate bipolar transistor (IGBT) and a 10 kV SiC MOSFETs module, respectively. The former design is in reference to the 6 kV DC, 3.3 kV line-line medium voltage industrial drive from ABB, the ACS 2000, where each phase-leg is an ANPC-5L topology. The complicated multilevel converter can be replaced by a simple half-bridge using a 10 kV, 240 A SiC MOSFET module, shown in Fig. 2.

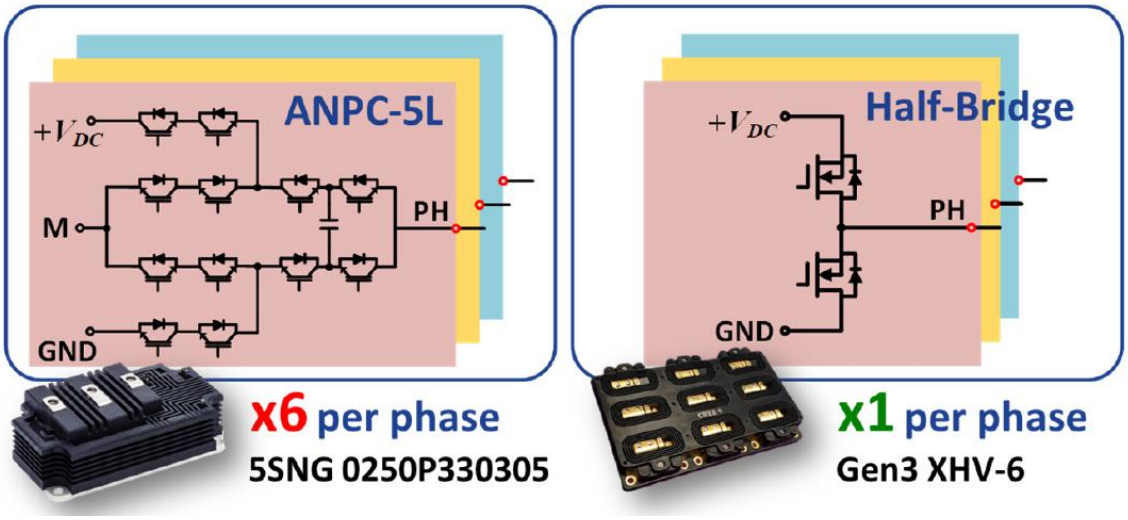
However, the high blocking voltage and high switching frequency of SiC MOSFETs also

TABLE 1. DEVICE COMPARISON FOR A THREE-PHASE INVERTER

Property	Si IGBT	SiC MOSFET
DC bus voltage (V_{dc})	6 ~7 kV	
3-phase output	4.16 kV, 100 A, 720 kVA	
Total module number	18	3
Total module volume	28.74 inch^3	12.52 inch^3
Switching frequency (f_{sw})	2.5 kHz	10 kHz
Switching loss per module	2250 W	3800 W
Conduction loss per module	210 W	400 W
Maximum operating temperature	150 ° C	175 ° C
Equivalent switchng frequency ($f_{sw,eqv}$)	10 kHz	10 kHz

bring some challenges to the gate-drive circuit design. In order to have a safe and reliable operation, the gate driver should have a high-voltage (HV), high-density (HD) design. The higher switching speed also increases the negative effect of the electronmagnetic interference (EMI) noise.

It should be fully considered that the isolated gate-drive power supply for the 10 kV, 240 A SiC MOSFETs module should have a careful HV insulation design, low $C_{I/O}$ transformer design,



(a) **(b)**

Fig. 2. (a) 3.3 kV, 250 A Si IGBT and (b) 10 kV, 240 A SiC MOSFET

good voltage regulation design, as well as resilience design, which will be discussed in detail in the following sections.

1.2 Challenges and Targets

1.2.1 HV Isolation Design

Electric assemblies must satisfy strong safety regulations regarding creepage and clearance distances to prevent hazards caused by electric sparks. The electrical clearance is the shortest distance through the air between two conductive elements, whereas the creepage distance is the shortest distance on the surface of an insulating material, which are both shown in Fig. 3.

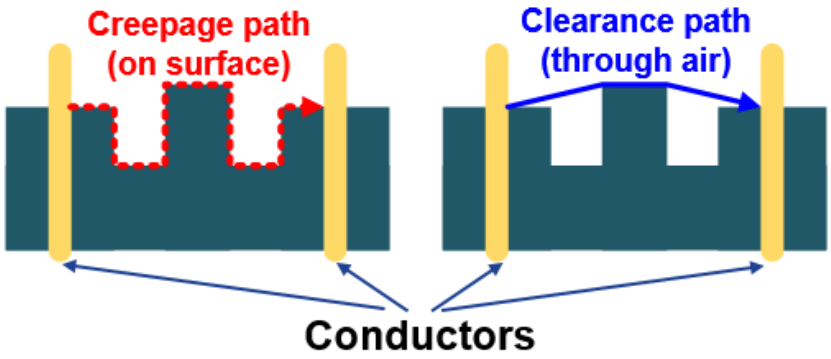


Fig. 3.Definition of creepage distance and clearance distance

According to the international standard, IEC 60664-1 [3], the minimum clearance distance and the creepage distance for 10 kV are 3.5 mm and 50 mm, respectively.

There are many techniques to increase creepage distance. One of the simplest and most popular ones is to insert slots into the printed circuit board (PCB), aligning the creepage path along the path of the transformer core, which is shown in Fig. 4. This results in a heavy and bulky circuit, as the transformer core should be large enough to provide sufficient creepage distance.

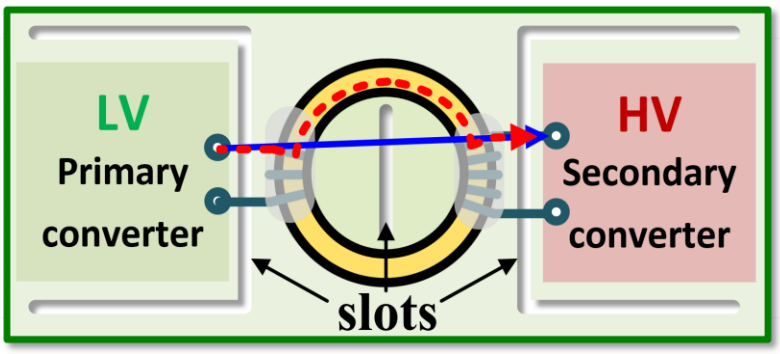


Fig. 4. Popular technique for increasing creepage distance

Taking a toroid core as an example, to satisfy 50 mm creepage distance, the inner diameter of the core should be at least 32 mm. The HV-HD objective is to satisfy a 10 kV creepage distance requirement and to design the volume to be less than 3 inch^3.

1.2.2 Low $C_{I/O}$ Transformer Design

The fast switching speed of SiC MOSFETs presents a better overall harmonic performance; however, as a trade-off, the common-mode (CM) noise tends to have an increasingly negative effect as the *dv/dt* grows. As illustrated in Fig. 5, the ground of the high-side isolated gate-drive power supply output is directly connected to the switching node of the phase-leg. A high *dv/dt*, up to 50 V/ns given by the high speed SiC MOSFETs module, might occur between the primary

and secondary side of the transformer of the high-side isolated gate-drive power supply, and therefore, across the transformer input-output coupling capacitor $C_{I/O}$.

$$i_{\mathrm{CM}} = C_{I/O} \cdot \frac{dv}{dt} \tag{1}$$

According to (1), $C_{I/O}$ will lead to a CM current i_{CM} through the isolation of the transformer, which will cause EMI issues. Zhang designs an isolated gate-drive power supply [9] with a $C_{I/O}$ of 3.5 pF, which is shown in Fig. 6. Following (1), this 3.5 pF $C_{I/O}$ will raise a CM current i_{CM} of 175 mA with 50 V/ns dv/dt.

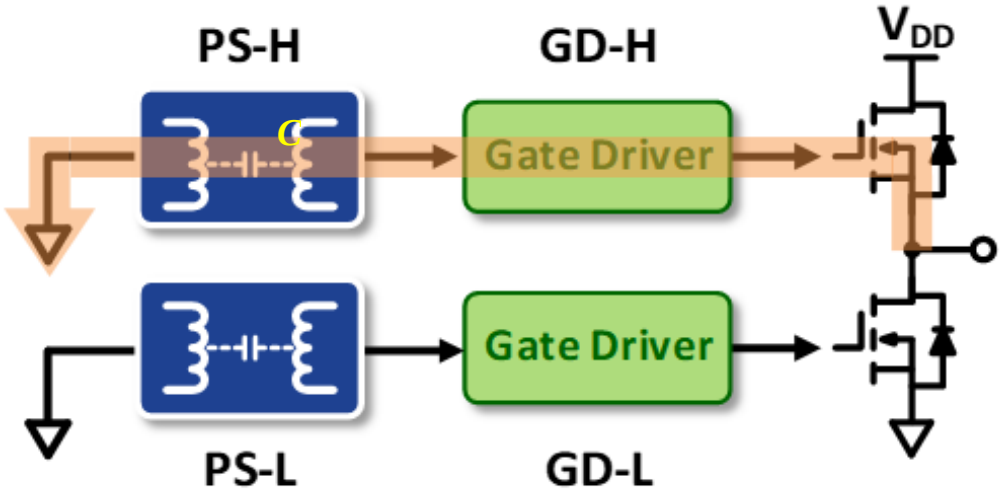


Fig. 5. CM noise propagation path in the gate drivers

Fig. 6. Gate drive with transformer-based isolated power supply designed by Zhang

To have good EMI mitigation, the target for the gate-drive power supply $C_{I/O}$ is less than 2 pF.

1.2.3 Voltage Regulation

Another challenge for the gate-drive power supply is the voltage regulation design. Since the gate driver might be switching at different frequency, the load for the power supply might change accordingly. Therefore, the power supply should be able to have a reliable performance at different load conditions. Generally, an isolated feedback control is used to regulate the output voltage (v_o), which is shown in Fig. 7. It is an efficient way to ensure the output regulation performance; however, adding an isolated feedback control from the secondary-side converter will create another coupling capacitor to the power supply, which one should try to avoid.

In regards to voltage regulation, the target is to design the output voltage measurement Δv_o at 20 percent to 100 percent of load condition to be less than 5 percent of the nominal output voltage v_o, which is 1.4 V.

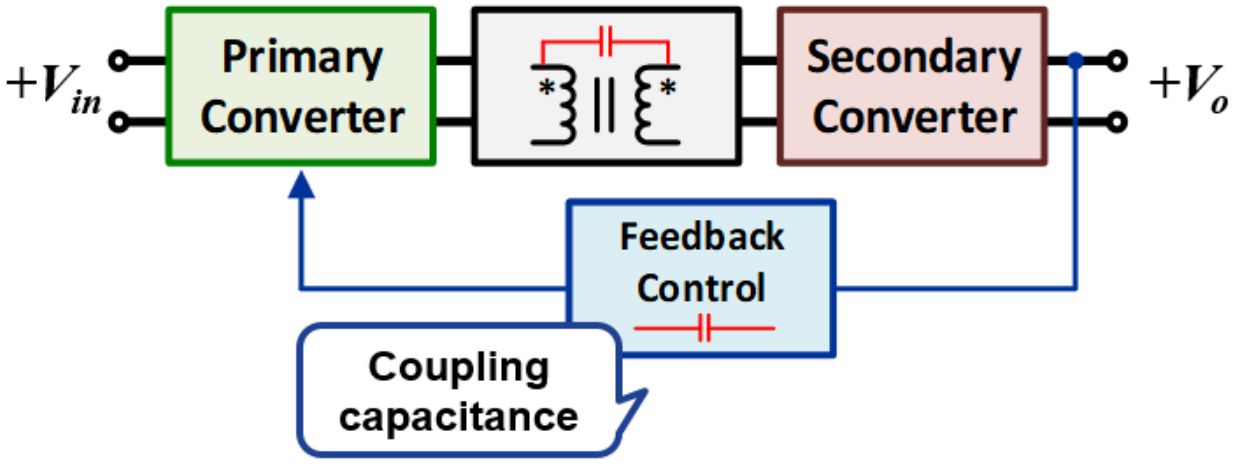


Fig. 7. Power supply structure with feedback control

1.2.4 Resiliency to Faults

The next challenge is the resiliency to faults. It is impossible to eliminate the faults during the operation, so protection design is also critical. When a fault exists at the load, the power supply should be able to limit the fault currents as well as protect the equipment. Furthermore, when the faults disappear, the isolated gate-drive power supply should be able to achieve restoration of service as well as ensure the circuit and equipment will not be damaged by the current or voltage spikes.

1.2.5 Specifications

The isolated gate-drive power supply specifications are shown in TABLE 2. As required by the gate drivers, the isolated power supply should provide 10 W to each load. The overall efficiency should not be less than 75 percent. Input voltage V_{in} is 24 V, and the output voltage V_o is 28 V. The power supply should also be able to sustain 10 kV DC to achieve the high insulation voltage design target. $C_{I/O}$ should be less than 2 pF to have good EMI mitigation and containment. The output voltage measurement Δv_o at 20 percent to full load should be less than

TABLE 2. SPECIFICATIONS

Property	Values
Power P_o	10 W
Efficiency η	>75%
Input voltage, V_{in}	24 V
Output voltage, V_o	28 V
Insulation, V_{ins}	10 kV
Volume	< 3 inch^3
Input-output capacitance, $C_{I/O}$	< 2 pF
ΔV_o @ 20% to 100% load	< 1.4 V

1.4 V.

1.3 Reviews of Gate Driver Power Supply HV Isolation Design

There are many gate-drive power supply techniques to achieve high insulation voltage. Fig. 8 shows the state-of-the-art isolation power supplies. One of the most common solutions is to utilize voltage-based transformers, which are shown in [5], [6], and [7]. A large magnetic core is used to isolate the primary and secondary windings keeping them at sufficient distance, which results in a heavy and bulky circuit. A secondary alternative design is the wireless power transfer (WPT) proposed in [8]. As the coupling coefficient is relatively weak in WPT, large space is still needed to increase the magnetizing inductance so the transmitted power can be increased. Xuan designs a power supply using an optic fiber technique. It is helpful to eliminate the $C_{I/O}$ coupling the power stage due to the lack of magnetic core, but the transmitted power is limited to 0.5 W [9]. Additionally, even though the laser receiver size shown in [9] is very small, the laser transmitter is still large. Gottschlich [10] designs a medium voltage power supply that uses a

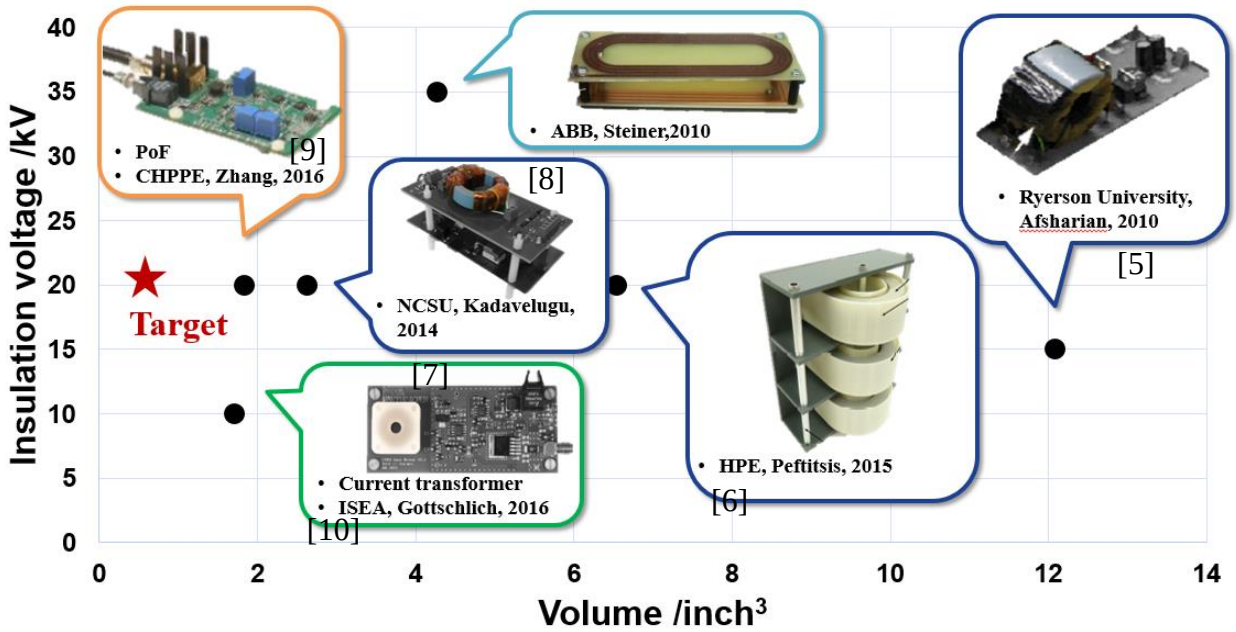


Fig. 8. State-of-the-Art HV isolation power supplies

current-loop AC-bus with a current-based transformer, achieving a $C_{I/O}$ of 1.05 pF and a relatively small volume of 1.7 inch^3. However, the switching frequency is below 50 kHz and the transmitted power is not large enough. In addition, it does not provide any further information related to the converter design.

Considering the design targets, wireless power transfer and optic fiber techniques are not considered due to their large size and limited transmitted power. The remaining power supply types can be classified as voltage-transformer based and the current-transformer based gate-drive power supply. A detailed comparison and analysis between these two types will be illustrated in the following chapters.

1.4 Thesis Outline

Considering all the challenges presented by the 10 kV, 240 A SiC MOSFETs module and its gate drivers, the focus of this work is to design a high-density, low $C_{I/O}$, multi-channel GaN power supply for gate drivers.

Chapter 1 introduces the benefits and challenges of the SiC MOSFETs module, followed by a summary of the targets and specifications. Chapter 2 compares the voltage-transformer based and current-transformer based gate-drive power supply. After careful comparison and analysis, the optimal structure in terms of HV isolation, EMI mitigation, voltage regulation and resilience will be determined. After selecting the transformer structure, the requirements will be shown. Later, the transformer input-output coupling capacitance $C_{I/O}$ is modeled and optimized. Transformer dimensions and input current frequency can be determined by the optimization results. In Chapter 3, topology candidates will be introduced. Simulation circuits are built to compare the performance of different candidates, and the LCCL-LC resonant converter is

chosen. Operation and design steps are provided in detail. With the estimated current and voltage ratings, power semiconductor devices can be selected in Chapter 4. The loss breakdown is also provided to estimate the gate-drive power supply efficiency. The test prototype and hardware assembly are shown in Chapter 5. Experimental testing results will be given to verify the design. Chapter 6 summarizes the work and conclusions derived from this thesis are given.

Chapter 2: Current Transformer Modeling and Design

2.1 Introduction

In terms of insulation, power density and EMI mitigation, the high-voltage, low $C_{I/O}$ transformer is the center of the isolated gate-drive power supply. Two transformer types are compared in this chapter and the current-source transformer is selected for the gate-drive power supply proposed in this thesis.

Applying a different approach than generally used with voltage-transformer based DC-DC converters, the gate-drive power supply, proposed in this thesis, designs and optimizes the transformer before topology selection. There are two reasons for this approach. First, the current-source input leads to various voltage across the transformer, bringing many limitations to the transformer design. Once the transformer dimensions change, its properties change. One cannot simply adjust the cross-section area and turn number to prevent saturation like a normal voltage-source transformer does.

The topology is only required to provide a current-source input, which is easy to approach, since the design of the topology is based on the transformer properties. It is difficult to design the passive components' value without the transformer properties. Additionally, changing topology will not lead to the modification of the transformer; therefore, designing the transformer before the selection of topology simplifies the task.

In this chapter, the voltage-transformer based and current-transformer based gate-drive power supply are compared to determine the transformer structure. The limitation of the transformer design will be illustrated, and the approach for satisfying the requirements will be given. The model of transformer input-output coupling capacitance $C_{I/O}$ will be built, and

experimental testing is shown to prove the model validation, after which, the transformer dimensions can then be selected. The current-source frequency of the transformer is selected based on the optimization results.

2.2 Voltage Source and Current Source Transformer Comparison and Selection

2.2.1 HV insulation design

As stated previously, there are several popular transformer techniques for high-voltage isolation design including wireless power transfer, optic fiber, voltage-source transformers and current-source transformers. Wireless power transfer and optic fiber techniques have already been eliminated and only voltage-source and current-source transformers are considered and analyzed here. In terms of the high-density design, voltage-source transformer structure is at a disadvantage. It needs a large magnetic core separating the primary- and secondary- windings to keep sufficient creepage distance, previously shown in Fig. 4. The current-source transformer, whose turn number of the primary side is designed to be one, enables the low-voltage (LV) and HV interfaces to be separated into two boards [10]. In this case, the creepage path will be the path along the primary-side cable instead of the transformer core, which is illustrated in Fig. 9. Cable length can be utilized to increase the creepage distance, and the transformer core is no longer needed to provide the creepage distance. Insulation design is also simplified by using the HV insulation material around the cable.

[10]

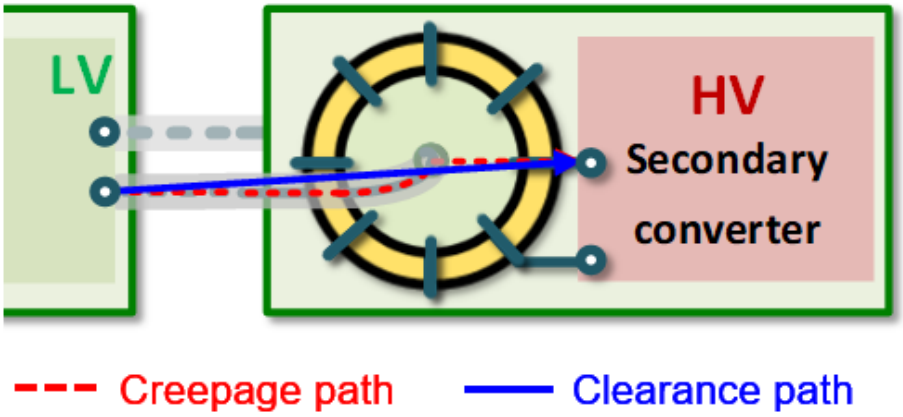


Fig. 9. HV isolation design of current-source transformer

2.2.2 Low $C_{I/O}$ Transformer Design

The next comparison is the low input-output coupling capacitance $C_{I/O}$ design. The value of input-output coupling capacitance $C_{I/O}$ is related to the transformer core material, size, and winding designs [11]. When the core material and dimensions are the same, the current-source transformer will have a smaller input-output coupling capacitance $C_{I/O}$ due to its lower turn number and winding area.

2.2.3 Voltage Regulation Design

Fig. 10 and Fig. 11 show the equivalent circuit of the voltage-source and current-source transformer, respectively, where L_{pk}, L_m and n are the leakage inductance, magnetizing

inductance, and transformer ratio. The secondary leakage inductance has been reflected to the primary side. For the voltage-source transformer, the output voltage can be given by (2), where v_m is the voltage across the magnetizing inductance.

$$\vec{V}_o = n \cdot \vec{V}_m \tag{2}$$

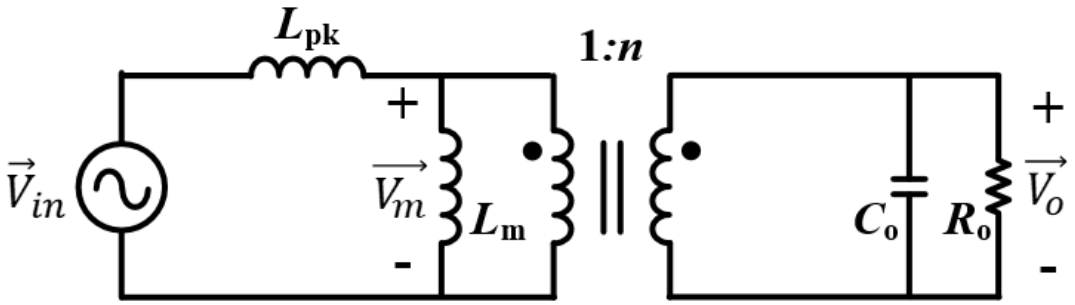


Fig. 10. Equivalent circuit of voltage-source transformer

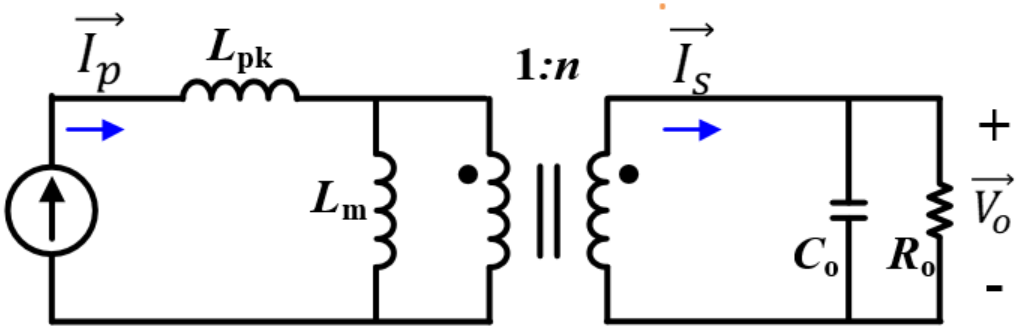


Fig. 11 Equivalent circuit of current-source transformer

$$\vec{V}_m = \vec{V}_{in} \cdot \frac{L_m}{L_p} \tag{3}$$

$$L_p = L_m + L_{pk} \tag{4}$$

It can be seen that for the voltage-source transformers, the equations of output voltage do not contain the load resistor R_o, so, in different load conditions, V_o stays constant, which is a benefit to the voltage regulation design.

However, for the current-source transformer, the output voltage is:

$$\vec{V}_o = \frac{\vec{I}_p}{n} \cdot \left(\frac{1}{j\omega C_o} \,||\, R_o\right) \tag{5}$$

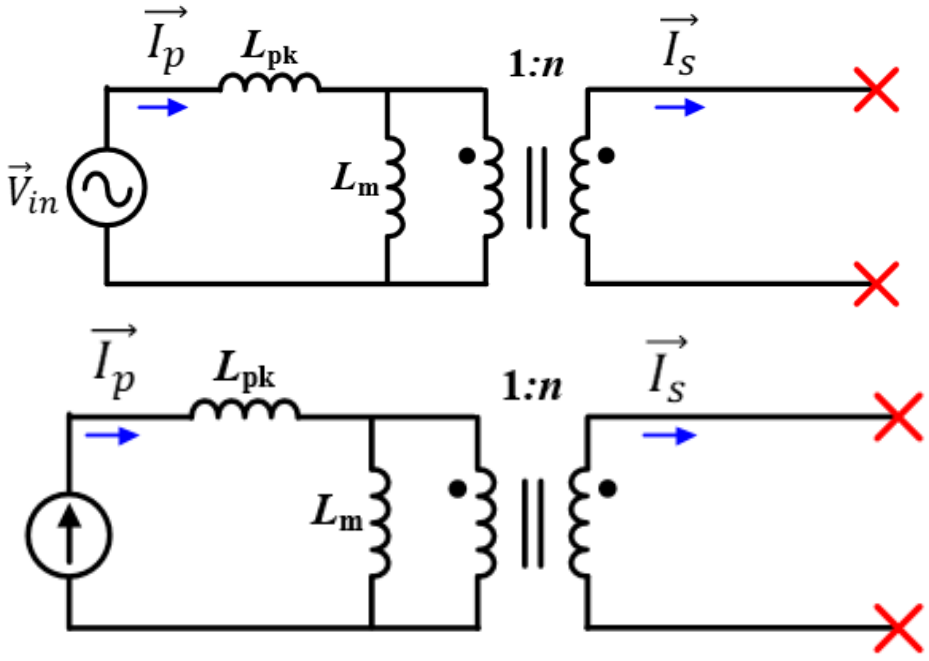
Equation (5) contains the load resistor, so V_o may vary with the change of R_o, which brings difficulty to output voltage regulation.

2.2.4 Resilience Design

Short-circuit and open-circuit faults are the most common and critical faults at the load. The equivalent circuits of voltage-source and current-source transformer when faults exist are shown in Fig. 12 and Fig. 13.

Fig. 12 shows the condition that the load is opened. According to Fig. 10, the input impedance Z_{in} without faults is:

$$Z_{in} = j\omega L_{pk} + (j\omega L_m) \,||\, \frac{Z_o}{n^2} \tag{6}$$



(b)

Fig. 12. Equivalent circuit of open-circuit fault existing at (a) voltage-source and (b) current-source transformer

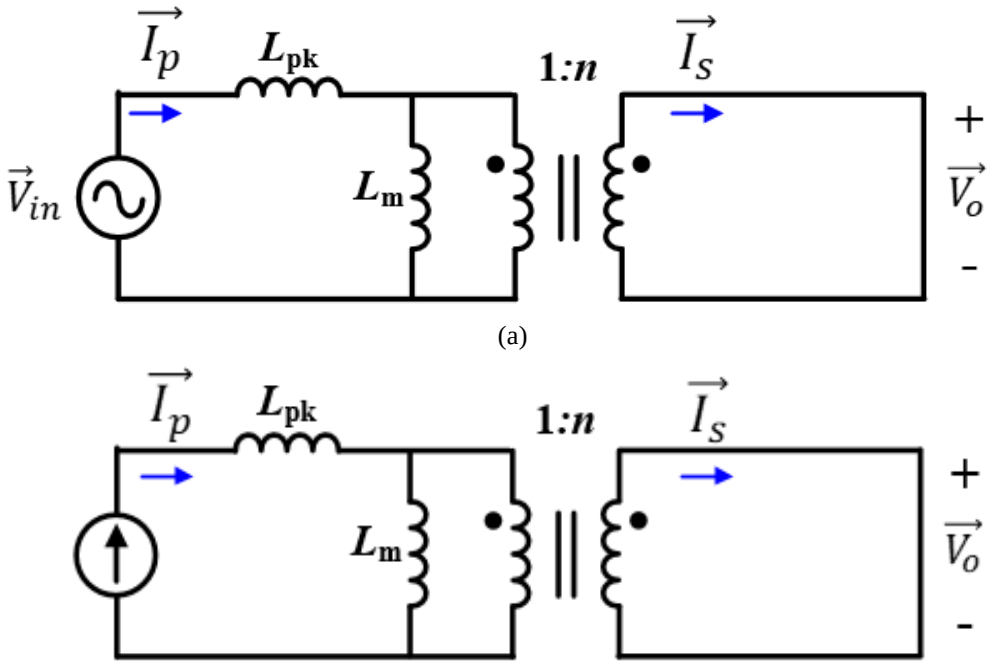


Fig. 13 Equivalent circuit of short-circuit fault existing at (a) voltage-source and (b) current-source transformer

When the load is opened, then the input impedance Z_{in} changes to Z_{in_o}:

$$Z_{in\_o} = j\omega L_{pk} + j\omega L_m = j\omega L_p > Z_{in} \tag{7}$$

It equals to the transformer primary-side self-inductance, which is larger than Z_{in}. The primary-side current I_p will not boost and damage the circuit, so both the voltage-source transformer and current-source transformer have the capability to restore in the open-circuit condition.

However, the short-circuit fault will bring challenges. The equivalent circuits when the load is shorted are shown in Fig. 13.

When the load is shorted, it also means that the magnetizing inductance is also shorted. The input impedance Z_{in} changes to Z_{in_i}:

$$Z_{in\_i} = j\omega L_{pk} < Z_{in} \tag{8}$$

For the voltage-source transformer, its magnetizing inductance L_m is always designed to be much larger than the leakage inductance L_{pk} to maximize the transmitted power. Therefore, shorting the magnetizing inductance L_m leads to a drastic reduction of the input impedance. As a result, the primary-side current will boost and damage the circuit. Another possible solution is to add a large air gap to increase leaking inductance, but a resulting drawback of that method would be an increase of the loss.

The current-source transformer does not need to be concerned about this problem, as the leakage inductance given by the long primary-side HV cable is large enough to avoid short-circuit damage (shown in Fig. 13 (a)). Thus, the current-source transformer still has restoration of service when the faults disappear.

TABLE 3 summarizes the benefits and drawbacks between voltage-source and current-source transformers. To be summarized, the current-source transformer is more competitive in terms of the HV, HD insulation design, $C_{I/O}$ design and resilience design.

TABLE 3. COMPARISON OF VOLTAGE- AND CURRENT-SOURCE TRANSFOREMR

	HV insulation requirement	$C_{I/O}$ design	Voltage regulation	Resilience to faults
Voltage-source input	Large profile (creepage)	High (same core)	Easy to meet	Shutdown and no automatic resart
Current-source input	Small profile (no creepage)	Low (same core)	Requires careful design	Faul ridethrough and automatic recover

Furthermore, the number of primary converters can be reduced to half as the two secondary converters can share the same high-voltage cable, which is greatly beneficial for the compact design.

The structure for one SiC MOSFETs module is shown as Fig. 14.

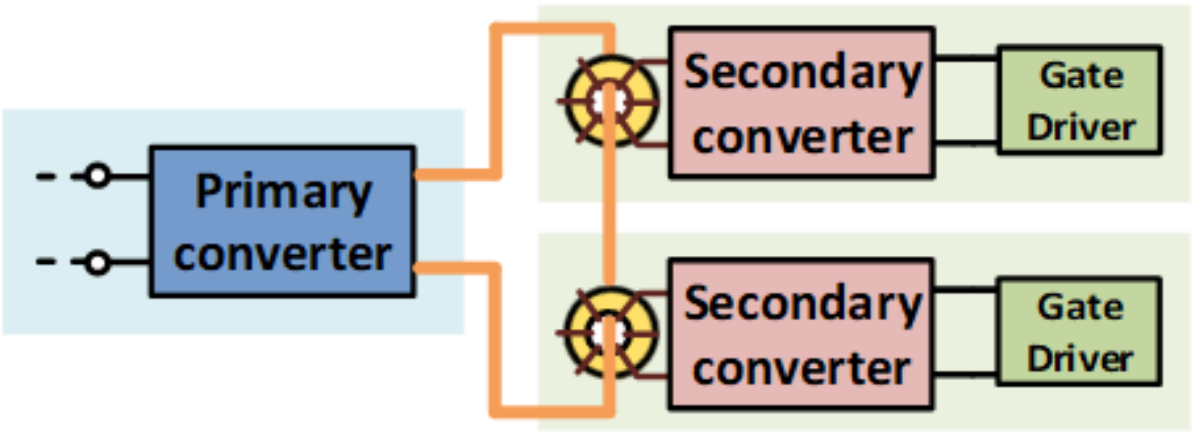


Fig. 14. Structure of gate-drive power supply for one module

2.3 Transformer Design

Flux density design is at the center of the transformer design because a high flux density may lead to a high loss or even cause core saturation, a very undesirable effect. The relationship between peak flux density B_p and peak voltage V_p across the transformer primary-side are shown as equation (9).

$$B_p = \frac{V_p}{\omega \cdot N_p \cdot A_c} \tag{9}$$

Where N_p, A_c and $\omega=2\pi f$ are the transformer primary-side turn number, cross-section area and the angular frequency respectively.

According to the equation, N_p, A_c and ω can be increased to reduce the value of B_p when V_p is fixed. However, for the current-source transformer, this approach is no longer available. First, N_p is fixed to one, as one of the optimizable parameters is unavailable. Second, the primary-side peak voltage V_p varies with the inductances, which are determined by the core geometry A_c. We cannot simply increase ω and A_c to reduce the flux density, as V_p will also grow with the change of A_c. Detail analysis and transformer inductances optimization for B_p will be illustrated in Section A.

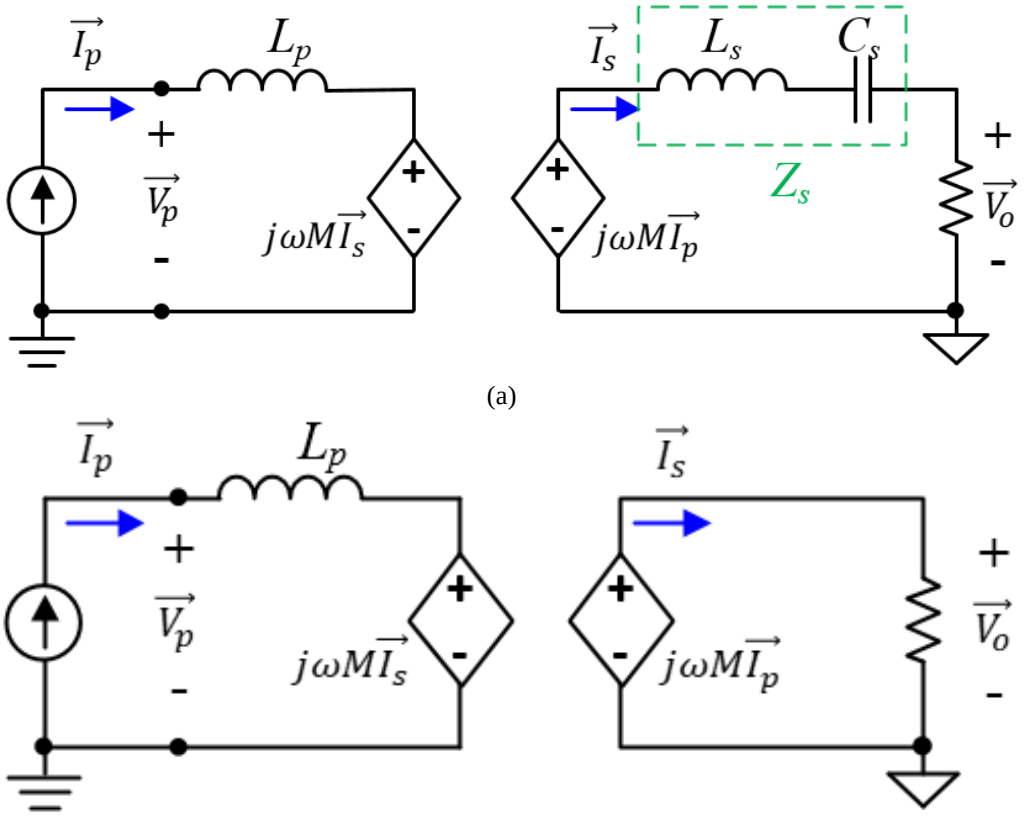
A. Mutual Inductance Design

A simplified equivalent circuit of a current-source input transformer is shown in Fig. 15 (a). To maximize the power transfer, an extra compensation capacitor C_s is added in series with the secondary self-inductance L_s. The value of C_s is decided by equation (20).

$$L_s \cdot C_s = \frac{1}{\omega^2} \tag{10}$$

$$Z_s = j\omega Ls + \frac{1}{j\omega C_s} = 0 \tag{11}$$

When L_s and C_s are in resonance, their equivalent impedance Z_s is equal to zero at frequency ω, so it can be removed from the path. Fig. 15 (a) can be further simplified as Fig. 15 (b). The secondary output current (load current) I_s can be given by equation (12) and (13). It can be seen that the primary-side current I_p and secondary-side current I_s have a 90 ° phase shift if L_s and C_s



(a)

(b)

Fig. 15. Simplified equivalent circuit

are in well resonant. The amplitude of I_s, which is shown by equation (13). decreases with the growth of load resistor R_o. According to equation (14), we can design the I_p value to have the required V_o. Combining (13), (14), and (15), transformer primary-side peak voltage can be given by equation (16).

$$\vec{I}_s = \frac{j\omega M \cdot \vec{I}_p}{R_o} \tag{12}$$

$$I_s = \frac{P_o}{V_o} \tag{13}$$

$$\vec{V}_o = j\omega M \cdot \vec{I}_p \tag{14}$$

$$\vec{V}_p = \mathrm{j}\omega M \cdot \vec{I}_s + j\omega L_p \cdot \vec{I}_p \tag{15}$$

$$V_p = \sqrt{(\omega M \frac{P_o}{V_o})^2 + (L_p \cdot \frac{V_o}{M})^2} \tag{16}$$

Combing equation (9) and (16), the peak flux density B_p can be derived and shown as following:

$$B_p = \frac{1}{\omega \cdot A_c} \cdot \sqrt{(\omega M \frac{P_o}{V_o})^2 + (L_p \cdot \frac{V_o}{M})^2} \tag{17}$$

If we assumed that the transformer primary-side self-inductance L_p and $\omega=2\pi f$ are fixed, the mutual inductance is the only variable. B_p has a minimal value B_{p_min} when M is equals to M_{op}:

$$M_{op} = \sqrt{\frac{L_p \cdot V_o^2}{\omega P_o}} \tag{18}$$

$$B_{p\_\min} = \frac{1}{A_c}\sqrt{\frac{2P_o L_p}{\omega}} \tag{19}$$

One can examine a particular case as an example to describe the equations analyzed previously, using the parameters summarized in TABLE 4. When all the values shown in

TABLE 4 into equation (17) are substituted, the equation changes to (20), which is also described in Fig. 16. The green dot is the point (M_{op}, B_{p_min}) in TABLE 4.

TABLE 4. TANSFORMER DESIGN EXAMPLE

Lp	Vo	*Po*	*f*	A_c	M_{op}	B_{p_min}
1.5 μH	28 V	10 W	1 MHz	20 mm^2	4.33 μH	0.11

$$B_p(\mathrm{M}) = \frac{1}{40\pi} \cdot \sqrt{\left(\frac{\pi \times 10^7}{14}\mathrm{M}\right)^2 + \left(\frac{4.2 \times 10^{-5}}{M}\right)^2} \tag{20}$$

Further, as the transformer only has one turn at primary side, the secondary-side self-inductance L_s, mutual inductance M can be given by equation (21) and (22), where k and N_s are the transformer coupling coefficient, secondary-side turn number, respectively. Combining equation (18) and (22), N_s should be designed as in the following equation (23) to have a minimum B_p.

$$L_s = N_s^2 \cdot L_p \tag{21}$$

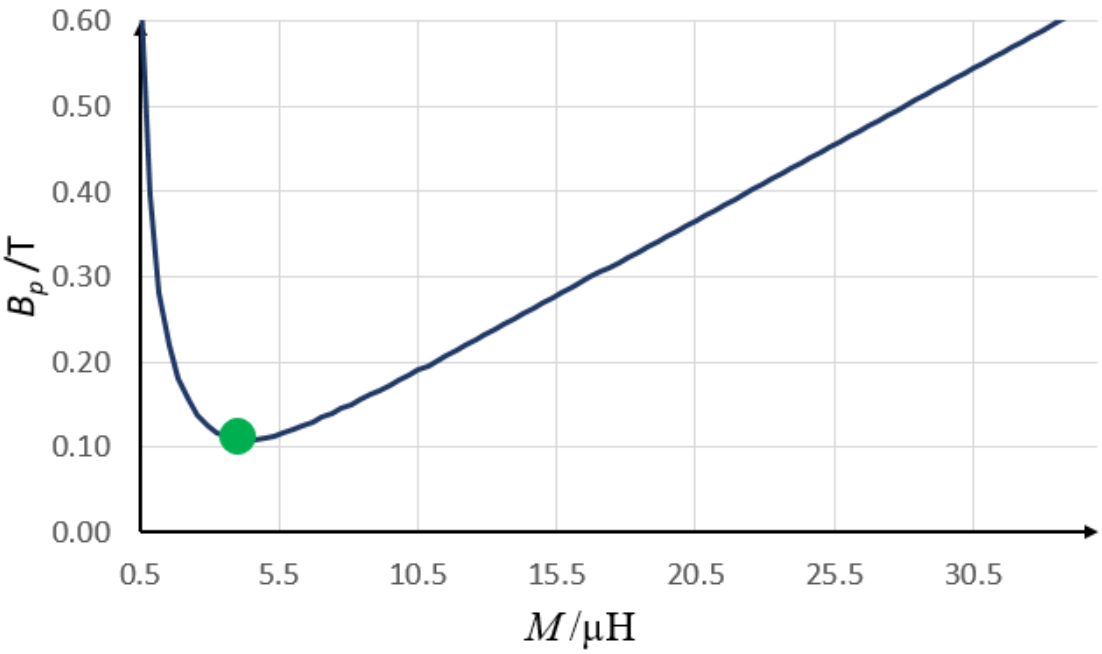


Fig. 16. Transformer mutual inductance design

$$M = k \cdot \sqrt{L_p \cdot L_s} = k \cdot \sqrt{L_p \cdot N_s^2 \cdot L_p} = k \cdot N_s \cdot L_p \tag{22}$$

$$N_s = \frac{1}{k} \cdot \sqrt{\frac{P_o}{\sqrt{2}\omega L_p}} \tag{23}$$

The transformer design discussed in the previous analysis assumes that L_p is fixed. However, L_p varies with core material and dimensions. It can be derived by the following equations:

(24)

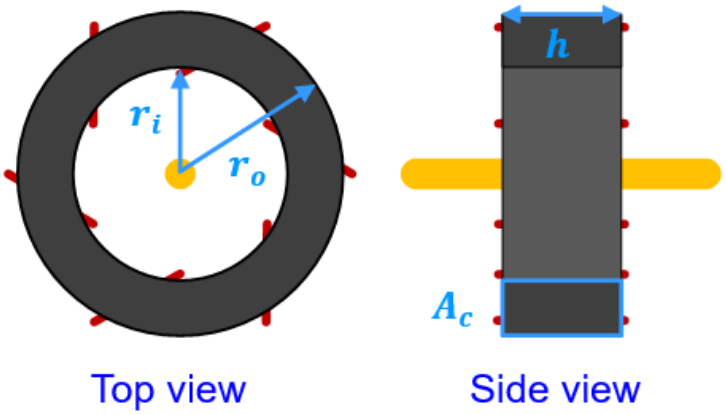


Fig. 17. Transformer structure with toroid core

$$L_p = \frac{\Phi}{I} = \frac{\mu \cdot h \cdot \ln(\frac{r_o}{r_i})}{2\pi}$$

Where, μ, ϕ, B, H *and* I are the core permeability, flux, flux density, magnetizing force and the current respectively. l_c is the effective core length, A_c is the toroid core cross-section area, r_o is the toroid core outer radius, r_i is the toroid core inner radius, and h is the core height, which are shown in Fig. 17.

$$\Phi = B \cdot A_c$$

$$A_c = (r_o - r_i) \cdot h \tag{26}$$

$$B = \mu \cdot H \tag{27}$$

$$H = \frac{I}{l_c} \tag{28}$$

$$l_c = \frac{2\pi(r_o - r_i)}{\ln(\frac{r_o}{r_i})} \tag{29}$$

After the optimization of $C_{I/O}$, it is also very important to calculate the L_p value and put it into equation (19) to make sure that B_p meets the material maximum flux density requirement.

B. $C_{I/O}$ Modeling and Optimization

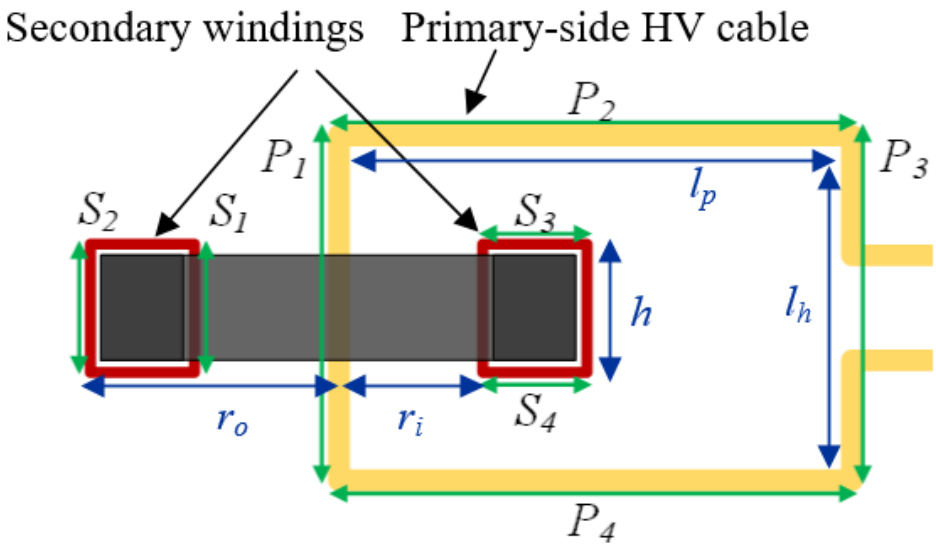


Fig. 18. Transformer winding geometry

In this section, the mathematical derivation of the $C_{I/O}$ using an electric energy method proposed by K. Nguyen-Duy [12] is utilized to build the parasitic capacitance model. Experiment results will be shown to prove the validity of the approach.

The total calculation is divided into six parts, which are the parasitic capacitor caused by segments P_1 and S_1, P_1 and S_2, P_3 and S_1, P_3 and S_2, P_2 and S_3, P_4 and S_4 (refer to Fig. 18).

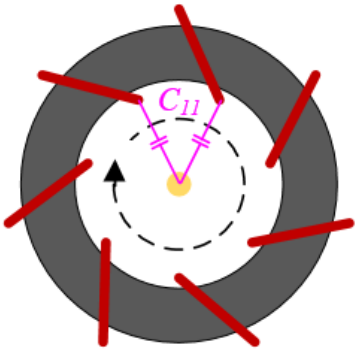


Fig. 19. Cross-sectional top view: static capacitance from the winding of segment P_1 and S_1

Firstly, the input-output capacitance caused by the segments P_1 and S_1 is calculated. The static capacitance (see Fig. 19) can be expressed as following:

$$C_{11} = \frac{\varepsilon_0}{r_i} \cdot \left(\frac{1}{\frac{1}{S_{p1}} + \frac{1}{S_{s1}}}\right) \tag{30}$$

Where ε_0 is the permittivity of free air space, S_p and S_s are the equivalent plate area of the primary windings and secondary windings. Assuming the voltage potential distribution along the secondary turns varies linearly,

$$V_p[\mathrm{i}] = \frac{i}{N_s - 1} \cdot V_p, (\mathrm{i} = 0,1,2,\ldots N_s - 1) \tag{31}$$

Then the total stored electric energy between primary cable and all secondary turns is:

$$E_{11} = \frac{1}{2} C_{11} \cdot \sum_{i=0}^{N_s-1} \left(\mathrm{V_p} - \frac{V_s \cdot i}{N_s - 1}\right)^2 \tag{32}$$

Similarly, the static capacitance caused by segments P_1 and S_2 (shown in Fig. 20) and their total stored electric energy are given by equation (33) and (34).

$$C_{12} = \frac{\varepsilon_0}{r_o} \cdot \left(\frac{1}{\frac{1}{S_{p1}} + \frac{1}{S_{s2}}}\right) \tag{33}$$

$$E_{12} = \frac{1}{2} C_{12} \cdot \sum_{i=0}^{N_s-1} \left(V_p - \frac{V_s \cdot i}{N_s - 1}\right)^2 \tag{34}$$

The capacitances caused by the side segments P_2 and S_3, P_4 and S_4 are:

$$C_{23/44} = \frac{\varepsilon_0}{\frac{1}{2}(l_h - h)} \cdot \left(\frac{1}{\frac{1}{S_{p\,2/4}} + \frac{1}{S_{s\,3/4}}}\right) \tag{35}$$

As segments P_2 and S_3, P_4 and S_4 face the middle parts of the secondary winding, it is appropriate to assume that there are three turns from the secondary winding, which lie in segment S_3 or S_4 of Fig. 17, facing segment P_2, P_4, respectively. They are turn number (N_s-1)/2-1, (N_s-1)/2 and (N_s-1)/2+1. The stored electric energy caused will be:

$$E_{23/44} = 2 \cdot \left(\frac{1}{2} C_{23/44} \cdot \sum_{(N_s-1)/2-1}^{(N_s-1)/2+1} \left(V_p - \frac{V_s \cdot i}{N_s - 1}\right)^2 \right) \tag{36}$$

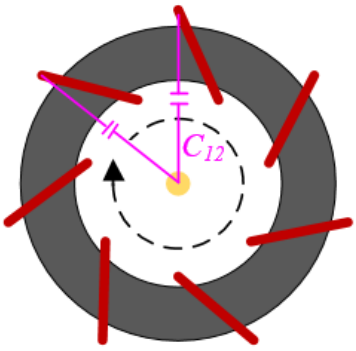


Fig. 20. Cross-sectional top view: static capacitance from the winding of segment P_1 and S_2

Next, the contribution of segment P_3 and S_1 is computed. Referring to Fig. 21, in triangle AOB, distance AB is calculated by equation (37).

$$\begin{aligned}\overline{AB}^2 &= \overline{AO}^2 + \overline{OB}^2 - 2\overline{AO \cdot OB}\cdot\cos(\Phi) \\ &= \mathrm{r_o}^2 + \mathrm{l_p}^2 - 2\,\mathrm{r_o}\cdot\mathrm{l_p}\cdot\cos(\pi - \frac{2\pi}{N_s})\end{aligned} \tag{37}$$

Therefore, distance from point B to the i^{th} turn of segment S_1 is:

$$r_{31,\,j} = \sqrt{\mathrm{r_i}^2 + \mathrm{l_p}^2 - 2\,\mathrm{r_i}\cdot\mathrm{l_p}\cdot\cos(\pi - \frac{j\cdot 2\pi}{N_s})},\ (j = 0,1,2,\ldots,\mathrm{N_s}-1) \tag{38}$$

The static capacitance from point B to the j^{th} turn of segment S_1 is:

$$C_{31,\,j} = \frac{\varepsilon_0}{r_{31,\,j}}\cdot\left(\frac{1}{\frac{1}{S_{p3}} + \frac{1}{S_{s1}}}\right) \tag{39}$$

The total stored energy is derived by equation (40)

$$E_{31} = \frac{1}{2}\sum_{j=0}^{N_s-1}\sum_{i=0}^{N_s-1} C_{31,\,j}\cdot\left(\mathrm{V_p} - \frac{V_s\cdot i}{N_s - 1}\right)^2 \tag{40}$$

Similarly, the static capacitance and stored energy caused by segment P_3 and S_2 are shown in equation (41), (42) and (43) respectively.

$$r_{32,\,j} = \sqrt{\mathrm{r}_o^2 + \mathrm{l_p}^2 - 2\,\mathrm{r_o}\cdot\mathrm{l_p}\cdot\cos(\pi - \frac{j\cdot 2\pi}{N_s})},\ (j = 0,1,2,\ldots,\mathrm{N_s}-1) \tag{41}$$

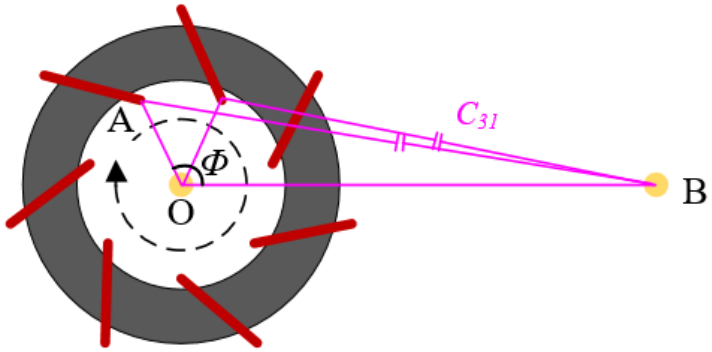


Fig. 21. Cross-sectional top view: static capacitance from the winding of segment P_3 and S_1

$$C_{32,\,j} = \frac{\varepsilon_0}{r_{32,\,j}} \cdot \left(\frac{1}{\frac{1}{S_{p3}} + \frac{1}{S_{s2}}}\right) \tag{42}$$

(43)

TABLE 5. TRANSFORMER PROPERTIES

Xformer #	Materials	Manufacturor	r_o(mm)	r_i (mm)	h (mm)	N_s
1	P61	ACME	12	7	2	8
2	P61	ACME	14	12	6	10
3	ML12D	Hitachi	11	7	5	6
4	P61	ACME	11	7	10	5
5	ML12D	Hitachi	11	7	15	5

$$E_{32} = \frac{1}{2} \sum_{j=0}^{N_s-1} \sum_{i=0}^{N_s-1} C_{32,\,j} \cdot \left(\mathrm{V_p} - \frac{V_s \cdot i}{N_s - 1}\right)^2$$

The total stored electric energy is then:

$$E_{total} = E_{11} + E_{12} + E_{23} + E_{44} + E_{31} + E_{32} = \frac{1}{2} \cdot C_{I\,/\,O} \cdot (\mathrm{V_p} - \mathrm{V_s})^2$$

Based on equation (44), the $C_{I/O}$ can be calculated.

To validate the model, five transformers with different transformer core materials and dimensions summarized in TABLE 5 have been selected. They are tested by an Agilent 4294A Precision Impedance Analyzer.

The comparison between calculation and measurement is shown in Fig. 22.

The red curve represents measurement whereas the blue curve represents the calculated results. It is illustrated that they match well with each other, thereby proving the accuracy of the model.

2.4 Frequency Determination

The next parameter that needs to be determined is the frequency ω.

There are several material candidates for the transformer core at different frequency range considering the loss behavior. After comparison, 3F3 from Ferroxcube is considered under 200 kHz whereas Hitachi ML95S is considered for the frequency between 200 kHz and 1 MHz. ML91S from Hitachi is the chosen candidate for the frequency starting from 1 MHz. With given material and frequency, we can start to use the model built in Chapter 2.3 to figure out the

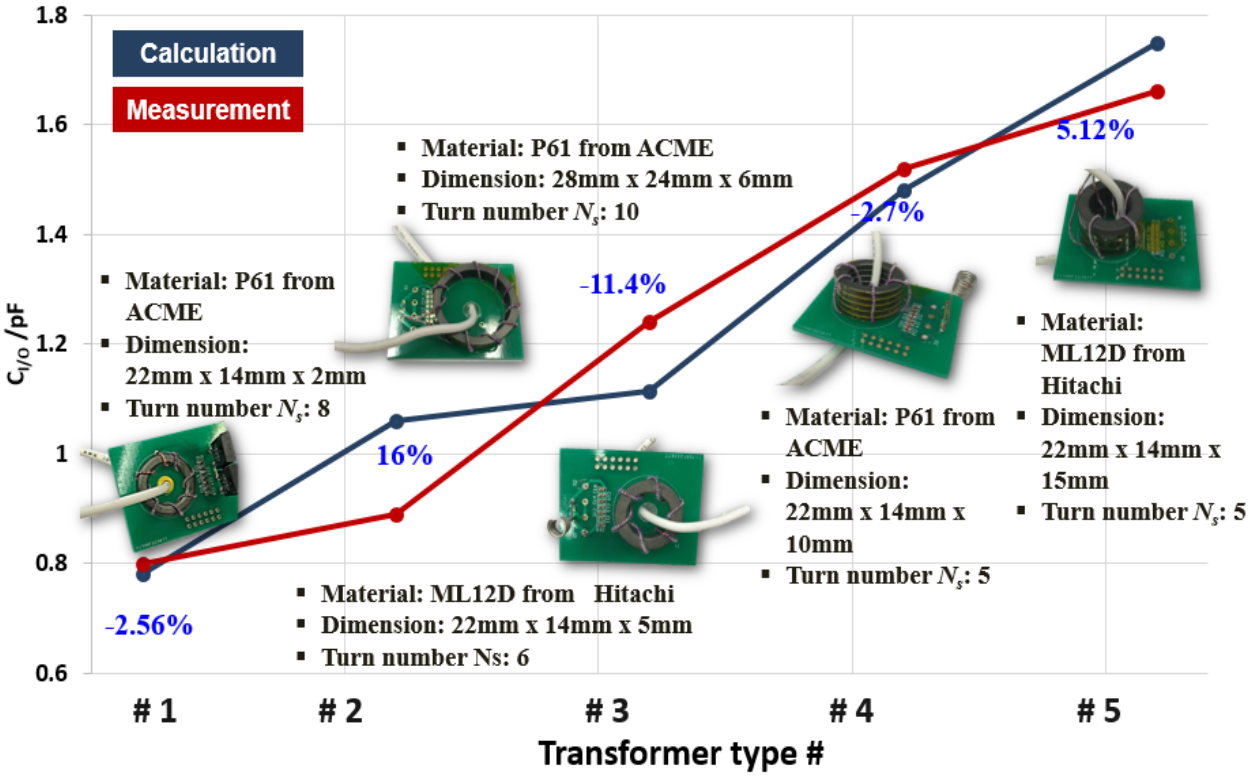


Fig. 22. $C_{I/O}$ model verification

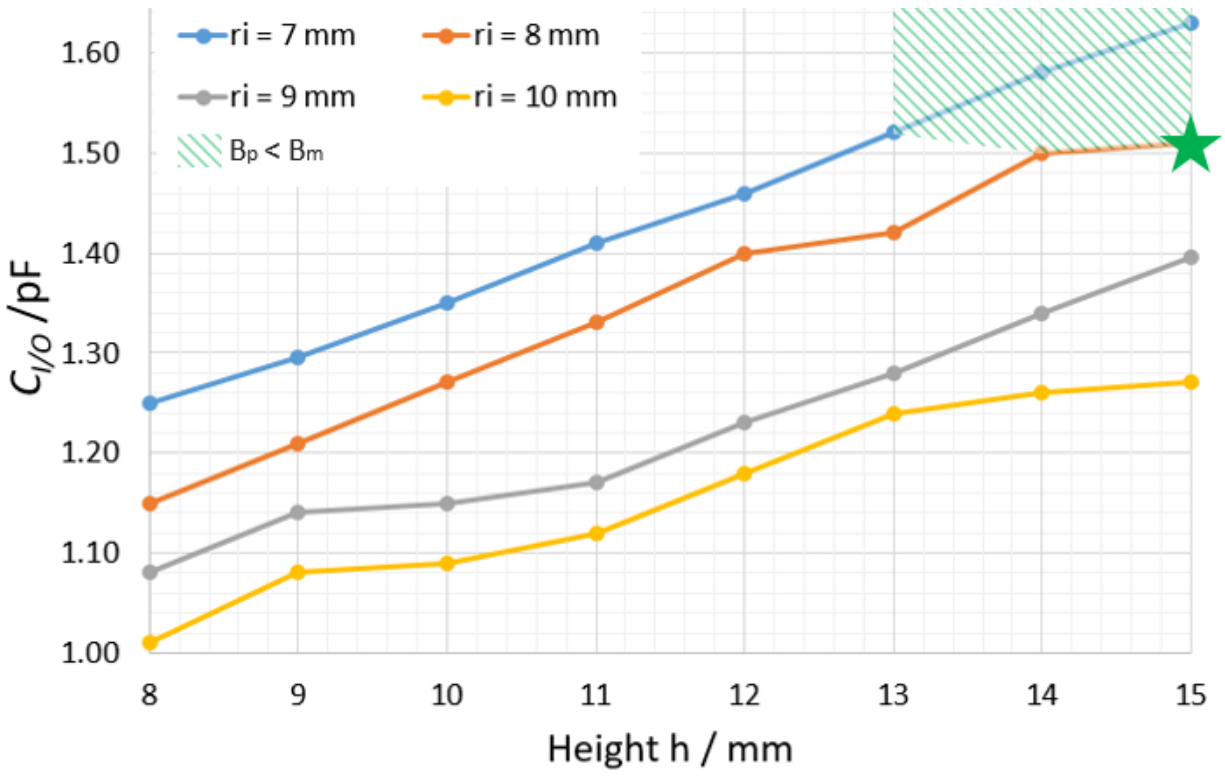


Fig. 23. $C_{I/O}$ of different sizes at 700 kHz for ML95S from Hitachi

optimal core dimension that has the lowest $C_{I/O}$.

Following are two examples. The first one uses Hitachi ML95S and it will be switching at 700 kHz. The second one utilized Hitachi ML91S and designed to switch at 1MHz.

For the Hitachi ML95S, the maximum flux density B_{max} at 700 kHz will be 70 mT. Fig. 23 shows the $C_{I/O}$ calculated by the model with different core sizes. There are four curves in the chart. Each curve has a different inner radius r_i. Therefore, there is only one variable, height h, in each curve. The green pattern-filled area shows the boundary for the B_p requirement. The points within this area have a B_p value that is smaller than B_{max}.

Obviously, if other dimensions remain unchanged, the input-output capacitance $C_{I/O}$ decreases with the growth of inner radius r_i. When we fix the inner radius r_i, the input-output capacitance $C_{I/O}$ increases with the growth of height h. However, the peak flux density B_p has an

opposite trend. Therefore, there is a trade-off between input-output capacitance $C_{I/O}$ and peak flux density B_p. The purpose for this chart is to figure out the dimensions that has the smallest input-output capacitance $C_{I/O}$ and the maximal allowable B_p. This point will be located at the boundary of the green pattern fill region, which is marked by green star in the chart. The lowest point for $C_{I/O}$ is 1.52 pF. The dimensions are a 25 mm outer radius r_o, an 8 mm inner radius r_i

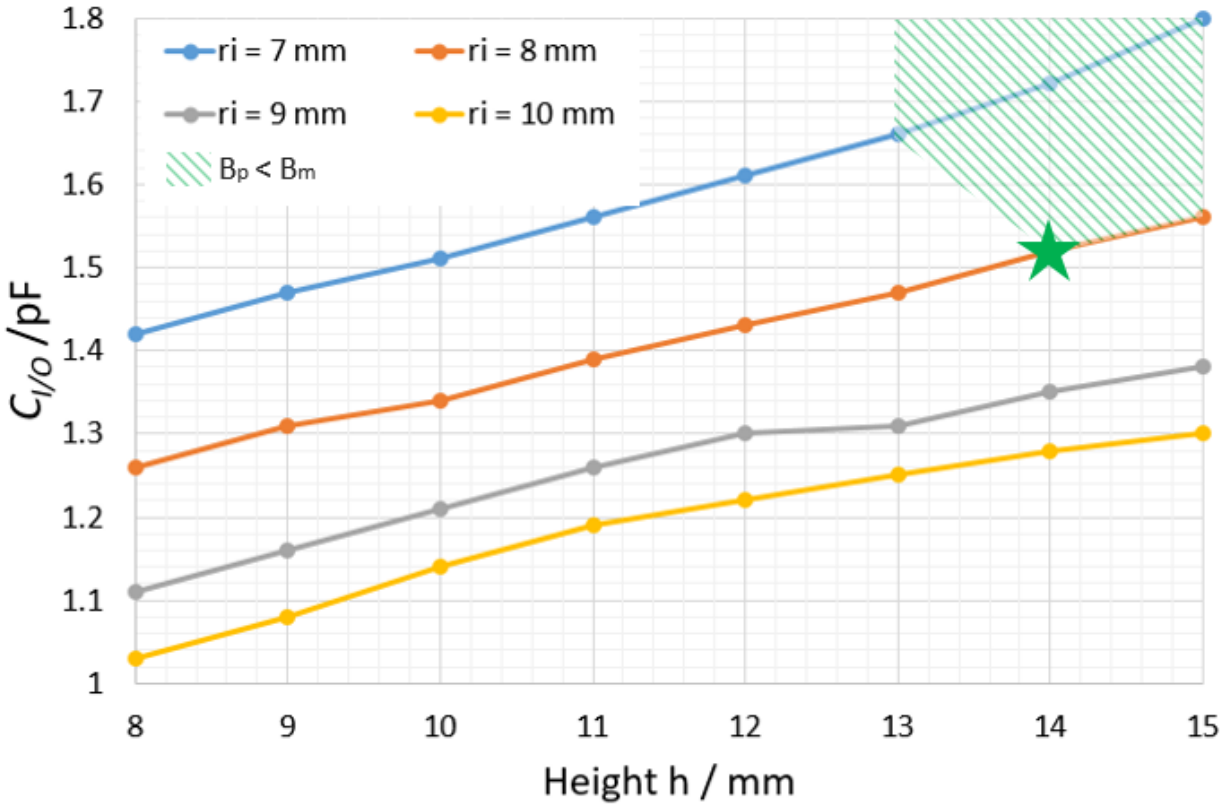


Fig. 24. $C_{I/O}$ of different sizes at 1 MHz for ML91S from Hitachi

and a 15 mm height respectively

The other example is shown in Fig. 24. The maximum flux density B_{max} at 1 MHz will be 50 mT. Similarly, all the points that have a peak flux density B_p smaller than 50 mT have been collected by the green pattern fill region. The lowest point is marked by the green star.

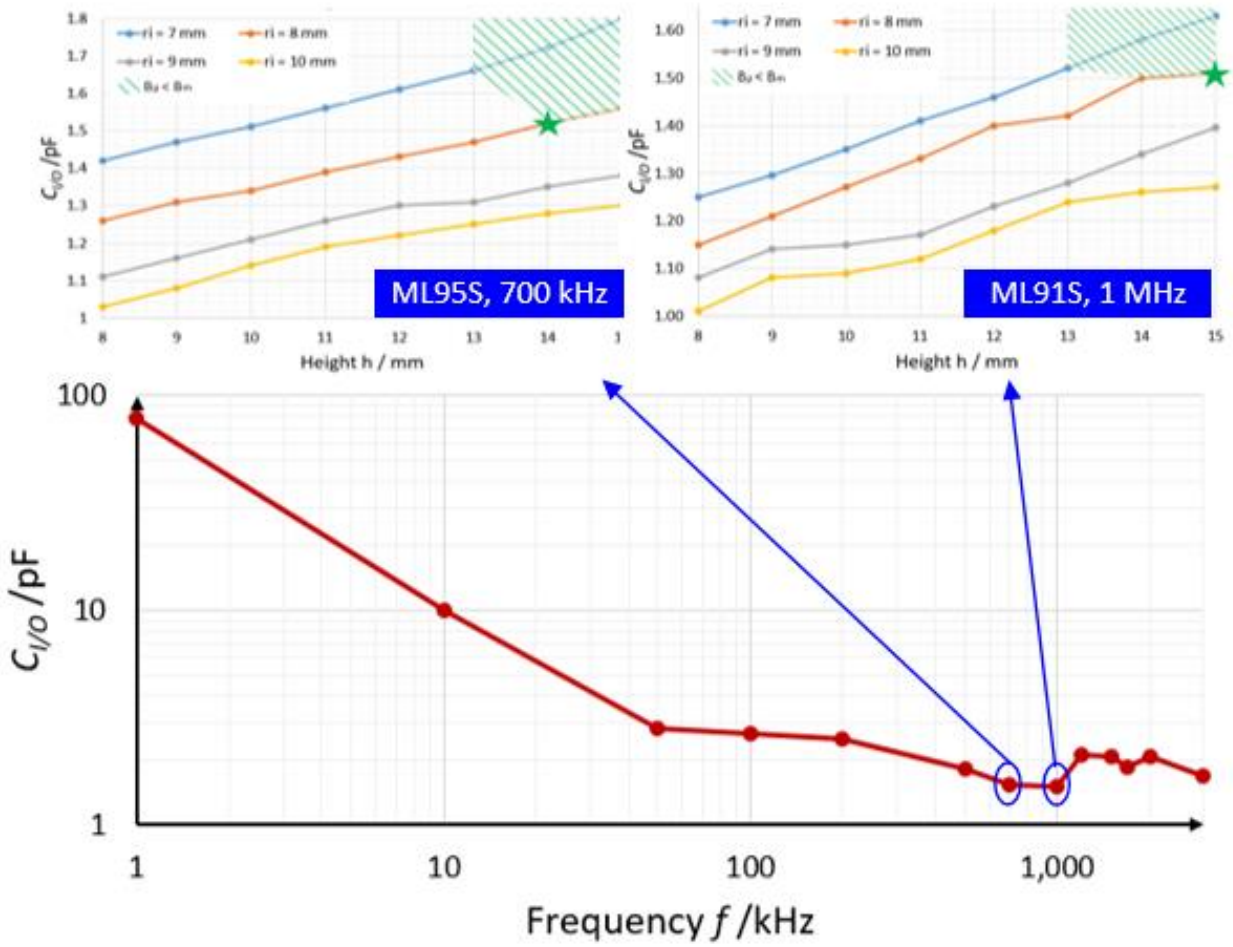


Fig. 25. $C_{I/O}$ at different frequency

The smaller $C_{I/O}$ is 1.51 pF and the dimensions are a 25 mm outer radius r_o, an 8 mm inner radius r_i and a 14 mm height, respectively.

With the same approach, the lowest $C_{I/O}$ and its corresponding core volume under each frequency are summarized at Fig. 25 and Fig. 26.

According to Fig. 25 and Fig. 26, the input-output capacitance $C_{I/O}$ increases rapidly when the frequency is less than 50 kHz. Input-output capacitance $C_{I/O}$ may reach 80 pF at reach 1 kHz. Therefore, the frequency of the transformer input current should be designed at least 500 kHz. The volume also grows quickly as the frequency gets smaller. This occurs because the cross-section area A_c of the transformer core needs to be increased to reduce the peak flux density B_p to avoid the high loss and saturation.

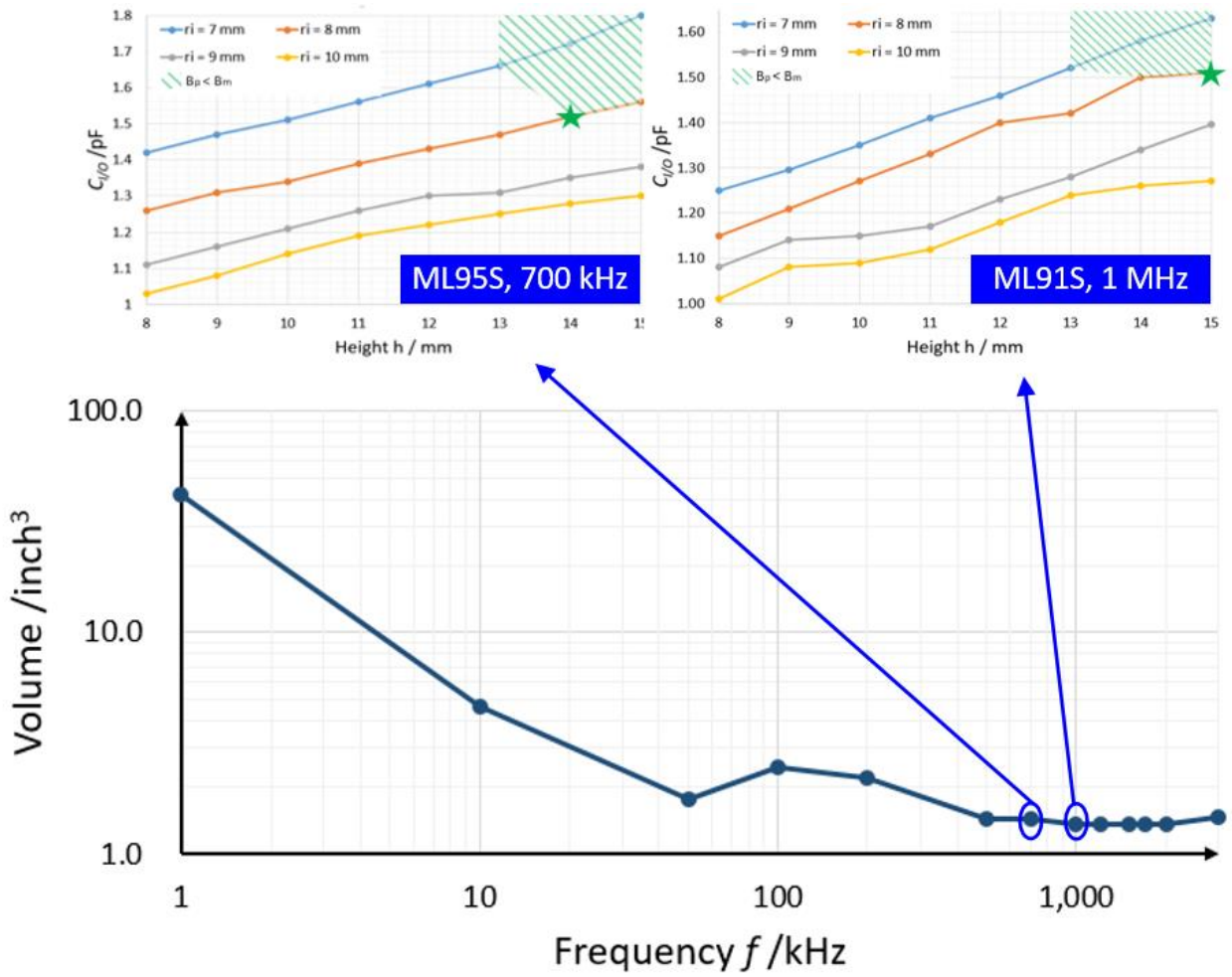


Fig. 26. Volume at different frequency

When the input current frequency goes high, the input-output capacitance $C_{I/O}$ and the volume stays low, however, it also has some problem. Core loss density P_v can be calculated based on the Steinmetz Equation shown in equation (45), where k_v, α and β are the constants given by the manufacturer, f and B_m are the frequency and flux density. The core loss can be given by (46), where A_c and l_c are the cross-section area and the effective length of the core.

$$P_v = k_v \cdot f^{\alpha} \cdot B_m^{\beta} \tag{45}$$

$$P_{core} = P_v \cdot A_c \cdot l_c$$

With the same constant k_v, α and β, the core loss density P_v increases a lot when the frequency increases. The core loss density P_v of ML91S from Hitachi at 1 MHz and 50 Mt. Flux

Fig. 27. Optimized transformer

TABLE 6. OPTIMIZED TRANSFORMER PROPERTIES

r_o(mm)	r_i (mm)	h (mm)	N_s	L_p (μH)	L_s (μH)	M (μH)
25	15	14	5	1.53	32.67	6.53

density is 100 kW/m^3 while at 2 MHz and 50 mT, and the core loss density P_v becomes 700 kW/m^3 [13]. The core loss of these two different frequencies will be 2.46 W and 17.22 W respectively with the same size of 1.5 inch^3. Therefore, the frequency should not be designed larger than 2 MHz.

Considering all factors, the ML91S from Hitachi at 1 MHz is selected. Based on the optimization method, the optimized transformer is shown in Fig. 27. Its dimensions and properties are summarized at TABLE 6.

2.5 Litz Wire Design

Litz wire is a common tool for the power electronics. It reduces the DC loss and the AC loss by reducing the DC resistor R_{dc} and the AC resistor R_{ac} of the wire. The method used for the litz

wire design is proposed in [14]. Compared with the approaches including Bessel functions [15]-[19], combinations of Bessel functions [20] or complex permeability models [21], [22], it only needs the skin depth at the frequency of operation and the number of turns.

The first step is to compute the skin depth, which is given as:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}} \tag{47}$$

Where ρ is the resistivity of the copper at room temperature, which is $2 \times 10^{-8}\,\Omega\cdot$m at 60°C. f is the frequency of a sinusoidal current in the winding. μ_0 is the permeability of free space, which is $4 \times 10^{-8}\,\pi$ H/m. This equation uses MKS units for all variables and the unit of calculated skin depth is meter. The frequency of the current is 1 MHz, therefore, the skin depth is 0.066 mm.

$$\delta = \sqrt{\frac{1.72\times10^{-8}}{\pi\cdot10^{6}\cdot4\times10^{-7}\pi}} = 6.6\times10^{-5} \tag{48}$$

The strand AWG size can be determined by the calculated skin depth. The diameter of the strand should be smaller than the skin depth to reduce the AC resistor. The parameters for the litz wire are shown in TABLE 7 and AWG 46 is selected.

TABLE 7. PARAMETERS FOR ECONOMICAL LITZ-WIRE DESIGNS

Strand AWG size	38	39	40	41	42	43	44	45	46	47	48
Strand diameter (mm)	.101	.090	.080	.071	.063	.056	.050	.045	.040	.035	.032

The strand number of the litz wire is determined by the current level. The RMS value of the secondary current I_s is 0.4 A, therefore, the strand number is designed as 140.

The DC resistor R_{dc} can be calculated as:

$$R_{dc} = \frac{\rho \cdot l}{S} \tag{49}$$

$$l = N_s \cdot 2(r_o - r_i + h) \tag{50}$$

$$S = \pi(\frac{d_s}{2})^2 \tag{51}$$

Where ρ is the resistivity of the copper at room temperature, which is 2×10^{-8} Ω·m at 60°C, l is the wire length of the secondary winding. S is the cross-section area of the single strand.

2.6 Transformer Loss Modeling

A 3D model of the transformer was built and imported to the FEA simulation. The AC loss can be given by the equation derived in [23]:

$$P_{ac} = \frac{\pi l d_s^4}{64\rho_c}\langle\overline{(\frac{dB}{dt})^2}\rangle \tag{52}$$

$$R_{ac} = \frac{P_{ac}}{I_{p\_rms}^2} \tag{53}$$

Where P_{ac} is the time average AC loss in winding, $\bar{x}$ represents time average, and $\langle x\rangle$ represents the spatial average over the region of the winding. R_{ac} is the AC resistor. The *dB/dt* can be given by FEA simulation.

The winding loss can be given by:

$$P_{winding} = P_{ac} + P_{dc} \tag{54}$$

$$P_{dc} = I_{p\_rms}^2 \cdot R_{dc} \tag{55}$$

Where P_{dc} is the dc loss in winding.

2.7 $C_{I/O}$ Measurement Result

The input-output capacitance $C_{I/O}$ of the transformer is 1.67 pF, which is shown in Fig. 28. It is measured by the Agilent 4294A Precision Impedance Analyzer.

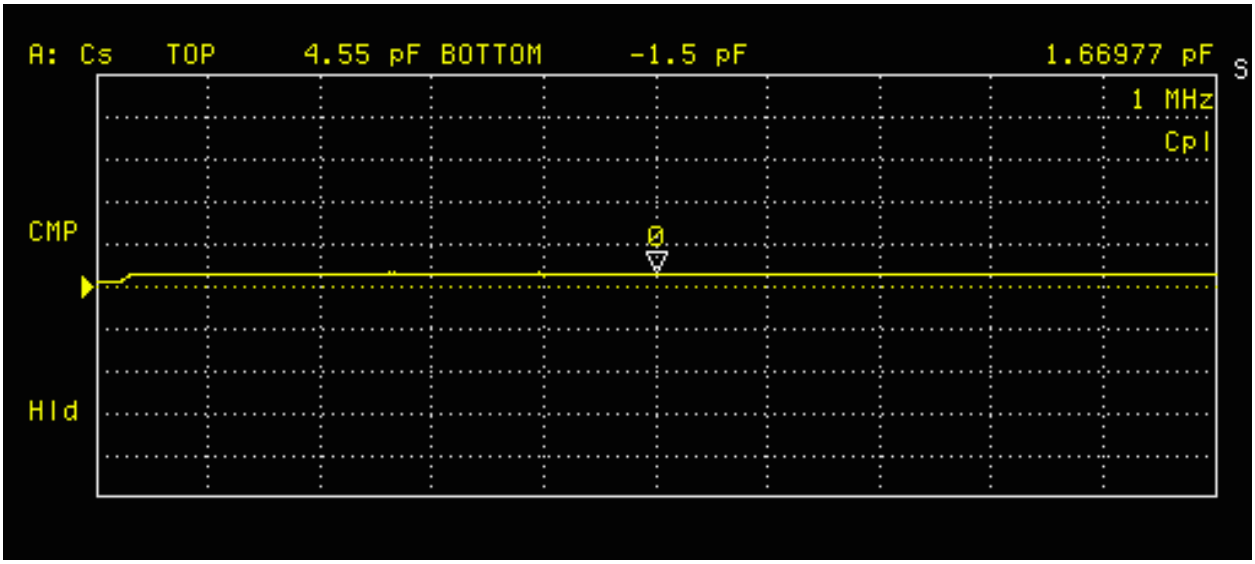


Fig. 28. Measurement of $C_{I/O}$

Compared with the value given by the model, which is 1.52 pF, the error is:

$$error = \frac{1.67\,pF - 1.52\,pF}{1.67\,pF}\% = 8.98\% \tag{56}$$

First, the Agilent 4294A Precision Impedance Analyzer creates error during the measurement. Second, the air space between the winding and the core is fixed. In real case, it might vary, which also leads to the error. The error between the model and measurement is 8.98 percent, which at less than 10 %, is acceptable.

2.8 Summary

Voltage-source transformer and current-source transformer structures are analyzed and compared in this chapter. Considering the high-voltage isolation design, low input-output coupling capacitance $C_{I/O}$ design, voltage regulation design and the resiliency to faults, a current-

source transformer is determined to be more competitive and is selected. The challenges of the current-source transformer design are also illustrated. Detailed derivation of the transformer peak flux density is given to provide the guideline for the current-source transformer design. The mathematical model of the transformer input-output coupling capacitance $C_{I/O}$ is built and used for the capacitance optimization. The optimal input-output coupling capacitance $C_{I/O}$ and its corresponding core volume under various frequency are shown to determine the optimal frequency. ML91S and 1 MHz are eventually selected. Litz wire is used for the transformer secondary winding reduce the loss. Strand AWG size is determined by the frequency and the strand number is decided by the current level. The transformer is shown and its input-output coupling capacitance $C_{I/O}$ is measured by the Agilent 4294A Precision Impedance Analyzer. The measured input-output coupling capacitance $C_{I/O}$ is 1.67 pF at 1 MHz. Compared with the model, which is 1.51 pF, the error is 8.98%. This error is given by the error in the model and the error caused by the Agilent 4294A Precision Impedance Analyzer. Since the error is smaller than 10%, it is acceptable.

Chapter 3: Topology Selection and Design

3.1 Introduction

It has been shown, through analysis in the previous chapter that the transformer requires a current-source input. There are several topology candidates. Conventionally, a single-phase inverter is used to generate the sinusoidal current source. The equivalent circuit of single-phase

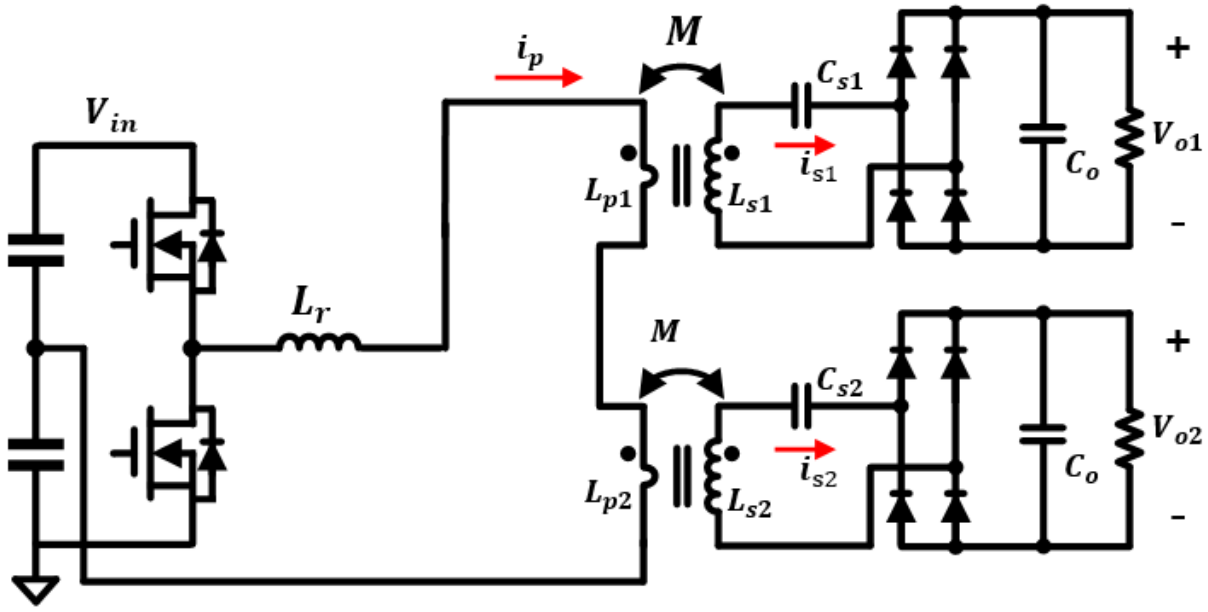


Fig. 29. Equivalent circuit of single-phase inverter for one module

inverter with two loads is shown in Fig. 29.

One advantage of this topology is that the structure of the inverter is simple, containing only a half-bridge and a phase inductor. However, it requires a bulky DC-link capacitor tank and a large phase inductor, which adds volume to the gate-drive power supply. In addition, the current source frequency is much lower than the primary-side switching frequency. According to the Fig. 25 and Fig. 26, when the frequency is below 50 kHz, both the transformer size and $C_{I/O}$ will increase rapidly. The large size is due to the big cross-section area of the magnetic core needed

to prevent saturation. A low frequency also results in a large secondary turn number of the secondary-side winding, both of which contrite to a high $C_{I/O}$. Consequently, a single-phase inverter is not a suitable topology candidate in this case. Therefore, another solution will be sought.

Resonant converters are another option to build a high frequency current source, but the high switching speed may lead to a high turn-off switching loss. Thus, apart from the current-source requirement, the resonant converters should be also able to achieve soft switching to reduce the turn-off switching loss.

3.2 Fundamental Concept of Resonant Converters

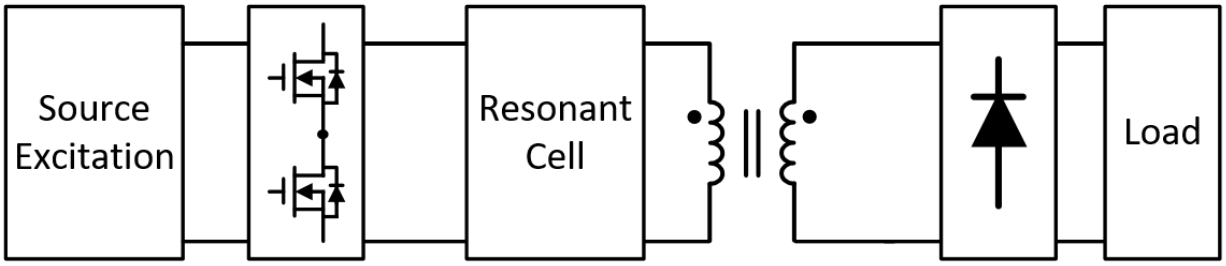


Fig. 30. Simplified general DC-DC resonant converter block diagram

Generally, DC-DC resonant converters can be presented in a simplified block diagram, which is shown in Fig. 30. The input source can be either voltage or current. Square waveforms can be given after the primary switches. The resonant cells are formed by the frequency selective network that transfers or blocks the energy from the source to load. The output circuit includes the rectifier circuit and the load consists of a load resistor either in series with an inductor or in parallel with a capacitor.

3.3 Topology Selection

Basic resonant cells start from two-element resonant tanks. For two energy storage elements, there are eight different resonant configuration types, which is shown in Fig. 31. Tank A, B, C and D are suitable for voltage excitation while tank E, F, G and H are suitable for current excitation. As the isolated gate driver power supply proposed in this thesis has a voltage excitation after switches, the number of resonant tank candidates reduces to four, which are tank A, B, C and D.

Among these four resonant tank candidates, tank B and tank C can provide current-source input for the transformer. To examine in further detail, an equivalent circuit in one load condition is provided and analyzed as follows.

As illustrated in Fig. 15, a compensation capacitance has been added in series with the secondary self-inductance L_s. Their equivalent impedance Z_s equals to zero when C_s is in resonant with L_s. After applying the resonant tank B and tank C to the primary circuit, their equivalent circuit are shown in Fig. 32 and Fig. 33 respectively. L_{r_B} and C_{r_B}, L_{r_C} and C_{r_C} form

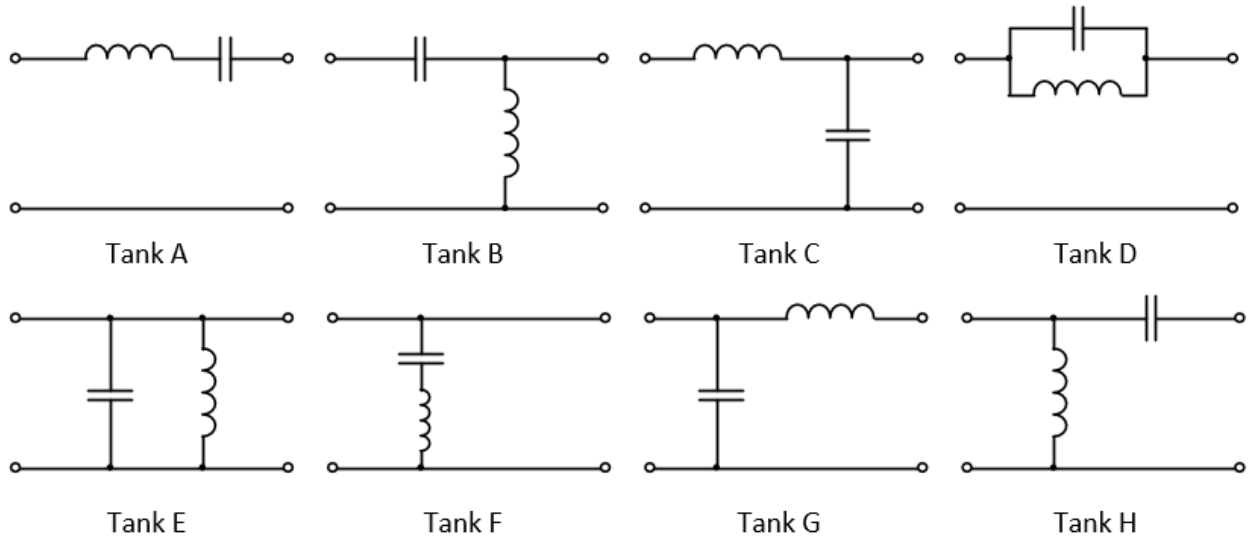


Fig. 31. Two-element resonant tanks

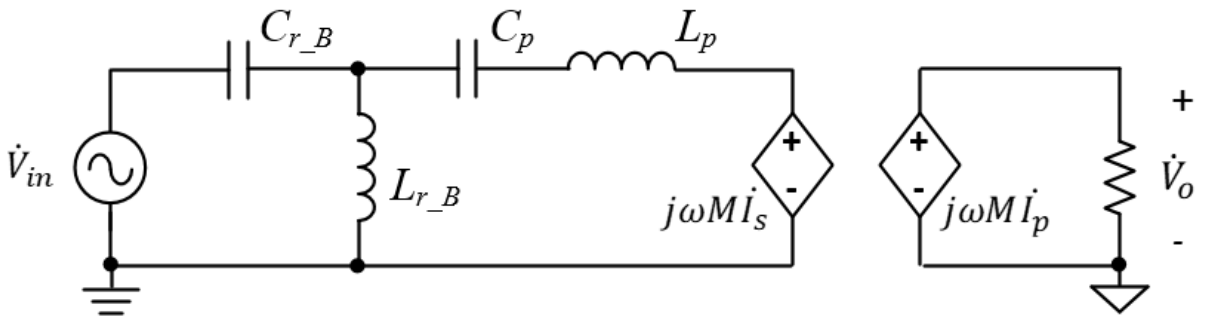


Fig. 32. Equivalent circuit with tank B

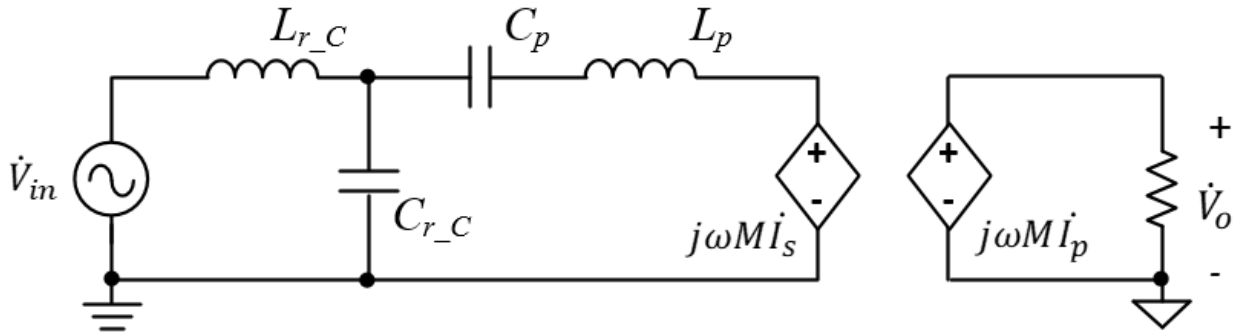


Fig. 33. Equivalent circuit with tank C

the resonant tank and blocking capacitance C_p is needed.

By Norton's theorem, both Fig. 32 and Fig. 33 can be further simplified as Fig. 34, where:

$$\vec{I}_{in} = \frac{\vec{V}_{in}}{j\omega L_{r\_C}} \tag{57}$$

As L_{r_C} and C_{r_C} are in parallel resonance, their equivalent impedance can be seen as infinitely large, so they can be removed from the path. I_{in} can be treated as a current source and becomes the transformer input current I_p.

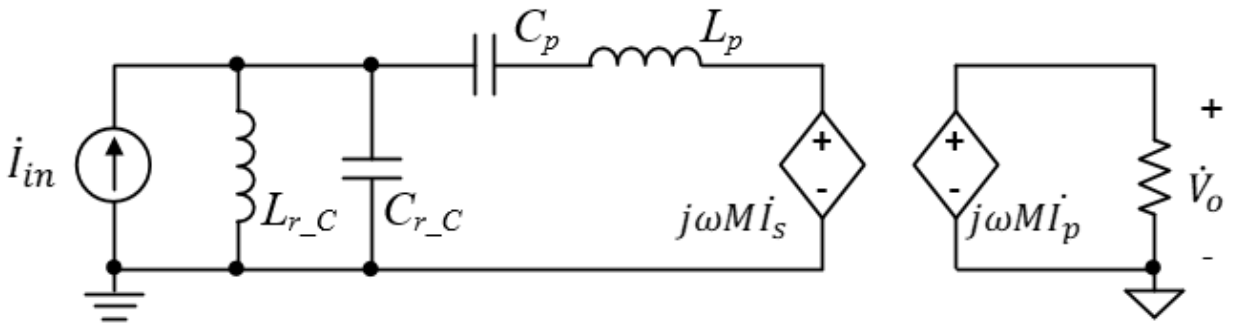


Fig. 34. Equivalent circuit after Norton's theorem.

$$L_{r\_C} \cdot C_{r\_C} = \frac{1}{\omega^2} \tag{58}$$

$$Z_r = j\omega L_{r\_C} \| \frac{1}{j\omega C_{r\_C}} \to \infty \tag{59}$$

$$\vec{I}_p = \frac{\dot{V}_{in}}{j\omega L_{r\_C}} \tag{60}$$

Then, the circuit show in Fig. 15 in Chapter 2 can be given. Combining equation (14) and (60), the value of L_{r_C} can be designed by (61) and (64). Therefore, with given transformer properties, all the components in the circuit can be derived.

$$L_{r\_C} = \frac{\dot{V}_{in}}{\dot{V}_o \cdot M} \tag{61}$$

$$C_{r\_C} = \frac{1}{\omega^2 \cdot L_{r\_C}} \tag{62}$$

In order to determine which resonant tank has a better performance with the same transformer properties and specifications, simulation circuits are built in SIMPLIS, which are shown in Fig. 35 and Fig. 36.

Fig. 37 and Fig. 38 are the simulation results for tank B and tank C. It can be seen that for the same output voltage, which is 28.1 V, the peak value of the current though resonant tank i_{Cr}

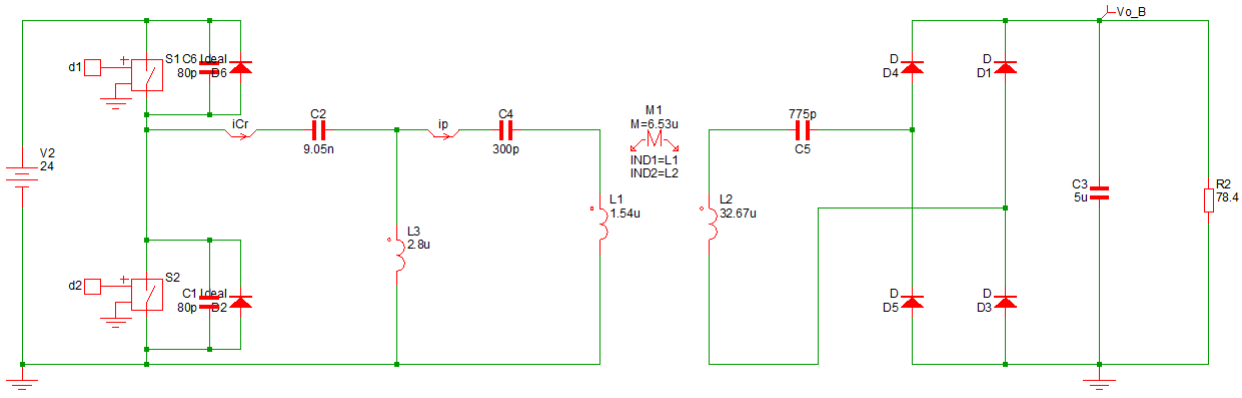


Fig. 35. Simulation circuit of tank B

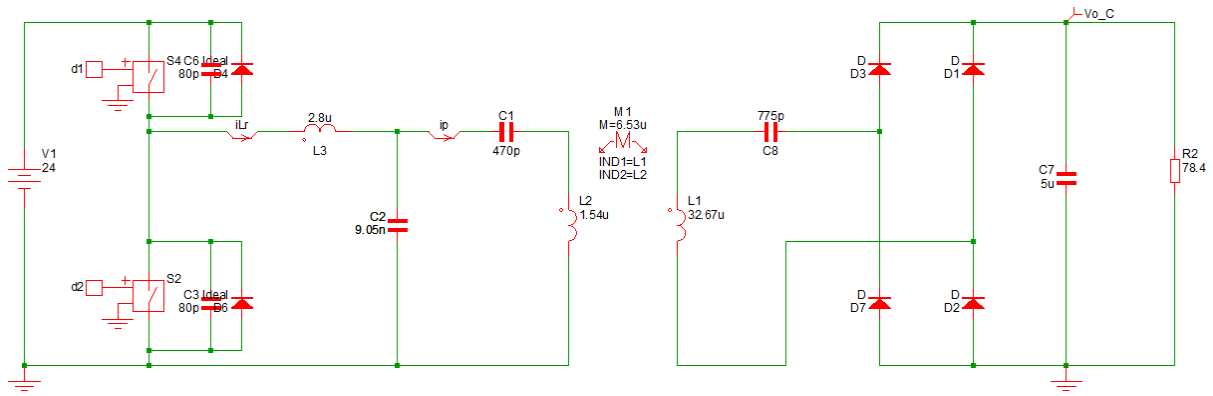


Fig. 36. Simulation circuit of tank C

(shown in Fig. 37) is 25.6 A whereas that of i_{Lr} shown in Fig. 38 is 17.3 A.

With a smaller current, tank C configuration is less stressful for the switches and passive components. A smaller drain-source current leads to a less conduction loss, which is explained by the equation (65).

$$P_{con} = I_{ds}{}^2 \cdot R_{ds\_on} \tag{63}$$

Where I_{ds} is the drain-source current, and R_{ds_on} is the on-state resistor of the power devices.

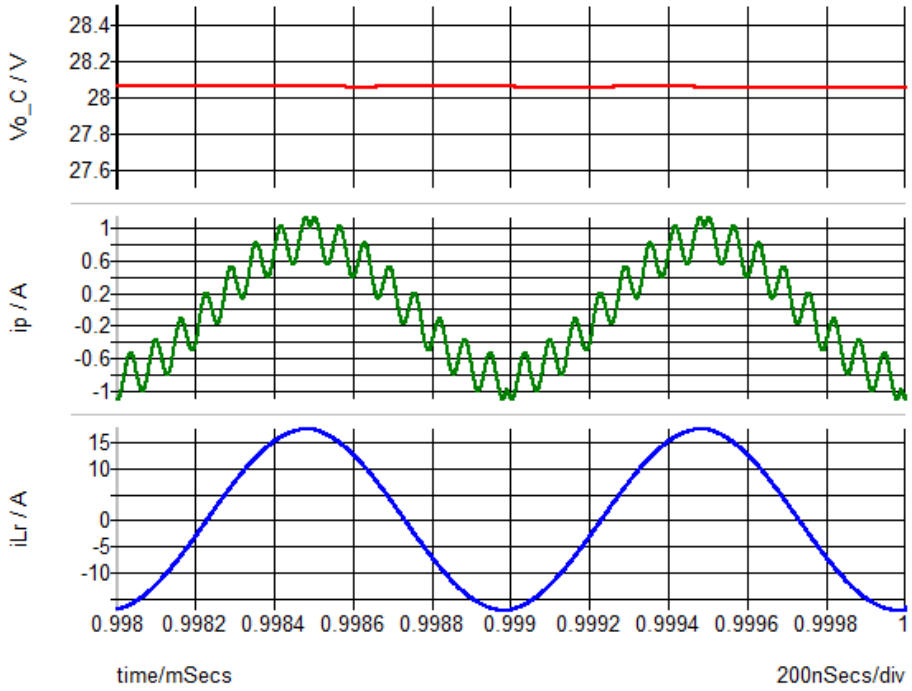


Fig. 37. Simulation result of tank B

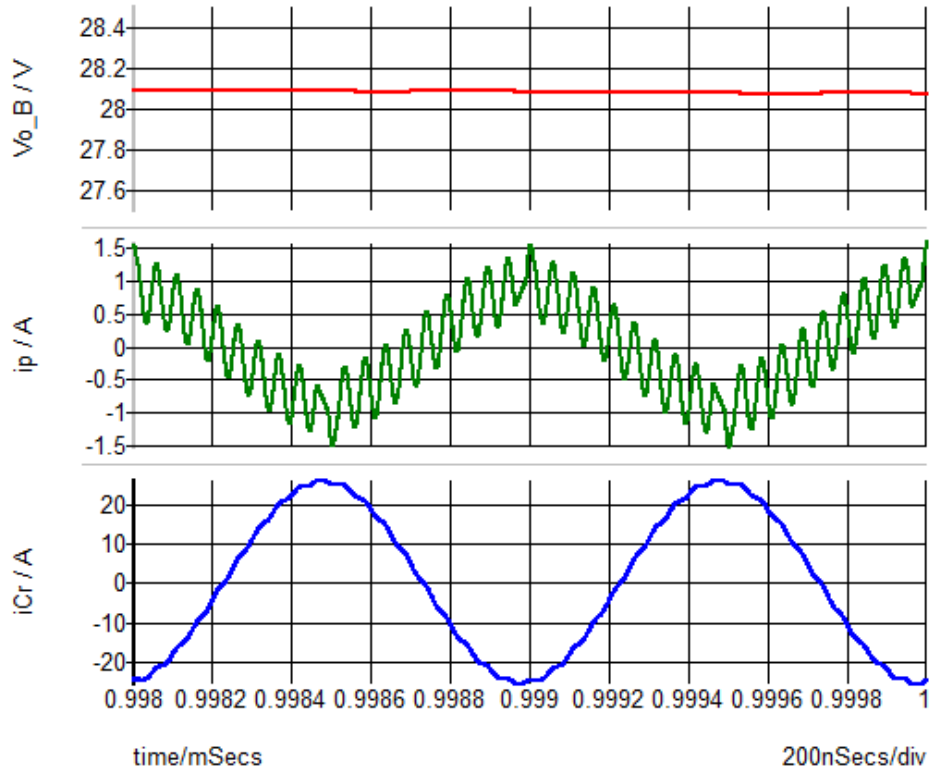


Fig. 38. Simulation result of tank C

Additionally, the transformer input current i_p of tank B configuration contains more high order harmonic components. The equivalent impedances of L_r, C_r and L_s, C_s are no longer infinitely large and zero under frequencies that are unequal to ω. Conclusively, more harmonic components, and weaker voltage regulation are present.

These high order harmonic components can only be reduced, not removed completely. The specifications determine the properties of the transformer. Once the properties of the transformer are decided, the resonant tank values are decided. The quality factor Q under these specifications is large, worsening the performance of the resonant tanks.

In summary, tank C is more competitive and therefore selected to build the primary resonant circuit. The completed circuit, which is called LCCL-LC, is shown in Fig. 39. A resonant current bus (RCB) (shown in Fig. 40) is built by L_r and C_r to provide power to the load.

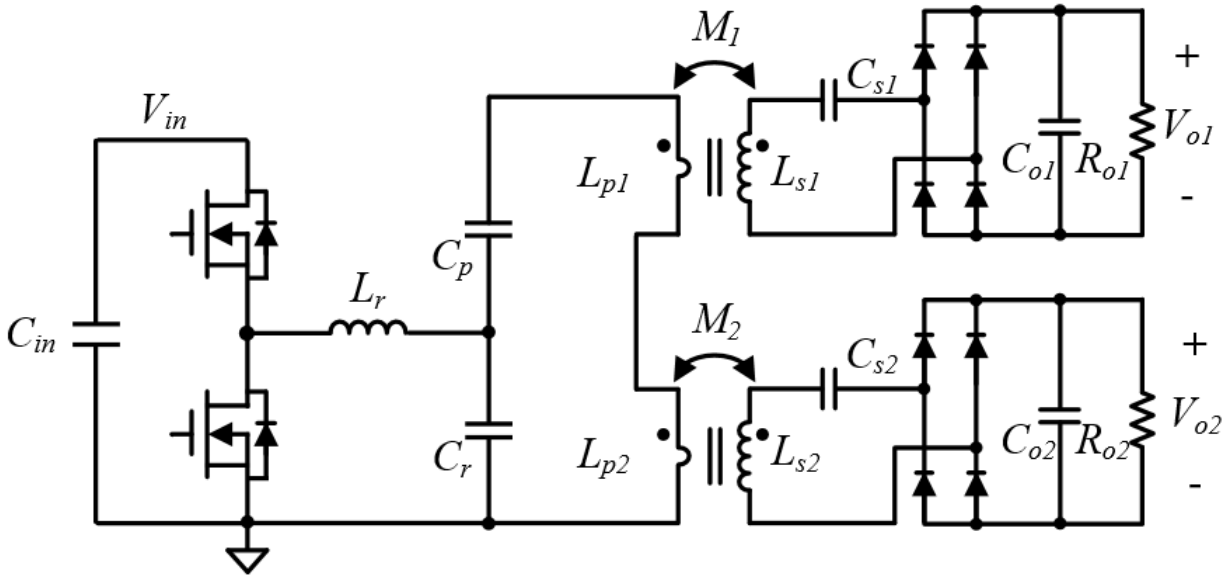


Fig. 39. LCCL-LC resonant converter

3.4 Overview of LCCL-LC Resonant Converter

This section offers an overview analysis for the LCCl-LC resonant converter. Fig. 40 shows a half-bridge LCCL-LC resonant converter with a full-bridge rectifier. The switching bridge generates a square waveform to excite the LC parallel resonant tank, which helps to build the RCB. A blocking capacitor C_p is needed to block the DC bias as well as to adjust the impedance. After the isolated transformer, a LC series resonant tank compensates the voltage drop on

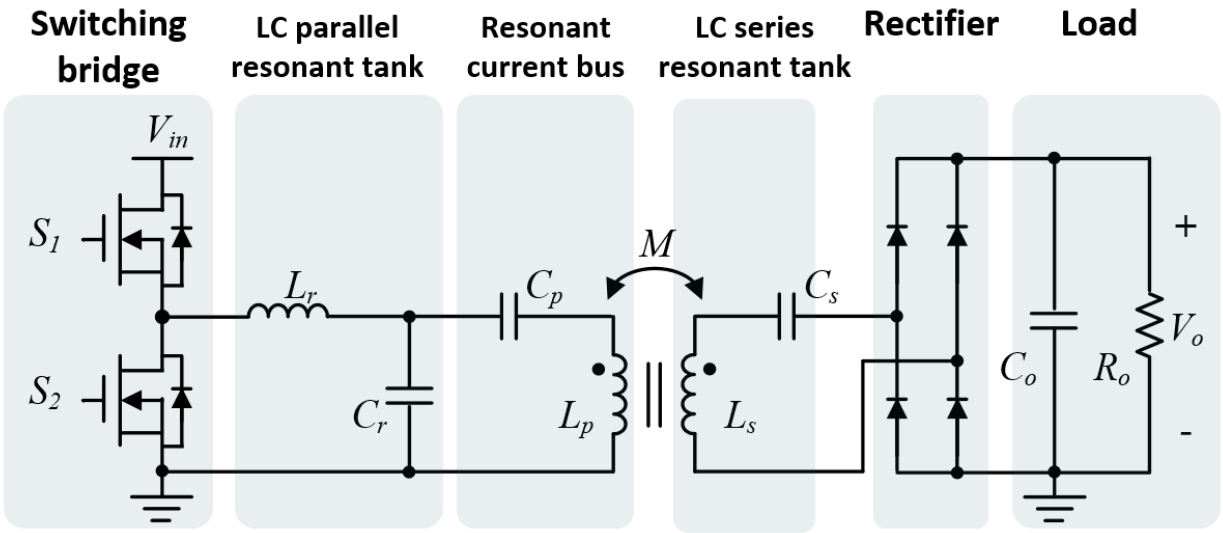


Fig. 40. LCCL-LC resonant converter in one load condition

secondary self-inductance L_s to maximize the transmitted power. The output capacitor filters the rectified ac current and outputs a DC voltage.

3.4.1. Converter voltage gain

Voltage gain curve is a very useful and common tool that helps to analyze and design the resonant converter. The gain curve of a LCCL-LC resonant converter in different load condition has been shown in Fig. 41, where Q is the equality factor, R_{ac} is the reflected load resistance, n is the transformer ration, F_x is the normalized switching frequency, f_s is the switching frequency and f_r is the resonant frequency.

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}} \tag{64}$$

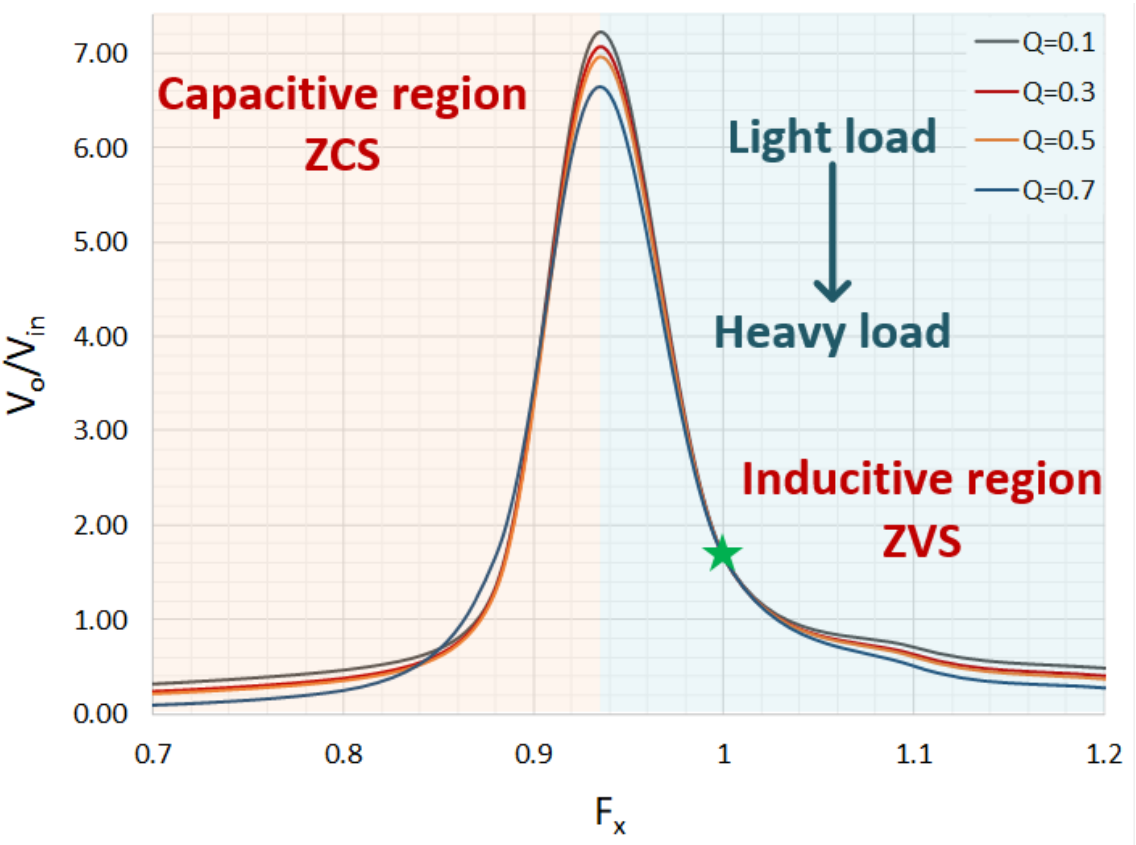


Fig. 41. Gain curves of LCCL-LC resonant converter in different load condition

$$R_{ac} = \frac{8}{\pi^2} \cdot \frac{1}{n^2} \cdot R_o \tag{65}$$

$$n = \frac{L_s}{M} \tag{66}$$

$$F_x = \frac{f_s}{f_r} \tag{67}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \tag{68}$$

It can be seen in Fig. 41 that low Q also means light load operation whereas higher Q curves represent heavier loads.

The gain peaks represent the boundary between the inductive region and capacitive region. The capacitive region can be also defined as the Zero-Current-Switching (ZCS) region, where the resonant tank is in a capacitive operation. During this region, the current leads the voltage. Before the switches turn off, the current through the switches will reverse its direction. After the switch is turned off, this current will flow in the switch's body diode, resulting in hard commutation in body diode once the other switch in the bridge is turned on. It will cause reverse recovery losses and noise. Additionally, it might also case high current spikes and device failure.

On the other hand, in the inductive region, which is also called Zero-Voltage-Switching (ZVS), the resonant tank presents inductive characteristics. In this region, the voltage leads the current. During the dead-time period, the device drain-source voltage (V_{ds}) drops to zero before the gate signal (V_g) arrives, which helps to reduce the switching loss. Based on the analysis above, it is desired to work in the inductive region across the entire input voltage and load current range.

It is also seen that all Q curves cross at the resonant frequency point at $F_x = 1$, that is, all load conditions will have a unity gain when $f_s = f_r$ (the green star in Fig. 41). When the input

voltage V_{in} is fixed, the output voltage V_o can remain constant even when the load changes. This happens because the load can be removed from the path only when $f_s = f_r$, where the equivalent impedance of L_r, C_r and Ls, C_s are infinitely large and zero. In terms of the voltage regulation design, the switching frequency f_s should be designed to be equal to f_r = 1 MHz, which has been analyzed in the last chapter.

3.5 Operation Mode

The steady state of the LCCL-LC resonant converter contains six operation modes in one switching period T_s, shown in Fig. 42. The detailed operations are described as follows.

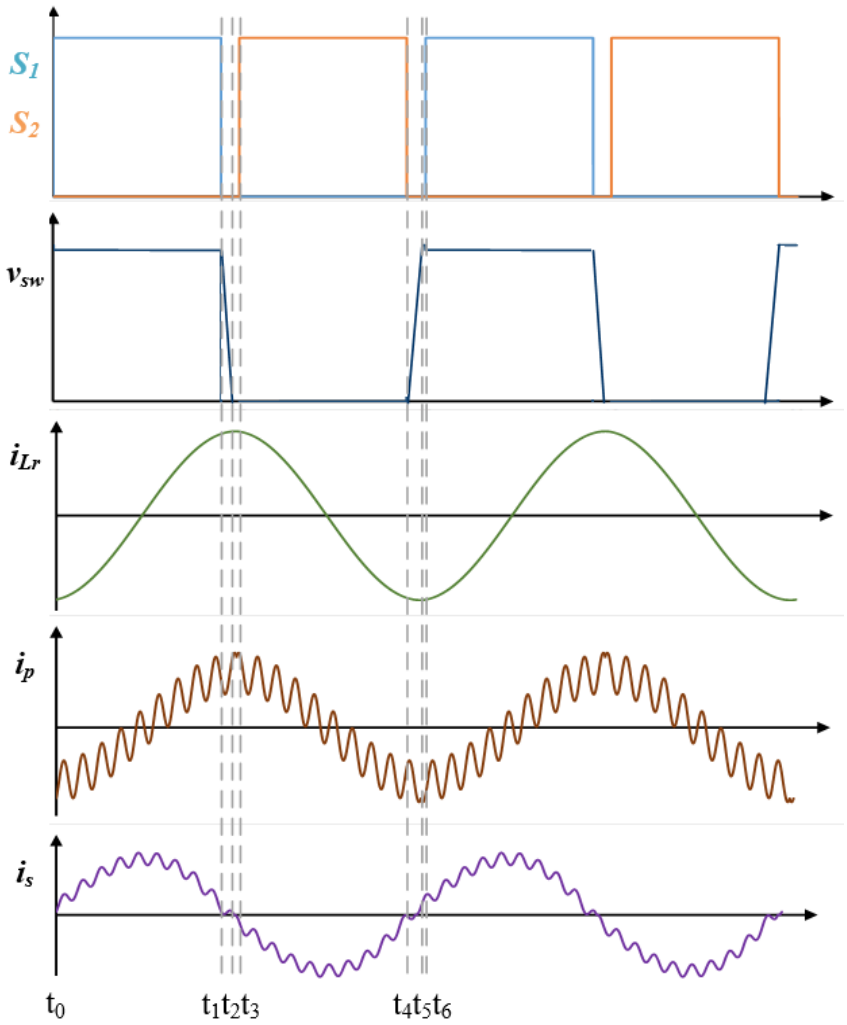
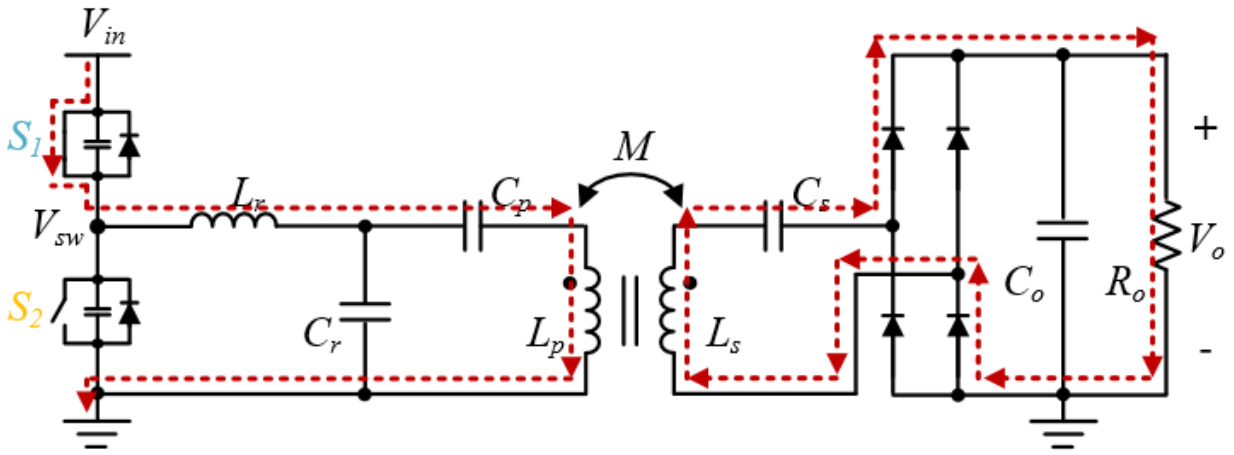


Fig. 42. Main waveforms in steady-state operation

1) Mode 1(Inductance Charging, $t_0 < t < t_1$)

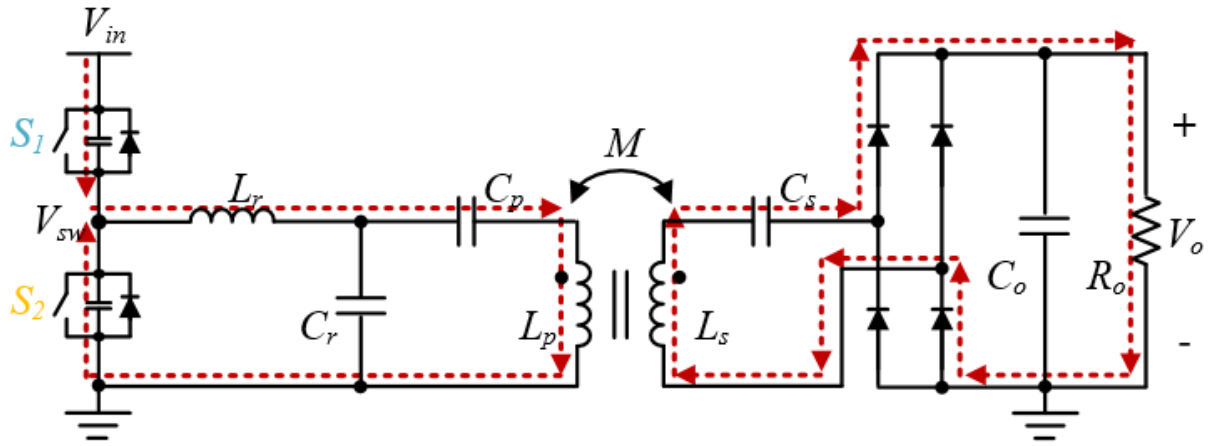
At t_0, the half-bridge high-side (HS) switch is turned on. During this mode, the input of the resonant tank is connected to the DC input. The resonant tank outputs a current-source to the transformer, which outputs a positive current to the rectifier.



Mode 1: $t_0 < t < t_1$

2) Mode 2(Dead-time, $t_1 < t < t_2$)

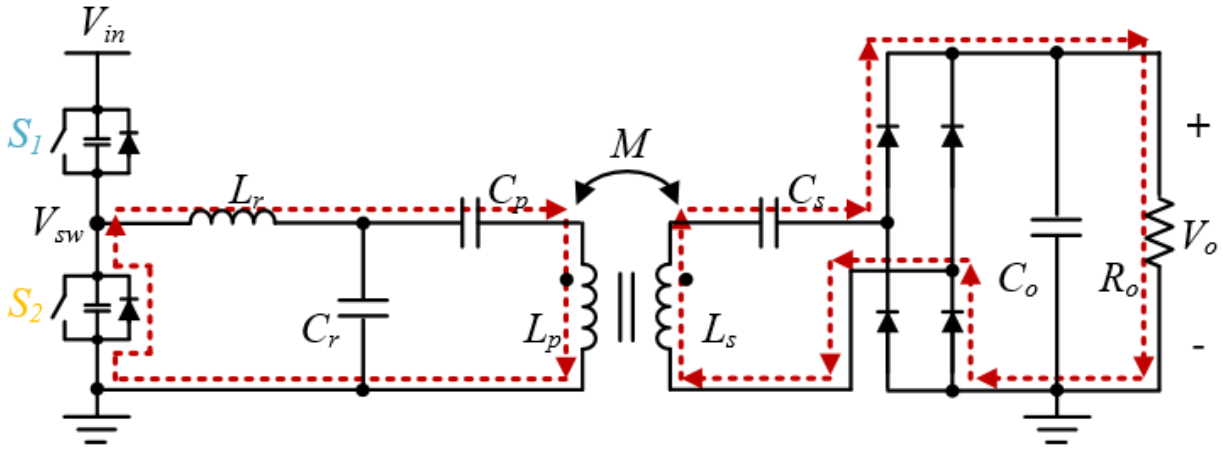
At t_1, the HS switch is turned off. The output capacitors of the HS-switch C_{oss_H} start to be charged while that of the low-side (LS) switch C_{oss_L} is discharged for part of the dead-time duration. This mode ends when the capacitances are fully charged or discharged.



Mode 2: $t_1 < t < t_2$

3) Mode 3(Dead-time, $t_2 < t < t_3$)

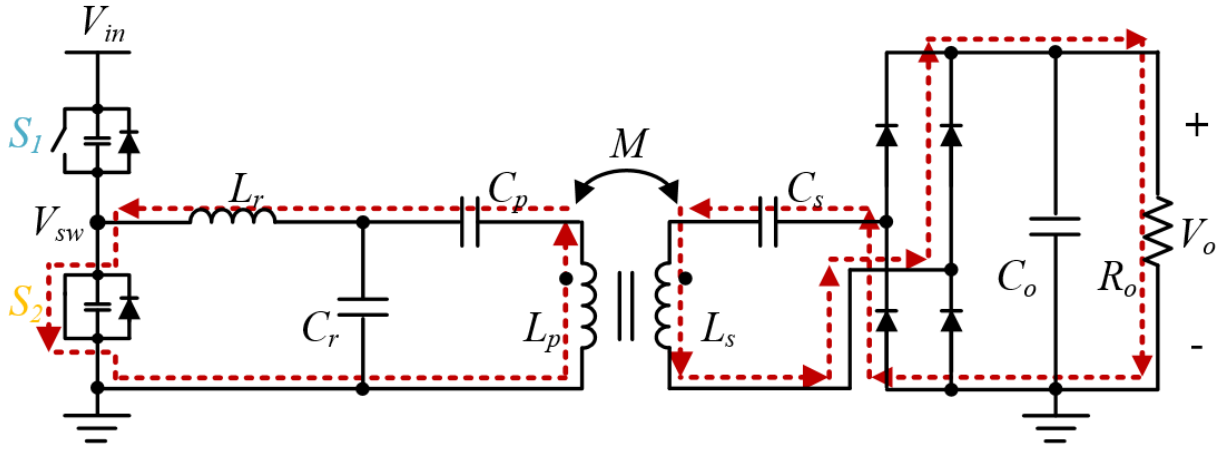
As the C_{oss_H} and C_{oss_L} are fully charged and discharged, the drain-source voltage of the LS-switch as well as the switching node voltage V_{sw} drops to zero and the body diode of the LS-switch starts to conduct. ZVS is realized due to the body diode conduction.



Mode 3: $t_2 < t < t_3$

4) Mode 4(Inductance Discharging, $t_3 < t < t_4$)

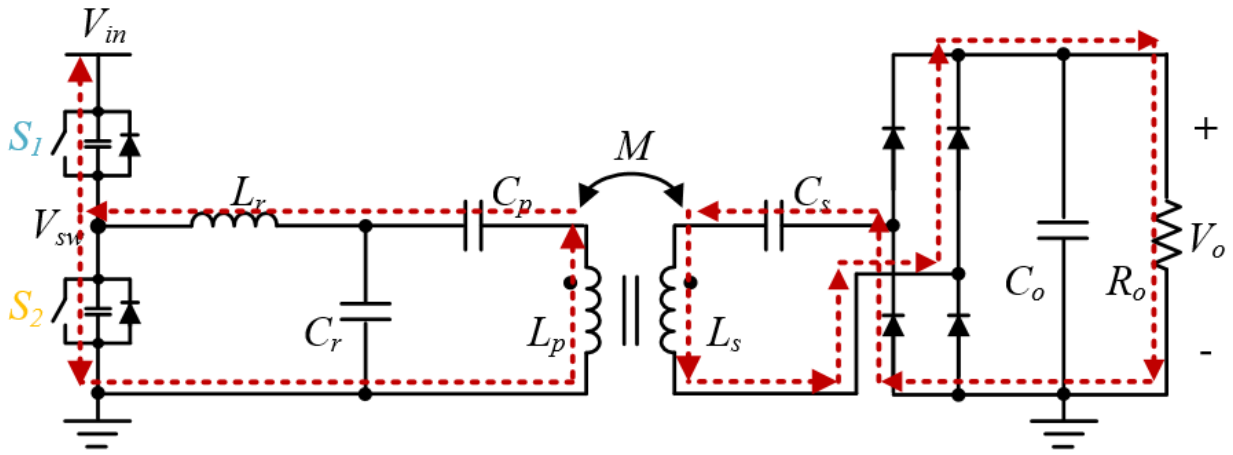
At t_3, the HS switch is soft-turned on and the resonant tank provides a current-source input to transformer. The direction of secondary-side output current is reversed.



Mode 4: $t_3 < t < t_4$

5) *Mode 5(Dead-time, $t_4 < t < t_5$)*

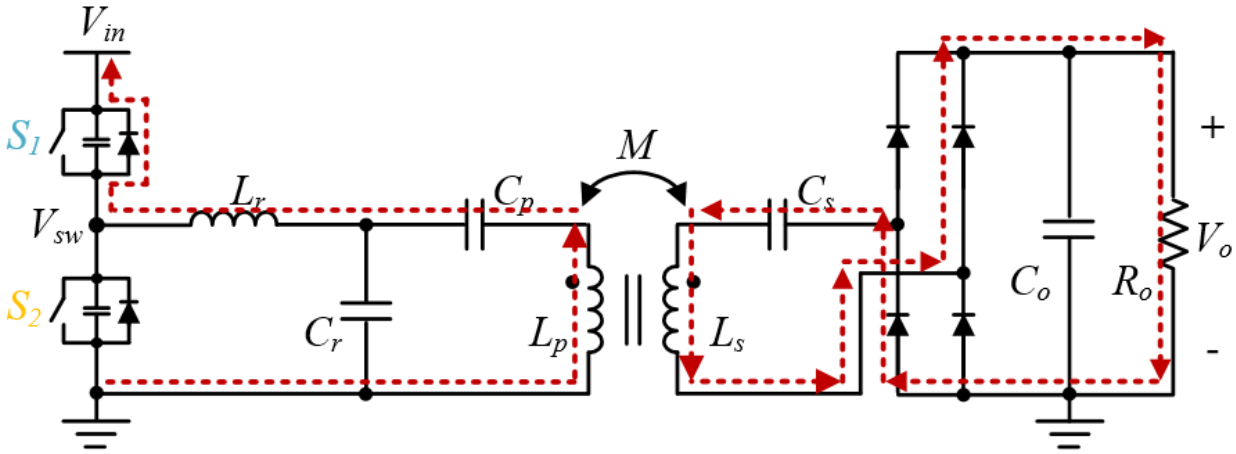
Similar to *mode 2*, the output capacitor C_{oss} of HS-switch and LS-switch start to discharged and charges. The process ends when they are fully charged or discharged.



Mode 5: $t_4 < t < t_5$

6) *Mode 6(Dead-time, $t_5 < t < t_6$)*

During this mode, the switching node voltage V_{sw} reaches DC input voltage V_{in}, the body diode of the HS-switch starts to conduct. ZVS is realized due to the body diode conduction.



Mode 6: $t_5 < t < t_6$

3.6 Design Steps

Fig. 43 shows the design flow chart of the LCCL-LC resonant converter design.

The first step is to design and optimize the primary-side single-turn transformer using the approach in Chapter 2. After the making sure that the peak flux density B_p is not too much to

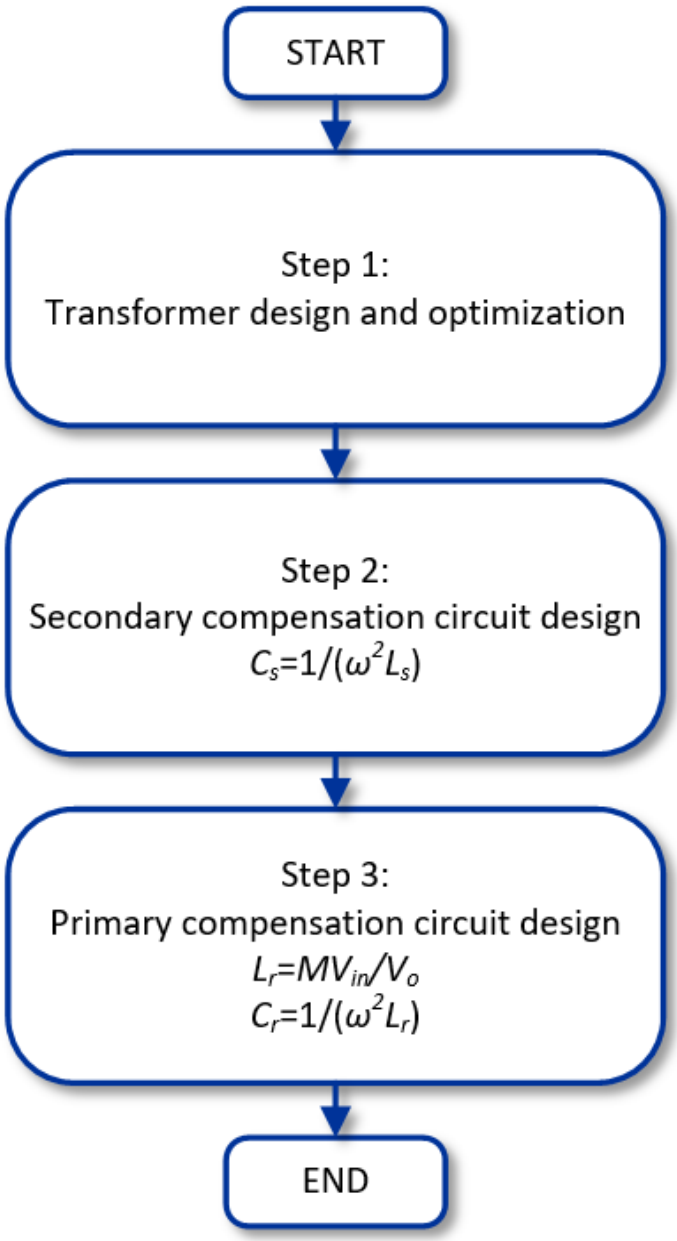


Fig. 43. Design flow chart

cause high loss and transformer saturation, the transformer properties including primary-side self-inductance L_p, secondary-side self-inductance L_s and mutual inductance M can be given.

The next step is to design the secondary compensation capacitance C_s. It should be designed to be in resonance with the secondary-side self-inductance L_s to compensate for the voltage drop of L_s, by which the transmitted power can be maximized.

Step 3 is to design the primary resonant tank to build the resonant current bus RCB for the transformer input. Their values can be designed by the transformer mutual inductance M and the specifications of the gate-drive power supply.

3.7 Summary

In this chapter, several topology candidates are introduced and analyzed. LCCL-LC resonant converter is selected due to its less stressful current and voltage for the switches and due to the fewer high order harmonic components involved. The gain curve is shown and helps in analyzation. Detailed operation modes of the LCCL-LC resonant converter are shown. The design flow chart is given to provide the guideline of the LCCL-LC resonant converter.

Chapter 4: Selection of Power Semiconductors

4.1 Introduction

Power semiconductor devices play a significant role in power electronic converters. Currently, most of the power devices are based on the very mature and well-established Si technology. This technology encompasses a large market of applications, from 20 V up to several kV. However, Si-based power devices show some limitations of high switching frequency and thermal capability which reduces the efficiency of the power converters.

A new generation of wide bandgap (WBG) semiconductor materials are expected to

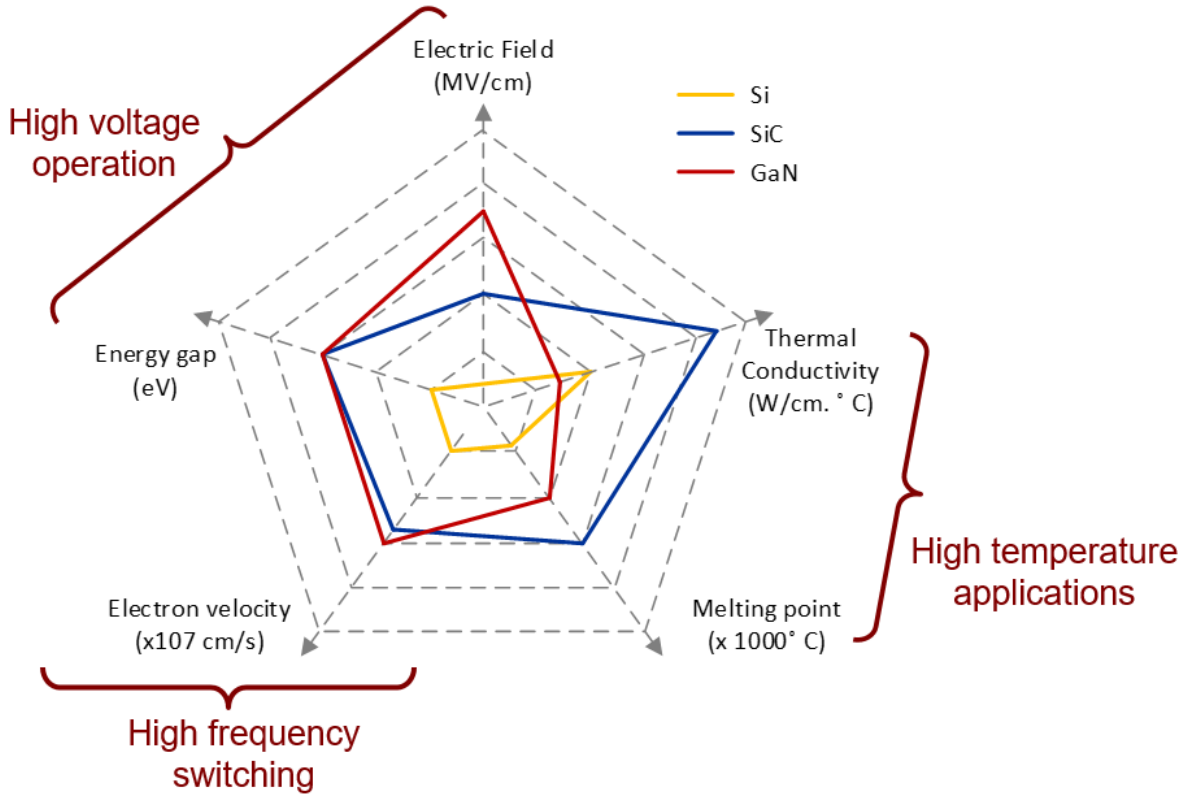


Fig. 44. Summary of Si, SiC, and GaN relevant material properties [24]

revolutionize the performance of power converters. SiC and Gallium Nitride enhancement-mode high electron mobility transistors (GaN EHEMTs) are the most advanced WBG semiconductor materials available for power devices. Fig. 44 shows the key characteristics of WBG semiconductors candidates to replace Si [24]. According to the chart in Fig. 44, it is shwon that GaN devices offer a better high frequency performance whereas SiC devices are more competitive at high temperature applications.

The gate-drive power supply proposed in this thesis works at a high frequency and low voltage condition; therefore, GaN devices are considered power device candidates.

4.2 Active Components Comparison and Selection

In the last decade, as production volume increased and the cost dropped, the industrial interest for GaN devices increased significantly. GaN devices are now used in many power electronic applications, such as wireless chargers, travel adapters, smart home applications, high efficiency power supplies, industrial motor drives, distributed energy generation and storage systems, aerospace applications, automotive traction inverters, on-board EV battery chargers, etc., [24]–[33].

The selection of power device candidates should leave enough margin for both voltage rating and current rating. As the input voltage is 24 V and the RMS value of the input current is approximately 1 A by simulation, the voltage rating and the current rating should be at least 50 V and 10 A. TABLE 8 shows the device candidates and their maximal drain-source voltage V_{ds_max} and the maximum continuous drain-source current I_{ds}.

TABLE 8. POWER DEVICE CANDIDATES

Manufacturer	Configuration	Part #	V_{ds_max}	I_{ds}
EPC	Half-bridge	EPC 2102	60 V	30 A
EPC	Half-bridge	EPC 2103	80 V	6.8 A
EPC	Single	EPC 2016C	100 V	18 A
EPC	Single	EPC 2045	100 V	16 A
EPC	Half-bridge	EPC 2104	100 V	30 A

In order to compare their performance with the same specifications, a simulation circuit with a switch SPICE model has been built in LTSPICE, and is shown in Fig. 45.

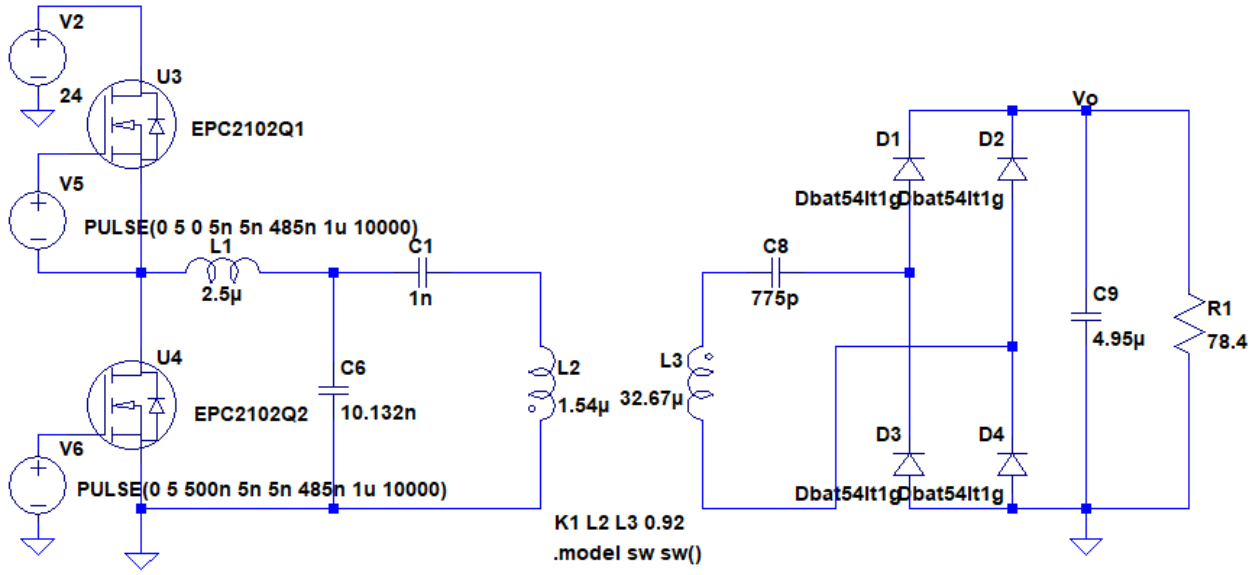


Fig. 45. Simulation circuit with SPICE model

The conduction loss P_{con} can be calculated by the device RMS drain-source current I_{ds_rms}:

$$P_{con} = I_{ds\_rms}^{2} \cdot R_{ds\_on} \tag{69}$$

The total loss P_{total} can be given by the simulation, then the switching loss P_{sw} can be estimated by the following equation:

$$P_{sw} = P_{total} - P_{con} \tag{70}$$

The loss information for power device candidates is summarized in TABLE 9. It is clearly evident that the GaN power transistor half-bridges EPC 2102, EPC 2103, and EPC 2104 have a

superior performance compared to the single GaN power transistors, including EPC 2016C and EPC 2045.

Additionally, the assembly half-bridge configuration minimizes the power loop due to their compact design, which significantly reduces the parasitic inductance. Conclusively, the half-bridge configuration is more competitive. According to TABLE 9, EPC 2102, EPC 2103, and EPC 2104 have a similar performance. EPC 2102 is selected due to its small on-state resistor R_{ds_on} and output capacitor C_{oss}.

TABLE 9. POWER DEVICE LOSS BREAKDOWN

Part #	HS-switch		LS-switch		Conduction loss P_{con}	Switching loss P_{sw}	Total loss P_{total}
	R_{ds_on}	C_{oss}	R_{ds_on}	C_{oss}			
EPC 2102	4.9 mΩ	0.51 nF	4.9 mΩ	0.71 nF	129 mW	47 mW	176 mW
EPC 2103	5.5 mΩ	0.46 nF	5.5 mΩ	0.63 nF	145 mW	28 mW	173 mW
EPC 2016C	16 mΩ	0.31 nF	16 mΩ	0.31 nF	421 mW	37 mW	458 mW
EPC 2045	7 mΩ	0.39 nF	7 mΩ	0.39 nF	184 mW	124 mW	308 mW
EPC 2104	6.8 mΩ	0.45 nF	6.8 mΩ	0.6 nF	179 mW	20 mW	199 mW

Furthermore, Schottky diodes SS25FACT are applied as the full-bridge rectifier.

The gate driver candidates, LM 5113, UCC27212 from Texas Instruments, and IR2110 from Infineon Technologies, for the GaN transistor half-bridge are summarized in TABLE 10. The highly integrated chip LM 5113 from Texas Instruments is selected as the gate driver for the half-bridge transistor due to its small rising and falling time and 107 V high-side voltage.

TABLE 10. GATE DRIVER CANDIDATES

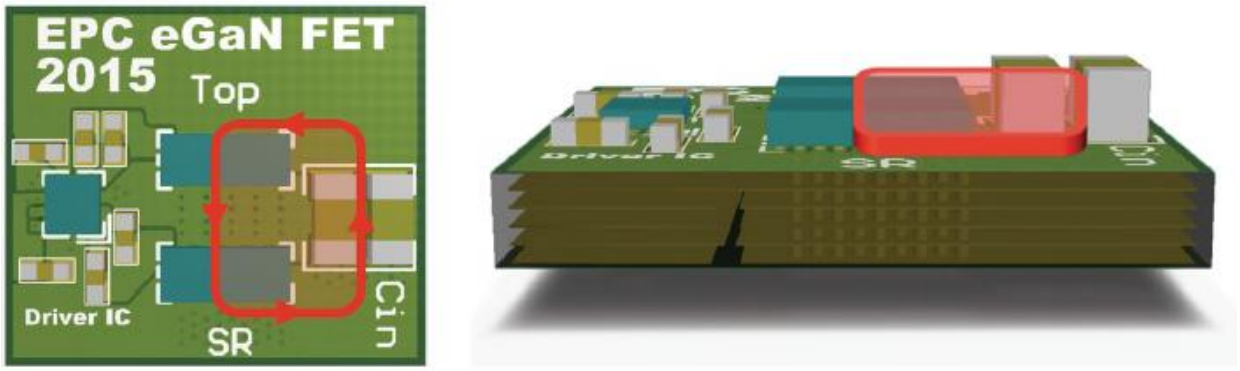
Manufacturer	Driven Configuration	Part #	High-side voltage	Rise / fall time
Texas Instruments	Half-bridge	LM 5113	107 V	7 ns, 1.5 ns
Texas Instruments	Half-bridge	UCC27212	100 V	7.8 ns, 6 ns
Infineon Technologies	Half-bridge	IR2110	500 V	25 ns, 17 ns

4.3 PCB layout design

The PCB layout design is critical for minimizing the parasitic inductance of the converter. A large parasitic inductance has a negative effect on converter performance, such as slowing the power devices driving speed, increasing the switching commutation time, causing a high peak drain to source voltage spike, and increasing the power loss [34].

Reusch introduces two conventional PCB layouts for eGaN FETS, the lateral power loop and the vertical power loop, and proposes an optimal power loop as well [35].

The conventional lateral power loop design is shown in Fig. 46. In this design, the power devices and the input capacitors are located on the same side of the PCB. The power flows on the board plane on a single layer, which is shown as the red loop in Fig. 46. The distance between the power loop and the shield layer must be minimized to reduce loop inductance.



(a) (b)

Fig. 46. Conventional lateral power loop (a) top view, and (b) side view. [35]

The second conventional PCB layout design involves placing the power devices and the input capacitors on opposite sides of the PCB. The input capacitors are generally located directly underneath the power devices to minimize the physical loop size, as shown in Fig. 47. In this vertical power loop design, the loop inductance is highly dependent on the board thickness; therefore, the board thickness must be minimized to reduce loop inductance.

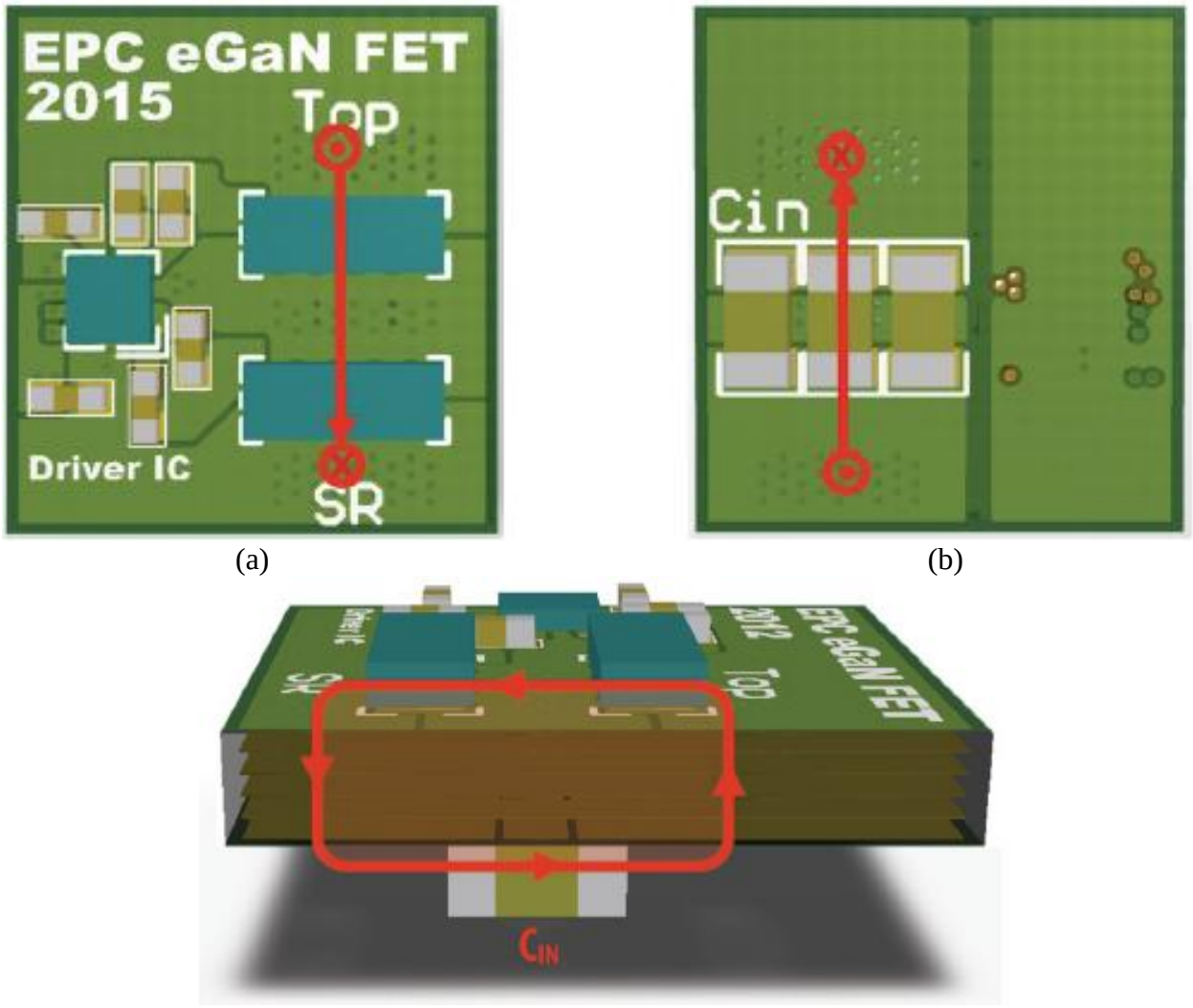
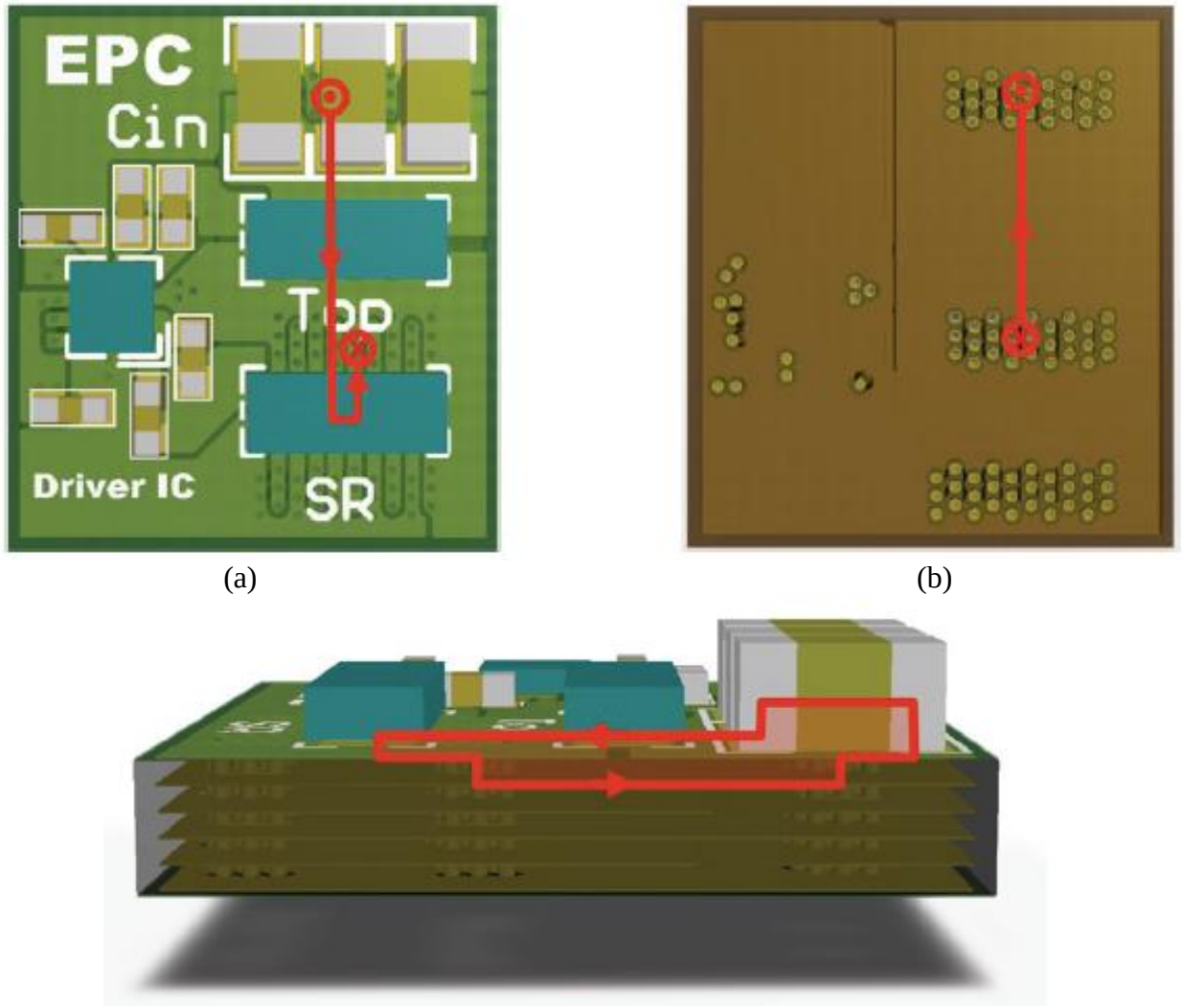


Fig. 47. Conventional vertical power loop (a) top view, (b) bottom view, and (c) side view. [35]

The optimal power loop design for the PCB layout is shown in Fig. 48. The input capacitors are placed close to the top device, and the input voltage terminal is located next to the drain connections of the top device. A series of interleaved switching nodes and ground vias are placed between the two devices. These interleaved vias provide a reduced length high frequency loop inductance path, resulting in a reduction of loop inductance. Additionally, the interleaving of the via sets with current flowing in opposing directions helps to reduce eddy and proximity effects, which leads to reductions in AC conduction losses.



(a) (b)

(c)

Fig. 48. Optimal power loop (a) top view, (b) top view of inner layer 1, and (c) side view. [35]

Therefore, the optimal power loop design proposed in that work [35] is used in the PCB layout design of an isolated gate-drive power supply. The 3D view of the EPC 2102, input capacitors and the gate driver LM5113 of the isolated gate-drive power supply primary converter are shown in Fig. 49. The red loop is the power loop. The power flows in the top layer and goes into the GND layer through vias. The gate driver LM 5113 is placed as close as possible to the switches to reduce the signal loop.

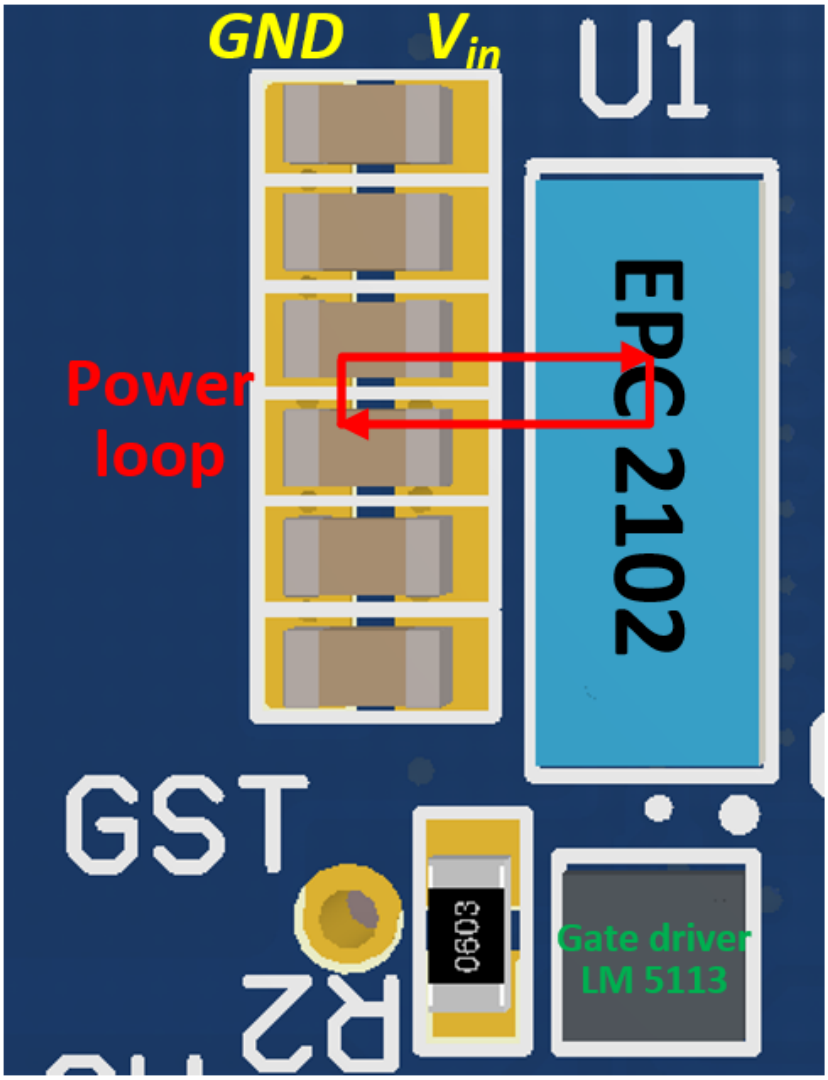


Fig. 49. Power loop using optimal PCB layout design

4.4 Hardware Assembly

Fig. 50 shows the primary converter of the gate-drive power supply. The length, width and height of the primary converter are 1.57 inches, 1.38 inches, and 0.67 inches, respectively. The resonant inductor L_r is located at the bottom of the board while the resonant capacitors C_r are placed on the top of the converter, beside the half-bridge switches, as shown in the figure. The volume of the primary-side converter is 1.45 inches^3.

The secondary converter is shown in Fig. 51. The resistors on the right are equivalent resistors that represent the gate driver. These resistors do not exist in the real circuit, so they do

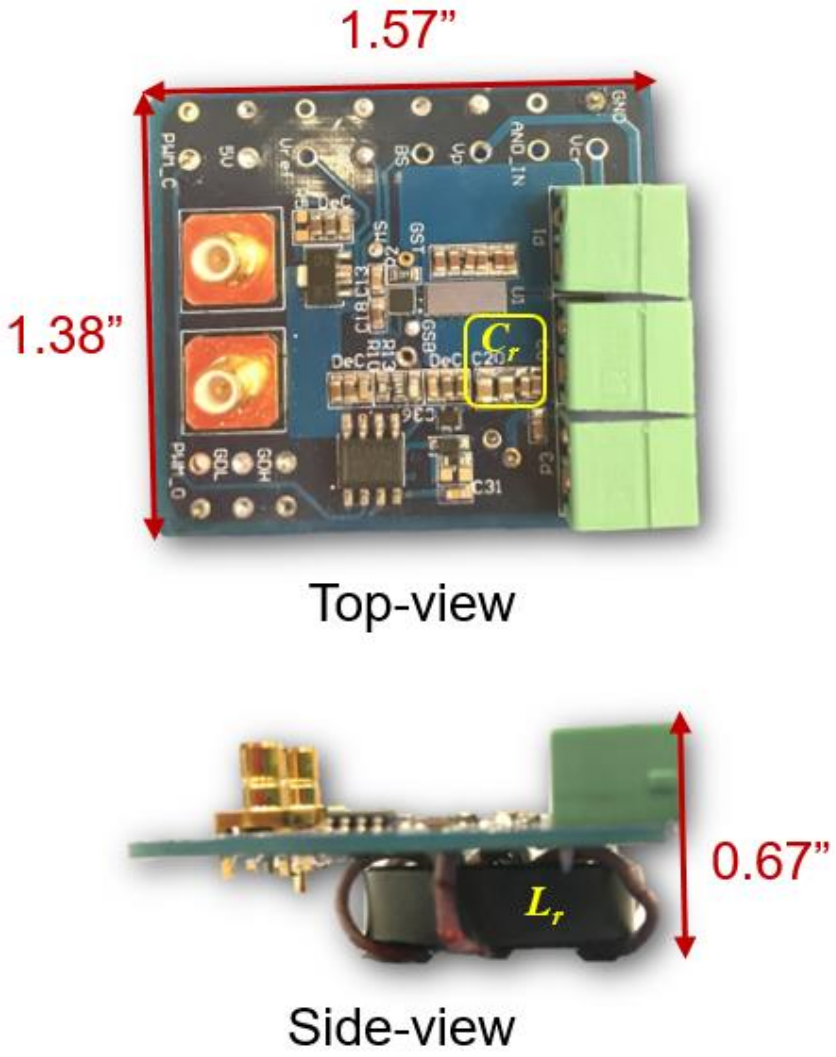


Fig. 50. Top-view and side-view of primary converter

not count toward the converter volume. The length, width, and height of the secondary converter are 1.89 inches, 1.46 inches, and 0.55 inches, respectively. The volume of the secondary-side converter is 1.52 inches^3.

The test prototype is shown in Fig. 52. The primary converter is on the left; two secondary converters are shown on the right. The HV cable [36], which is able to sustain 20 kV DC voltage, is used to connect the primary converter and the two secondary converters.

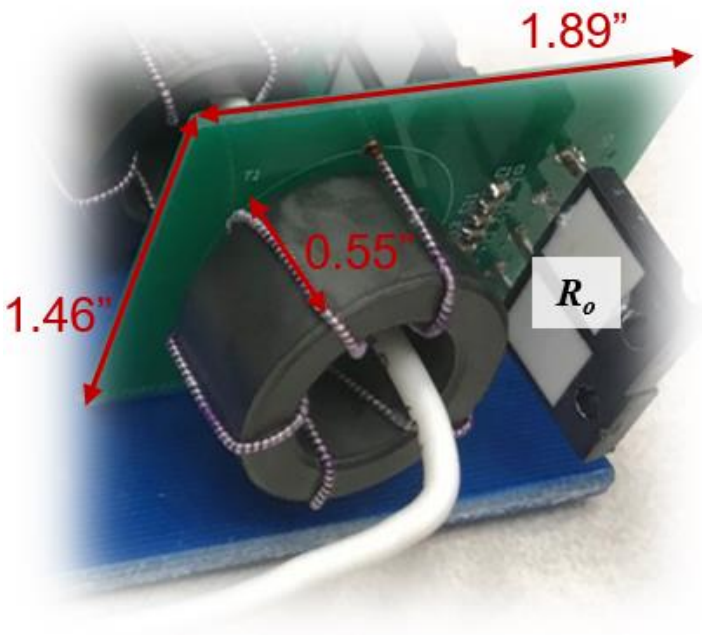


Fig. 51. Secondary converter

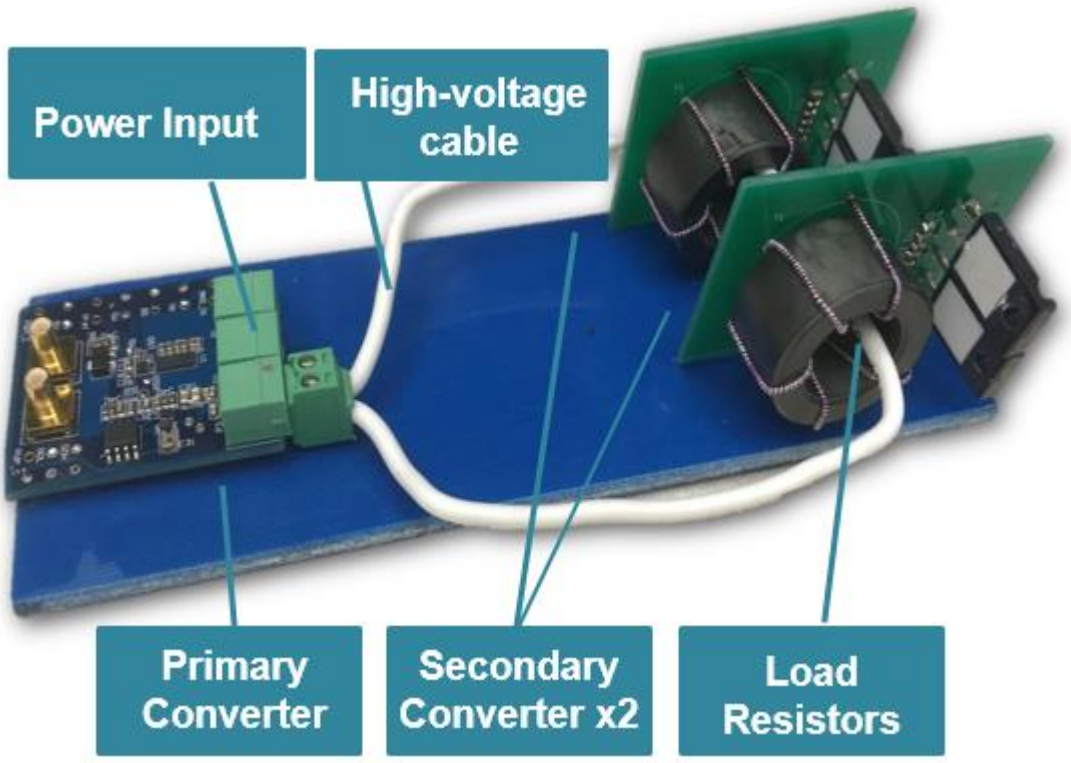


Fig. 52. Test prototype

4.5 Summary

In this chapter, three popular power device materials, Si, SiC, and GaN, are introduced. GaN devices are considered for use as the half-bridge switches of the isolated gate-drive power supply because of their superior high-frequency performance. Considering the DC-input voltage is 28 V and input current is approximately 1A, several candidates are selected and analyzed. A simulation circuit is built using a SPICE model. The half-bridge transistor EPC 2102 is selected due to its levels of conduction loss and switching loss. The highly integrated chip LM5113 from Texas Instruments is selected as the gate driver for the GaN devices. Schottky diodes SS25FACT are applied as the full-bridge rectifier.

Lastly, the primary converter, secondary converter and the test prototype of the isolated gate-drive power supply are shown.

Chapter 5: Experimental Testing

In this chapter, experimental testing results will be shown to verify the functionalities and design.

5.1 Load Independence

Fig. 53 shows the waveforms of RCB current i_{RCB}, the transformer's secondary-side output current i_s and the output voltage V_o in the one-load condition. It can be seen that the RMS value of the output voltage is 28.47 V. The load resistor here is 74 Ω, and the power can be given as:

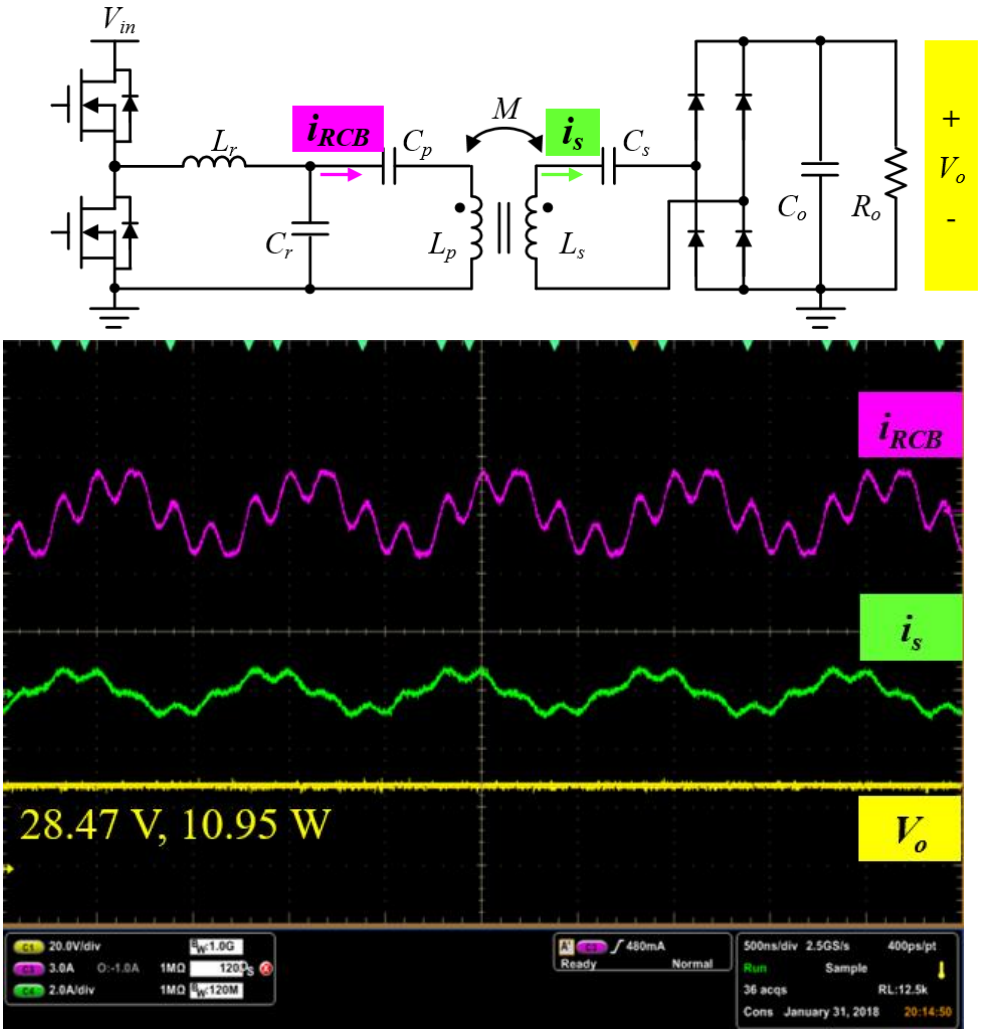


Fig. 53. Experimental result in one load condition

$$P_o = \frac{V_o^2}{R_o} = 10.95W \tag{71}$$

The input voltage and input current of the converter are 23.89 V and 0.61 A, respectively. The efficiency can be given by:

$$P_{in} = V_{in} \cdot I_{in} = 14.57W \tag{72}$$

$$\eta = \frac{P_o}{P_{in}}\% = 75.15\% \tag{73}$$

The efficiency is affected by the load condition. The efficiency curve with different load is shown in Fig. 54.

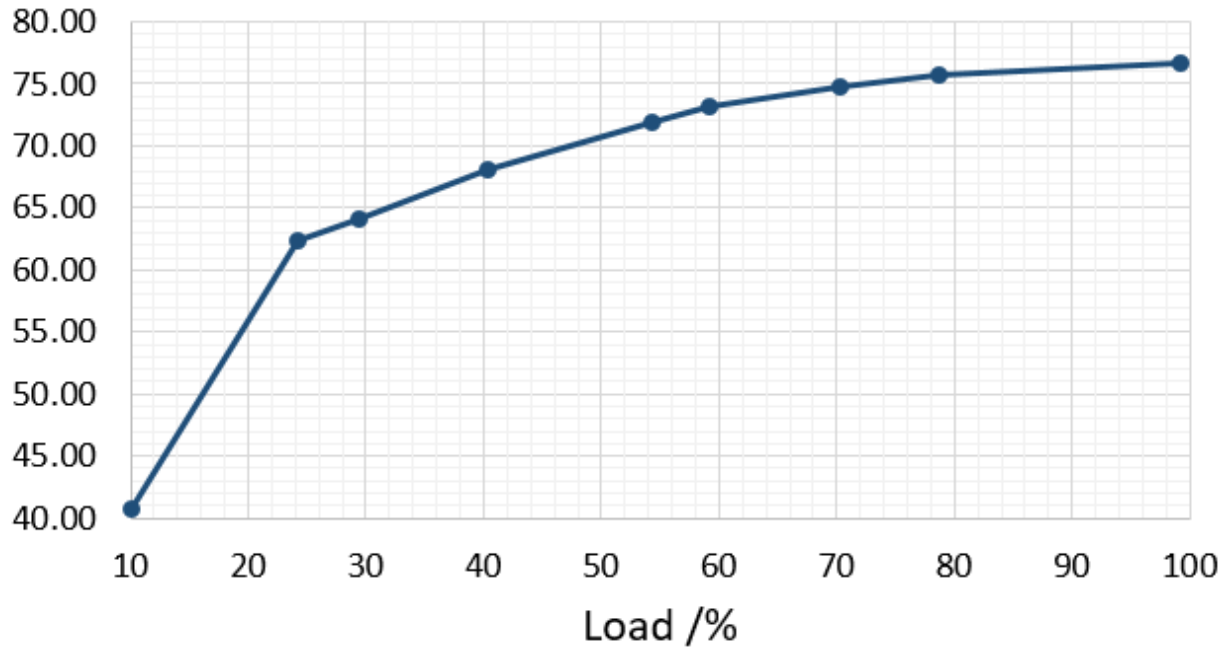


Fig. 54. Efficiency of 10% to 100% load

The testing results in the two loads condition are shown in Fig. 55. Fig. 55 shows the transformer secondary-side output currents and output voltage V_o of two loads, which are $i_{s1,}$ V_{o1} and $i_{s2,}$ V_{o2} respectively.

It can be seen that V_{o1} and $i_{s2,}$ V_{o2} overlap each other very well, and that both of them achieve approximately 28 V. The error between the output voltages of two-load conditions is:

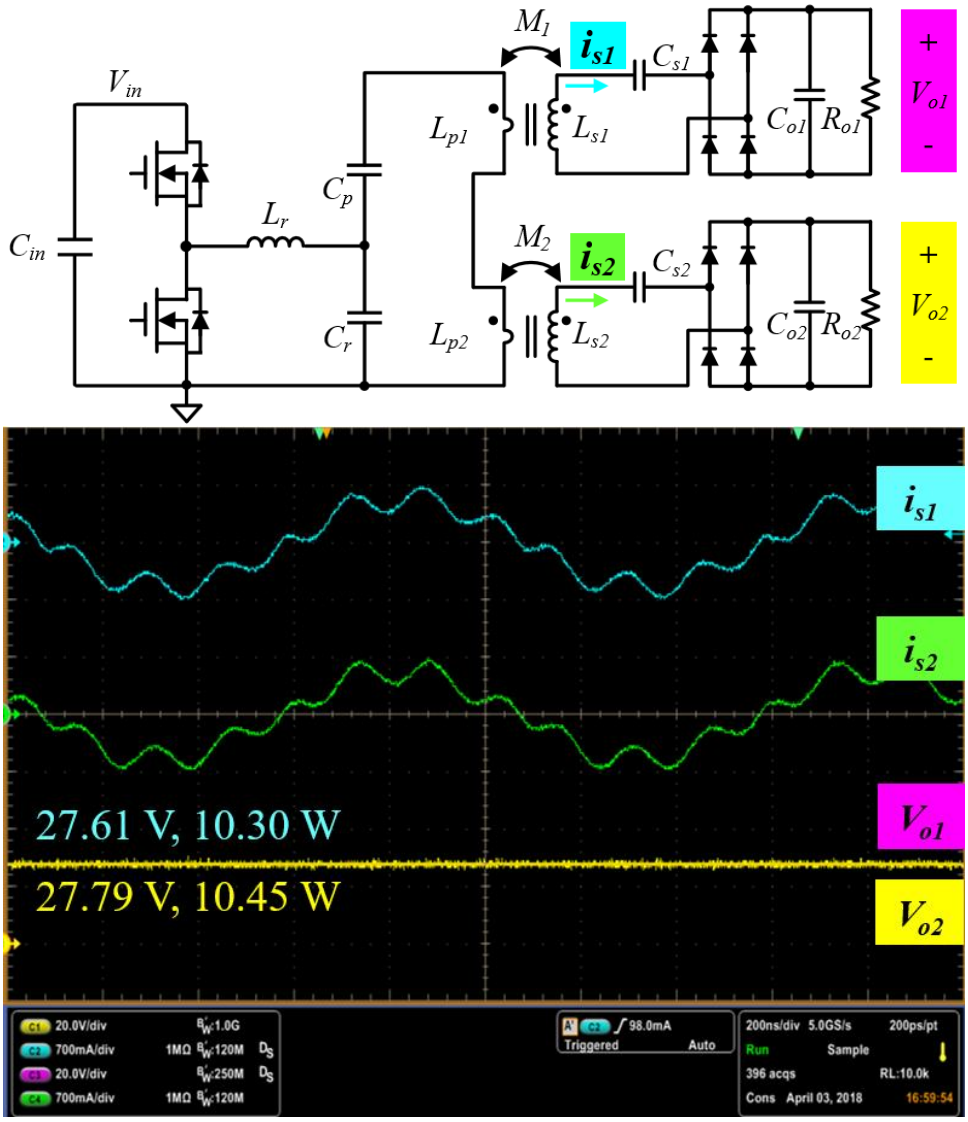


Fig. 55. Experimental result in two loads condition

$$error = \frac{27.79 - 27.61}{28V}\% = 0.64\% \tag{74}$$

This error is brought about by slight differences in the properties of the transformer, as it is difficult to make two transformers identical. This error is small enough to validate the load-independence design of the isolated gate-drive power supply proposed in this thesis. Without modifying any component in the power supply, adding another secondary converter will not change the output voltage V_o.

The output voltages for the two loads are 27.61 V and 27.79 V, and their output powers are:

$$P_{o1} = \frac{{V_{o1}}^2}{R_{o1}} = 10.30W \tag{75}$$

$$P_{o2} = \frac{{V_{o2}}^2}{R_{o2}} = 10.45W \tag{76}$$

The input voltage and input current of the converter are 23.89 V and 1.01 A, respectively. The efficiency can be given by:

$$P_{in} = V_{in} \cdot I_{in} = 24.13W \tag{77}$$

$$\eta = \frac{P_{o1} + P_{o2}}{P_{in}} \% = 85.99\% \tag{78}$$

The efficiency in a two loads condition is higher than that in a one load condition. The loss is decreased because the structure of this isolated gate-drive power supply reduces the number of the resonant inductor L_r by half, compared with those conventional converter structures with one primary converter and one secondary converter.

5.2 Zero-Voltage Switching

Another validation facet is zero-voltage switching (ZVS) in both one-load and two-load conditions. Fig. 56 shows the waveforms of two gate signals V_{gs_H}, V_{gs_L} and the switching node voltage, which is also the drain-to-source voltage of the low-side switch, V_{sw}. It is evident that the V_{sw} drops to zero before the low-side switch gate signal V_{gs_L} arrives; therefore, the low-side switch can be turned on softly. Similarly, the V_{sw} reaches 24 V before the high-side switch gate signal V_{gs_H} arrives. The high-side switch can be turned on in zero drain-source voltage.

In the two-load condition, which is not shown, ZVS is also achieved.

ZVS is easier to achieve with two loads than in the one-load condition. This is because of

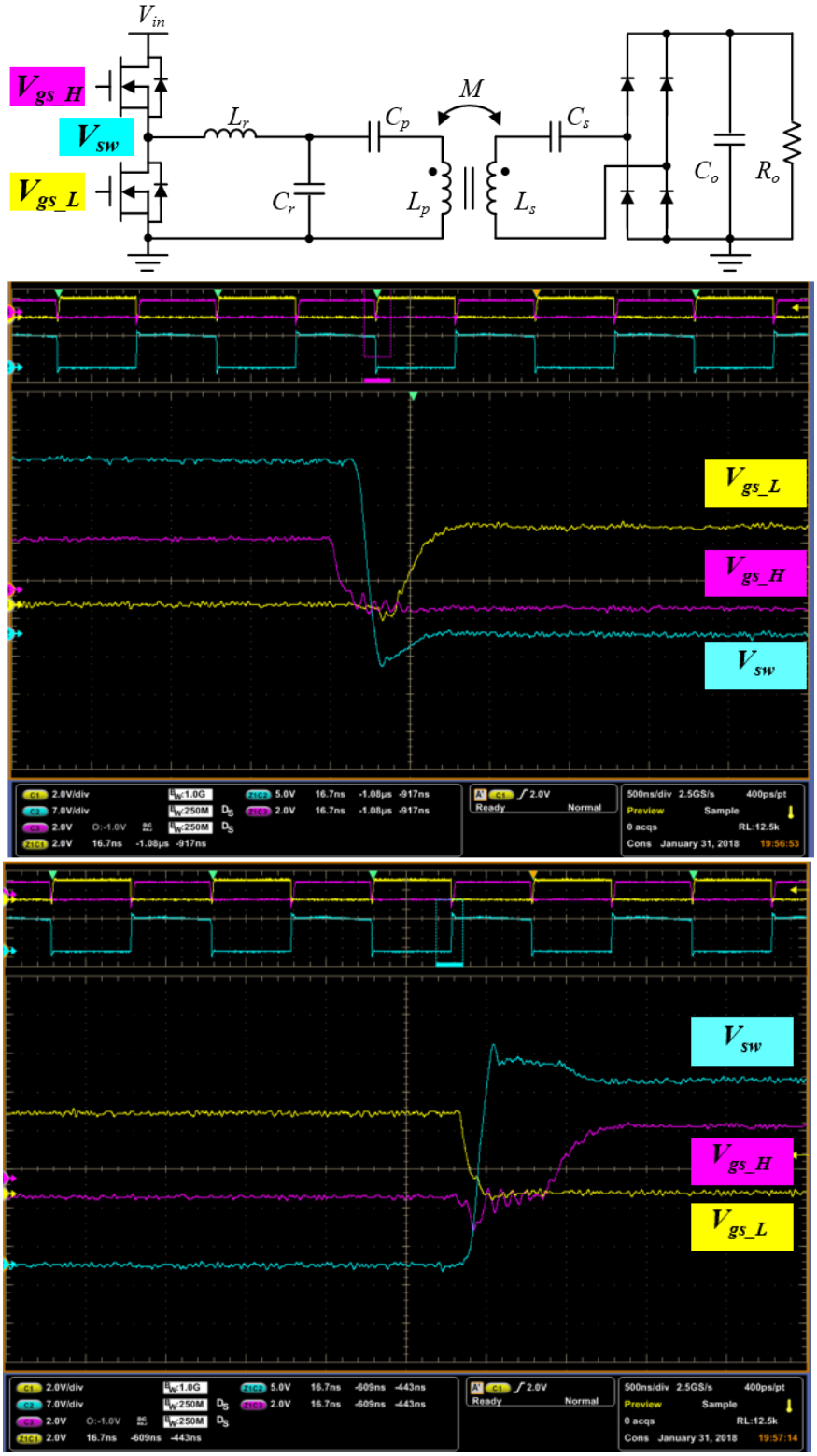


Fig. 56. ZVS validation in two loads condition

the larger input current that goes through the switches. Larger current can more quickly charge or discharge the switches' output capacitor C_{oss}. Therefore, if ZVS can be achieved in the one-load condition, it can also be achieved in two-load condition.

5.3 Voltage Regulation

In order to test the voltage regulation performance for the isolated power supply, only one load is tested. Fig. 57 shows the output voltage V_o with different load percentages. The input

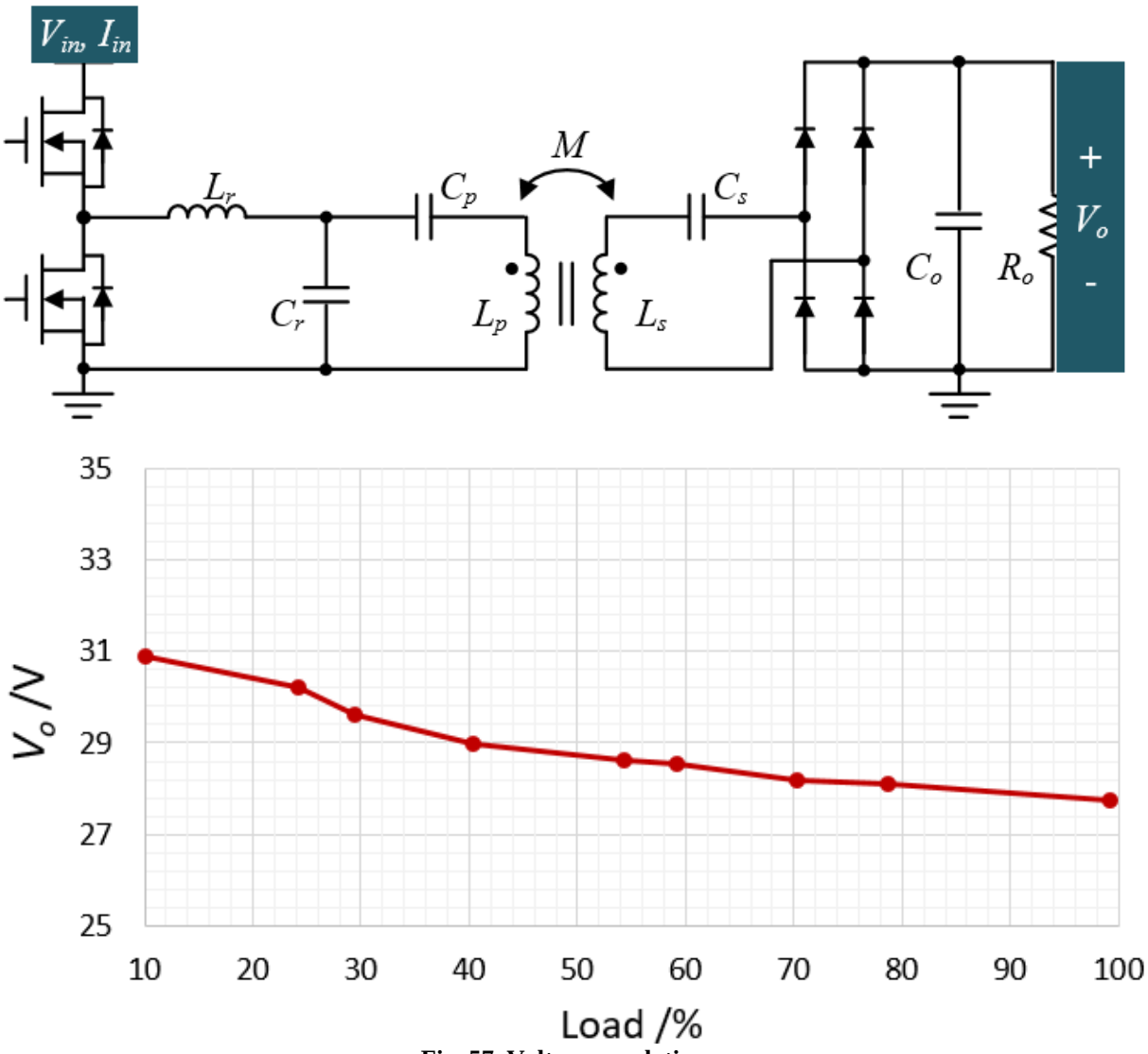


Fig. 57. Voltage regulation

voltage of the outside DC power supply V_{in}, input current of the converter I_{in} and the output voltage V_o are measured with a different load resistor. The maximum output voltage V_{o_max} exists in a 10 percent load condition, which is 30.87 V, whereas the minimum output voltage V_{o_min} exists in a 100 percent load condition, which is 27.76 V. The voltage difference is:

$$\Delta V_o = \frac{V_{o\_\max} - V_{o\_\min}}{V_{o\_\text{nom}}}\% = 11.1\% \tag{79}$$

Where V_{o_nom} is the nominal output voltage, which is 28 V. The difference of the output voltage is larger than the specification, and can be difficult to reduce due to the high quality factor of the resonant tank. The high quality factor worsens the performance of the resonant tank; therefore, the output current of the resonant tank is not a good current source.

5.4 Resilience

Another important aspect of testing is resiliency to faults. As mentioned in Chapter 2, it is very important to make sure the power supply will not shut down and damage the system. The short-circuit tests under one-load condition and two-load conditions are completed, and the waveforms are shown as follows to verify the design.

Fig. 58 shows the principle of the short-circuit test in the one-load condition.

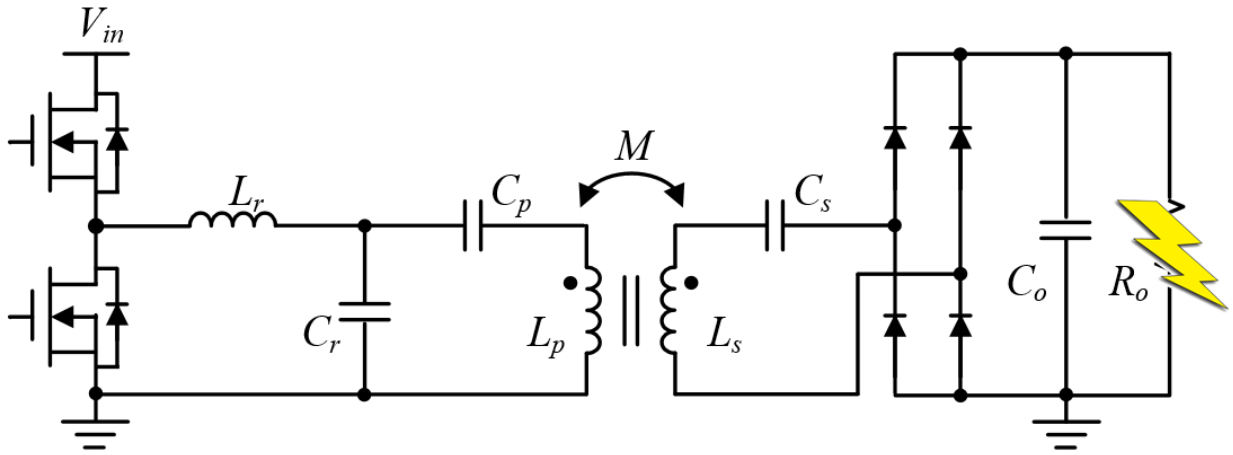


Fig. 58. Principle of short-circuit test, one-load condition

During the short-circuit test, the load resistor R_o will be shorted by a switch. The RCB current i_{RCB} will be measured to see whether it will or will not maintain a current-source characteristic. The high-side switch gate signal V_{gs_H}, the low-side switch gate signal V_{gs_L} and the switching node voltage V_{sw} are also measured to verify the ZVS performance of the primary converter. After the short-circuit testing, the recovery test will be done. The switch that shorts the load resistor will be removed, and the same current and voltage information mentioned above will be collected to show the restoration of service when faults disappear. The experimental testing waveforms are shown in Fig. 59.

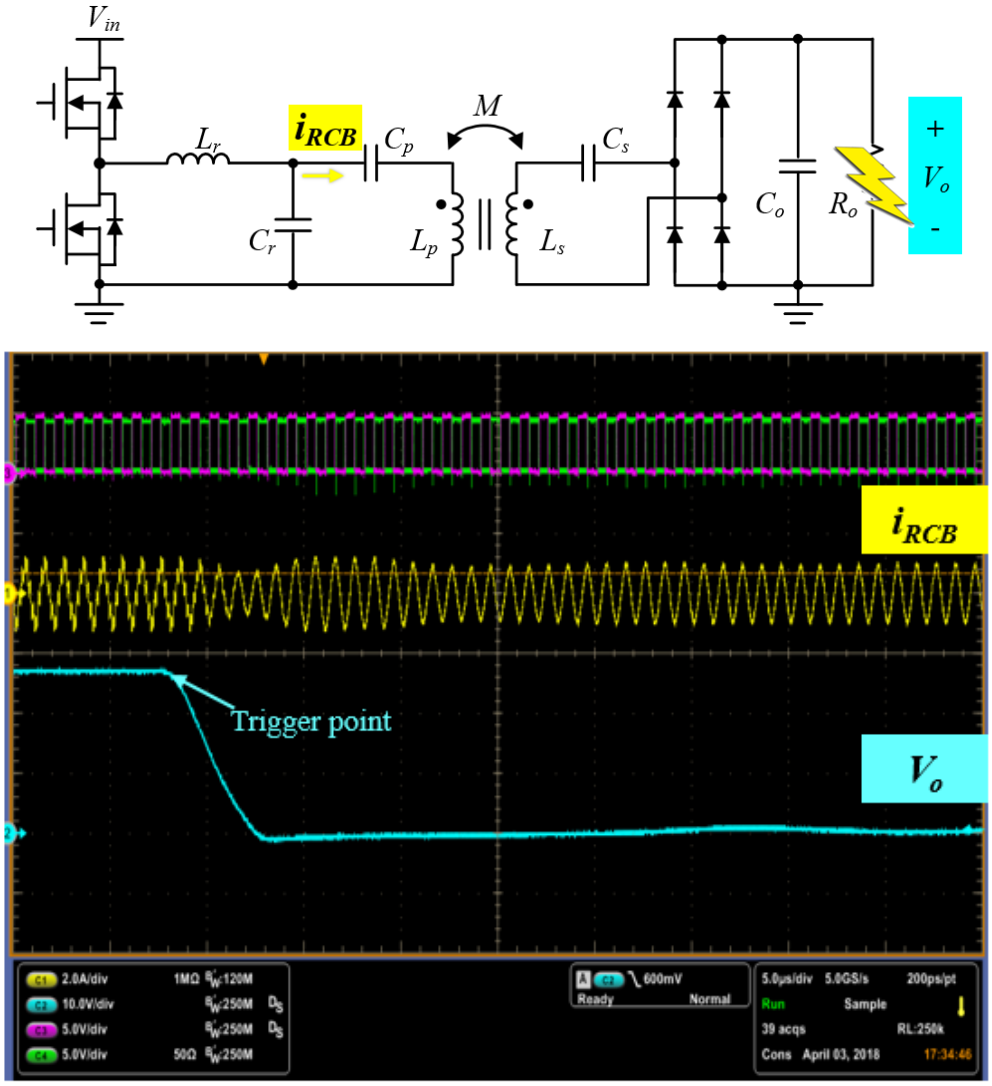


Fig. 59. i_{RCB} in short-circuit testing

Fig. 59 shows the waveforms of the RCB current $i_{RCB.}$ The blue waveform is the output voltage V_o.

When the load resistor is shorted (marked as trigger point in Fig. 59), the RCB current i_{RCB} will be slightly affected at the same time; however, it goes very quickly into steady state. It can be seen that the current remains almost the same compared with the RCB current i_{RCB} without the faults.

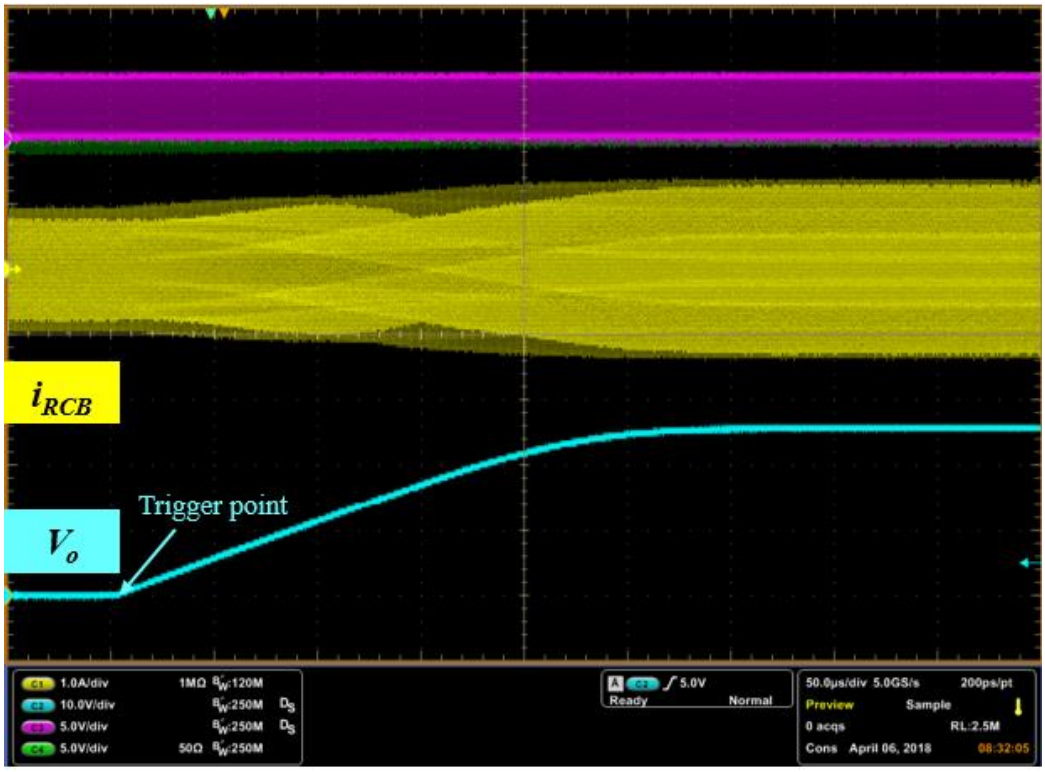


Fig. 60. i_{RCB} in short-circuit recovery testing

When the load is recovered, which is shown in Fig. 60, the output voltage V_o slowly returns back to the nominal voltage 28 V. The output voltage recovers slowly due to the large output capacitance in parallel with the load resistor, and there is no voltage overshoot in the output, which protects the gate driver. The RCB current i_{RCB} also recovers.

This proves this gate-drive power supply achieves restoration of service when the load is recovered.

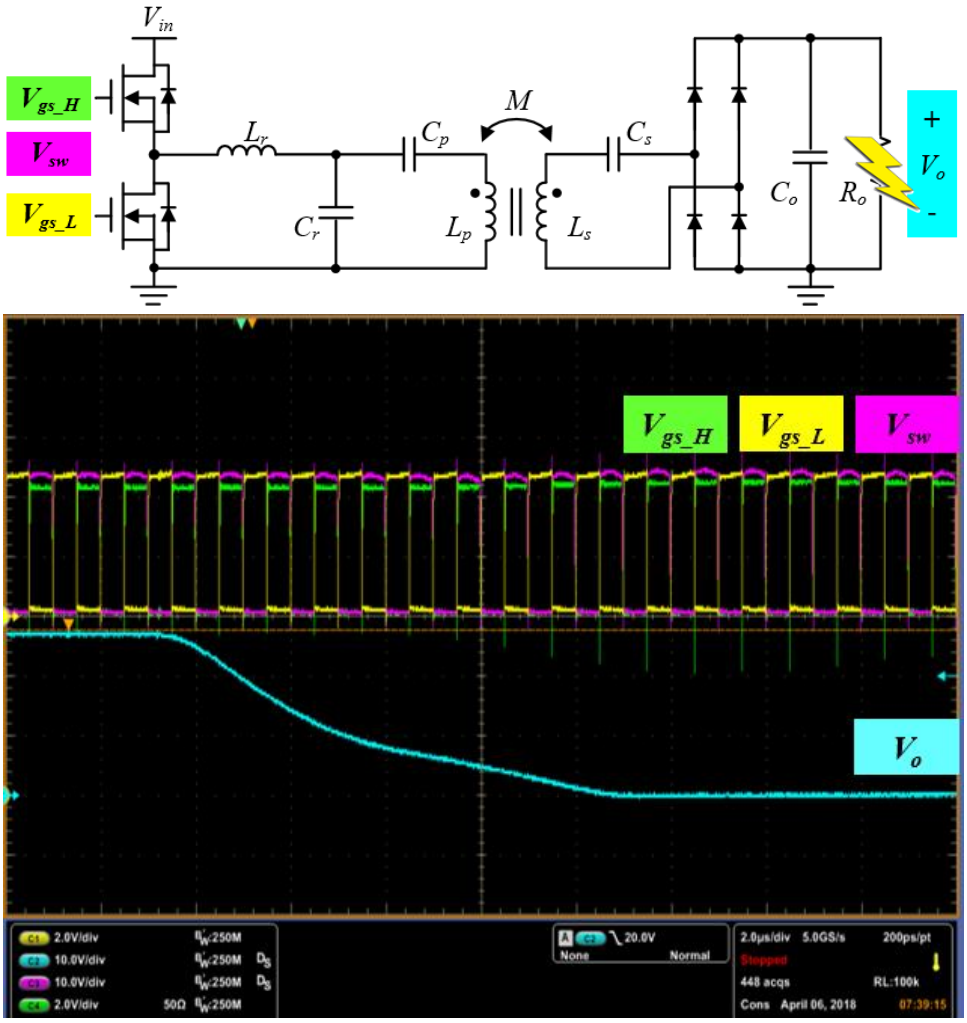


Fig. 61. ZVS in short-circuit testing

Fig. 61 shows the waveforms of output voltage V_o, high-side switch gate signal V_{gs_H}, the low-side switch gate signal V_{gs_L}, and the switching node voltage V_{sw} when the load is shorted.

The zoomed-in waveforms of the high-side switch gate signal V_{gs_H}, low-side switch gate signal V_{gs_L}, and the switching node voltage V_{sw} when V_o has dropped to zero are shown in Fig. 62.

The red curve is V_{sw} while the blue curve and green curve are the gate signals V_{gs_H} and V_{gs_L} respectively. It is clear that the V_{sw} drops to zero before the low-side switch gate signal V_{gs_L}

arrives; therefore, the low-side switch can be turned on softly. Similarly, the V_{sw} reaches 24 V before the high-side switch gate signal V_{gs_H} arrives. The high-side switch can be turned on with zero drain-to-source voltage.

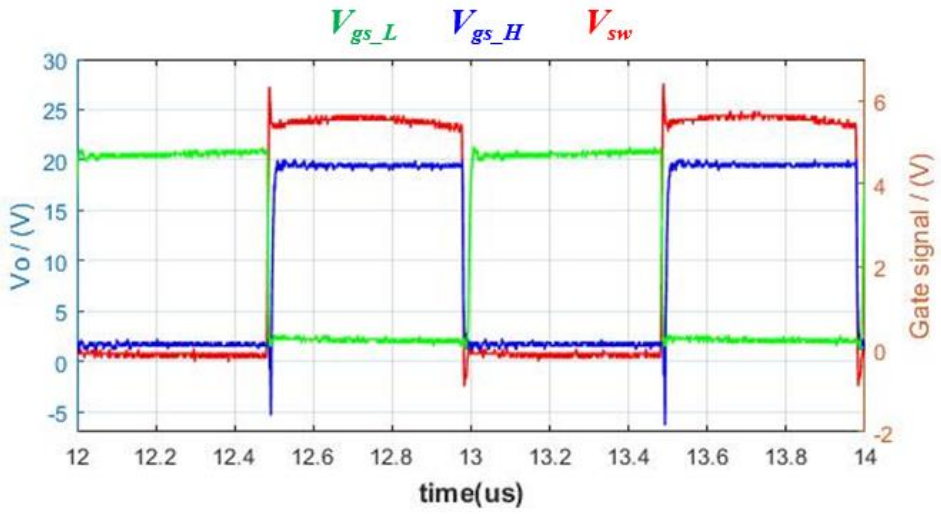


Fig. 62. Zoom-in waveforms of ZVS in short-circuit testing

Fig. 63 shows the principle of the short-circuit test in the two-load condition. The purpose of this test is to determine whether the primary converter will be damaged if there are faults in one of the loads; and whether the other load without faults is affected. During the short-circuit test, one of the load resistors will be shorted by a switch (R_{o1} shown in Fig. 63). The RCB current i_{RCB} will be measured to see whether or not it will maintain a current-source characteristic. The other output voltage V_{o2} and the transformer secondary output current i_{s2} are measured to see if it will affect the secondary converter without faults. The high-side switch gate signal V_{gs_H}, the low-side switch gate signal V_{gs_L}, and the switching node voltage V_{sw} are also measured to verify the ZVS performance of the primary converter.

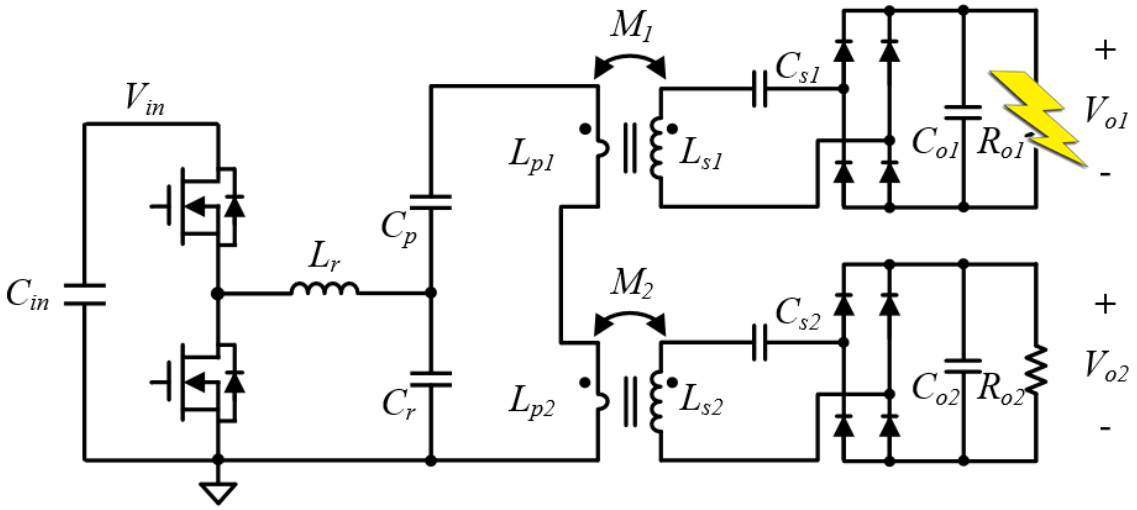


Fig. 63. Principle of short-circuit test in two loads condition

The blue waveform in Fig. 64 is RCB current i_{RCB} and the yellow waveform is the transformer's secondary output current i_{s2} of the converter without any faults. The green waveform and the purple waveform are the output voltages V_{o1} and V_{o2}, respectively. The load resistor of V_{o1} is going to be shorted.

It is clear to see that the output voltage V_{o2} maintains 28 V when the other load is shorted. This is because the change of the RCB current i_{RCB} is very small. The transformer's secondary output current i_{s2} increases but it will not affect the output voltage due to the capacitor C_r, which removes the load resistor R_{o2} from the path. Equation (14) also helps to explain this concept.

With the compensation C_r, the output voltage V_o is only related to the mutual inductance M and the RCB current i_{RCB}. If these remain unchanged, the output voltage V_o can maintain 28 V. These waveforms prove that the faults in one of the loads will not damage the primary converter or the other load.

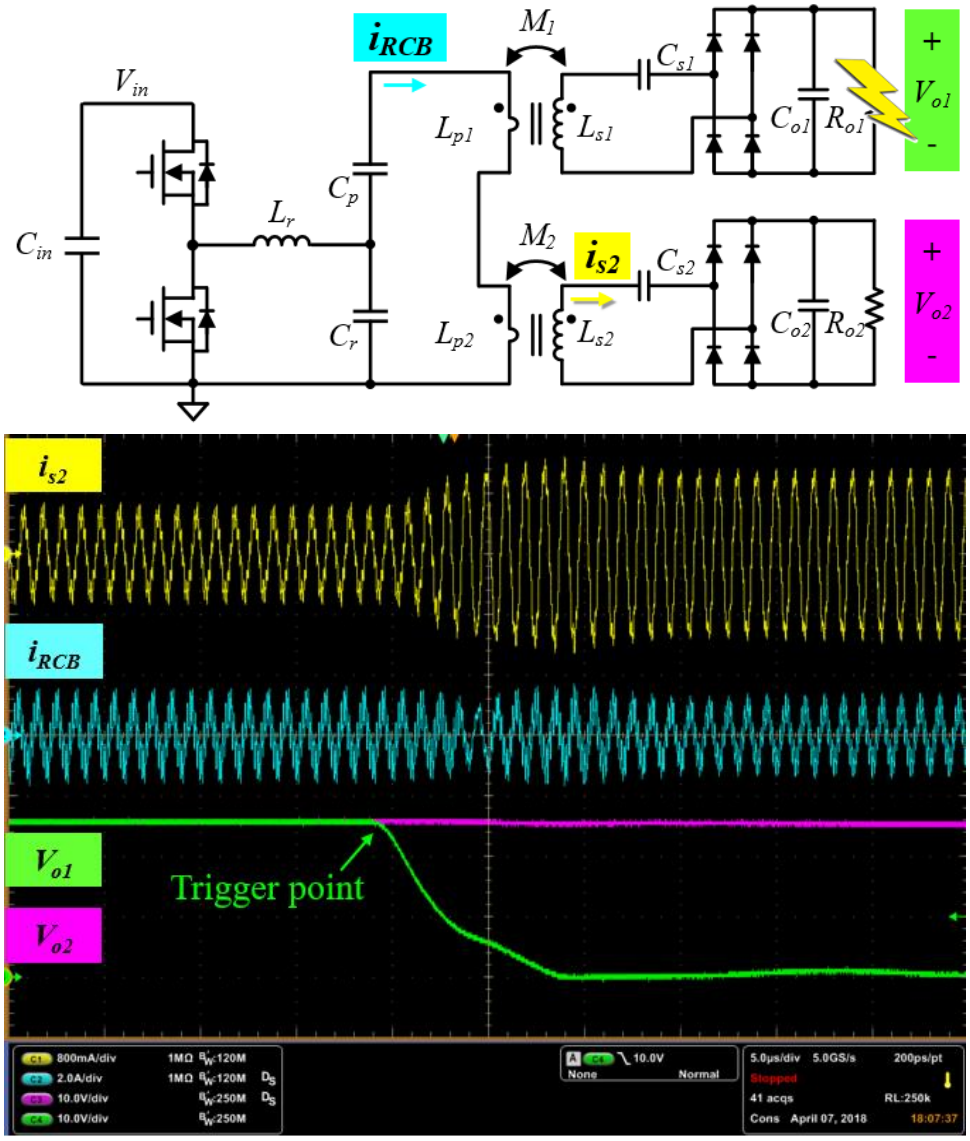


Fig. 64. i_{RCB} in short-circuit testing in two load condition

Fig. 65 shows the waveforms when the fault hass disappeared. The output voltage V_{o1} recovers slowly to 28 V due to the large output capacitance, which is in parallel with the load resistor. The RCB current i_{RCB} also recovers. It proves that this gate-drive power supply achieves restoration of service when the load is recovered in the two-load condition.

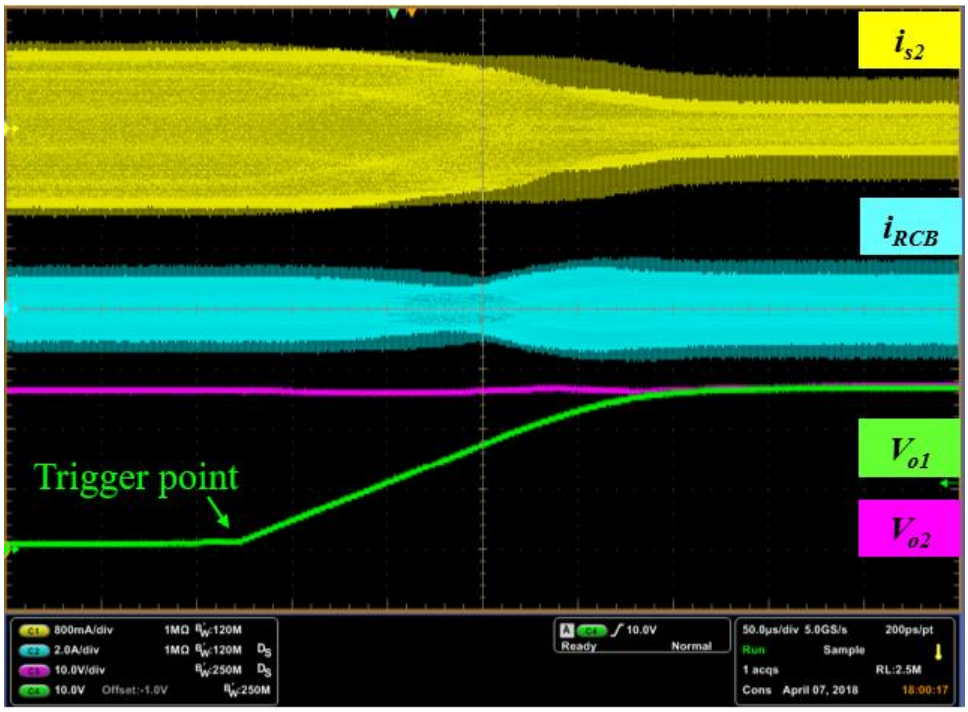


Fig. 65. i_{RCB} in short-circuit recovery testing in two loads condition

Fig. 66 shows the waveforms of high-side switch gate signal V_{gs_H}, the low-side switch gate signal V_{gs_L}, and the switching node voltage V_{sw} of the primary converter. These waveforms are used to analyze the ZVS performance.

Their zoomed-in waveforms are shown in Fig. 67. The red curve is V_{sw} while the blue curve and green curve are the gate signals V_{gs_H} and V_{gs_L}, respectively. It is clear to see that the V_{sw} drops to zero before the low-side switch gate signal V_{gs_L} arrives. Therefore, the low-side switch can be turned on softly. Similarly, the V_{sw} reach 24 V before the high-side switch gate signal V_{gs_H} arrives. The high-side switch can be turned on with zero drain-to-source voltage.

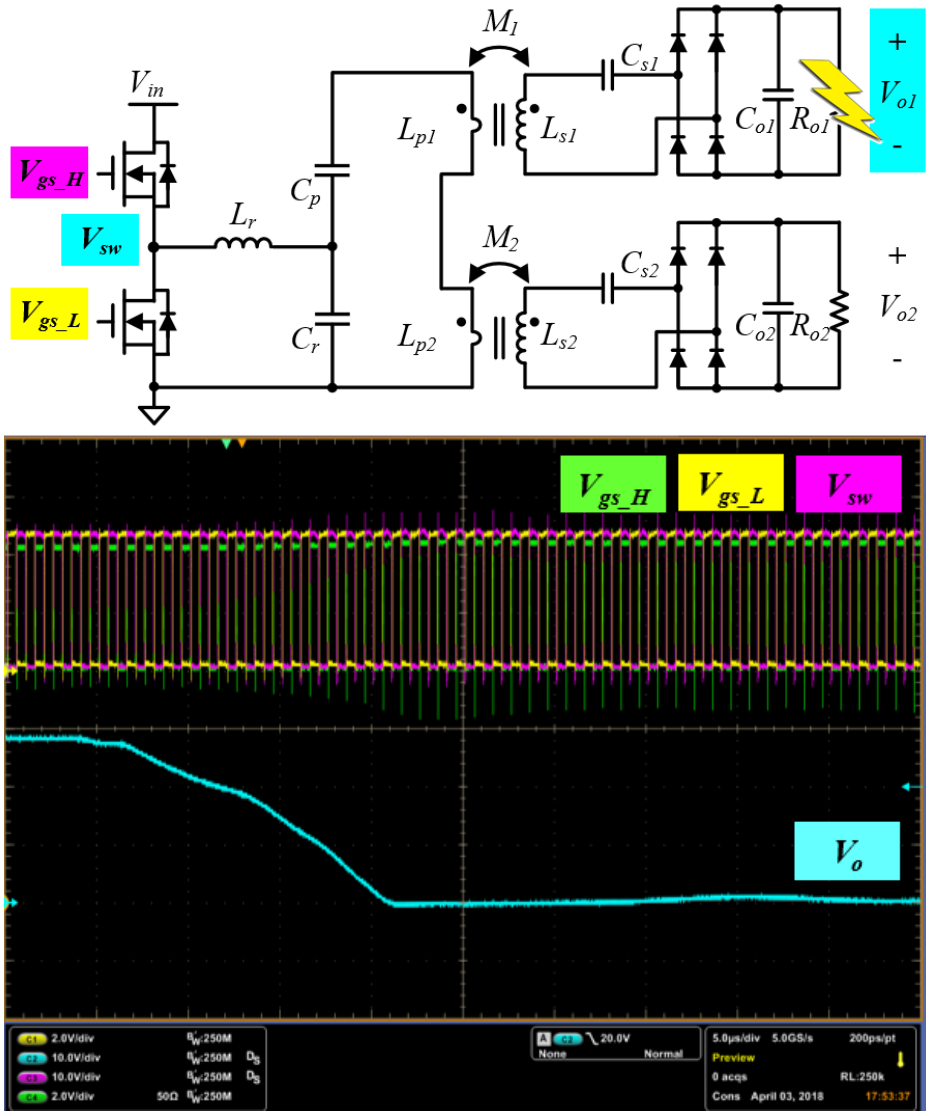


Fig. 66. ZVS in short-circuit testing

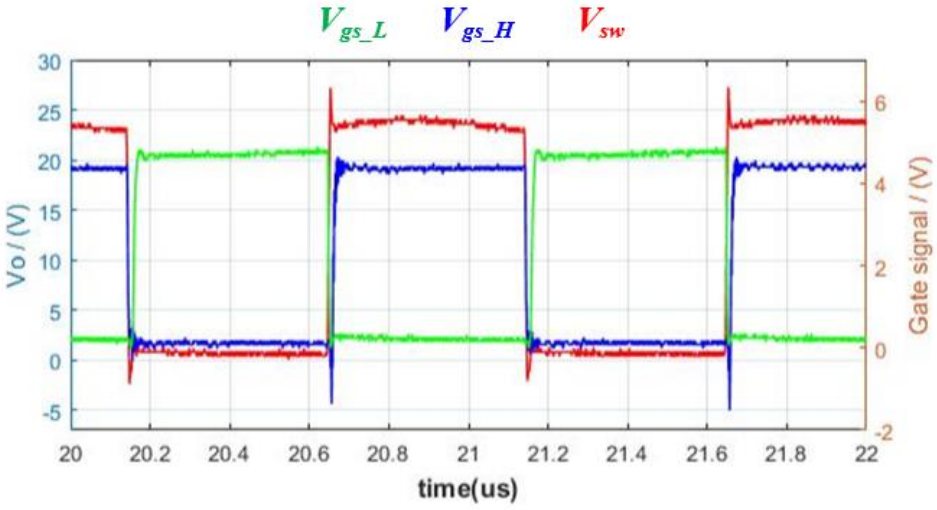


Fig. 67. Zoom-in waveforms of ZVS in short-circuit testing

5.5 Summary

In this chapter, the experimental testing results are shown to verify the design.

First, the experimental testing results for the one-load condition are given. The output voltage V_o reaches 28 V and the output power is 11 W. The efficiency is 75 percent. The loss mainly consists of the core loss of the transformer and the primary side resonant tank inductor L_r. ZVS is achieved. The experimental testing results for the two-load condition are also provided, and again, ZVS is achieved.

Second, the experimental testing results for voltage regulation are provided. The maximum output voltage V_{o_max} exists in the 10 percent load condition, which is 30.87 V; whereas the minimum output voltage V_{o_min} exists in the 100 percent load condition, which is 27.76 V. The voltage difference reaches 11%, which happens because the transformer's input current is not an ideal current source. The high order harmonic components cannot be neglected.

Next, the experimental testing results for the resilience are given. Short-circuit tests in the one-load and two-load condition are completed. The results show that the short -circuit in the load will not damage the primary converter, and thus this isolated gate-drive power supply has the capability to restore service when faults disappear.

Chapter 6: Summary and Conclusion

This thesis proposes an isolated gate-drive power supply that supplies multiple gate drivers for 10 kV, 240 A SiC MOSFETs module.

A current transformer configuration is adopted due to its simpler accomplishment of high-voltage isolation, low input-output coupling capacitance $C_{I/O}$, and resiliency to faults. The equivalent circuit of the current transformer is analyzed to design the transformer properties, including the mutual inductance M and the turns number N_s. A mathematical model of transformer input-output coupling capacitance $C_{I/O}$ is built and utilized to optimize the core dimensions. The frequency of the resonant current bus (RCB) is designed at 1 MHz, and the ML91S from Hitachi is selected. The hardware is shown, and the input-output coupling capacitance $C_{I/O}$ of 1.67 pF is measured by an Agilent 4294A Precision Impedance Analyzer.

For voltage regulation design, a capacitor C_s is added in series with the transformer secondary self-inductance L_s to compensate the voltage drop across the L_s. With this capacitor C_s, the output voltage V_o is only related to the transformer's mutual inductance M and the transformer primary-side input current I_p. A parallel resonant inductor/capacitor (LC) circuit is utilized to build the RCB, and a blocking capacitance C_p is needed. The completed circuit, which is called an LCCL-LC resonant converter, is analyzed, and the design guidelines are provided in this thesis.

Experimental testing results are shown to validate the design. The isolated gate-drive power supply outputs 28 V and 10W per load. The isolated gate-drive power supply achieves 75 percent and 86 percent, respectively, in the one-load and two-load conditions, respectively. ZVS is achieved in both one load and two loads condition. The waveforms for the short-circuit testing are shown to prove that the isolated gate-drive power supply will not damage the circuit when

faults exist. More importantly, ZVS is maintained during short circuits. This power supply has the capability to restore service when faults disappear.

References

[1]. J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, J. Rebollo, “A survey of wide bandgap power semiconductor devices,” *IEEE Trans. Power Electron*., vol. 29, no. 5, May 2014, pp. 2155-2163.

[2]. Datasheet, “The ACS2000 Industrial Drive”, [Online]. Available: https://library.e.abb.com/public/b05122db521e4764ab0e72cf0c065529/ACS2000-Product-brochure_low-res_US-Rev-G.pdf

[3]. IEC 60664-1 https://webstore.iec.ch/p-preview/info_iec60664-1%7Bed1.2%7Den_d.pdf

[4]. X. Zhang, et al., “A gate drive with power over fiber-based isolated power supply and comprehensive protection functions for 15-kV SiC MOSFET,” *IEEE Trans. Emerg. Sel. Topics Power Electron*, 2016.

[5]. J. Afsharian, N. Zaragari, and W. Bin, “A special high-frequency soft-switched high-voltage isolated DC/DC power supply for multiple GCT gate drivers,” in Proc. of *IEEE ECCE,* 2010, pp. 2441-2445.

[6]. D. Peftitsis, M. Antivachis, and J. Biela, “Auxiliary power supply for medium-voltage modular multilevel converters”, in Power Electronics and Applications (EPE’15 ECCE-Europe), 2015 17th *European Conference* on, 2015, pp. 1–11. DOI: 10.1109/EPE.2015.7309388.

[7]. K. Mainali, A. Tripathi, S. Madhusoodhanan, A. Kadavelugu, D. Patel, S. Hazra, K. Hatua, and S. Bhattacharya, "A Transformerless Intelligent Power Substation: A three-phase SST

enabled by a 15-kV SiC IGBT," *IEEE Power Electronics Magazine*, vol. 2, no. 3, Sept. 2015, pp. 31-43.

[8]. R. Steiner, P. Steimer, F. Krismer and J. Kolar, "Contactless energy transmission for an isolated 100W gate driver supply of a medium voltage converter," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, 2009.

[9]. X. Zhang et al., "A 15 kV SiC MOSFET gate drive with power over fiber based isolated power supply and comprehensive protection functions," *IEEE Trans. Appl. Power Electron. Conf. Expo. (APEC)*, Long Beach, CA, 2016, pp. 1967-1973.

[10]. J. Gottschlich et al., “A Galvanically Isolated Gate Driver with Low Coupling Capacitance for Medium Voltage SiC MOSFETs” Power Electronics and Applications, 2016

[11]. K. Mainali, S. Madhusoodhanan, A. Tripathi, K. Vechalapu, A. De, and S. Bhattacharya, “Design and evaluation of isolated gate driver power supply for medium voltage converter applications”, in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), 2016, pp. 1632–1639.

[12]. K. Nguyen-Duy, Z. Ouyang, A. Knott, and M. A. E. Andersen, “Minimization of the transformer inter-winding capacitance for modular stacking power supply applications,” in Proc. 16th Eur. Conf. Power Electron. Appl., 26–28, Aug. 2014.

[13]. Product report. “Hitachi Metals Creates New Soft Ferrite Core Material with Outstanding High-Frequency Characteristics,” April. 2016. [Online]. Available: https://www.hitachi-metals.co.jp/e/press/news/2016/n0404.html.

[14]. C. R. Sullivan and R. Y. Zhang, "Simplified design method for litz wire," in Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE, 2014, pp. 2667-2674

[15]. J. A. Ferreira, "Analytical computation of ac resistance of round and rectangular litz wire windings," IEE Proceedings-B Electric Power Applications, vol. 139, no. 1, Jan. 1992, pp. 21-25.

[16]. -, "Improved analytical modeling of conductive losses in magnetic components," IEEE Trans. on Pow. Electr., vol. 9, no. 1, Jan. 1994, pp. 127-31.

[17]. J. Acero, P. J. Hernandez, J. M. Burdó, R. Alonso, and L. Barragdan, "Simple resistance calculation in litz-wire planar windings for induction cooking appliances," IEEE Trans. on Magnetics, vol. 41, no. 4, 2005, pp. 1280-1288.

[18]. J. Acero, R. Alonso, J. M. Burdio, L. A. Barragan, and D. Puyal, "Frequency-dependent resistance in litz-wire planar windings for domestic induction heating appliances," IEEE Trans. on Pow. Electr., vol. 21, no. 4, 2006, pp. 856-866.

[19]. C. Carretero, J. Acero, and R. Alonso, "Tm-te decomposition of power losses in multi-stranded litz-wires used in electronic devices," Progress In Electromagnetics Research, vol. 123, 2012, pp. 83-103.

[20]. H. Rossmanith, M. Doebroenti, M. Albach, and D. Exner, "Measurement and characterization of high frequency losses in nonideal litz wires," IEEE Trans. on Pow. Electr., vol. 26, no. 11, 2011, pp. 3386-3394.

[21]. Xi Nan and C. R. Sullivan, "An equivalent complex permeability model for litz-wire windings," in Fortieth IEEE Industry Applications Society Annual Meeting, 2005, pp. 2229-2235

[22]. D. C. Meeker, "An improved continuum skin and proximity effect model for hexagonally packed wires," Journal of Computational and Applied Mathematics, vol. 236, no. 18, 2012, pp. 4635-4644.

[23]. C. Sullivan, “Computationally efficient winding loss calculation with multiple windings, arbitrary waveforms, and two-dimensional or three-dimensional field geometry,” Power Electronics, IEEE Transactions on, vol. 16, no. 1, 2001, pp. 142–150.

[24]. J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, “A survey of wide bandgap power semiconductor devices,” IEEE Trans. Power Electron., vol. 29, no. 5, May 2014, pp. 2155–2163.

[25]. Jungwon Choi, D. Tsukiyama, Y. Tsuruda and J. Rivas, "13.56 MHz 1.3 kW resonant converter with GaN FET for wireless power transfer," 2015 IEEE Wireless Power Transfer Conference (WPTC), Boulder, CO, 2015,pp.1-4. doi: 10.1109/WPT.2015.7140167

[26]. L. Sun, Z. Ding, D. Guo, L. Yan and C. Yan, "High efficiency high density telecom rectifier with GaN device," 2 015 IEEE International Telecommunications Energy Conference (INTELEC), Osaka, 2015, pp. 1- 5.doi: 10.1109/INTLEC.2015.7572401

[27]. J. Lu, H. K. Bai, S. Averitt, D. Chen and J. Styles, "An E-mode GaN HEMTs based three-level bidirectional DC/DC converter used in Robert Bosch DC-grid system," 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, 2015, pp. 334-340.doi: 10.1109/WiPDA.2015.736925

[28]. Y. Qiu, L. Wang, H. Wang, Y. F. Liu, and P. C. Sen, "Bipolar Ripple Cancellation Method to Achieve Single-Stage Electrolytic-CapacitorLess High-Power LED Driver," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, pp. 698-713, 2015.

[29]. J. L. Lu., Q.Tian., & H.Bai. (2015). An Indirect Matrix Converter based 97 % - efficiency On-board Level 2 Battery Charger Using E-mode GaN HEMTs. IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA), T11.8011, 351–358.

[30]. R. Hou and A. Emadi, “Applied integrated active filter auxiliary power modules for electrified vehicles with single-phase onboard chargers,” IEEE Transactions on Power Electronics. vol. 32, no. 3, Mar. 2017, pp. 1860-1871.

[31]. R. Hou and A. Emadi, “A Primary full-integrated active filter auxiliary power module in electrified vehicle applications with single-phase onboard chargers,” IEEE Transactions on Power Electronics. vol. 32, no. 11, Nov. 2017, pp. 8393-8405.

[32]. J. Lu et al., "A Modular Designed Three-phase High-efficiency Highpower-density EV Battery Charger Using Dual/Triple-Phase-Shift Control," in IEEE Transactions on Power Electronics, vol. PP, no. 99, pp. 1-1. doi: 10.1109/TPEL.2017.2769661

[33]. J. Lu et al., "Applying Variable-Switching-Frequency Variable-PhaseShift Control and E-Mode GaN HEMTs to an Indirect Matrix ConverterBased EV Battery Charger," in IEEE Transactions on Transportation Electrification, vol. 3, no. 3, pp. 554-564, Sept. 2017.doi: 10.1109/TTE.2017.2723944

[34]. D. Reusch, “eGaN-Silicon Power Shoot-Out Vol. 13, Part 1: Impact of Parasitics on Performance” white paper, 2013. [Online] Available: http://epc-

co.com/epc/Portals/0/epc/documents/papers/impact%20of%20parasitcs%20on%20performance.pdf

[35]. D. Reusch, “Optimizing PCB Layout with eGaN FETs” white paper, 2014. [Online] Available: http://epc-co.com/epc/Portals/0/epc/documents/papers/optimizing%20pcb%20layout%20with%20egan%20fets.pdf

[36]. Datasheet: High-voltage Continuous-Flex Wire. [Online]. Available: https://www.mcmaster.com/#high-voltage-wire/=1cj2rw7