SIEMENS

Function manual

SIMATIC

S7-1500, S7-1500R/H, ET 200SP, ET 200pro

Cycle and response times

SIEMENS

SIMATIC

S7-1500, S7-1500R/H, ET 200SP, ET 200pro
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Function Manual

Legal information

Warning notice system

This manual contains notices you have to observe in order to ensure your personal safety, as well as to prevent damage to property. The notices referring to your personal safety are highlighted in the manual by a safety alert symbol, notices referring only to property damage have no safety alert symbol. These notices shown below are graded according to the degree of danger.

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indicates that death or severe personal injury **will** result if proper precautions are not taken.

⚠ WARNING
indicates that death or severe personal injury **may** result if proper precautions are not taken.

⚠ CAUTION
indicates that minor personal injury can result if proper precautions are not taken.

NOTICE
indicates that property damage can result if proper precautions are not taken.

If more than one degree of danger is present, the warning notice representing the highest degree of danger will be used. A notice warning of injury to persons with a safety alert symbol may also include a warning relating to property damage.

Qualified Personnel

The product/system described in this documentation may be operated only by **personnel qualified** for the specific task in accordance with the relevant documentation, in particular its warning notices and safety instructions. Qualified personnel are those who, based on their training and experience, are capable of identifying risks and avoiding potential hazards when working with these products/systems.

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Trademarks

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We have reviewed the contents of this publication to ensure consistency with the hardware and software described. Since variance cannot be precluded entirely, we cannot guarantee full consistency. However, the information in this publication is reviewed regularly and any necessary corrections are included in subsequent editions.

Preface

Purpose of the documentation

The controller offers various options for program execution with different run priorities. Cyclic-driven and time-driven program execution have the largest share. The response times of a controller are therefore significantly determined by the processing cycles.

There is also the possibility of event-driven program execution. The event-driven program execution is normally limited to a few selected events.

This manual provides information on the following topics:

- Types of program execution
- Run priorities
- Cycle and response times, and the influences to which they are subject
- Configuration options for the optimization of your user program

Basic knowledge required

The following knowledge is required in order to understand the documentation:

- General knowledge of automation technology
- Knowledge of the SIMATIC industrial automation system
- Knowledge of the use of Windows-based computers
- Knowledge of working with STEP 7

Conventions

STEP 7: In this documentation, "STEP 7" is used as a synonym for all versions of the configuration and programming software "STEP 7 (TIA Portal)".

Please also observe notes marked as follows:

Note

A note contains important information on the product described in the documentation, on the handling of the product or on the section of the documentation to which particular attention should be paid.

Scope of the documentation

This documentation mainly covers the description of the CPU components of the cycle and response times of the following systems:

- SIMATIC S7-1500 automation system

- SIMATIC S7-1500R/H redundant system

- The CPUs of the ET 200SP distributed I/O system

- The CPUs of the ET 200pro distributed I/O system based on SIMATIC S7-1500

You can find links to more information on the ET 200MP, ET 200SP and ET 200pro distributed I/O systems at the corresponding points in this manual.

Note

F-specific monitoring and response times are not covered by the Cycle and Response Times function manual.

For F-specific monitoring and response times, refer to the programming and operating manual SIMATIC Safety - Configuration and Programming (https://support.industry.siemens.com/cs/ww/en/view/54110126).

What's new in edition 02/2021 compared to edition 11/2019?

What's new?		What are the customer benefits?	Where can I find information?
Changed contents	Scope of the function manual expanded to include CPU 1518HF-4 PN of the S7-1500R/H redundant system	The CPU 1518HF-4 PN extends the R/H CPU portfolio by an HF CPU. The CPU offers the following advantages: • High-performance H-CPU with integrated F-functionality • The CPU can also be used for safety functions according to IEC 61508 up to SIL 3 and ISO 13849 up to PLe for safety applications. • 3 PROFINET interfaces	Starting from section Program execution (Page 15)
	Scope of the function manual expanded to include CPU 1518T-4 PN/DP of the S7-1500 automation system	CPU 1518T-4 PN/DP offers a very large program and data memory for demanding applications in applications that contain distributed I/O in addition to central automation structures. CPU 1518T-4 PN/DP features high-performance, extended Motion Control functions, for example: • Synchronous operation • Cams Important technical specifications: • Code work memory: 9 MB • Data work memory: 60 MB • Motion Control resources: 15360 • Extended Motion Control resources: 512	Starting from section Program execution (Page 15)
	Scope of the function manual expanded to include CPU 1518TF-4 PN/DP of the S7-1500 automation system	CPU 1518TF-4 PN/DP offers a very large program and data memory for demanding applications in applications that contain distributed I/O in addition to central automation structures. The CPU can also be used for Safety functions according to IEC 61508 up to SIL 3 and ISO 13849 up to PLe for safety applications. CPU 1518TF-4 PN/DP features high-performance, extended Motion Control functions, for example: • Synchronous operation • Cams Important technical specifications: • Code work memory: 9 MB • Data work memory: 60 MB • Motion Control resources: 15360 • Extended Motion Control resources: 512	Starting from section Program execution (Page 15)

What's new in edition 11/2019 as compared to edition 10/2018?

What's new?		What are the customer benefits?	Where can I find information?
Changed contents	Improved visualization of the communication load in the web server	The visualization of the current communication load and its effects on the cycle time helps you to find suitable values for the parameterization of the communication load.	• In section Extension of cycle time due to communication load (Page 37) • In the Web Server (https://support.industry.siemens.com/cs/ww/en/view/59193560) function manual

What's new in edition 10/2018 as compared to edition 09/2016?

What's new?		What are the customer benefits?	Where can I find information?
Changed contents	Scope of the function manual expanded to include CPUs of the S7-1500R/H redundant system	The determination of the cycle and response times of the S7-1500R/H redundant system follows the same principle as for the CPUs of the S7-1500 automation system.	Section Cycle and response times of the S7-1500R/H redundant system (Page 64)

What's new in the 09/2016 edition compared to the 02/2014 edition?

What's new?		What are the customer benefits?	Where can I find information?
Changed contents	Scope of the function manual expanded to include the CPUs of the ET 200SP distributed I/O system and CPU 1516pro-2 PN of the ET 200pro distributed I/O system	Functions that you will be familiar with from the SIMATIC S7-1500 CPUs are implemented in CPUs in other designs (ET 200SP) and in the CPU 1516pro-2 PN (degree of protection IP 65, IP 66 and IP 67).	Starting from section Program execution (Page 15)

Recycling and disposal

For environmentally friendly recycling and disposal of your old equipment, contact a certified electronic waste disposal company and dispose of the equipment according to the applicable regulations in your country.

Security information

Siemens provides products and solutions with industrial security functions that support the secure operation of plants, systems, machines and networks.

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Customers are responsible for preventing unauthorized access to their plants, systems, machines and networks. Such systems, machines and components should only be connected to an enterprise network or the internet if and to the extent such a connection is necessary and only when appropriate security measures (e.g. firewalls and/or network segmentation) are in place.

For additional information on industrial security measures that may be implemented, please visit (https://www.siemens.com/industrialsecurity).

Siemens' products and solutions undergo continuous development to make them more secure. Siemens strongly recommends that product updates are applied as soon as they are available and that the latest product versions are used. Use of product versions that are no longer supported, and failure to apply the latest updates may increase customers' exposure to cyber threats.

To stay informed about product updates, subscribe to the Siemens Industrial Security RSS Feed visit (https://www.siemens.com/industrialsecurity).

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You can find current information on the following topics quickly and easily here:

- **Product support**

  All the information and extensive know-how on your product, technical specifications, FAQs, certificates, downloads, and manuals.

- **Application examples**

  Tools and examples to solve your automation tasks – as well as function blocks, performance information and videos.

- **Services**

  Information about Industry Services, Field Services, Technical Support, spare parts and training offers.

- **Forums**

  For answers and solutions concerning automation technology.

- **mySupport**

  Your personal working area in Industry Online Support for messages, support queries, and configurable documents.

This information is provided by the Siemens Industry Online Support in the Internet (https://support.industry.siemens.com).

Industry Mall

The Industry Mall is the catalog and order system of Siemens AG for automation and drive solutions on the basis of Totally Integrated Automation (TIA) and Totally Integrated Power (TIP).
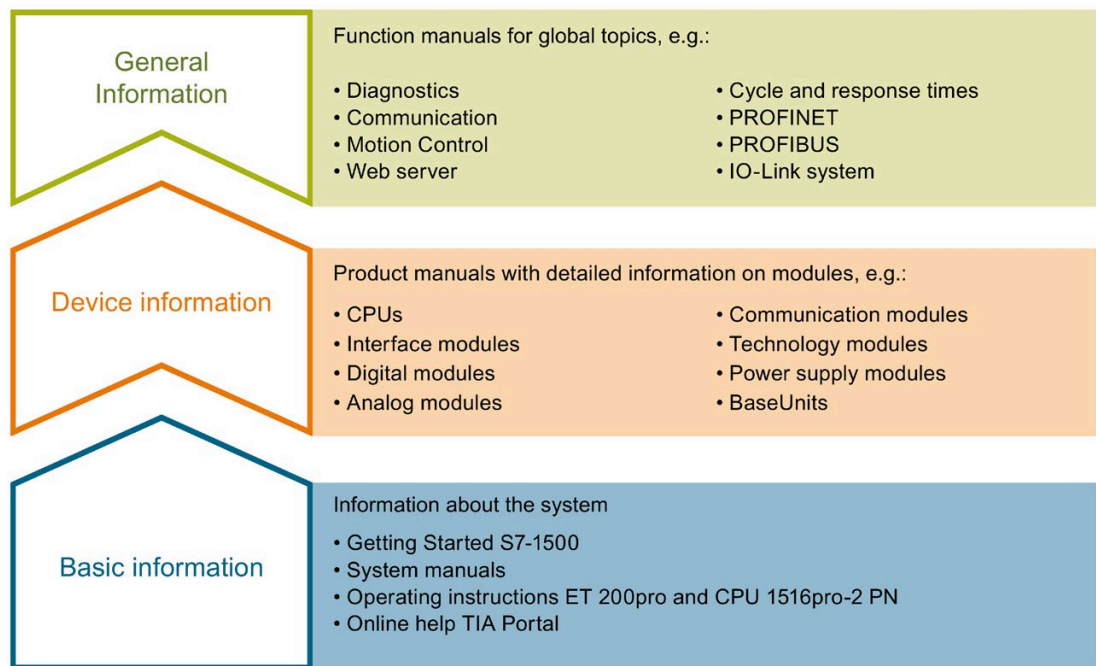
You can find catalogs for all automation and drive products on the Internet (https://mall.industry.siemens.com).

Table of contents

Function manuals Documentation Guide

The documentation for the SIMATIC S7-1500 automation system, the
CPUs 1513/1516pro-2 PN based on SIMATIC S7-1500, and the distributed I/O systems
SIMATIC ET 200MP, ET 200SP and ET 200AL is divided into three areas.
This division allows you easier access to the specific information you require.

General Information

Function manuals for global topics, e.g.:

• Diagnostics
• Communication
• Motion Control
• Web server

• Cycle and response times
• PROFINET
• PROFIBUS
• IO-Link system

Device information

Product manuals with detailed information on modules, e.g.:

• CPUs
• Interface modules
• Digital modules
• Analog modules

• Communication modules
• Technology modules
• Power supply modules
• BaseUnits

Basic information

Information about the system

• Getting Started S7-1500
• System manuals
• Operating instructions ET 200pro and CPU 1516pro-2 PN
• Online help TIA Portal

Basic information

System manuals and Getting Started manuals describe in detail the configuration,
installation, wiring and commissioning of the SIMATIC S7-1500, ET 200MP, ET 200SP and
ET 200AL systems. Use the corresponding operating instructions for the
CPUs 1513/1516pro-2 PN. The STEP 7 online help supports you in the configuration and
programming.

Device information

Product manuals contain a compact description of the module-specific information, such as
properties, terminal diagrams, characteristics and technical specifications.

General information

The function manuals contain detailed descriptions on general topics such as diagnostics, communication, Motion Control, Web server, OPC UA.

You can download the documentation free of charge from the Internet (https://support.industry.siemens.com/cs/ww/en/view/109742705).

Changes and additions to the manuals are documented in product information sheets.

You will find the product information on the Internet:

- S7-1500/ET 200MP (https://support.industry.siemens.com/cs/us/en/view/68052815)

- ET 200SP (https://support.industry.siemens.com/cs/us/en/view/73021864)

Manual Collections

The Manual Collections contain the complete documentation of the systems put together in one file.

You will find the Manual Collections on the Internet:

- S7-1500/ET 200MP (https://support.industry.siemens.com/cs/ww/en/view/86140384)

- ET 200SP (https://support.industry.siemens.com/cs/ww/en/view/84133942)

- ET 200AL (https://support.industry.siemens.com/cs/ww/en/view/95242965)

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With "mySupport", your personal workspace, you make the best out of your Industry Online Support.

In "mySupport", you can save filters, favorites and tags, request CAx data and compile your personal library in the Documentation area. In addition, your data is already filled out in support requests and you can get an overview of your current requests at any time.

You must register once to use the full functionality of "mySupport".

You can find "mySupport" on the Internet (https://support.industry.siemens.com/My/ww/en).

"mySupport" - Documentation

With "mySupport", your personal workspace, you make the best out of your Industry Online Support.

In "mySupport", you can save filters, favorites and tags, request CAx data and compile your personal library in the Documentation area. In addition, your data is already filled out in support requests and you can get an overview of your current requests at any time.

You must register once to use the full functionality of "mySupport".

You can find "mySupport" on the Internet (https://support.industry.siemens.com/My/ww/en/documentation).

"mySupport" - CAx data

In the CAx data area of "mySupport", you can access the latest product data for your CAx or CAe system.

You configure your own download package with a few clicks.

In doing so you can select:

• Product images, 2D dimension drawings, 3D models, internal circuit diagrams, EPLAN macro files

• Manuals, characteristics, operating manuals, certificates

• Product master data

You can find "mySupport" - CAx data on the Internet (https://support.industry.siemens.com/my/ww/en/CAxOnline).

Application examples

The application examples support you with various tools and examples for solving your automation tasks. Solutions are shown in interplay with multiple components in the system - separated from the focus on individual products.

You will find the application examples on the Internet (https://support.industry.siemens.com/cs/ww/en/ps/ae).

TIA Selection Tool

With the TIA Selection Tool, you can select, configure and order devices for Totally Integrated Automation (TIA).
This tool is the successor of the SIMATIC Selection Tool and combines the known configurators for automation technology into one tool.
With the TIA Selection Tool, you can generate a complete order list from your product selection or product configuration.

You can find the TIA Selection Tool on the Internet (https://support.industry.siemens.com/cs/ww/en/view/109767888).

SIMATIC Automation Tool

You can use the SIMATIC Automation Tool to perform commissioning and maintenance activities simultaneously on various SIMATIC S7 stations as a bulk operation independent of TIA Portal.

The SIMATIC Automation Tool provides a multitude of functions:

- Scanning of a PROFINET/Ethernet system network and identification of all connected CPUs
- Address assignment (IP, subnet, gateway) and station name (PROFINET device) to a CPU
- Transfer of the date and the programming device/PC time converted to UTC time to the module
- Program download to CPU
- RUN/STOP mode switchover
- CPU localization by means of LED flashing
- Reading out of CPU error information
- Reading of the CPU diagnostics buffer
- Reset to factory settings
- Firmware update of the CPU and connected modules

You can find the SIMATIC Automation Tool on the Internet (https://support.industry.siemens.com/cs/ww/en/view/98161300).

PRONETA

SIEMENS PRONETA (PROFINET network analysis) allows you to analyze the plant network during commissioning. PRONETA features two core functions:

- The topology overview automatically scans the PROFINET and all connected components.
- The IO check is a fast test of the wiring and the module configuration of a plant.

You can find SIEMENS PRONETA on the Internet (https://support.industry.siemens.com/cs/ww/en/view/67460624).

SINETPLAN

SINETPLAN, the Siemens Network Planner, supports you in planning automation systems and networks based on PROFINET. The tool facilitates professional and predictive dimensioning of your PROFINET installation as early as in the planning stage. In addition, SINETPLAN supports you during network optimization and helps you to exploit network resources optimally and to plan reserves. This helps to prevent problems in commissioning or failures during productive operation even in advance of a planned operation. This increases the availability of the production plant and helps improve operational safety.

The advantages at a glance

- Network optimization thanks to port-specific calculation of the network load

- Increased production availability thanks to online scan and verification of existing systems

- Transparency before commissioning through importing and simulation of existing STEP 7 projects

- Efficiency through securing existing investments in the long term and the optimal use of resources

You can find SINETPLAN on the Internet (https://www.siemens.com/sinetplan).

Program execution

2

2.1 Principle of operation

Introduction

You often program your user program with a program cycle OB, usually in OB 1. With complex applications, it is often necessary to comply with short response times required by the application. You can often meet the response time requirements by splitting the user program up into several parts with different response time requirements. The CPU offers a number of different OB types for this purpose, the properties (priority, frequency, etc.) of which can be adapted to meet your requirements.

Program organization

You can choose from the following types of program execution for running your user program:

Program execution in the cyclic program of the CPU:

The CPU executes the user program cyclically. When the execution has reached the end of a cycle, the program execution starts again in the next cycle. In the simplest case, you execute the entire user program in the cyclic program of the CPU. All tasks in the user program are then processed with equal rank. This also results in the same response times for all tasks.

In addition to program execution in the cyclic program, there is time-driven and event-driven program execution.

Time-driven execution:

In a complex user program, there are frequently portions with different response time requirements. You can optimize the response times by taking advantage of these differences in the requirements. To do so, you can break down the program parts with higher response time requirements into higher-priority OBs with shorter cycles, for example cyclic interrupt OBs.

The execution of these parts can thus occur at different frequencies and with different priorities.

Event-driven execution:

Depending on the I/O modules used, you can configure hardware interrupts for specific process events (such as an edge change of a digital input) that result in the call of the assigned hardware interrupt OB. The hardware interrupts have a higher priority and interrupt the cyclic program of the CPU. You can achieve very short response times in the CPU with hardware interrupts by directly triggering program execution.

Keep in mind that the time characteristics of your application becomes less predictable with intense use of hardware interrupts. The reason for this is that the time at which the triggering events occur can result in drastically different response times.

Tip: Use hardware interrupts only for a few selected events.

Special consideration for hardware interrupts: If you have assigned an OB to an event (hardware interrupt), the OB then has the priority of the event.

Using process image partitions

If you have distributed a program over various OBs, for example, due to different response time requirements, it is advisable and often necessary to assign the update of the used I/O data directly to these OBs. You can use process image partitions for this purpose.

You group the input and output data in a process image partition according to their use in the program and assign the data to the OB.

A process image partition of the inputs (PIPI) permits the associated input data for an OB program to be updated immediately before the OB program starts.

A process image partition of the outputs (PIPQ) permits the output data associated with an OB program to become effective on the outputs immediately after the OB program runs.

You have 32 (0 ... 31) process image partitions at your disposal. The I/O is assigned to the process image partition 0 by default (setting: "Automatic update"). Process image partition 0 is permanently assigned to cyclic execution.

You have to configure the "system-side update of process image partitions". You can find additional information on configuration of process image partitions in the online help for STEP 7 under the keyword "Assign process image/process image partition".

Interruptibility of program execution

Each organization block is processed according to the priority it has been assigned. You can adapt the priority according to the response time requirements for most organization blocks.

All program cycle OBs always have the lowest priority of 1. The highest priority is 26.

Communication tasks always have priority 15. If necessary, you can change the priority of your blocks and select a higher priority than the communication.

Organization blocks or system activities with higher priority interrupt organization blocks or system activities with lower priority. Organization blocks or system activities with higher priority interrupt thus extend the runtime of the interrupted organization blocks or system activities. If two pending tasks have the same priority, these tasks are processed in the order in which the relevant start events occurred.

Note

Higher priority OBs

Communication functionality is strongly influenced by too many and/or runtime-intensive OBs with a priority > 15.

When using OBs with a priority ≥ 15, you should therefore consider the runtime load that they cause.

Reference

You can find additional information on the subject of "priorities" in the "Events and OBs" section of the following manuals:

- S7-1500 automation system
  (https://support.industry.siemens.com/cs/ww/en/view/59191792) system manual

- S7-1500R/H redundant system
  (https://support.industry.siemens.com/cs/ww/en/view/109754833) system manual

- ET 200SP distributed I/O system
  (https://support.industry.siemens.com/cs/ww/en/view/58649293) system manual

- Operating instructions CPU 1513pro-2 PN
  (https://support.industry.siemens.com/cs/ww/en/view/109769507) and CPU 1516pro-2 PN
  (https://support.industry.siemens.com/cs/ww/en/view/109482416)

You can find additional information on organization blocks and their priorities for Motion Control on the Internet (https://support.industry.siemens.com/cs/ww/en/view/109751049).

2.2 Overload behavior

CPU overload behavior

An occurring event triggers the execution of the associated OB. Depending on the OB priority and the current processor load, a time delay may occur before the OB is executed when there is an overload. The same event can therefore occur once or several times before the user program processes the OB belonging to the preceding event. The CPU handles such a situation as follows: The operating system queues the events in the queue associated with their priority in the order of their occurrence. The CPU then takes the oldest event for the highest priority and processes the associated OB. After the OB has been processed, the CPU processes the OB for the next event.

To control temporary overload situations, you can limit the number of queued events that originate from the same source. The next event is discarded as soon as the maximum number of pending triggers of a specific cyclic interrupt OB, for example, is reached.

Overload occurs when similar events occur faster than the CPU can process these events. Similar events are events from a single source, such as start events for a specific cyclic interrupt OB.

Configuration of the overload response

In the properties of an organization block in which an overload can occur, you can select the response to overload under "Attributes" and "Event queuing".
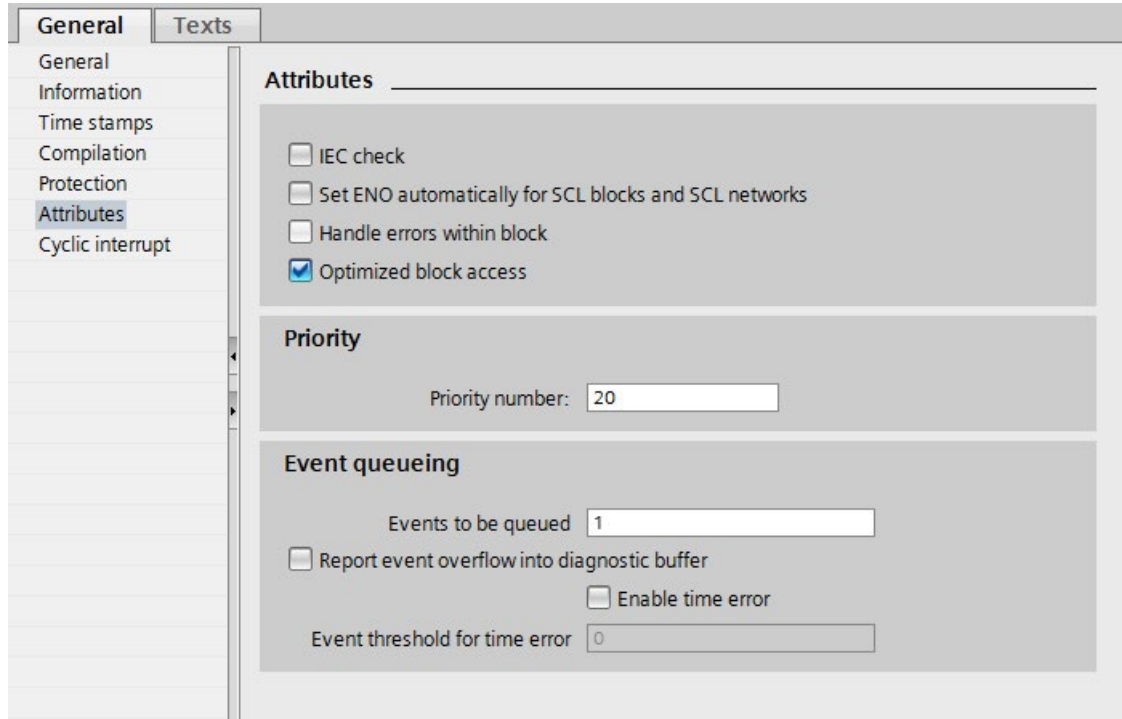

Figure 2-1   Configuration of the overload response in the block properties

Events to be queued

The OB parameter "Events to be queued" is used to specify how many similar events the operating system places in the associated queue and therefore post-processes. If this parameter has the value 1, for example, exactly one event is stored temporarily.

If the maximum number of similar start events is reached in the queue, each additional start event is only counted and subsequently discarded. During the next scheduled processing of the event, the CPU provides the number of discarded start events in the "Event_Count" input parameter (in the start information). You can then react appropriately to the overload situation. The CPU then resets the counter for lost events to zero.

Note

Post-processing of cyclic events is often not desirable, as this can lead to an overload with OBs of the same or lower priority. Therefore, it is generally advantageous to discard similar events and to react to the overload situation during the next scheduled OB processing. A low value of the "Events to be queued" parameter mitigates an overload situation.

To ensure that the CPU processes the OB of at least one queued event, the minimum number of events to be queued is "1". The maximum number of events that can be queued is "12".

Report event overflow into diagnostic buffer

If the CPU first discards a start event of a cyclic interrupt OB, for example, its further behavior depends on the OB parameter "Report event overflow into diagnostic buffer". If you have selected the check box, the CPU enters the event in the diagnostic buffer for the overload situation at this event source. If an overload situation occurs again (overflow counter changes from 0 to 1), another diagnostic buffer entry is made at the next OB end.

Enable time error

The cyclic interrupt OB parameter "Enable time error" is used to specify whether the CPU is to call a time error OB when a specific overload level is reached for similar events. You use the OB parameter "Enable time error" to program a reaction to an overload before the limit for similar events is reached. The reaction occurs before the CPU discards similar events.

By default, the "Enable time error" parameter is not set.

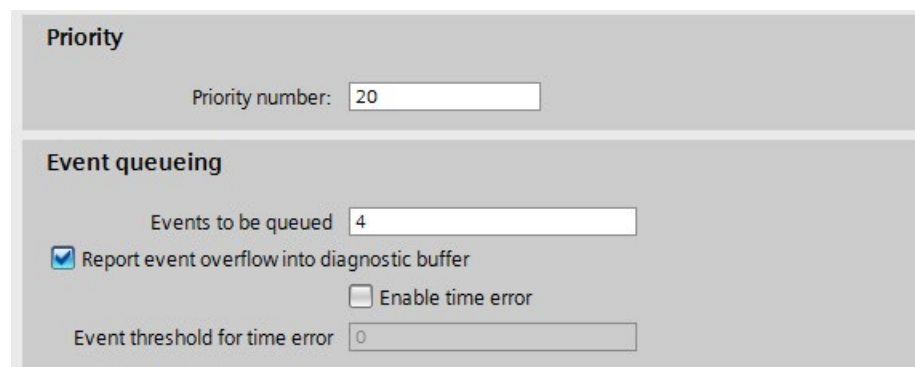### Event threshold for time error

Select the "Enable time error" check box to enable the "Event threshold for time error" OB parameter. You use the "Event threshold for time error" OB parameter to specify how many similar events in the queue are permitted before the CPU calls a time error OB.

The following value range applies to the "Event threshold for time error" parameter:

1 ≤ "Event threshold for time error" ≤ "Events to be queued".

Example 1

The following example shows the response of the CPU when multiple similar events occur faster than the CPU can process the associated OBs. In example 1, the user selected the following parameter assignment:

Figure 2-2   Example of parameter assignment for the overload behavior

The figure below shows the processing sequence as soon as an event calls an associated OB.
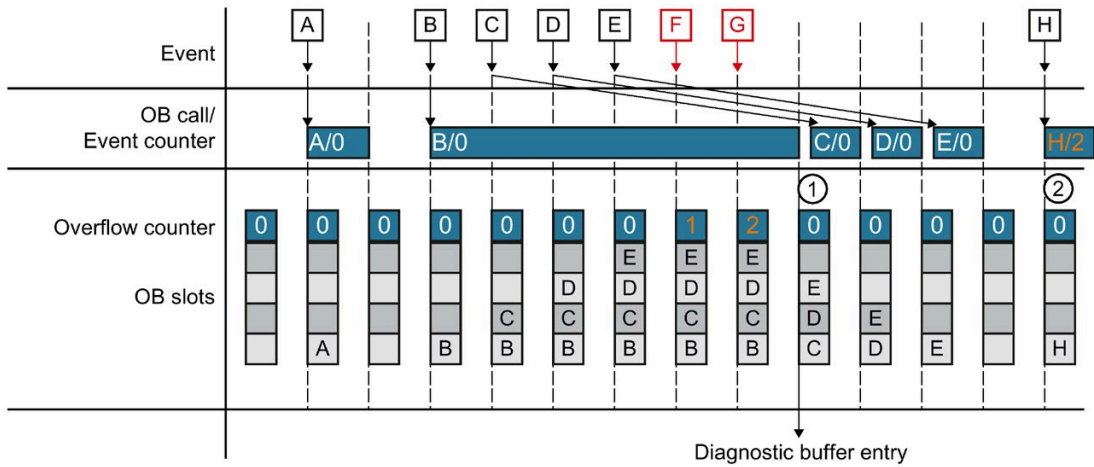

Figure 2-3   Example 1

As soon as an occurring event calls an OB, the event occupies a slot of the OB. The occupied slot is free again as soon as the CPU has processed the event. If the CPU has not completed processing the OB of an occurring event, additional occurring events each occupy an additional slot of the OB during this time. As soon as this number exceeds the configured number of events to be queued, these events are discarded and counted by the overflow counter. When an OB which takes a long time to run is completed, the CPU creates an entry in the diagnostic buffer and sets the overflow counter to zero (①). After the CPU has processed this long-running OB, the CPU then processes the OBs of the events that are queued one after the other. At the next new occurring event, the CPU writes the previous value of the reset overflow counter to the start information of the OB. The CPU then processes the OB (②).

Example 2

In example 2, the user has selected the following parameter assignment:

Figure 2-4   Example of parameter assignment for the overload behavior

Contrary to example 1, the CPU in example 2 requests a time error as soon as the configured event threshold has been exceeded. An additional time error can then only occur if all slots of the OB have been free once in the meantime.
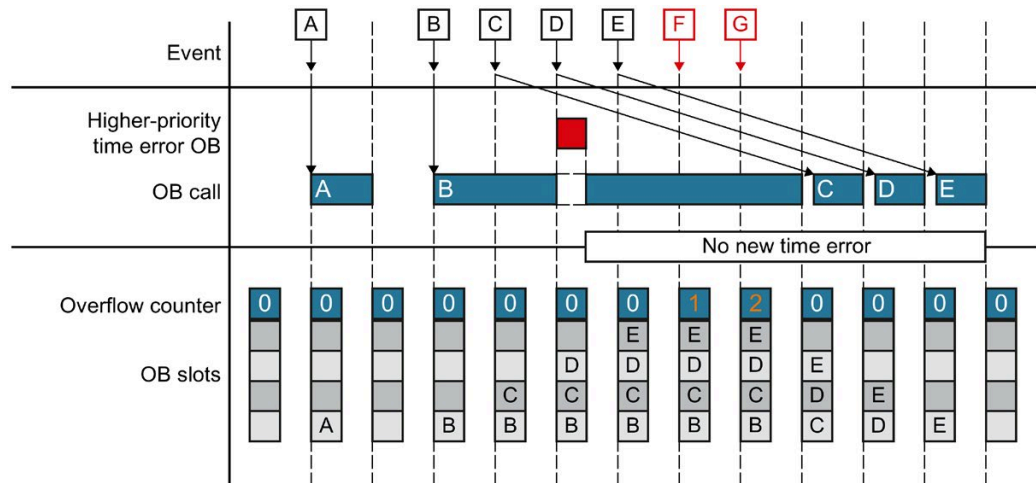

Figure 2-5   Example 2

Cyclic program execution

3

Validity

The statements of the section "Cyclic program execution" apply to the CPU components of the following systems:

- S7-1500 automation system

- ET 200MP and ET 200SP distributed I/O systems

- The CPUs of the ET 200pro distributed I/O system based on SIMATIC S7-1500

- S7-1500R/H redundant system (in RUN-Solo system state)
  In RUN-Redundant system state, the statements of section **"**Cycle and response times of the S7-1500R/H redundant system (Page 64)" apply.

Restrictions

With the S7-1500R/H redundant system, there are restrictions compared to the S7-1500 automation system. The S7-1500R/H redundant system does not support all hardware properties and firmware functions of the S7-1500 automation system (for example, it does not support PROFIBUS DP, central I/O, web server, etc.).

The restrictions are described in the S7-1500R/H redundant system (https://support.industry.siemens.com/cs/ww/en/view/109754833) system manual.

3.1   Cycle

Definition of cycle

A cycle includes the following sections:

- Automatic update of process image partition 0 of the outputs (PIPQ 0)
- Automatic update of process image partition 0 of the inputs (PIPI 0)
- Execution of the cyclic program

The process image partition 0 is automatically updated in the cycle. You assign the I/O addresses to these process image partitions (PIPI 0/PIPQ 0) when you configure the I/O modules via the "Automatic update" setting (default).
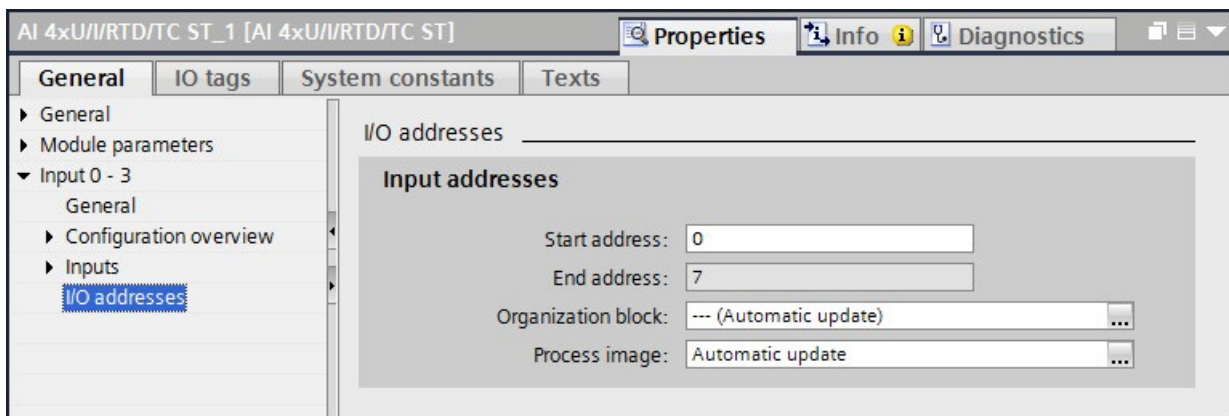
Figure 3-1   Assigning I/O addresses to process image partitions

The figure below illustrates the phases that are passed through during a cycle. In the example below the user has configured a minimum cycle time. Updating of the process image partitions and processing of the cyclic program is completed before the end of the configured minimum cycle time. Therefore, the CPU waits until the configured minimum cycle time has expired before the next program cycle starts.
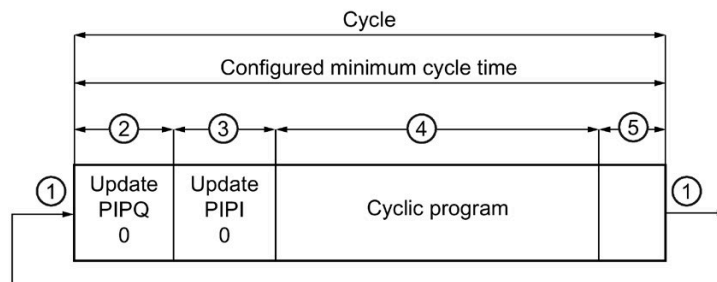
①   Cycle control point at which the operating system starts measurement of the cycle time.

②   The CPU writes the states from the process image output to the output modules.

③   The CPU reads the status of the inputs at the input modules and writes the input data to the process image input.

④   The CPU processes the user program and executes the instructions specified in the program.

⑤   Wait phase until end of configured minimum cycle time

Figure 3-2   Cycle

Cycle control point

When the cycle control point is reached, the CPU has completed the cycle program and is no longer executing OBs. All user data are consistent at this time. The requirement is that no communication that modifies user data (such as HMI communication or PUT/GET communication) is active.

The cycle control point marks:

- The end of a cycle and its cycle time statistics

- The start of the next cycle and its cycle time statistics

- The restart of the monitoring of the configured maximum cycle time
  (time-out counter is reset)

The cycle control point is reached depending on which of the following events occurred last:

- End of the last program cycle OB

- Expiry of the minimum cycle time (if configured)

After the cycle control point has been reached, the CPU executes the following steps:

1. Writes the process image outputs to the output modules

2. Reads in the status of the inputs from the input modules into the process image input

3. Executes the first program cycle OB

3.2 Cycle time

Definition of cycle time

The cycle time is the time the CPU needs for:

- Updating the process image inputs/outputs

- Executing the cyclic program

- All program parts and system activities interrupting this cycle

- Waiting for the minimum cycle time (if it is parameterized and is longer than the program execution time)

3.2.1 Different cycle times

Introduction

The cycle time (T_{cyc}) is not the same in each cycle because the processing times may vary. Causes of this include:

- For example, different program runtimes:

  - Program loops

  - Conditional commands

  - Conditional block calls

  - Different program paths

- Lengthening due to interruptions, for example:

  - Time-driven interrupt processing

  - Event-driven interrupt processing

  - Communication

Causes of different cycle times

The figure below shows the different cycle times T_{cyc1} and T_{cyc2} using an example.

Because the cyclic program is interrupted by a cyclic interrupt OB in this example (for example: OB 30), the cycle time T_{cyc2} is greater than T_{cyc1}. The cyclic interrupt OB in turn is interrupted by Motion Control functions and communication.
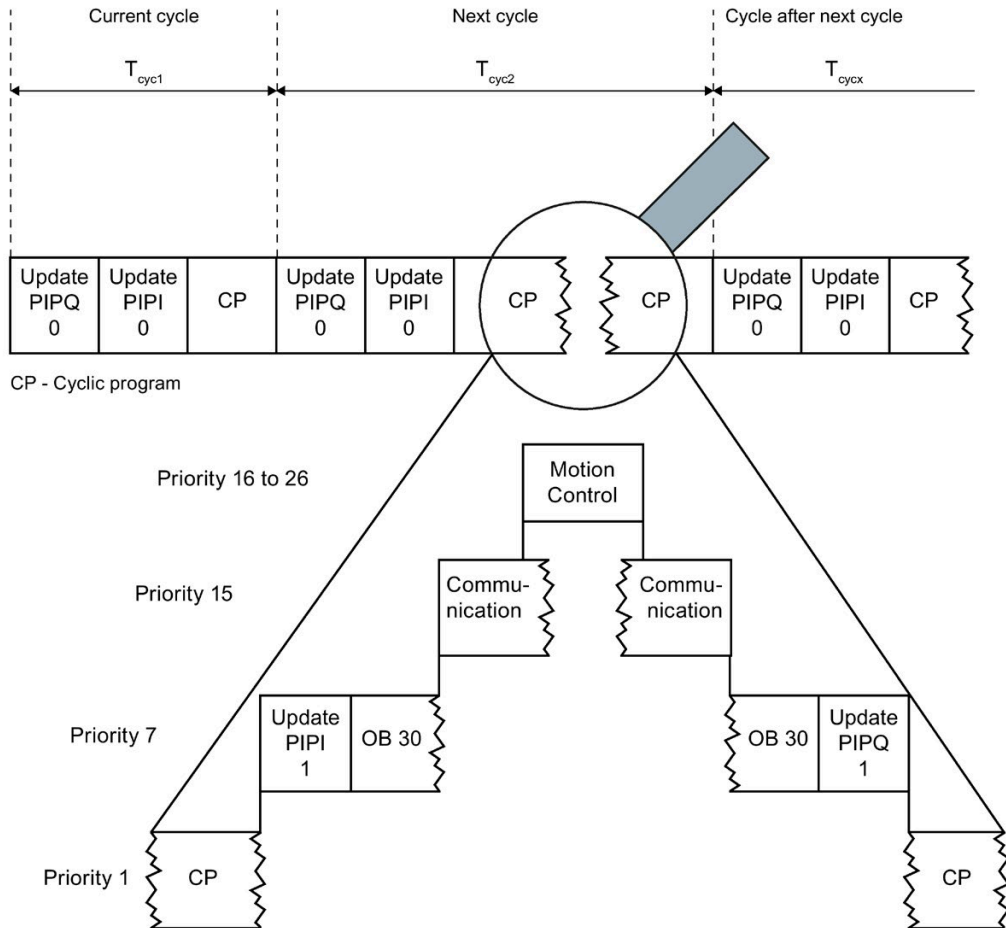
Figure 3-3   Possible causes of differing cycle times

Minimum cycle time

In STEP 7, you can set a minimum cycle time for a CPU. The default setting for the minimum cycle time of the non-redundant CPUs is one millisecond. It is advisable to increase this setting in the following cases:

- To reduce the cycle time's fluctuation range.

- To make remaining computing time available for communication tasks. The CPU then processes these communication tasks until the minimum cycle time has expired. Making the remaining computing time available to communication tasks offers the following advantages:

  – Longer minimum cycle times prevent that process images are updated unnecessarily often and thus lead to less load on the backplane bus.

  – Longer minimum cycle times result in an increase in communication performance.

Maximum cycle time

The maximum cycle time is a configurable upper limit of the cyclic program runtime. The task of the maximum cycle time is to monitor the response time required for the respective process.

The maximum cycle time of non-redundant CPUs is set to 150 ms by default. You can set this value from 1 ms to 6000 ms when assigning parameters to the CPU. When the time of the cycle currently being processed is longer than the maximum cycle time, the time error OB (OB 80) is called. You specify how the CPU responds to the time error with the user program in OB 80.

The following table shows the response of the CPU to the cycle time being exceeded with and without a configured OB 80:

Table 3- 1   Response of the CPU to cycle time being exceeded

Number of times cycle time is exceeded ⇒	Operating mode
First time cycle time is exceeded without OB 80 ⇒	STOP
First time cycle time is exceeded with OB 80 ⇒	RUN
Second time cycle time is exceeded with OB 80 ⇒	STOP

For the behavior of the R/H CPUs in the event of cycle time overruns, refer to the section Maximum cycle time and time errors (Page 65).

Cycle time statistics

You can read the cycle time statistics either directly from STEP 7 ("Online tools" task card) or with the "RT_INFO" instruction.

You can use the "RT_INFO" instruction to generate statistics in STEP 7 on the runtime of specific organization blocks for communication or for the user program. For example, this includes

- The shortest and longest cycle time

- The portions of runtime used for communication and the user program

---

Note

Showing the cycle time statistics on the display and Web server

With the S7-1500 CPUs, you also have the option of calling the cycle time statistics via the display of the CPU. As of firmware version 2.0 of the CPUs, the cycle time statistics are also displayed in the Web server.

To view the cycle time statistics directly in STEP 7, follow these steps:

1. Establish an online connection to the CPU with STEP 7.

2. Select the "Online tools" task card.

Result: The diagram of the cycle time statistics is displayed in the cycle time section.

The following figure shows an extract from STEP 7 with the cycle time statistics. In this example, the cycle time fluctuates between 7 ms and 12 ms. The current cycle time is 10 ms. The maximum cycle time in this example is set to 40 ms.
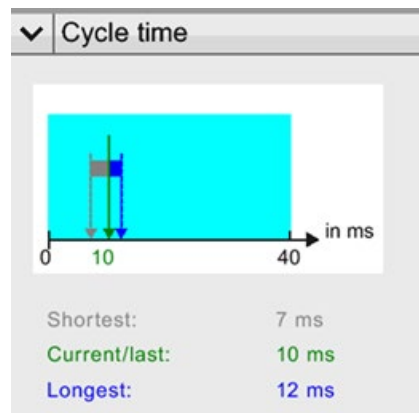
Figure 3-4   Cycle time statistics

You can find additional information on the runtime characteristics of the CPU with the "RT_INFO" instruction in the user program. The instruction includes information about:

- The utilization of the CPU by the user program and communication in percentage

- The runtimes of the individual OBs

Reference

Additional information on the "RT_INFO" instruction is available in the STEP 7 online help.

3.2.2 Influences on the cycle time

3.2.2.1 Update time for process image partitions

Estimating update time for process image partitions

The update time of the process image partitions depends on the volume of assigned central and distributed I/O module data.

You can estimate the update time using the following formula:

Base load for process image update
+   Number of words in the process image x copy time for central I/O
+   Number of words in the process image via DP x copy time for PROFIBUS I/O
+   Number of words in the process image via PROFINET x copy time for PROFINET I/O

= Update time of the process image partition

Update times of the process image partitions

The following table contains the times for estimating the typical update times of the process image partitions.

Table 3- 2   Data for estimating the typical update time of the process image partitions

Components	Update times of the CPUs			
	S7-1500			
	1511(F)-1 PN 1511T(F)-1 PN 1511C-1 PN 1512C-1 PN 1513(F)-1 PN	1515(F)-2 PN 1515T(F)-2 PN 1516(F)-3 PN/DP 1516T(F)-3 PN/DP	1517(F)-3 PN/DP 1517T(F)-3 PN/DP	1518(F)-4 PN/DP 1518(F)-4 PN/DP MFP 1518T(F)-4 PN/DP
Basic load for updating process image partitions	35 µs	30 µs	7 µs	5 µs
Copy time for central I/O	9 µs/word	8 µs/word	5 µs/word	4 µs/word
Copy time for distributed I/O via PROFIBUS	0.5 µs/word	0.5 µs/word	0.4 µs/word	0.3 µs/word
Copy time for distributed I/O via PROFINET	0.5 µs/word	0.5 µs/word	0.4 µs/word	0.3 µs/word

Components	Update time of the CPU in RUN-Solo system state		
	S7-1500R/H*		
	1513R-1 PN	1515R-2 PN	1517H-3 PN 1518HF-4 PN
Basic load for updating process image partitions	35 µs	30 µs	7 µs
Copy time for distributed I/O via PROFINET	0.5 µs/word	0.5 µs/word	0.4 µs/word

* Additional information about cycle and response times of R/H CPUs is available in the section "Cycle and response times of the S7-1500R/H redundant system"

Components	Update time of the CPU		
	ET 200SP		
	1510SP(F)-1 PN	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Basic load for updating process image partitions	60 µs	60 µs	30 µs
Copy time for central I/O	0.5 µs/word	0.5 µs/word	0.5 µs/word
Copy time for distributed I/O via PROFIBUS	0.5 µs/word	0.5 µs/word	0.5 µs/word
Copy time for distributed I/O via PROFINET	0.5 µs/word	0.5 µs/word	0.5 µs/word

Note

Update time of the backplane bus for ET 200SP CPUs

For the update time of the ET 200SP CPUs, observe also the information in table "Update time of the ET 200SP CPUs" of the section Response time for cyclic and time-driven program execution (Page 54).

Components	Update time of the CPU	
	ET 200pro	
	1513pro(F)-2 PN	**1516pro(F)-2 PN**
Basic load for updating process image partitions	35 µs	30 µs
Copy time for central I/O	140 µs/word	120 µs/word
Copy time for distributed I/O via PROFIBUS	0.5 µs/word	0.5 µs/word
Copy time for distributed I/O via PROFINET	0.5 µs/word	0.5 µs/word

3.2.2.2 User program execution time

Introduction

Organization blocks or system activities with higher priority interrupt organization blocks or system activities with lower priority, and thus extend their runtime.

Program execution time without interruptions

The user program has a certain runtime without interruptions. The runtime depends on the number of operations that are executed in the user program.

The following table contains the typical durations of operations.

Table 3- 3   Duration of an operation

	S7-1500						
	1511(F)-1 P N 1511T(F)-1 P N 1511C-1 PN	1512C-1 P N	1513(F)-1 P N	1515(F)-2 P N 1515T(F)-2 P N	1516(F)-3 P N/DP 1516T(F)-3 P N/DP	1517(F)-3 P N/DP 1517T(F)-3 P N/DP	1518(F)-4 P N/DP 1518(F)-4 P N/DP MFP 1518T(F)-4 PN/DP
Bit operations, typ.	60 ns	48 ns	40 ns	30 ns	10 ns	2 ns	1 ns
Word operations, typ.	72 ns	58 ns	48 ns	36 ns	12 ns	3 ns	2 ns
Fixed-point arithmetic, typ.	96 ns	77 ns	64 ns	48 ns	16 ns	3 ns	2 ns
Floating-point arithmetic, typ.	384 ns	307 ns	256 ns	192 ns	64 ns	12 ns	6 ns

	S7-1500R/H* in RUN-Solo system state		
	1513R-1 PN	1515R-2 PN	1517H-3 PN 1518HF-4 PN
Bit operations, typ.	40 ns	30 ns	2 ns
Word operations, typ.	48 ns	36 ns	3 ns
Fixed-point arithmetic, typ.	64 ns	48 ns	3 ns
Floating-point arithmetic, typ.	256 ns	192 ns	12 ns

* Additional information about cycle and response times of R/H CPUs is available in the section "Cycle and response times of the S7-1500R/H redundant system"

	ET 200SP		
	1510SP(F)-1 PN	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Bit operations, typ.	72 ns	48 ns	30 ns
Word operations, typ.	86 ns	58 ns	36 ns
Fixed-point arithmetic, typ.	115 ns	77 ns	48 ns
Floating-point arithmetic, typ.	461 ns	307 ns	192 ns

	ET 200pro	
	1513pro(F)-2 PN	**1516pro(F)-2 PN**
Bit operations, typ.	40 ns	10 ns
Word operations, typ.	48 ns	12 ns
Fixed-point arithmetic, typ.	64 ns	16 ns
Floating-point arithmetic, typ.	256 ns	64 ns

Note

Instruction "RUNTIME"

Please note that the times specified in the tables are typical values. There can therefore be user programs that deviate from the specified typical values.

Make sure to check the runtime of critical program sequences beforehand with the "RUNTIME" instruction.

Extension due to nesting of higher-priority OBs and/or interrupts

The interruption of a user program by a higher-priority OB causes a certain basic time expenditure. Take account of this basic time expenditure in addition to the update time of the assigned process image partitions and the execution time of the contained user program. The following tables contain the typical times for the various interrupts and error events.

Table 3- 4   Basic time expenditure for an interrupt

	S7-1500			
	1511(F)-1 PN 1511T(F)-1 PN 1511C-1 PN 1512C-1 PN 1513(F)-1 PN	1515(F)-2 PN 1515T(F)-2 PN 1516(F)-3 PN/DP 1516T(F)-3 PN/DP	1517(F)-3 PN/DP 1517T(F)-3 PN/DP	1518(F)-4 PN/DP 1518(F)-4 PN/DP MFP 1518T(F)-4 PN/DP
Hardware interrupt	90 µs	80 µs	20 µs	12 µs
Time-of-day interrupt	90 µs	80 µs	20 µs	12 µs
Time-delay interrupt	90 µs	80 µs	20 µs	12 µs
Cyclic interrupt	90 µs	80 µs	20 µs	12 µs

	S7-1500R/H* in RUN-Solo system state		
	1513R-1 PN	1515R-2 PN	1517H-3 PN 1518HF-4 PN
Hardware interrupt	170 µs	140 µs	20 µs
Time-of-day interrupt	170 µs	140 µs	20 µs
Time-delay interrupt	170 µs	140 µs	20 µs
Cyclic interrupt	170 µs	140 µs	20 µs

* Additional information about cycle and response times of R/H CPUs is available in the section "Cycle and response times of the S7-1500R/H redundant system"

	ET 200SP		
	1510SP(F)-1 PN	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Hardware interrupt	90 µs	90 µs	80 µs
Time-of-day interrupt	90 µs	90 µs	80 µs
Time-delay interrupt	90 µs	90 µs	80 µs
Cyclic interrupt	90 µs	90 µs	80 µs

	ET 200pro	
	1513pro(F)-2 PN	**1516pro(F)-2 PN**
Hardware interrupt	90 µs	80 µs
Time-of-day interrupt	90 µs	80 µs
Time-delay interrupt	90 µs	80 µs
Cyclic interrupt	90 µs	80 µs

Table 3- 5   Basic time expenditure for an error OB

	S7-1500			
	1511(F)-1 PN **1511T(F)-1 PN** **1511C-1 PN** **1512C-1 PN** **1513(F)-1 PN**	**1515(F)-2 PN** **1515T(F)-2 PN** **1516(F)-3 PN/DP** **1516T(F)-3 PN/DP**	**1517(F)-3 PN/DP** **1517T(F)-3 PN/DP**	**1518(F)-4 PN/DP** **1518(F)-4 PN/DP MFP** **1518T(F)-4 PN/DP**
Programming error	90 µs	80 µs	20 µs	12 µs
I/O access error	90 µs	80 µs	20 µs	12 µs
Time error	90 µs	80 µs	20 µs	12 µs
Diagnostic interrupt	90 µs	80 µs	20 µs	12 µs
Module failure/recovery	90 µs	80 µs	20 µs	12 µs
Station failure/recovery	90 µs	80 µs	20 µs	12 µs

	S7-1500R/H* in RUN-Solo system state		
	1513R-1 PN	**1515R-2 PN**	**1517H-3 PN** **1518HF-4 PN**
Programming error	170 µs	140 µs	20 µs
I/O access error	170 µs	140 µs	20 µs
Time error	170 µs	140 µs	20 µs
Diagnostic interrupt	170 µs	140 µs	20 µs
Module failure/recovery	170 µs	140 µs	20 µs
Station failure/recovery	170 µs	140 µs	20 µs

* Additional information about cycle and response times of R/H CPUs is available in the section "Cycle and response times of the S7-1500R/H redundant system"

	ET 200SP		
	1510SP(F)-1 PN	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Programming error	90 µs	90 µs	80 µs
I/O access error	90 µs	90 µs	80 µs
Time error	90 µs	90 µs	80 µs
Diagnostic interrupt	90 µs	90 µs	80 µs
Module failure/recovery	90 µs	90 µs	80 µs
Station failure/recovery	90 µs	90 µs	80 µs

CPU	ET 200pro	
	1513pro(F)-2 PN	**1516pro(F)-2 PN**
Programming error	90 µs	80 µs
I/O access error	90 µs	80 µs
Time error	90 µs	80 µs
Diagnostic interrupt	90 µs	80 µs
Module failure/recovery	90 µs	80 µs
Station failure/recovery	90 µs	80 µs

Reference

You can find additional information on the topic of error handling in the Events and OBs section of the

- S7-1500 automation system (http://support.automation.siemens.com/WW/view/en/59191792) system manual

- S7-1500R/H redundant system (https://support.industry.siemens.com/cs/ww/en/view/109754833) system manual

- ET 200SP distributed I/O system (http://support.automation.siemens.com/WW/view/en/58649293) system manual

- In the CPU 1513pro-2 PN (https://support.industry.siemens.com/cs/ww/en/view/109769507) and CPU 1516pro-2 PN (https://support.industry.siemens.com/cs/ww/en/view/109482416) operating instructions, each in the Events and OBs chapter

You can find additional information on the topic of the complete cycle time of a program in an FAQ on the Internet (https://support.industry.siemens.com/cs/ww/en/view/87668055).

3.2.2.3 Extension of cycle time due to communication load

Impact of communication on the cycle time

In the sequence model of the CPU, communication tasks are processed with priority 15. All program parts with priority > 15 (e.g. for Motion Control functions) are unaffected by communication.

Configured communication load

The CPU operating system provides the maximum specified percentage of total CPU processing power for communication tasks. The communication load can be set in STEP 7 for the CPUs of the S7 series. The default value when creating a CPU depends on the type and version of CPU used. If the processing power is not needed for communication, then the processing power is available to the operating system and the user program.

Communication is allocated the requisite computing time in 1 ms increments, with priority 15. At 50% communication load, 500 µs of each 1 millisecond are used for communication.

The following formula may be used to estimate the extension of the cycle time by communication.

$$\text{Actual cycle time} = \frac{\text{Cycle time without communication}}{} \times \frac{100}{100 - \text{"configured communication load in \%"}}$$

Figure 3-5   Formula: Impact of communication load

With a complete use of the communication load of 50% (default), the following value results:

$$\text{Actual cycle time} = \text{Cycle time without communication} \times 2$$

Figure 3-6   Extension of cycle time due to communication load

The actual cycle time is up to twice as long as the cycle time without communication when you use the default communication load.

Dependency of maximum cycle time on the configured communication load

The chart shows the nonlinear relationship between maximum cycle time and configured communication load with a cycle time without communication of 10 ms. In the example, there are no OBs with a priority > 1.
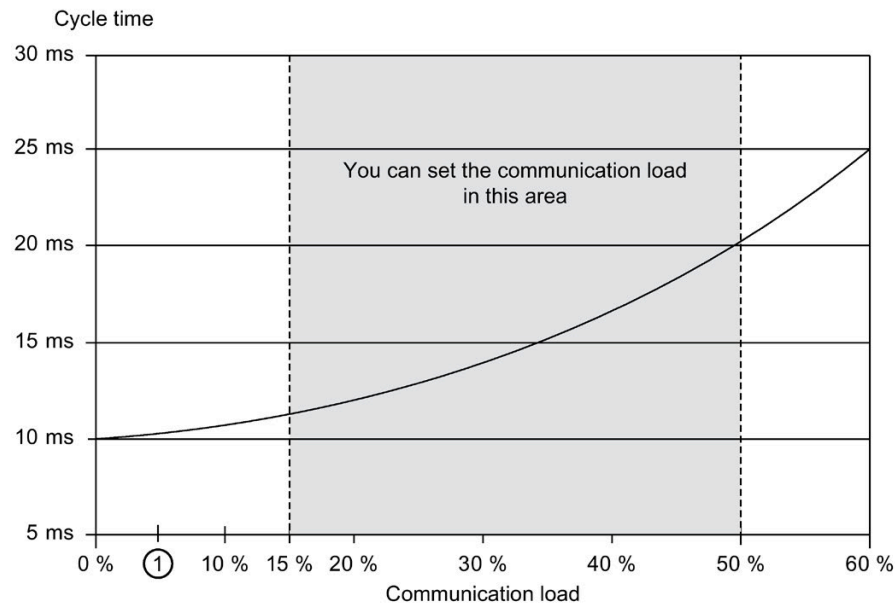
① CPUs 1516T(F)-3 PN/DP, 1517(F)-3 PN/DP, CPU 1517T(F)-3 PN/DP, CPU 1518(F)-4 PN/DP, 1518(F)-4 PN/DP MFP: The (minimum) communication load that can be set is 5%.

Figure 3-7   Maximum cycle time depending on the configured communication load

Reducing the cycle time with a lower communication load

You can reduce the setting for the communication load in the hardware configuration. If you set a communication load of 20% instead of 50%, for example, the cycle time extension due to the communication is reduced from a factor of 2 to 1.25.

Effect on the actual cycle time

Communication is only one cause of extension of the cycle time. All configured events that extend the cycle time (e.g. hardware interrupts) mean that more asynchronous events can occur within a cycle. These asynchronous events further extend the cyclic program. The extension depends on the number of events that occur and are processed in the cycle.

Note

Checking parameter changes

• Check the effects of a value change on the "Cycle load due to communication" parameter during system operation. You can use the "RT_INFO" instruction to determine which portions of runtime are used for communication and the user program.

• Take the communication load into consideration when setting the maximum cycle time to prevent time errors (for example, exceeding the cycle time within a cycle) from occurring.

Effect of load on the actual cycle time

The following examples show how the cycle time increases depending on the load.

Example 1

Example 1 shows an OB 1 with a runtime of 100 ms. The runtime of OB 1 is neither interrupted by communication load nor by higher-priority OBs.
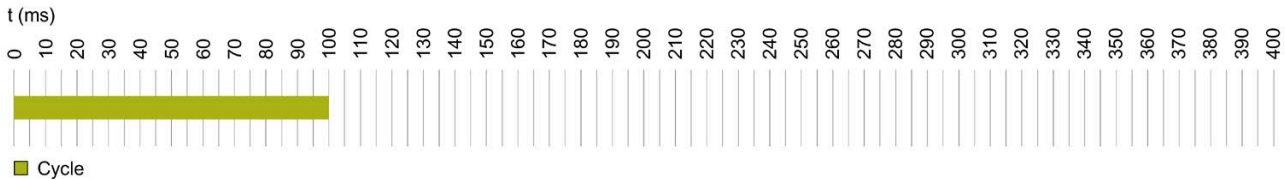

Figure 3-8   Cycle time without interruptions

Example 2

Example 2 shows that the runtime of OB 1 increases by a factor of 2 to 200 ms with a communication load of 50%.
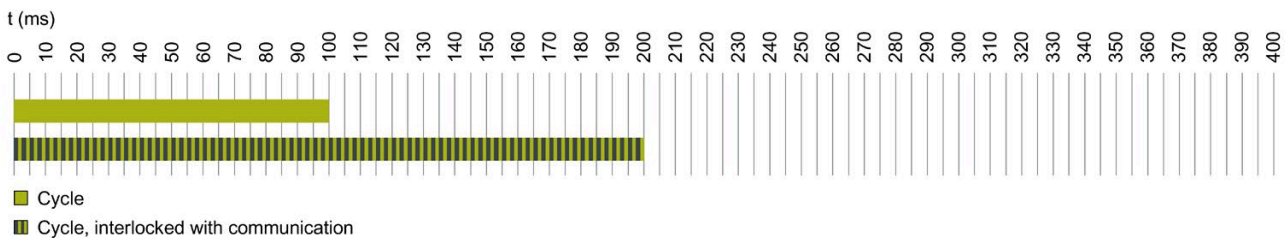

Figure 3-9   Cycle time with communication

Example 3

In example 3, OB 1 is interrupted every 20 ms by a cyclic higher-priority OB 30 (orange) with a runtime of 5 ms. The cycle time is extended to 135 ms by the higher-priority OB.
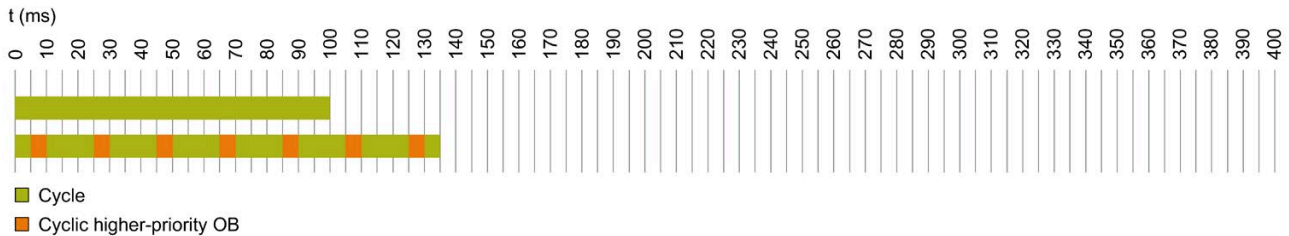

Figure 3-10   Cycle time with higher-priority OB

Example 4

In example 4, OB 1 is also interrupted by an OB 30 with priority 13. In addition, OB 1 and OB 30 are interrupted by communication tasks (priority 15). The cycle time increases to 400 ms.
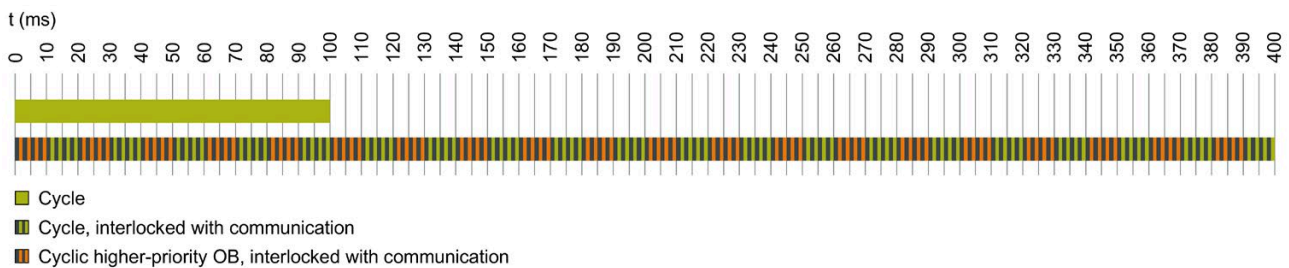

Figure 3-11   Cycle time with higher-priority OB and communication load

Example 5

In example 5, OB 1 is also interrupted by an OB 30 with priority 17. In addition, OB 1 is interrupted by communication tasks. Because the priority of OB 30 (priority 17) is higher than the priority of the communication tasks (priority 15), the interrupt points differ from example 4. The communication tasks suppressed by OB 30 are made up for within specific limits. Communication therefore completely suppresses the cyclic program within this time, 5 ms in the example. The cycle time increases to 400 ms, just like in example 4.
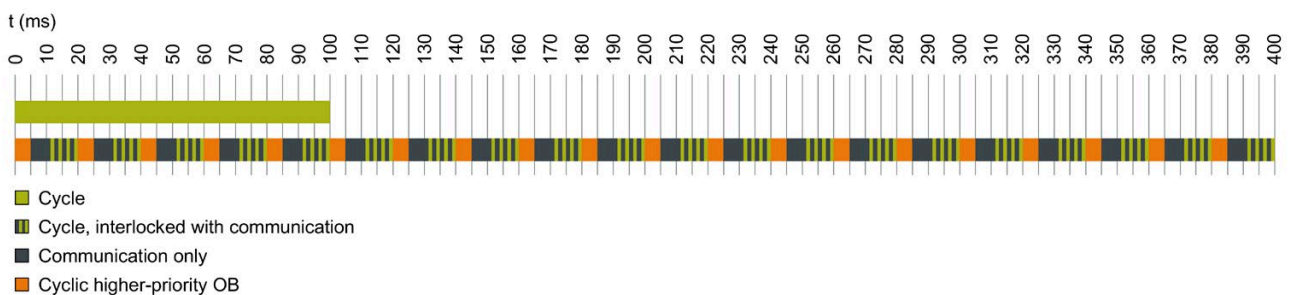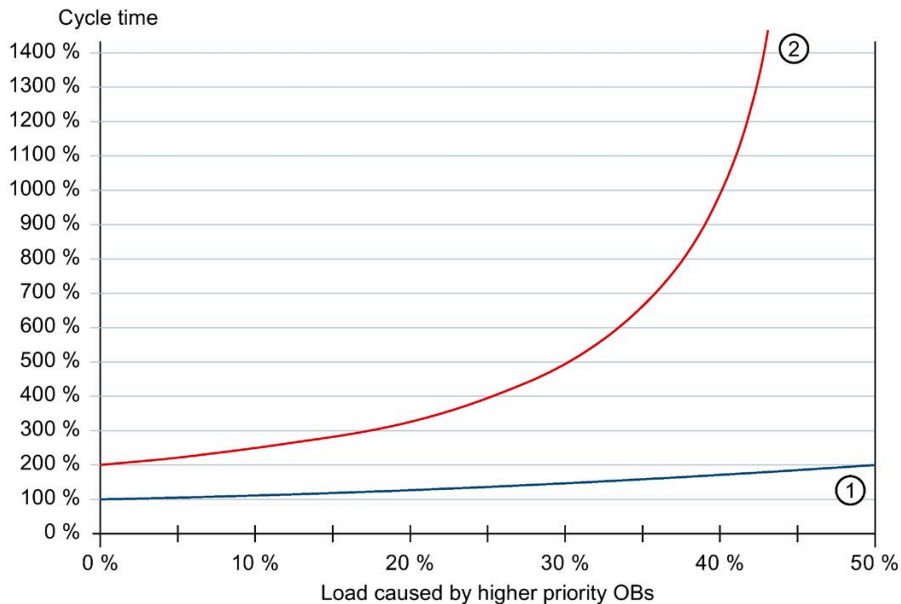

Figure 3-12   Cycle time with higher-priority OB and communication load

Cycle time curve for low and high loads

The y-axis of the following diagram indicates the cycle time in %. The value 100% stands for a cycle time of the CPU without higher-priority OBs and without communication. The x-axis indicates the load in % which is caused by higher priority OBs.

The blue curve ① of the diagram shows the course of the cycle time without communication load. The red curve ② shows the course of the cycle time with maximum communication and a parameterized communication load of 50%.

① Cycle time without communication load
② Cycle time with maximum communication

Figure 3-13   Cycle time for low and high loads

The course of the two curves shows the extent to which the communication load and the load from the higher-priority OBs influence the cycle time.

The longer the cycle time, the more the interruptions of OB 1 caused by higher-priority OBs and communication increase.

If both the base load and the communication load are at 50%, no computing capacity remains for the cyclic program and a time error occurs.

Note

Parameter assignment of the communication load

When the load in higher-priority OBs is high, reduce the configurable communication load.

Note

Parameter assignment of the communication load for the S7-1500R/H redundant system

Due to the synchronization of data between primary CPU and backup CPU, the S7-1500R/H redundant system is subject to an additional synchronization load. Therefore, choose a lower value for the communication load than for a non-redundant system.

Additional information on the particular features of the CPUs of the S7-1500R/H redundant system is available in the section Cycle and response times of the S7-1500R/H redundant system (Page 64).

Display of program and communication load

In the web server, you can find information on the current program/communication load and cycle time of your user program on the "Diagnostics > Runtime Information" web page.
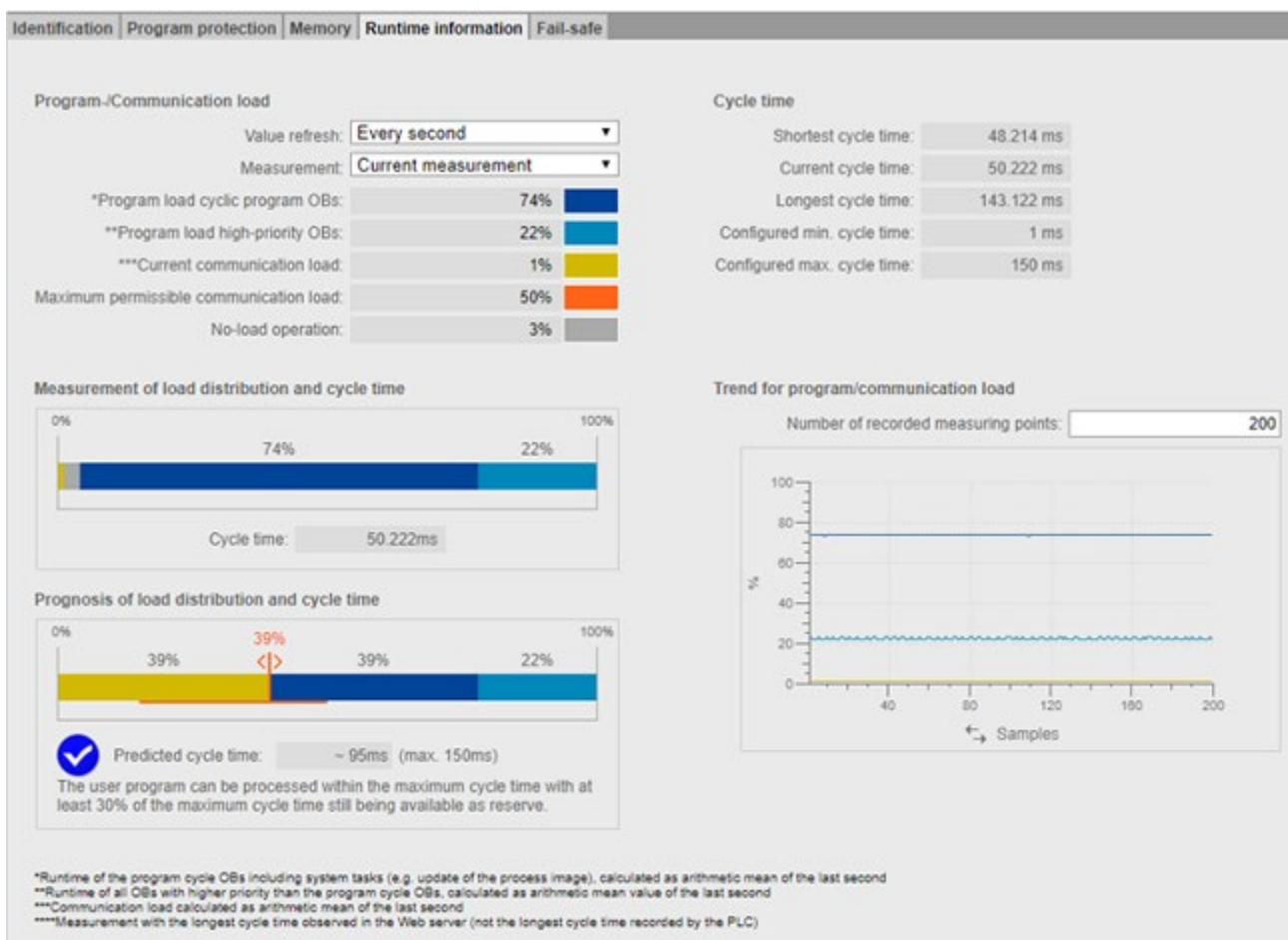

Figure 3-14   Graphical display of program and communication load

Program/communication load

With the "Value refresh" function, you update the data displayed in the bar charts:

- At intervals of 1 second
- Automatic (as configured in STEP 7)

With the "Measurement" function, you can decide which measurement the bar charts display. You can choose between:

- The current measurement
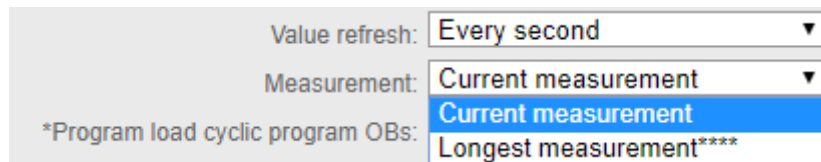- The measurement of the longest cycle time

Figure 3-15   Program/communication load

The legend of the program/communication load shows information on the following values, highlighted in color:

- "Program load cyclic program OBs"

  Required calculation time in percent within a cycle for program cycle OBs

- "Program load high-priority OBs"

  Required calculation time in percent within a cycle for higher-priority OBs

- "Current communication load"

  Required calculation time in percent for current communication tasks within a cycle

- "Maximum permissible communication load"

  The configured maximum communication load as a percentage

- "No-load operation"

  There is no program/communication load

Note

When you have configured a minimum cycle time, it can happen that no-load operation displays a high percentage value, although the value of the cycle time is also high.

The reason for this is that the loads are recorded as mathematical average of the last second, but the cycle time relates to the last cycle.
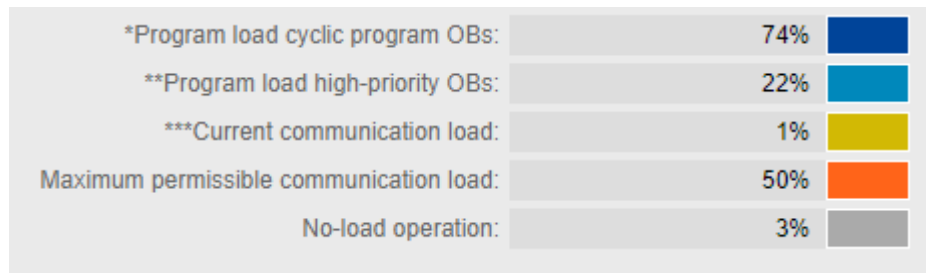
Figure 3-16   Color legend

If you click on a specific color, the selected color is highlighted in the chart. If you click on a highlighted color, you remove the highlighting.

Measurement of load distribution and cycle time

The "Measurement of load distribution and cycle time" bar chart shows the percentage of the calculation time within a cycle for the following values:

- "Program load cyclic program OBs"
- "Program load high-priority OBs"
- "Current communication load"
- "No-load operation"

Prognosis of load distribution and cycle time

The "Prognosis of load distribution and cycle time" bar chart predicts whether the CPU can process the user program with maximum communication load within the maximum cycle time.

Example 1:

Figure 3-17   Cycle time < 70% of the maximum cycle time

Example 1 shows that the CPU can process the user program within the maximum cycle time of 150 ms when the maximum communication load of 38% is reached. The predicted cycle time is < 70% of the configured maximum cycle time.

Example 2:

Figure 3-18   Cycle time ≥ 70% of the maximum cycle time

In example 2, the CPU can also process the user program with maximum communication load within the maximum cycle time. However, the predicted cycle time is already at 129 ms. If the predicted cycle time is ≥ 70% of the maximum cycle time, the chart outputs a warning.
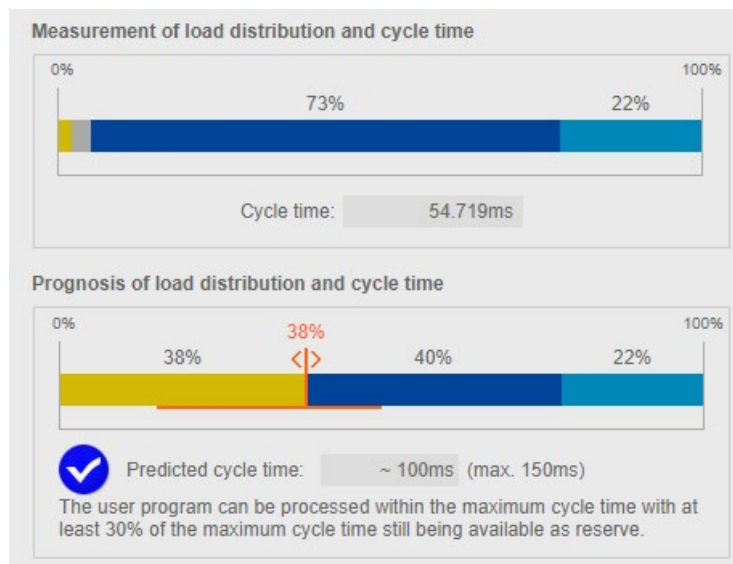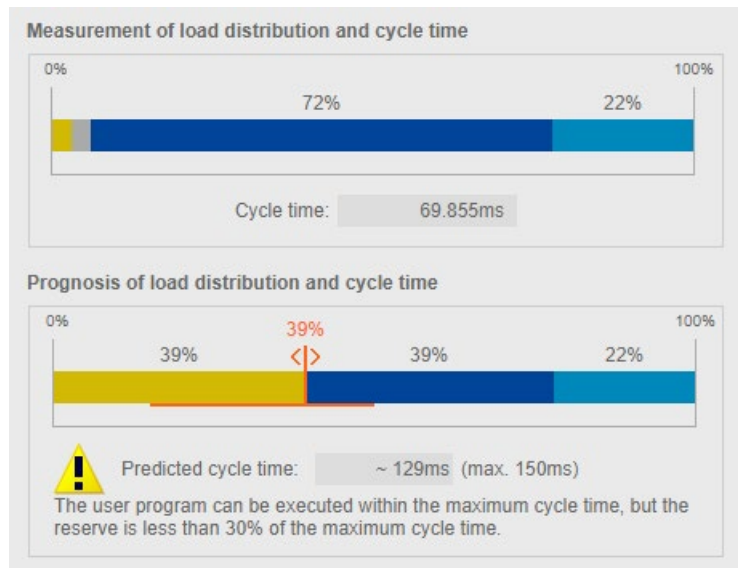
Example 3:
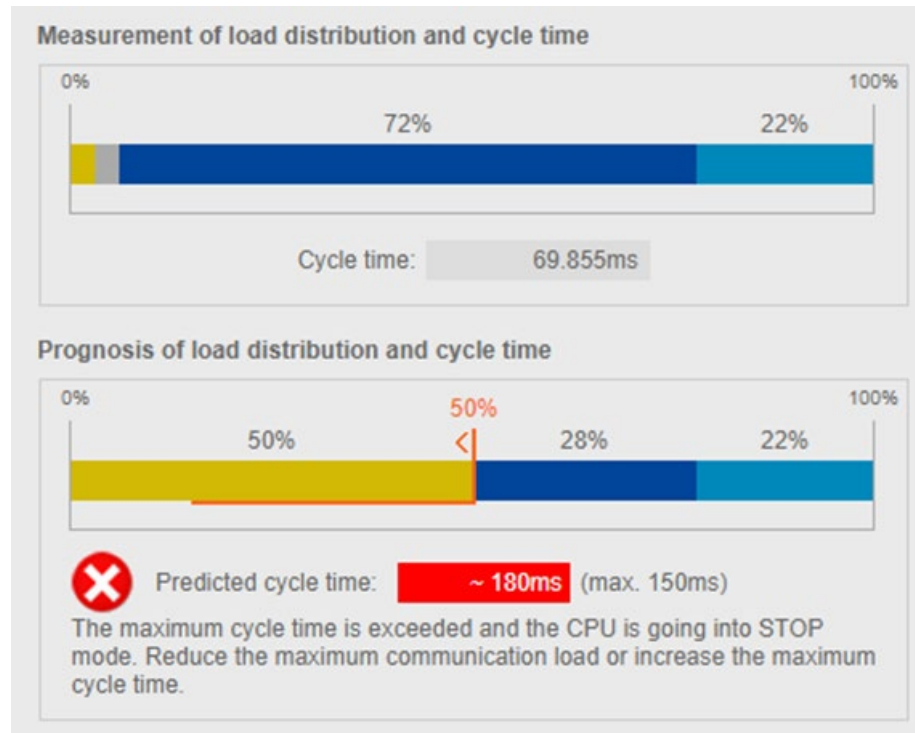
Figure 3-19   Cycle time longer than maximum cycle time

Example 3 shows that the CPU can no longer process the user program within the maximum cycle time when the maximum communication load is reached. If the predicted cycle time is longer than the maximum cycle time, the chart outputs an error message.

If it is predicted that the maximum cycle time will be exceeded, use the following controller in order to reduce the maximum communication load.
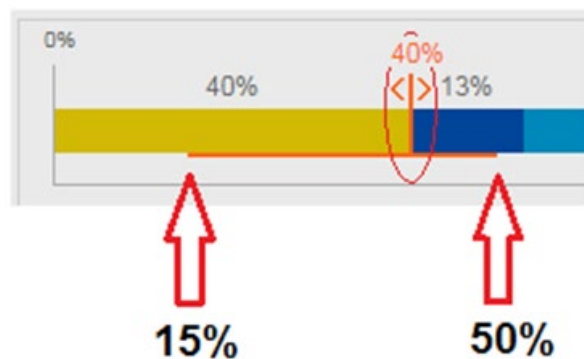
Figure 3-20   Controller for setting the maximum communication load

---

Note

Setting the communication load

The controller predicts the effects of the changed communication load on the cycle time. You configure the maximum communication load in STEP 7.

Note

For non-measurable fluctuations in the user program, e.g. for future changes in the user program, plan a sufficiently low value for the maximum communication load.

Note

Due to the different acquisition base of cycle time and load, a settled system state is required to display reliable measured values.

Progression of program/communication load

If your browser supports the display of SVG (Scalable Vector Graphics), the display in the "Runtime information" tab is expanded to show the progression of the program/communication load.

With the line charts in the "Trend for program/communication load" area, you can track the progression of the following values:

- "Program load cyclic program OBs"

- "Program load high-priority OBs"

- "Current communication load"

With the "Number of recorded measuring points" option, you can choose between the last 20 to 1 000 measured values for the display of the measured values.

For the trend on the x-axis, you can choose between "Time" (CPU time) and "Measuring points" by clicking on the desired unit.

Note

If you have selected the "Time" unit on the x-axis, all measured values that are more than 24 hours old are deleted automatically.
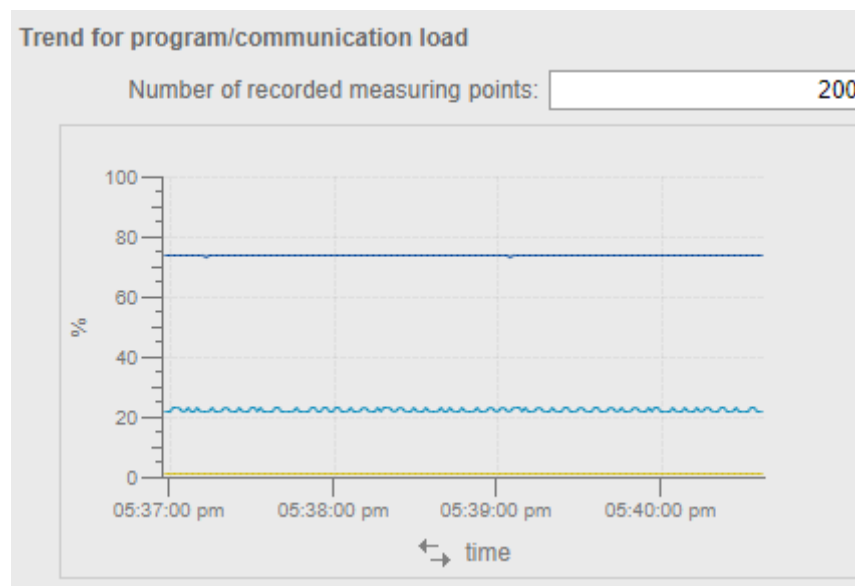
Figure 3-21   Line chart

3.2.2.4 Special consideration when PROFINET IO communication is configured on the 2nd PROFINET interface (X2)

If you configure the PROFINET IO communication at the 2nd PROFINET interface (X2) on the following CPUs as of firmware version 2.0, an additional system load occurs:

- CPU 1515(F)-2 PN

- CPU 1515T(F)-2 PN

- CPU 1516(F)-3 PN/DP

- CPU 1516T(F)-3 PN/DP

- CPU 1513(F)pro-2 PN (as of firmware version V2.8)

- CPU 1516(F)pro-2 PN

This additional system load has a higher priority than the user program (>26) and extends its run time. The execution of synchronous cycle interrupts or hardware interrupts, for example, can be delayed as a result.

The additional system load depends on:

- Communication traffic at the 2nd PROFINET interface (X2)
  The communication traffic at the interface in frames per second causes communication load as well as system load. You cannot limit the communication traffic using the "Communication load" parameter.

- Number of IO devices which the CPU at the 2nd PROFINET interface (X2) updates within a millisecond

You determine the additional system load with the "RT_INFO" (read RUNTIME statistics) instruction at the Mode parameter with mode 10 or mode 20.

Reducing additional system load

You reduce the communication load at the 2nd PROFINET interface, e.g. with:

- Fewer connected HMI devices or slower update cycles on the HMI devices

- Less or slower communication with other CPUs

Increase the update times in STEP 7 for all IO devices that are assigned to the 2nd PROFINET interface (X2):

1. Select the "IO Communication" in the "Network view" of STEP 7.

2. Set the "Update mode" parameter to "Adjustable".

3. Select a higher value for the "Update time [ms]" parameter in the drop-down list.
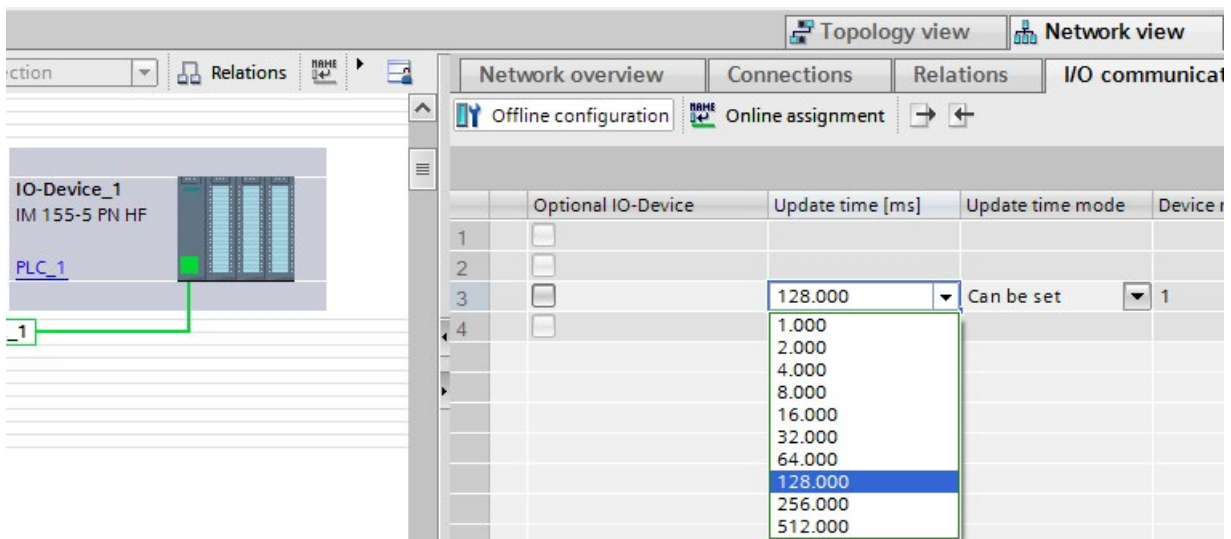
4. Repeat this setting for the other IO devices.

Figure 3-22   Increasing update times

3.3 Time-driven program execution in cyclic interrupts

With a cyclic interrupt you have the option of having a specific OB processed in a time interval. The time interval is independent of the execution time of the cyclic program. A priority from 2 to 24 can be selected for the cyclic interrupt. This makes the priority of cyclic interrupts higher than the priority of the cyclic program. A cyclic interrupt increases the execution time of the cyclic program.

In STEP 7 the organization blocks OB 30 to OB 38 are intended for processing cyclic interrupts. You can create additional cyclic interrupts starting with organization block OB 123. The number of available organization blocks depends on the CPU used.

Cyclic interrupt

A cyclic interrupt is an interrupt initiated according to a defined cycle that causes a cyclic interrupt OB to be processed. A cyclic interrupt OB is assigned to the "Cyclic interrupt" event class.

Cycle of a cyclic interrupt

The cycle of a cyclic interrupt is defined as the time between the occurrence of two consecutive events that each call the associated cyclic interrupt OB.

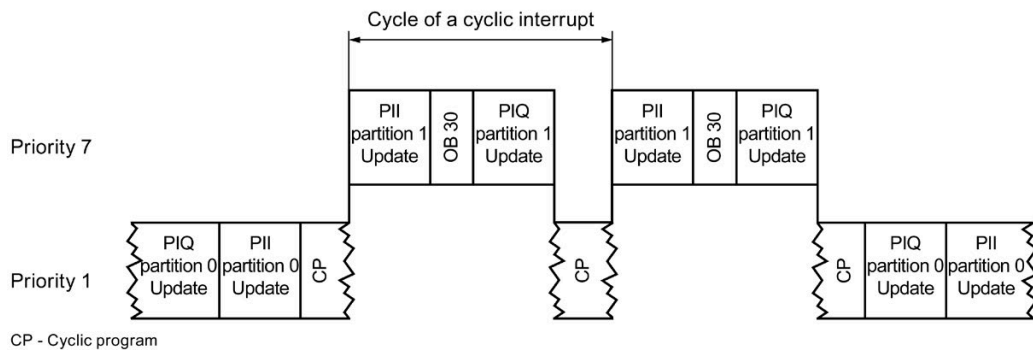The following figure shows an example of the cycle of a cyclic interrupt.

Figure 3-23   Call interval of a cyclic interrupt

Accuracy of a cyclic interrupt

Even if a cyclic interrupt is not delayed by a higher-priority OB or communication activities, the accuracy with which it is started is nevertheless subject to system-dependent fluctuations.

The following table shows the accuracy with which a cyclic interrupt is triggered:

Table 3- 6   Accuracy of cyclic interrupts

	S7-1500			
	1511(F)-1 PN **1511T(F)-1 PN** **1511C-1 PN** **1512C-1 PN** **1513(F)-1 PN**	**1515(F)-2 PN** **1515T(F)-2 PN** **1516(F)-3 PN/DP** **1516T(F)-3 PN/DP**	**1517(F)-3 PN/DP** **1517T(F)-3 PN/DP**	**1518(F)-4 PN/DP** **1518(F)-4 PN/DP MFP** **1518T(F)-4 PN/DP**
Cyclic interrupt	±90 µs	±80 µs	±30 µs	±25 µs

	S7-1500R/H* in RUN-Solo system state		
	1513R-1 PN	**1515R-2 PN**	**1517H-3 PN** **1518HF-4 PN**
Cyclic interrupt	±390 µs	±300 µs	±90 µs

* Additional information about cycle and response times of R/H CPUs is available in the section "Cycle and response times of the S7-1500R/H redundant system"

	ET 200SP		
	1510SP(F)-1 PN	**1512SP(F)-1 PN**	**1515SP(F)-PC**
Cyclic interrupt	±90 µs	±90 µs	±80 µs

	ET 200pro	
	1513pro(F)-2 PN	**1516pro(F)-2 PN**
Cyclic interrupt	±90 µs	±80 µs

Note

Scope of validity

Please note that the accuracy data for the cyclic interrupt also applies to all other higher-priority execution levels/OBs.

Processing sequence of cyclic interrupts

> **Note**
>
> With several cyclic interrupt OBs with identical parameterization, the processing sequence of the cyclic interrupt OBs cannot be predicted.
>
> If you want to ensure a defined execution sequence of cyclic interrupt OBs with the same cycle time and priority, configure a different phase offset in each case.

For information on how to assign parameters for cyclic interrupt OBs, refer to the STEP 7 online help.

3.4 Response time for cyclic and time-driven program execution

Introduction

In this section you learn:

- How the response time is composed
- How to calculate the response time

Definition

The response time in the case of cyclic or time-controlled program execution is the time between the detection of an input signal and the change of a connected output signal.

Fluctuation in the response time of the CPU

The actual response time of the CPU fluctuates between one and two cycles for cyclic program execution and between one and two cyclic interrupt cycles for time-controlled program execution.

You should always assume the longest response time when configuring your system.

The following figure shows the shortest and longest response times of the CPU to an event.
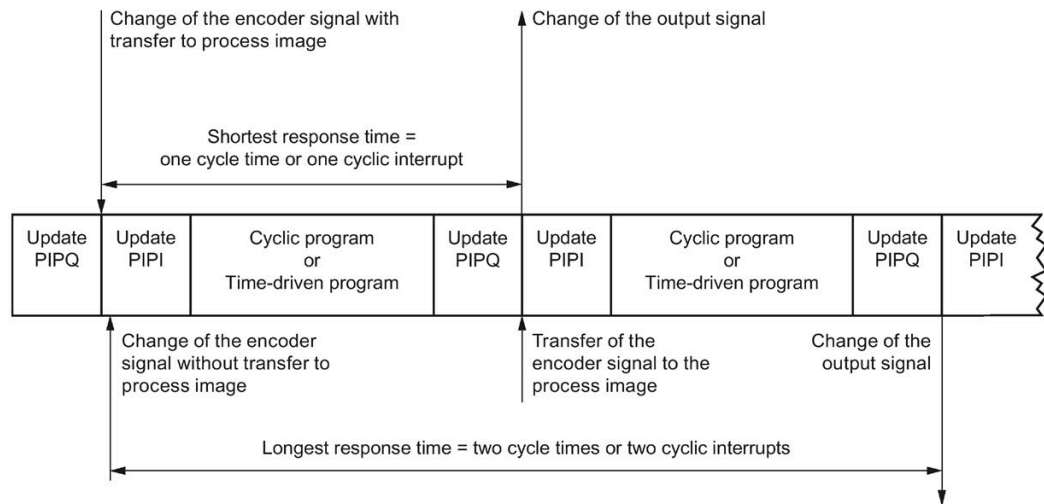
Figure 3-24   Shortest and longest response times of the CPU

Factors

To determine the process response time, you must take account of the following factors in addition to the CPU response time described above:

* Delay of the inputs and outputs at the I/O module

* Switching times of the sensors and actuators used

* Update times for PROFINET IO or DP cycle times on PROFIBUS DP; update time of the backplane bus for ET 200SP CPUs

---

Note

Backplane bus of the S7-1500 CPUs

The update time of the backplane bus of the S7-1500 CPUs can be ignored here.

Delay at the inputs and outputs of the modules

The delay and cycle times can be found in the technical specifications of the I/O modules.

Update times for PROFINET IO and DP cycle times on PROFIBUS DP

When distributed I/O is used, the maximum response time is additionally extended by the bus transmission times of PROFIBUS or PROFINET. These bus transmission times occur during both the reading and output of the process image partitions. The bus transmission times correspond to the bus update cycle of the distributed device.

PROFINET IO

If you use STEP 7 to configure your PROFINET IO system, STEP 7 calculates the update time. To display the update time, follow these steps:

- Select the PROFINET interface of the I/O module.

- In the General tab, select "Advanced options > Real time settings > IO cycle".

The update time is displayed in the "Update time" field and can be set for each IO device.

PROFIBUS DP

If you use STEP 7 to configure your PROFIBUS DP master system, STEP 7 calculates the DP cycle time. To display the DP cycle time, follow these steps:

- Select the PROFIBUS subnet in the network view.

- In the General tab of the Inspector window, navigate to the Bus parameters.

The DP cycle time is displayed in the "Parameters" field at "Typical Ttr".

The following figure illustrates the additional bus runtimes using distributed I/O.
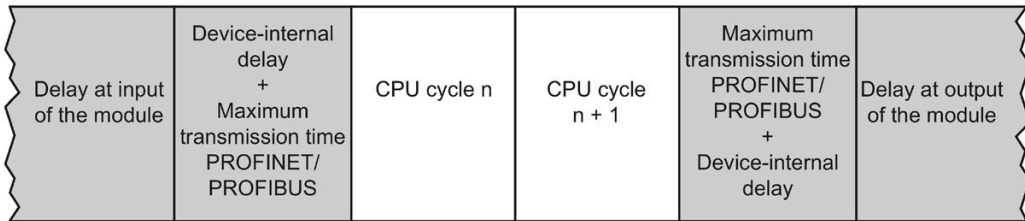

Figure 3-25   Additional bus runtimes with distributed I/O

A further optimization of the response times is achieved by using isochronous mode.

Update time of the backplane bus for ET 200SP CPUs

The following table shows the central (typical) update times of the backplane bus for the ET 200SP CPUs.

Table 3- 7   Update time of the ET 200SP CPUs

	Update time of the CPU		
	ET 200SP		
	1510SP(F)-1 PN	1512SP(F)-1 PN	1515SP(F)-PC
Update time for central I/O	250 µs to 1 ms, depending on number and type of central I/O modules[1]		

[1]   The duration of the update time depends on the number of the I/O modules and their type (ST, HF, HS). The update time is set at 1 ms for a max. central I/O configuration with standard I/O modules. You can reduce the update time down to 250 µs, for example, by using HF I/O modules and by reducing the number of modules.

The table below is an orientation guide. It shows the approximate relationship between the number of ET 200SP I/O modules and the bus cycle that is used. As an example, 8 bytes of I/O data per I/O module are assumed in the table.

Number of ET 200SP I/O modules	Input data (bytes)	Output data (bytes)	Used bus cycle (µs)
8	64	64	250
16	128	128	250
24	192	192	281.25
32	256	256	312.5
40	320	320	343.75
48	384	384	375
56	448	448	406.25
64	512	512	437.5

For I/O modules with more than 32 bytes of I/O data, the bus cycle is calculated with an I/O module of 32 bytes. In this case the I/O module requires multiple bus cycles to update its I/O data.

Reference

The following links provide additional information:

- Application example for determining the response time for PROFINET (https://support.industry.siemens.com/cs/ww/en/view/21869080)

- Transmission times and isochronous mode in function manual PROFINET with STEP 7 V15 (https://support.industry.siemens.com/cs/ww/en/view/49948856); see also the section "Tips on assembly"

- Transmission times and isochronous mode in function manual PROFIBUS with STEP 7 V15 (https://support.industry.siemens.com/cs/ww/en/view/59193579); see also the section "Network settings"

- Delays at the input or output of the modules can be found in the manual for the respective device.

- Information on device-internal delays can be found in the manuals for the ET 200MP and ET 200SP distributed I/O systems.

3.5 Summary of response time with cyclic and time-controlled program execution

Estimation of the shortest and longest response time

The following formulas may be used to estimate the shortest and longest response time:

Estimation of the shortest response time

The shortest response time is the sum of:

	1 x delay of the input/output module for inputs
+	1 x (update PROFINET IO or PROFIBUS DP)*; (update time of the backplane bus for the ET 200SP CPUs)
+	1 x transfer time of the process image input
+	1 x execution of the user program
+	1 x transfer time of the process image output
+	1 x (update PROFINET IO or PROFIBUS DP)*; (update time of the backplane bus for the ET 200SP CPUs)
+	1 x delay of the input/output module for outputs

_____

= Shortest response time

* Time is dependent on the configuration and the extent of the network.

The shortest response time is equivalent to the sum of the cycle time plus the input and output delay times.

Estimation of the longest response time

The longest response time is the sum of:

	1 x delay of the input/output module for inputs
+	2 x (update PROFINET IO or PROFIBUS DP)*; (update time of the backplane bus for the ET 200SP CPUs)
+	2 x transfer time of the process image input
+	2 x execution of the user program
+	2 x transfer time of the process image output
+	2 x (update PROFINET IO or PROFIBUS DP)*; (update time of the backplane bus for the ET 200SP CPUs)
+	1 x delay of the input/output module for outputs

_____

= Longest response time

* Time is dependent on the configuration and the extent of the network.

The longest response time is equivalent to the sum of twice the cycle time plus the delay times of the inputs and outputs. Twice the update time for PROFINET IO or twice the DP cycle time on PROFIBUS DP is added to the longest response time.

Event-driven program execution 4

4.1 Response time of the CPUs when program execution is event-controlled

Introduction

Hardware interrupts are used to detect events in the process in the user program and to react to them with an appropriate program. In STEP 7, the organization blocks OB 40 to OB 47 are intended for processing hardware alarms. You can create additional hardware interrupts starting with organization block OB 123. The number of available organization blocks depends on the CPU used.

Hardware interrupt

A hardware interrupt is an interrupt that occurs during the running program execution, due to an interrupt-triggering process event. The operating system calls the assigned interrupt OB; as a result, the execution of the program cycle or of lower priority program parts is interrupted. A hardware interrupt OB is assigned to the "Hardware interrupt" event class.

Interrupt response times of the CPUs for hardware interrupts

The interrupt response time starts with the occurrence of a hardware interrupt event in the CPU. The interrupt response time ends with the start of processing of the assigned hardware interrupt OB.

This time is subject to system-inherent fluctuations, and this is expressed using a minimum and maximum interrupt response time.

The following table contains the length of the typical response times of the CPUs for hardware interrupts.

Table 4- 1   Response times of the CPUs for hardware interrupts

		S7-1500			
		1511(F)-1 PN 1511T(F)-1 PN 1511C-1 PN 1512C-1 PN 1513(F)-1 PN	1515(F)-2 PN 1515T(F)-2 PN 1516(F)-3 PN/DP 1516T(F)-3 PN/DP	1517(F)-3 PN/DP 1517T(F)-3 PN/DP	1518(F)-4 PN/DP 1518(F)-4 PN/DP MFP 1518T(F)-4 PN/DP
Interrupt response times	Min.	100 µs	90 µs	30 µs	20 µs
	Max.	400 µs	360 µs	120 µs	90 µs

		S7-1500R/H* in RUN-Solo system state		
		1513R-1 PN	1515R-2 PN	1517H-3 PN 1518HF-4 PN
Interrupt response times	Min.	100 µs	90 µs	30 µs
	Max.	400 µs	360 µs	120 µs

* Additional information about cycle and response times of R/H CPUs is available in the section "Cycle and response times of the S7-1500R/H redundant system"

		ET 200SP		
		1510SP(F)-1 PN	1512SP(F)-1 PN	1515SP(F)-PC
Interrupt response times	Min.	100 µs	100 µs	90 µs
	Max.	400 µs	400 µs	360 µs

		ET 200pro	
		1513pro(F)-2 PN	1516pro(F)-2 PN
Interrupt response times	Min.	100 µs	90 µs
	Max.	400 µs	360 µs

The specified times are extended:

- If higher-priority interrupts are queued for execution
- If the hardware interrupt OB is assigned to a process image partition

You can find these times in the tables in the section "Extension due to nesting of higher-priority OBs and/or interrupts" in the chapter User program execution time (Page 32).

If you need fast interrupt response times, do not assign a process image partition to the hardware interrupt OB and use direct access in the hardware interrupt OB instead.

You can find additional information on determining response times for PROFINET in the application example with the entry ID 21869080 on the Service&Support (https://support.industry.siemens.com/cs/ww/en/view/21869080) Internet page.

Influence of input modules on the interrupt response times of hardware interrupts

Digital input modules:

Interrupt response time of hardware interrupts = internal interrupt processing time + input delay (see section Technical specifications in the relevant manual)

Analog input modules:

Interrupt response time of hardware interrupts = internal interrupt processing time + conversion time (see section Technical specifications in the relevant manual)

Impact of communication on interrupts

Communication tasks are always processed by the CPU with priority 15. If you do not want the interrupt execution to be delayed or interrupted by communication, configure the interrupt execution with priority > 15. The default setting for interrupt execution is priority 16.

Special consideration when PROFINET IO communication is configured on the 2nd PROFINET interface (X2)

Additional information on this is available in section Special consideration when PROFINET IO communication is configured on the 2nd PROFINET interface (X2) (Page 50).

4.2 Process response time when program execution is event-driven

When program execution is event-driven, the process response time is determined by the following:

- Delay times of the input and output modules used
- Update times for PROFIBUS/PROFINET for distributed modules; update time of the backplane bus for ET 200SP CPUs
- Interrupt response time of CPU
- Runtimes of the interrupt OB including update of the process image partition

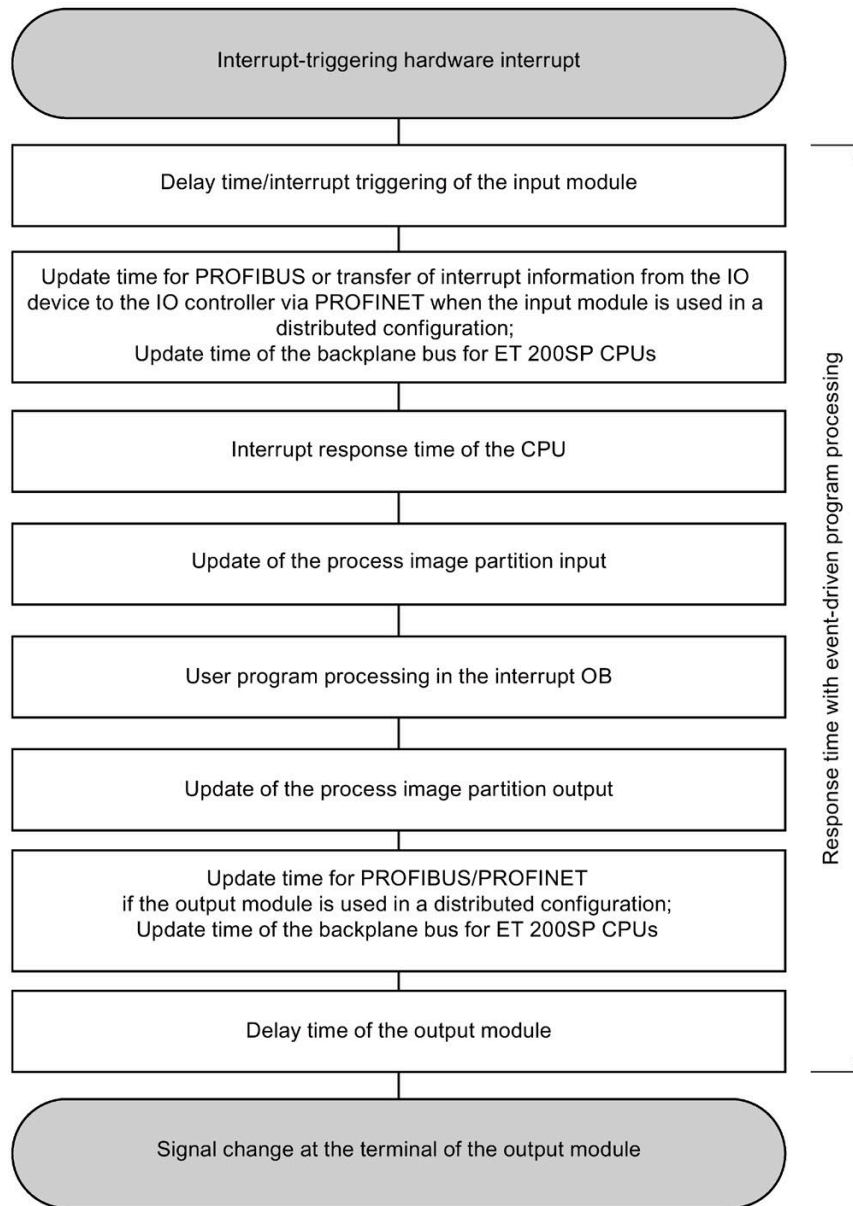The following figure shows the individual execution steps for event-driven program execution.

Figure 4-1   Schematic representation of event-driven program execution

Cycle and response times of the S7-1500R/H redundant system

5

5.1 Introduction

CPUs of the S7-1500R/H redundant system are designed as being redundant. The goal of the redundant configuration is to avoid production downtimes. When a CPU fails, the other CPU maintains control over the process.

Compared to non-redundant CPUs, the CPUs of the S7-1500R/H redundant system have the following special features:

- Longer cycle and response times
- Specific operating and system states
- Additional load and delays through synchronization

Contents of this section

This section describes the effects of the mode of operation of the S7-1500R/H redundant system on the cycle and response times.

It also describes how to estimate and control the cycle and response times of the CPUs. This prevents excessive cycle times.

Note

Classification of this chapter

The statements in the previous chapters describe the response of an individual CPU.

The section "Cycle and response times of the S7-1500R/H redundant system" supplements the information of the previous sections with information on the S7-1500R/H redundant system.

5.2 Maximum cycle time and time errors

Maximum cycle time

As with non-redundant CPUs, you can parameterize an upper limit of the cyclic program by setting the maximum cycle time.

The cycle time of redundant CPUs is usually longer compared to non-redundant CPUs (especially in the RUN-Redundant and SYNCUP system states).

The factor by which the cycle time for redundant CPUs is higher than that for non-redundant CPUs depends very strongly on your specific automation task.

Note

Maximum cycle time in SYNCUP system state

The length of the parameterized maximum cycle time also affects the SYNCUP system state.

If the following condition is fulfilled during the SYNCUP, the system initiates a transition to RUN-Redundant:
The actual cycle time is ≤ 80% of the maximum cycle time over several cycles.

More information on this is available in section Influences on the cycle time in SYNCUP system state (Page 67).

Maximum cycle time in RUN-Redundant system state

On the failure of one of the two CPUs, the cycle time also contains a dead time of up to 300 ms for R-CPUs and up to 50 ms for the H-CPU. You must schedule this time as cycle time reserve in case of failure of one of the two CPUs. Therefore, ensure that the longest cycle time plus this dead time is < 60% of the configured maximum cycle time in RUN-Redundant system state. By doing so, you prevent the parameterized maximum cycle time from being exceeded in case of load fluctuations and delays due to synchronization.

Time error

As with non-redundant CPUs, you can specify the response to a time error for the CPUs of the S7-1500R/H redundant system. In RUN-Solo system state, the redundant CPUs behave like non-redundant CPUs when the maximum cycle time is exceeded (see section Cycle time (Page 25)).

In the SYNCUP and RUN-Redundant system states the redundant CPUs behave as follows:

Table 5- 1   Response of the S7-1500R/H redundant system when cycle time is exceeded, without OB 80

Initial situation			1st time cycle time is exceeded			2nd time cycle time is exceeded		
System	Primary CPU	Backup CPU	System	Primary CPU	Backup CPU	System	Primary CPU	Backup CPU
RUN-Solo	RUN	STOP	**STOP**	STOP	STOP	---	---	---
SYNCUP[1]	RUN-Syncup	SYNCUP	**STOP**	STOP	STOP	---	---	---
SYNCUP[2]	RUN-Syncup	SYNCUP	**RUN-Solo**	RUN	STOP	**STOP**	STOP	STOP
RUN-Redundant	RUN-Redundant	RUN-Redundant	**RUN-Solo**	RUN	STOP	**STOP**	STOP	STOP

[1] SYNCUP up to snapshot of the work memory contents

[2] SYNCUP after snapshot of the work memory contents

Table 5- 2   Response of S7-1500R/H redundant system when cycle time is exceeded with OB 80

Initial situation			1st time cycle time is exceeded			2nd time cycle time is exceeded			3rd time cycle time is exceeded		
System	Primary CPU	Backup CPU	System	Primary CPU	Backup CPU	System	Primary CPU	Backup CPU	System	Primary CPU	Backup CPU
RUN-Solo	RUN	STOP	**RUN-Solo**	RUN + OB 80	STOP	**STOP**	STOP	STOP	---	---	---
SYNCUP [1]	RUN-Syncup	SYNCUP	**SYNCUP**	RUN-Syncup + OB 80	SYNCUP	**STOP**	STOP	STOP	---	---	---
SYNCUP [2]	RUN-Syncup	SYNCUP	**SYNCUP**	RUN-Syncup + OB 80	SYNCUP + OB 80	**RUN-Solo**	RUN + OB 80	STOP	**STOP**	STOP	STOP
RUN-Redundant	RUN-Redundant	RUN-Redundant	**RUN-Redundant**	RUN-Redundant + OB 80	RUN-Redundant + OB 80	**RUN-Solo**	RUN + OB 80	STOP	**STOP**	STOP	STOP

[1] SYNCUP up to snapshot of the work memory contents

[2] SYNCUP after snapshot of the work memory contents

Note

System state change after STOP with OB 80

The primary CPU also switches to STOP after the maximum cycle time has been exceeded three times in the same cycle.

Switchover of the backup CPU to STOP operating state when the maximum cycle time is exceeded

A switchover of the backup CPU to STOP operating state reduces the synchronization load and relieves the load on the primary CPU.

5.3 Influences on the cycle time of the S7-1500R/H redundant system

5.3.1 Influences on the cycle time in RUN-Solo system state

RUN-Solo system state

In RUN-Solo system state, the primary CPU is in RUN operating state. The primary CPU executes the cyclic, time- and interrupt-controlled program execution on its own. The backup CPU is in STOP operating state, is switched off or defective.

Influence on the cycle time

In RUN-Solo system state, the primary CPU behaves exactly the same as a standard CPU (non-redundant CPU) with regard to cycle time monitoring. Additional information on this is available in section "Cycle time (Page 25)".

5.3.2 Influences on the cycle time in SYNCUP system state

SYNCUP system state

In SYNCUP system state, the primary CPU is in RUN-Syncup operating state. The backup CPU is in SYNCUP operating state. The task of the SYNCUP system state is to synchronize the data of both CPUs so that the CPUs can subsequently work redundantly.

Influence on the cycle time

The figure below shows the chronological behavior of primary CPU and backup CPU during the SYNCUP system state.
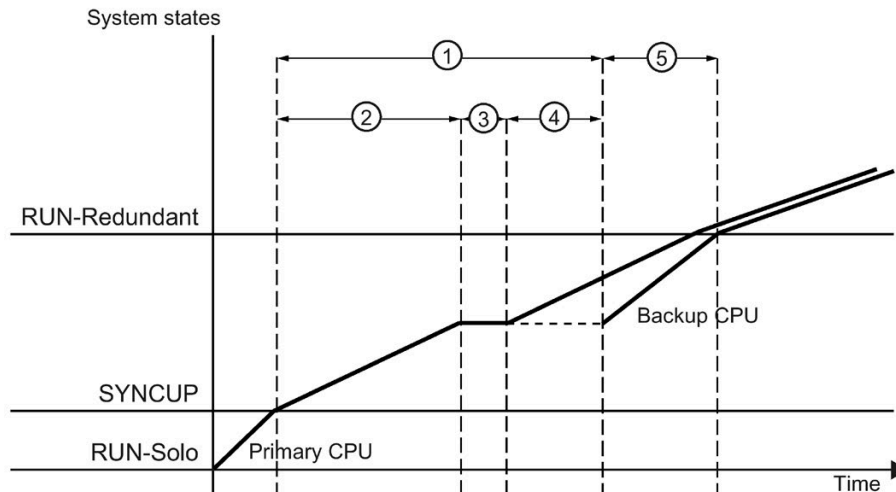
① Synchronization of data from the primary CPU to the backup CPU

② Copying the load memory and terminating the asynchronous instructions

③ Snapshot of the work memory contents

④ Transfer of the work memory contents to the backup CPU

⑤ Backup CPU makes up the time lag to the primary CPU caused by the synchronization of data

Figure 5-1   Effects of the SYNCUP on the cycle times of the CPUs

In SYNCUP system state, all relevant data is synchronized from the primary CPU to the backup CPU. At the end of SYNCUP, the backup CPU makes up the time lag to the primary CPU caused by the synchronization.

⚠️ **CAUTION**

SYNCUP system state

- The synchronization of data, in particular the snapshot of the work memory contents, extends the cycle time. In addition, most test and commissioning functions cannot be executed during SYNCUP.
- During SYNCUP, diagnostic interrupts are processed with a significant delay.
- The cycle time increases greatly during the transition from SYNCUP system state to RUN-Redundant.

Therefore, only execute the SYNCUP during uncritical process states.

---

① Synchronization of data from the primary CPU to the backup CPU

During this phase all relevant contents of the load memory, work memory, and system memory of the primary CPU are synchronized to the backup CPU.

② Copying the load memory and terminating the asynchronous instructions

The primary CPU copies parts of its load memory from its SIMATIC memory card to the SIMATIC memory card of the backup CPU. The backup CPU restarts and automatically switches to SYNCUP operating state. The backup CPU copies the transferred load memory contents to its work memory. Data blocks, process image, etc. are immediately overwritten with current data from the primary CPU.

③ Snapshot of the work memory contents

The primary CPU saves a consistent snapshot of its work memory contents at the next cycle control point.

When creating the snapshot of the work memory contents, the execution of the user program (on the primary CPU) is delayed during the SYNCUP by the following times:

Table 5- 3   Delay times when creating the snapshot of memory contents during SYNCUP

R/H CPUs	Duration of the snapshot of memory contents in the SYNCUP [ms] (typical values)		Max. data work memory [MB]
	With allocation of data work memory: 0%	With allocation of data work memory: 100%	
CPU 1513R-1 PN	105	145	1.5
CPU 1515R-2 PN	225	290	3
CPU 1517H-3 PN	18	23	8
CPU 1518HF-4 PN	25	47	60

④ Transfer of work memory contents to the backup CPU

During this phase the consistent snapshot is transferred from the primary CPU to the backup CPU. The transfer of the work memory contents extends the cycle time. The time required for the transfer of the work memory contents depends on the performance capability of the CPU and the amount of work memory data.

⑤ Backup CPU makes up the time lag to the primary CPU

During this phase the backup CPU makes up the time lag in program execution to the primary CPU. As in redundant mode, events are already synchronized during this phase as needed.

Note

No switchover possible during SYNCUP

If a fault occurs in the primary CPU during SYNCUP, no switchover to the backup CPU is possible. The SYNCUP is canceled and the backup CPU returns to STOP operating state.

Switchover from SYNCUP to RUN-Redundant

The system checks continuously which cycle time would result from a change to the RUN-Redundant system state. If this cycle time would be ≤ 80% of the maximum cycle time over multiple cycles, the transition is initiated. You can find more information in the system manual S7-1500R/H Redundant System (https://support.industry.siemens.com/cs/ww/en/view/109754833).

Note

Determination of the cycle time during the SYNCUP

You can track the progress of the SYNCUP on the display of the primary CPU and backup CPU. At each cycle control point the backup CPU sends a status message on its program progress to the primary CPU. The display of the primary CPU indicates the duration of the time lag of the backup CPU.

In addition to viewing the progress in the displays, the progress of the SYNCUP can also be read out using the "RT_INFO" instruction.

Reasons for cancellation of the SYNCUP

Possible causes for the cancellation of the SYNCUP are:

- The load of the user program or the load on the redundancy connections between primary and backup CPU is too high

- The maximum cycle time of the primary CPU was exceeded

An overview of all reasons for the cancellation of the SYNCUP and remedial measures is available in the system manual S7-1500R/H redundant system (https://support.industry.siemens.com/cs/ww/en/view/109754833).

Disable SYNCUP

To avoid the described effects of the SYNCUP on the cycle times during critical process states, use the instruction "RH_CTRL".

The "RH_CTRL" instruction can be used to disable the SYNCUP system state for the S7-1500R/H redundant system. If the disable is no longer required, the "RH_CTRL" instruction can be used to enable the SYNCUP system state once again.

More information on the "RH_CTRL" instruction is available in the system manual S7-1500R/H redundant system (https://support.industry.siemens.com/cs/ww/en/view/109754833).

Minimum cycle time

It is often necessary to set a longer minimum cycle time for the CPUs of the S7-1500R/H redundant system than for those of the non-redundant CPUs.

Recommendation: Select the minimum cycle time so that the cyclic program does not have to be executed more frequently than your process requires. A longer minimum cycle time that has been adapted to your process optimizes the entire system. The computing power that is available per cycle by extending the minimum cycle time is then available for system tasks such as communication.

The selected minimum cycle time should at least correspond to the measured cycle time in redundant mode of the user program (where the minimum cycle time is has yet to have an effect). A minimum cycle time that is significantly lower is only effective in solo mode of the system. It burdens and prolongs the SYNCUP system state and increases the probability of sporadic aborts of the SYNCUP.

Note

Too low cycle times

Cycle times that are too low can result in an excessive synchronization load and thus terminate the SYNCUP.

Parameter assignment of the communication load

Note

An increased synchronization load occurs in the SYNCUP system state. Because this synchronization load places a load on the cycle in addition to the communication, it is recommended to reduce the communication load to ≤ 30%.

### 5.3.3 Influences on the cycle time in RUN-Redundant system state

RUN-Redundant system state

In RUN-Redundant system state, the primary CPU controls the process. The primary CPU continuously synchronizes itself with the backup CPU. In the event of a failure of the primary CPU, the backup CPU adopts its role and thus control over the process.

Cycle time without interruption of the cyclic program

In RUN-Redundant system state, the backup CPU has a time lag compared to the primary CPU. This time lag results from the time required for event-controlled synchronization of data from the primary CPU to the backup CPU.

The following figure shows the phases which the CPUs run through without an interruption of the cyclic program.
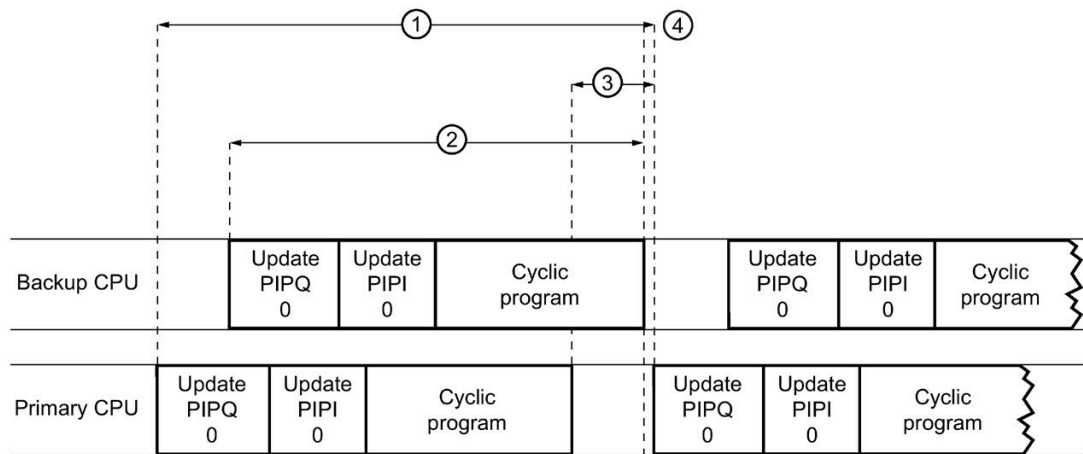
① Cycle time
② Cycle of the backup CPU
③ Time lag
④ Cycle end and start of the next cycle (cycle control point)

Figure 5-2   Cycle time without interruption of the cyclic program

The cycle time ① includes the cycle of the backup CPU ② and the time lag ③ of the backup CPU compared to the primary CPU. The time lag results from the time required for the synchronization of the data between primary CPU and backup CPU. The synchronization between primary CPU and backup CPU occurs automatically if required. The more data has to be synchronized between the CPUs during a cycle, the greater the time lag. The program cycle ends as soon as the backup CPU has reached the end of its cyclic program. The primary CPU starts the next cycle as soon as the backup CPU reports the cycle end to the primary CPU ④.

Extension of the cycle

As with non-redundant CPUs, an occurring event and the associated OB can extend the cycle. Events can occur both during the execution of the cyclic program and during the time lag.

In the following example the CPU must process a higher-priority OB (OB 30 with priority 7), while the primary CPU waits for the end of the cycle of the backup CPU. The figure below shows the phases which the CPUs run through in such a case.
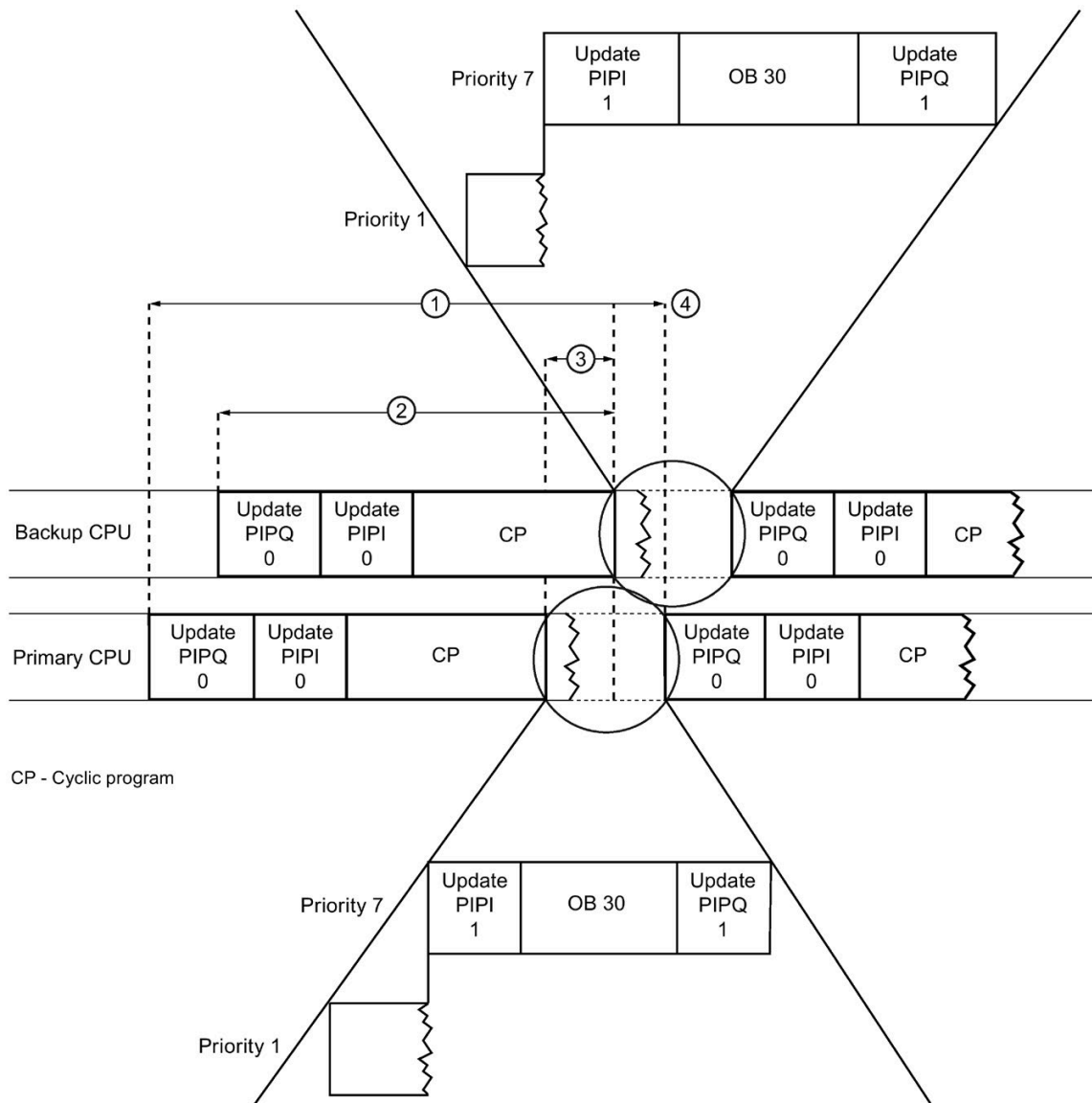
① Cycle time
② Cycle of the backup CPU
③ Time lag
④ Cycle end and start of the next cycle (cycle control point)

Figure 5-3   Processing of a higher-priority OB

Execution of the cyclic program (CP with priority 1) is complete. While the primary CPU waits for the end of the cycle of the backup CPU, a higher priority OB (OB 30 with priority 7) starts. The primary CPU starts the next cycle as soon as the following conditions have been fulfilled:

- The primary CPU has received the message from the backup CPU that the backup CPU has finished processing the cyclic program.

- The primary CPU has processed OB 30 and updated PIPQ1.

Note

Due to the change of the run level and the synchronization, interruptions of the program cycle by higher-priority OBs result in a higher load. Interruptions of the program cycle extend the cycle time.

Differences between the synchronization times

The available bandwidth has a significant impact on the synchronization time.

With the R-CPUs both the synchronization of data and the synchronization of communication tasks operate over the PROFINET ring. 25% of the bandwidth is reserved for the synchronization.

With the H-CPU, synchronization works independently of the PROFINET ring over fiber optic cables.

The table below provides an overview of performance features of R-CPUs and H-CPU.

Table 5- 4   Performance features of S7-1500R and S7-1500H

	S7-1500R		S7-1500H	
	CPU 1513R-1 PN	**CPU 1515R-2 PN**	**CPU 1517H-3 PN**	**CPU 1518HF-4 PN**

Performance	• Data transfer rate of 100 Mbps (for synchronization and communication)		• Significantly greater performance than S7-1500R due to
			  – Separate redundancy connections over fiber-optic cables
			  – Greater computing power
			  – Transmission rate of 1 Gbps (for the synchronization)	

	• Data work memory: max. 1.5 MB • Code work memory: max. 300 KB	• Data work memory: max. 3 MB • Code work memory: max. 500 KB	• Data work memory: max. 8 MB • Code work memory: max. 2 MB	• Data work memory: max. 60 MB • Code work memory: max. 9 MB

	S7-1500R		S7-1500H	
	CPU 1513R-1 PN	**CPU 1515R-2 PN**	**CPU 1517H-3 PN**	**CPU 1518HF-4 PN**
Hardware	• The CPUs are identical in design with the respective S7-1500 standard versions. • The synchronization of the CPUs takes place over the PROFINET ring. • The H-Sync-Forwarding function is recommended for all devices in the PROFINET ring. • Part of the bandwidth on the PROFINET cable is used to synchronize the CPUs. Less bandwidth is therefore available for PROFINET IO communication.		• The CPUs each have two optical interfaces. • The synchronization of the CPUs operates independently of the PROFINET ring over fiber-optic cables. • The bandwidth for PROFINET IO communication is not affected by the synchronization of the H-system.	

Technical specifications

More information about the technical specifications is available in the manuals of the specific CPUs.

5.3.4 Influences on the cycle time when a CPU fails

If one of the two CPUs fails during redundant operation, the other CPU controls the process alone. The system state then changes from RUN-Redundant to RUN-Solo. The CPU continues executing the user program in RUN operating state.

Note

Dead time in case of a CPU failure

On the failure of a CPU, the cycle time also contains a dead time of up to 300 ms for R-CPUs and up to 50 ms for the H-CPU. You must schedule this time as cycle time reserve for a CPU failure.

To avoid exceeding the maximum cycle time after a CPU failure, further increase the maximum cycle time by this value.


Note

Change of the system state from RUN-Redundant to Run-Solo by the user

If you deliberately trigger a change of the system state by switching the backup CPU to STOP via the display or with the "RH_CTRL" instruction (mode 9), for example, this will also extend the cycle time. However, the cycle time will not increase to the same extent as with switchover of the CPUs in the event of an error (failure of one of the CPUs).

Information on the causes for the failure of a CPU is available in the S7-1500R/H redundant system (https://support.industry.siemens.com/cs/ww/en/view/109754833) system manual.

Failure of the primary CPU

The figure below shows the impact of the failure of the primary CPU on the cycle time.
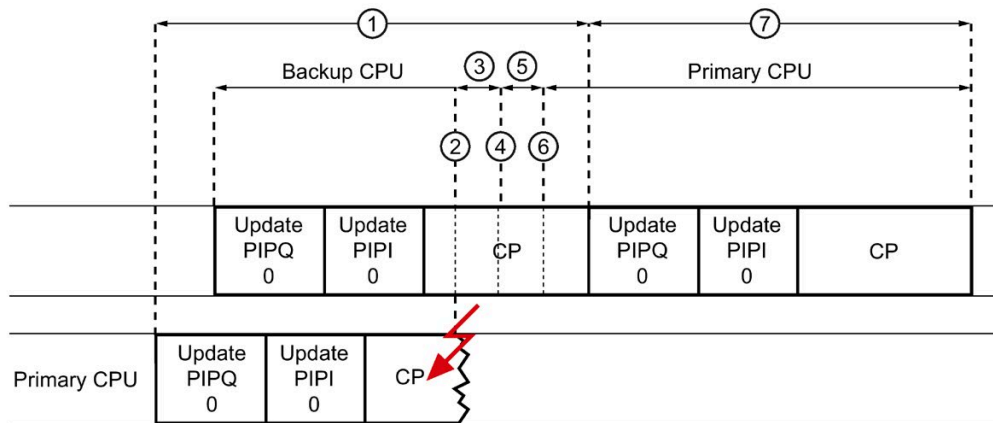
CP - Cyclic program

① Cycle time
② Failure of the primary CPU
③ Backup CPU continues processing the program
④ Backup CPU no longer receives synchronization telegrams
⑤ Backup CPU waits for the monitoring time to expire
⑥ End of the monitoring time, switchover time and system state transition
⑦ Cycle time of the new primary CPU in RUN operating state

Figure 5-4   Impact of the failure of the primary CPU on the cycle time

The example shows the failure of the primary CPU ② while it is processing the cyclic program. The primary CPU no longer sends any synchronization telegrams to the backup CPU. During the period ③, the backup CPU continues operating only on the basis of the synchronization data transferred before the failure of the primary CPU. At ④, the backup CPU has reached the point in the program where the primary CPU stopped sending synchronization telegrams. During the phase ⑤, the backup CPU waits to see whether data will again be sent from the primary CPU after all. Because no synchronization data is transferred until the monitoring time has expired, the backup CPU becomes the new primary CPU at point ⑥. The redundant system switches from RUN-Redundant system state to RUN-Solo system state.

The cycle time ① extends from the time processing of the cyclic program is started in RUN-Redundant to the time when processing of the cyclic program ends in RUN-Solo.

Because no more data is synchronized in the RUN-Solo system state, the cycle time ⑦ is shorter than the cycle time ①.


Note

Monitoring time

The monitoring time is an internal time with fixed duration. You cannot assign parameters for the internal time. The monitoring time starts as soon as synchronization data arrives on the respective CPU. If no synchronization data is received from the primary CPU, the system automatically performs a system state change (from RUN-Redundant to RUN-Solo) after the monitoring time has expired.

Failure of the backup CPU

The figure below shows the impact of the failure of the backup CPU on the cycle time.
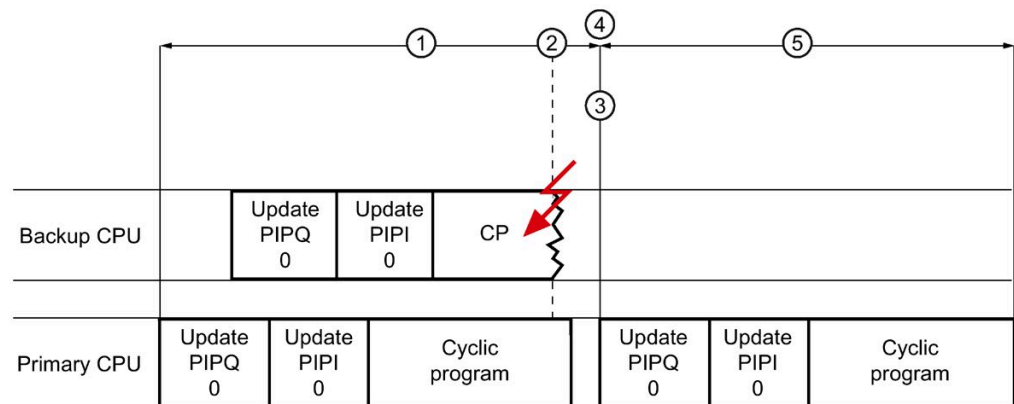
CP = Cyclic program

①	Cycle time
②	Failure of the backup CPU
③	Expiration of the monitoring time
④	System status transition
⑤	Cycle time of the primary CPU in RUN-Solo operating state

Figure 5-5   Impact of the failure of the backup CPU on the cycle time

The backup CPU fails before processing of the cyclic program has ended ②. The primary CPU detects the failure of the backup CPU because no synchronization data has been received until the monitoring time ③ has expired. The primary CPU terminates the synchronization with the backup CPU. The redundant system switches from RUN-Redundant system state to RUN-Solo system state ④.

Because no more data is synchronized in RUN operating state, the cycle time ⑤ is shorter than the cycle time ①.

5.4 Response time of R/H CPUs

### Relationship between the cycle time and response time

The cycle time of the system also forms the basis for its response time. The response time depends, among other things, on the cycle time of the individual program cycles.

Fluctuation of the response time

The actual response time fluctuates between one and two cycles during cyclic program execution. The actual response time fluctuates between one and two cyclic interrupt cycles for time-controlled program execution.

You should always assume the longest response time when configuring your system.

In the figure below the process image is updated immediately after the change of the encoder signal. The output can therefore respond to the signal change after a cycle has ended.
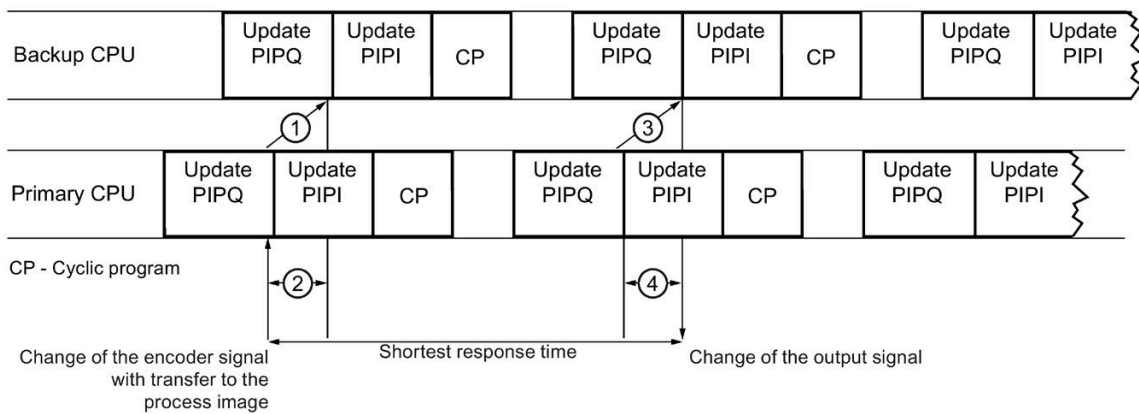
①	Synchronization of the encoder signal change in the backup CPU
②	Time lag of the backup CPU to the primary CPU
③	Synchronization of the output signal change in the backup CPU
④	Time lag of the backup CPU to the primary CPU until actual output of the signal change to the IO devices in the PROFINET ring

Figure 5-6   Shortest response time

In the figure below, the process image has already been updated by the time of the signal change. It therefore takes one cycle until the system detects the change and sets the input in the process image. The output signal is changed after an additional cycle.
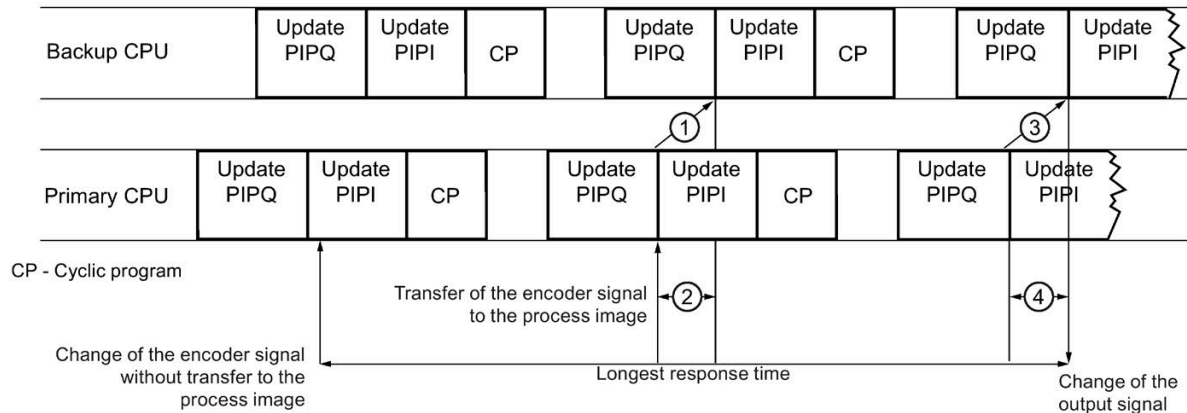
①   Synchronization of the encoder signal change in the backup CPU

②   Time lag of the backup CPU to the primary CPU

③   Synchronization of the output signal change in the backup CPU

④   Time lag of the backup CPU to the primary CPU until actual output of the signal change to the IO devices in the PROFINET ring

Figure 5-7   Longest response time

The cycle times include the time lag. The time lag of the backup CPU to the primary CPU depends on the synchronization load. The synchronization load results from the data to be synchronized in the user program and in the communication.

Note

Effect of the time lag

The synchronization and transfer of the changes requires computing time. The time lag therefore affects both CPUs (from the primary CPU to the backup CPU and from the backup CPU to the primary CPU). The slower the CPU and the slower and longer the synchronization connection, the greater the time lag.

Note

Response time when downloading a modified user program into the R/H CPUs in the RUN-Redundant system state

During the download process in the RUN-Redundant system state, the response time of the system is restricted compared with the normal redundant mode. The more changes the user program contains, the higher the impact on the response time.

Determination of cycle and response times

At the end of the cyclic program, the primary CPU waits until the backup CPU too has acknowledged the end of the cyclic program. The cycle time of the primary CPU therefore also includes the time lag of the backup CPU. The cycle is extended by the time lag.

Advantages

The fact that the cycle time includes the time lag of the backup CPU to the primary CPU offers the following advantages:

- By monitoring the cycle time in STEP 7, in the HMI or in the user program after SYNCUP, it is possible to determine the cycle time in the event of a failure of the primary CPU.

- During commissioning it is not necessary to perform complicated tests to determine whether the required response time can still be complied with if a CPU fails.

- During commissioning and ongoing operation you can estimate whether your automation task can meet the response times required for the process.

The same functions as those for the non-redundant CPUs are available for determining the cycle and response times:

Table 5- 5   Functions for determining the cycle and response times

Function	Additional information
Defining the minimum cycle time and the maximum cycle time in STEP 7	Section Cycle time (Page 25)
Defining the desired response of the user program if the maximum cycle time has been exceeded	
Reading out the cycle time statistics via STEP 7 and the display of the CPU	
Reading out the cycle time and reading out the progress in the SYNCUP system state with the instruction "RT_INFO"	• Section Different cycle times (Page 25) • STEP 7 online help
Display of measurements (traces) which record special time-critical signal characteristics	Function manual Using the trace and logic analyzer functions (https://support.industry.siemens.com/cs/ww/en/view/64897128)
Reading out the progress of the SYNCUP system state using the display of the CPU	S7-1500R/H redundant system (https://support.industry.siemens.com/cs/ww/en/view/109754833) system manual

5.5 Timetables for the RUN-Redundant system state

The following section describes the typical times of the CPUs of the S7-1500R/H redundant system in the RUN-Redundant system state.

Update times of the process image partitions

The following table contains the times for estimating the typical update times of the process image partitions.

Table 5- 6   Data for estimating the typical update time of the process image partitions

	Update times of the CPUs in the RUN-Redundant system state		
	CPU 1513R-1 PN	**CPU 1515R-2 PN**	**CPU 1517H-3 PN** **CPU 1518HF-4 PN**
Basic load for updating process image partitions	63 µs	57 µs	13 µs
Copy time for distributed I/O via PROFINET	6.5 µs/word	6.5 µs/word	2.6 µs/word

A table of the update times of the CPUs in the RUN-Solo system state is available in section Update time for process image partitions (Page 29).

Program execution time without interruptions

The user program has a certain runtime without interruptions. The runtime depends on the number of operations that are executed in the user program.

The following table contains the typical durations of operations.

Table 5- 7   Duration of an operation

	Program execution times of the CPUs in RUN-Redundant system state		
	CPU 1513R-1 PN	**CPU 1515R-2 PN**	**CPU 1517H-3 PN** **CPU 1518HF-4 PN**
Bit operations, typ.	80 ns	60 ns	4 ns
Word operations, typ.	96 ns	72 ns	6 ns
Fixed-point arithmetic, typ.	128 ns	96 ns	6 ns
Floating-point arithmetic, typ.	512 ns	384 ns	24 ns

A table of the program execution times of the CPUs in the RUN-Solo system state is available in section User program execution time (Page 32).

Extension due to nesting of higher-priority OBs and/or interrupts

The interruption of a user program at the end of an instruction by a higher-priority OB causes a certain basic time expenditure. Take account of this basic time expenditure in addition to the update time of the assigned process image partitions and the execution time of the contained user program. The following tables contain the typical times for the various interrupts and error events.

Table 5- 8   Basic time expenditure for an interrupt

	Basic time expenditure of the CPUs for an interrupt in the RUN-Redundant system state		
	CPU 1513R-1 PN	**CPU 1515R-2 PN**	**CPU 1517H-3 PN** **CPU 1518HF-4 PN**
Hardware interrupt	560 µs	430 µs	70 µs
Time-of-day interrupt	560 µs	430 µs	70 µs
Time-delay interrupt	560 µs	430 µs	70 µs
Cyclic interrupt	560 µs	430 µs	70 µs

A table of the time expenditure of the CPUs for an interrupt in the RUN-Solo system state is available in section User program execution time (Page 32).

Table 5- 9   Basic time expenditure for an error OB

	Basic time expenditure of the CPUs for an error OB in the RUN-Redundant system state		
	CPU 1513R-1 PN	**CPU 1515R-2 PN**	**CPU 1517H-3 PN** **CPU 1518HF-4 PN**
Programming error	560 µs	430 µs	70 µs
I/O access error	560 µs	430 µs	70 µs
Time error	560 µs	430 µs	70 µs
Diagnostic interrupt	560 µs	430 µs	70 µs
Module failure/recovery	560 µs	430 µs	70 µs
Station failure/recovery	560 µs	430 µs	70 µs

A table with the basic time expenditure of the CPUs for an error OB in the RUN-Solo system state is available in section User program execution time (Page 32).

Accuracy of a cyclic interrupt

Even if a cyclic interrupt is not delayed by a higher-priority OB or communication activities, the accuracy with which it is started is nevertheless subject to system-dependent fluctuations.

The following table shows the accuracy with which a cyclic interrupt is triggered:

Table 5- 10   Accuracy of cyclic interrupts

	Accuracy of cyclic interrupts of the CPUs in the RUN-Redundant system state		
	CPU 1513R-1 PN	**CPU 1515R-2 PN**	**CPU 1517H-3 PN** **CPU 1518HF-4 PN**
Cyclic interrupt	±5.8 ms	±3.2 ms	±1.6 ms

A table with the accuracy of cyclic interrupts of the CPUs in the RUN-Solo system state is available in section Time-driven program execution in cyclic interrupts (Page 52).

Note

Scope of validity

Please note that the accuracy data for the cyclic interrupt also applies to all other higher-priority execution levels/OBs.

Interrupt response times for hardware interrupts

The interrupt response times of the CPUs start with the occurrence of a hardware interrupt event in the CPU and end with the start of the assigned hardware interrupt OB.

This time is subject to system-inherent fluctuations, and this is expressed using a minimum and maximum interrupt response time.

The following table contains the length of the typical response times of the CPUs for hardware interrupts.

Table 5- 11   Interrupt response times for hardware interrupts

		Interrupt response times of the CPUs for hardware interrupts in the RUN-Redundant system state		
		CPU 1513R-1 PN	**CPU 1515R-2 PN**	**CPU 1517H-3 PN** **CPU 1518HF-4 PN**
Interrupt response times	Min.	180 µs	150 µs	40 µs
	Max.	1420 µs	1360 µs	470 µs

A table of the interrupt response times of the CPUs in the RUN-Solo system state is available in section Response time of the CPUs when program execution is event-controlled (Page 60).

Glossary

Backup CPU

Role of a CPU in the S7-1500R/H redundant system. If the R/H system is in RUN-Redundant system state, the primary CPU guides the process. The backup CPU processes the user program synchronously and can take over the process management if the primary CPU fails.

Cycle time

The cycle time represents the time a CPU requires to process the user program once.

Data block

Data blocks (DBs) are data areas in the user program that contain user data. The following data blocks exist:

- Global data blocks which you can access from all code blocks.

- Instance data blocks that are assigned to a specific FB call.

Diagnostic interrupt

See "Interrupt, diagnostic"

Diagnostics

Monitoring functions include:

- The detection, localization and classification of errors, faults and alarms.

- Displaying and further evaluation of errors, faults and alarms.

They run automatically during plant operation. This increases the availability of systems by reducing commissioning times and downtimes.

Diagnostics buffer

The diagnostics buffer represents a backup memory in the CPU, used to store diagnostics events in their order of occurrence.

Distributed I/O system

System with I/O modules that are configured on a distributed basis, at a large distance from the CPU controlling them.

Firmware of the CPU

In SIMATIC, a distinction is made between the firmware of the CPU and user programs.

The firmware is a software embedded in electronic devices, which means it is permanently connected with the hardware functionally. It is usually saved in a flash memory, such as EPROM, EEPROM or ROM, and cannot be replaced by the user or only with special means or functions.

User program: see glossary entry "User program"

H-Sync Forwarding

H-Sync forwarding enables a PROFINET device with MRP to forward synchronization data (synchronization frames) only within the PROFINET ring.

In addition, H-Sync forwarding forwards the synchronization data even during re-configuration of the PROFINET ring. H-Sync forwarding avoids a cycle time increase if the PROFINET ring is interrupted.

S7-1500R: H-Sync forwarding is recommended for all PROFINET devices with only 2 ports in the PROFINET ring. All PROFINET devices with more than 2 ports (e.g. switch) in the PROFINET ring must support H-Sync forwarding.

S7-1500H: H-Sync Forwarding is not relevant for redundant S7-1500H systems.

I/O module

Device of the distributed I/O that is used as interface between the controller and the process.

Interrupt

The CPU's operating system distinguishes between various priority classes that control the execution of the user program. These priority classes include interrupts, such as hardware interrupts. When an interrupt occurs, the operating system automatically calls an assigned organization block. The required response is programmed in the organization block (for example, in an FB).

Interrupt, cyclic

The CPU generates a cyclic interrupt periodically within a parameterizable time grid and then processes the corresponding organization block.

Interrupt, diagnostics

Diagnostics-capable modules signal detected system errors to the CPU using diagnostic interrupts.

Interrupt, hardware

A hardware interrupt is triggered by interrupt-triggering modules due to a certain event in the process. The hardware interrupt is reported to the CPU. The CPU then processes the assigned organization block according to the priority of this interrupt.

Interrupt, time-delay

The time-delay interrupt is one of the program execution priority classes of SIMATIC S7. The time-delay interrupt is generated after the expiration of a timer started in the user program. The CPU then processes the corresponding organization block.

Interrupt, time-of-day

The time-of-day interrupt is one of the program execution priority classes of SIMATIC S7. The time-of-day interrupt is generated depending on a specific date and time. The CPU then processes the corresponding organization block.

IO controller

See "PROFINET IO controller"

IO device

See "PROFINET IO device"

Operating states

Operating states describe the behavior of a single CPU at a specific time.

The CPUs of the SIMATIC standard systems have the STOP, STARTUP and RUN operating states.

The primary CPU of the redundant system S7-1500R/H has the operating states STOP, STARTUP, RUN, RUN-Syncup and RUN-Redundant. The backup CPU has the operating states STOP, SYNCUP and RUN-Redundant.

Organization block

Organization blocks (OBs) form the interface between the CPU operating system and the user program. The organization blocks determine the order in which the user program is executed.

Parameter

- Tag of a STEP 7 code block:

- Tag for setting the behavior of a module (one or more per module). In as-delivered state, every module has an appropriate basic setting, which you can change by configuring in STEP 7. There are static and dynamic parameters.

Parameters, dynamic

Dynamic parameters of modules can be changed during operation by calling an SFC in the user program, for example, limit values of an analog input module.

Parameters, static

Static parameters of modules cannot be changed by the user program but only by the configuration in STEP 7, e.g. input delay of a digital input module.

Primary CPU

If the R/H system is in RUN-Redundant system state, the primary CPU guides the process. The backup CPU processes the user program synchronously and can take over the process management if the primary CPU fails.

Process image (I/O)

The CPU transfers the values from the input and output modules to this memory area. At the start of the cyclic program, the CPU transfers the process image output as a signal state to the output modules. The CPU then transfers the signal states of the input modules into the process image input. The CPU then executes the user program.

PROFINET

PROcess **FI**eld **NET**work, open Industrial Ethernet standard which further develops PROFIBUS and Industrial Ethernet. A cross-manufacturer communication, automation, and engineering model defined by PROFIBUS International e.V. as an automation standard.

PROFINET IO

Communication concept for the realization of modular, distributed applications within the scope of PROFINET.

PROFINET IO controller

Device used to address connected I/O devices (e.g. distributed I/O systems). The IO controller exchanges input and output signals with assigned I/O devices. The IO controller often corresponds to the CPU in which the automation program is running.

PROFINET IO device

Distributed field device that can be assigned to one or more IO controllers (e.g. distributed I/O system, valve terminals, frequency converters, switches).

Redundancy connection

The redundancy connection in an S7-1500R system is the PROFINET ring with MRP. The redundancy connection uses part of the bandwidth on the PROFINET cable to synchronize the CPUs, which means the bandwidth is not available for PROFINET IO communication.

Contrary to S7-1500R, PROFINET ring and redundancy connection are separate in an S7-1500H. The two redundancy connections are fiber-optic cables which directly connect the CPUs to each other via synchronization modules. The synchronization of the H-system does not affect the available bandwidth for PROFINET IO.

Redundant systems

Redundant systems are identified by the fact that important automation components are available in multiple units (redundant). Process control is maintained if a redundant component fails.

Retentivity

A memory area whose content is retained even after a power failure and after a transition from STOP to RUN is retentive. The non-retentive bit memory area, timers and counters are reset after a power failure and after a STOP-RUN transition.

System states

The system states of the S7-1500R/H redundant system result from the operating states of the primary and backup CPU. The term system state is used as a simplified expression that identifies the operating states of the two CPUs that occur at the same time. The S7-1500R/H redundant system features the STOP, STARTUP, RUN-Solo, SYNCUP and RUN-Redundant system states.

TIA Portal

Totally Integrated Automation Portal

The TIA Portal is the key to the full performance capability of Totally Integrated Automation. The software optimizes all operating, machine and process sequences.

Timers

Timers are components of the CPU system memory. The operating system automatically updates the content of the "timer cells" asynchronously to the user program. STEP 7 instructions define the precise function of the timer cell (e.g. on-delay) and trigger its execution.

User program

In SIMATIC, a distinction is made between user programs and the firmware of the CPU.

The user program contains all instructions, declarations and data by which a system or process can be controlled. The user program is assigned to a programmable module (for example, CPU, FM) and can be structured in smaller units.

Firmware: see glossary entry "Firmware of the CPU"

Index

T

Time error OB
    OB 80, 27, 66
Times
    Basic expenditure for error OB, 35, 82
    Basic expenditure for interrupts, 34, 82
    Cyclic interrupts for S7-1500 CPUs, 53
    Cyclic interrupts for S7-1500R/H-CPUs, 83
    For one operation, 32, 35, 36, 36, 36, 82

U

Update times
    Backplane bus ET 200SP CPUs, 57
    PROFIBUS DP, 56
    PROFINET IO, 56
    S7-1500 CPUs, 30
    S7-1500R/H-CPUs, 81