D5.1 Final report on boron segregation and diffusion in silicon dioxide and simulation results for the demonstrator

Lead Beneficiary: Fraunhofer IISB

SEVENTH FRAMEWORK PROGRAMME

THEME ICT-1-3.1

Project # 216436

Table of Contents

1 EXECUTIVE SUMMARY 3

2 INTRODUCTION 4

3 CALIBRATION OF THE SEGREGATION MODEL FOR BORON 5

3.1 COMPARISON OF SIMS MEASUREMENTS WITH SIMULATIONS 5

3.2 FULL PROCESS AND DEVICE SIMULATION, COMPARISON OF ELECTRICAL CHARACTERISTICS 10

3.2.1 Process simulation using the two-phase segregation model 11

3.2.2 Process simulation using the three-phase segregation model 14

4 DISCUSSION OF THE RESULTS 19

5 CONCLUSIONS 21

6 REFERENCES 22

1 Executive Summary

The aim of the ATHENIS Task 5.1, process simulation methodology, was to develop a practical simulation approach for an adequate simulation of typical CMOS processes for conventional and high-voltage CMOS devices using state-of-the-art commercial simulation software. The state-of-the-art simulation tools of Synopsys were at the beginning of the project not able to reproduce the measured threshold voltages of CMOS transistors that were chosen at austriamicrosystems as target for this project. Therefore, a practical task was to reproduce the measured electrical properties of CMOS transistors of austriamicrosystems using the Sentaurus TCAD system of Synopsys. Since the major uncertainty in the process simulation is associated with the segregation of boron, we tested different models for boron segregation, chose the most promising one and performed a calibration of the model parameters in such a way that the profiles were compatible to the secondary ion mass spectroscopy (SIMS) measurements of dedicated experiments and that the basic electrical properties of four types of transistors were well reproduced in the simulation. The four transistor types considered are the NMOS and PMOS transistors with a supply voltage of 3 V as well as NMOS and PMOS transistors with a supply voltage of 5 V. A consistent set of the model parameters for boron segregation was obtained at the end of the project. The application of these parameters in process simulation resulted in threshold voltages that are in a good agreement with the measured ones for all the transistors considered in simulation. The model parameters for the simulation of boron segregation were transferred to austriamicrosystems and are now available for the simulation of other processes.

2 Introduction

At the beginning of the project, the state-of-the-art simulation tools of Synopsys were not able to predict the measured threshold voltages of the CMOS transistors chosen at austriamicrosystems as a challenging example. In particular, the usage of unipolarly doped gate electrodes for both NMOS and PMOS transistors in this technology was a challenge for the simulation. In this case, a complicated and very stringently defined doping profile which involves both boron and phosphorus doping impurities has to be realised in the channel of the PMOS transistors. Since the electrical properties of silicon essentially depend on the net-doping, i.e. on the difference between the donor (phosphorus) and acceptor (boron) doping, and since both boron and phosphorus are present in approximately the same concentrations, a stringent control of the net-doping profile requires a very high accuracy of simulation for each impurity. While the surface concentration of phosphorus is mainly determined by the diffusion coefficient in silicon, the concentration of boron near the surface is strongly impacted by the segregation of boron near the silicon-to-silicon-dioxide interface during the oxidation steps. Initial simulations done using commercial simulation tools that were available at the beginning of the project predicted positive threshold voltages for the PMOS transistors and an associated very high leakage. Compared to the measured (negative) threshold voltages, the deviation was was more than 1 V. In this project, we investigated possible reasons for the failure of the simulations, found a practicable solution and this document presents the results of these investigations and the model parameters that reproduce the electrical behaviour of CMOS transistors with a much better accuracy than at the beginning of the project.

An exhaustive analysis of the literature on boron segregation and diffusion in silicon dioxide was given in the intermediate report [1] earlier in this project. From this analysis we could conclude that the major uncertainty related to the simulation of CMOS transistors are the values of the segregation coefficient for boron which sensitively impact the boron concentration near the silicon surface. Therefore, in this report, we concentrate on the calibration of the boron segregation model with the aim to obtain adequate values of the threshold voltages for different types of CMOS transistors.

3 Calibration of the segregation model for boron

The threshold voltage of devices is one of the basic characteristic parameters of metal-oxide-semiconductor (MOS) devices. Its correct prediction is the goal of coupled process and device simulation. However, it is an unresolved problem in particular for technologies as used in this project where several types of MOS transistors with different gate oxide thicknesses and threshold voltages are realized on the same chip to cover the required range of supply voltages. To resolve the problems identified, the segregation and diffusion of boron in Si/SiO_2 was investigated in this task in close cooperation between austriamicrosystems, Fraunhofer IISB, and FBK. The calibration of the segregation model was done in two stages. First, an initial calibration was done using a comparison of simulated and measured boron profiles after some oxidation steps. Considering a finite depth resolution of the SIMS method on the one hand side, and an extreme sensitivity of the transistor properties to the doping concentration near the silicon surface on the other hand side, we came to the conclusion, that the SIMS method can only provide a qualitative indication for the boron concentration at the silicon surface. Therefore, a second stage of calibration was needed. In the second calibration stage, we varied parameters of the segregation models so that the threshold voltages for the four types of the transistors considered in this work were reproduced.

3.1 Comparison of SIMS measurements with simulations

It is known that boron is transported from silicon into oxide due to segregation during thermal oxidation. The segregation coefficient S is equal to the relation of the concentration of boron atoms at the surface of silicon to the concentration in silicon dioxide near the silicon-to-oxide interface. The segregation coefficient S depends on the oxidation temperature and is largely independent of the doping level. Therefore, experiments on boron segregation were performed at different temperatures and for different durations of oxidation.

Typical results on the redistribution of boron after dry oxidation are shown in Figure 1 and Figure 2. For both experiments, the oxidation temperature was 800 °C and the process duration was 50 min. For the former, the oxidation occurred in O2 while for the latter, the oxidation atmosphere was O2 with 0.8% HCl. On the figures, the measured profiles of boron near the silicon-to-oxide interface are compared with the simulated profiles. The measurements were performed at FBK using the SIMS method and simulations were done using the Sentaurus Process tool of Synopsys TCAD [2]. The initial distribution of boron

in silicon was homogeneous and the concentration amounted to $1 \cdot 10^{19}$ cm^{-3}. After the oxidation, SIMS measurements showed a by a factor of 4 to 5 higher concentration in the oxide and a by approximately the same factor lower concentration in silicon in comparison to the initial concentration. It should be noted that due to limited depth resolution of the SIMS measurements it is not possible to measure the boron concentration directly at the silicon surface. Nevertheless, there is a fair agreement between the measurement and simulation in silicon at depths larger that about 10 nm. The simulation results marked "STCAD" use the standard Sentaurus TCAD model for boron segregation, while the lines marked "STCAD, S=S0/10" refer to simulations for which the segregation coefficient of boron was set to a 10 times lower value than the default one.

As it is seen in Figure 1 and Figure 2, the major difference between two simulation results is at the silicon surface, where SIMS is unable to resolve the profile. At larger depths, the difference between the standard STCAD result and the result that uses a factor 10 lower segregation coefficient differ by less than 20%.

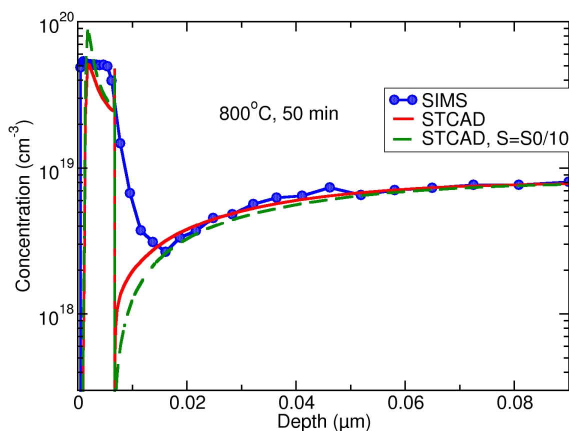

Figure 1: Boron profiles after dry oxidation of silicon samples at 800 °C for 50 min. Measurement (SIMS) and simulations (STCAD) using two different values for segregation coefficient are shown.

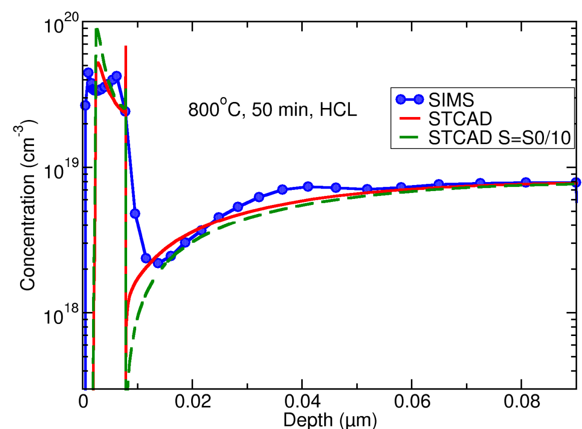

Figure 2: Boron profiles in silicon samples after dry oxidation with 0.8% HCL at 800 °C for 50 min. Measurement (SIMS) and simulations (STCAD) using two different values for segregation coefficient are shown.

Both the standard segregation model and a model with a factor 10 lower segregation coefficient reproduce well the experimental results at depths above 10 nm. The influence of HCL on the boron profile is seen, but is not significant for the comparison with simulation.

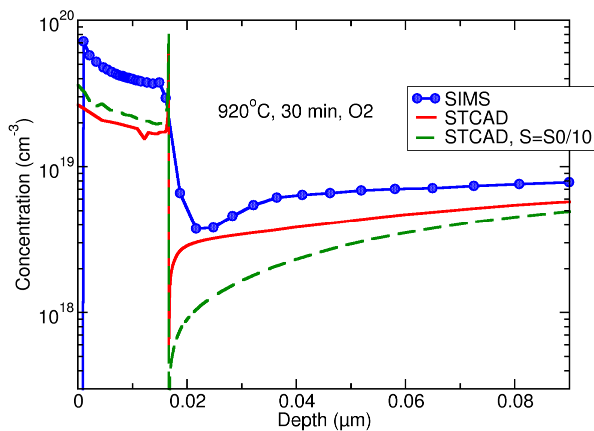

Figure 3: Boron profiles after dry oxidation of silicon samples at 920 °C for 30 min. Measurement (SIMS) and simulations (STCAD) using two different values for segregation coefficient are shown.

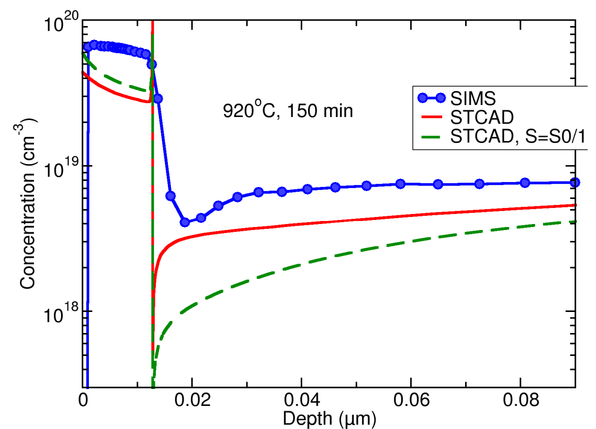

Figure 4: Boron profiles after dry oxidation of silicon samples at 920 °C for 150 min. Measurement (SIMS) and simulations (STCAD) using two different values for segregation coefficient are shown.

In Figure 3 and Figure 4, boron segregation during the dry oxidation at a higher temperature of 920°C is shown and compared to the respective simulation results. The first simulation marked STCAD used the standard segregation coefficient for boron and the second simulation (STCAD, S=S0/10) used a factor 10 lower segregation coefficient.

There is a larger difference between measurements and simulations at 920°C in comparison to that at 800°C. In both variants of the simulation, the measured boron concentration in both the oxide and in the silicon exceeds the simulated profiles. Nevertheless, the ratio of the boron concentration in silicon to the concentration in oxide which is the measure of segregation is similar in measurements and in simulations. Since mass conservation is obeyed in the simulations, the differences indicate either inhomogeneity in the initial doping of the samples used or uncertainties in the concentration calibration of the SIMS profiles. Since for the reliable prediction of the threshold voltages the absolute concentration of doping near the silicon surface is important, both the segregation and diffusion models must provide more accurate results on doping concentration near the surface than the standard models do.

The basic two-phase segregation model parameters for the calculation of the segregation coefficient and the transport coefficient at the silicon to oxide interface are presented in Table 1.

Table 1: Parameters of the two-phase segregation model of boron in Sentaurus Process (Version C-2009.06) and in ICECREM [4]

Parameter name	Prefactor	Activation energy (eV)
SPROCESS Segregation coefficient	404.66	0.822
SPROCESS Transport coefficient ($cm \cdot s^{-1}$)	$1 \cdot 10^4$	2.0
ICECREM Segregation coefficient	20.0	0.52

Although the values of the prefactors differ in the process simulators Sentaurus Process and ICECREM by a factor of about 20 in the formula for the segregation coefficient, the values of the segregation coefficients for the temperature range of the oxidation processes used are similar in both programs. For example S=0.226 in Sentaurus Process and S=0.175 in ICECREM for 1000 °C. The transport coefficient is only defined in Sentaurus Process, in ICECREM the segregation condition without any time delay is assumed.

In order to simulate the effect of boron accumulation at the silicon-to-oxide interface, another segregation model is available in Sentaurus Process, namely the three-phase segregation model.

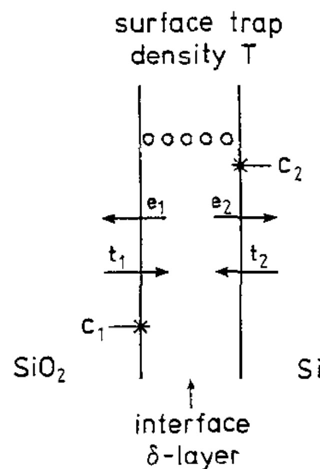

Figure 5: Description of the SiO_2/Si interface in the three-phase segregation model (from [3]).

It was first proposed by Lau and coworkers [3] and is implemented in Sentaurus Process under the name ThreePhaseSegregation. It describes the Si/SiO2 interface with three areas: SiO2, Si and an interface layer assumed to be a δ–layer. It is illustrated in Figure 5.

The three-phase segregation model has five parameters, four fluxes and one trap density, all temperature dependent, which offers more flexibility than the two-phase model, which has only two parameters. The results of three-phase model are illustrated in Figures Figure 6 and Figure 7 where boron segregation after a dry oxidation at 800 °C, 16 min, with 0.8% HCl, was simulated using different models and variants of model calibration.

As can be seen in Figure 6, the three-phase segregation model allows simulating boron redistribution at the oxide/silicon interface, like the two-phase model. A set of parameters was found that allows simulating the SIMS profiles with the three-phase segregation model. However, care must be taken when using these parameters, as is illustrated on Figure 7. Due to a limited depth resolution of the SIMS method, an exact observation of the boron concentration near the silicon surface is not possible. Only the concentration of boron in the oxide and the concentration in silicon at depths larger than about 10 nm can be measured reliably. It can be seen that it is possible to use two different calibrations (Calibration 1 and 2), and yet to obtain simulation results in agreement with the SIMS profiles at larger depths. In this example, in Calibration 2, the prefactor for the trapping rate on the silicon side was set to 1·10-9 cm3.s-1 instead of 4·10-9 cm3.s-1 and all other parameters are the same as in Calibration 1. This means that the SIMS profiles are not accurate enough to give a unique calibration for the three-phase model.

The calibration presented in Table 2 allows simulating the SIMS profiles, but the accuracy of the three-phase model coefficients is not good enough to ensure the accuracy of the electrical simulations of the transistors shown in the sections below. More accurate experimental data on profile measurements, possibly using alternative methods that can ensure a better depth resolution near the silicon surface, would have been needed to refine the calibration.

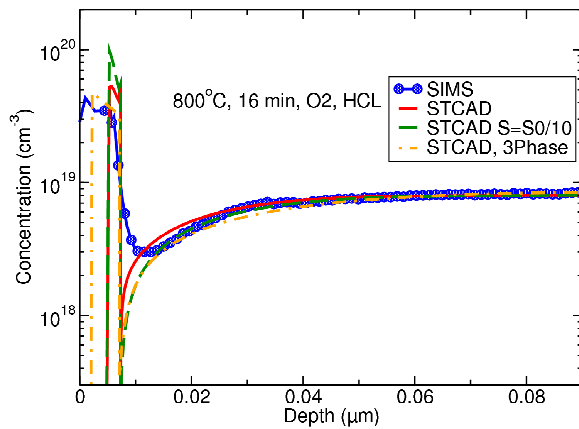

Figure 6: Boron profiles after dry oxidation of silicon samples with 0.8% HCl at 800 °C for 16 min. Measurement (SIMS) and simulations using the two-phase (STCAD, STCAD S=S0/10) and the three-phase model (STCAD, 3Phase) are shown..

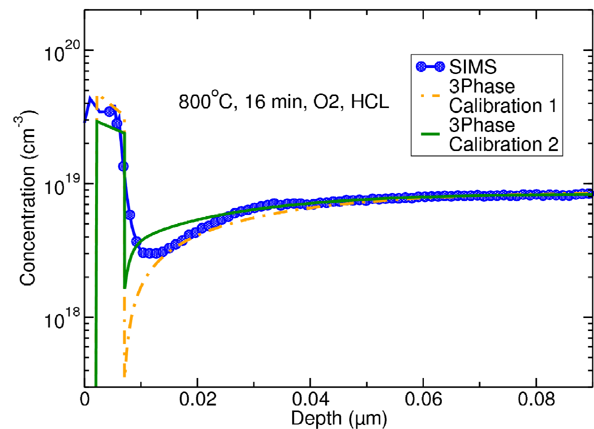

Figure 7: Boron profiles in silicon after dry oxidation with 0.8% HCl at 800 °C for 16 min. Measurement (SIMS) and simulations using the three-phase model with two different calibration versions (Calibration 1 and 2) are shown.

The parameters of the calibration set “Calibration 1” are summarised in Table 2.

Table 2: Calibration parameters “Calibration 1” for the three-phase segregation model in Sentaurus Process obtained from comparison to SIMS profiles

Parameter name	Prefactor	Activation energy (eV)
Trapping rate on Si side ($cm^3.s^{-1}$)	$4{\cdot}10^{-9}$	2.5
Emission rate on Si side ($cm^3.s^{-1}$)	$5{\cdot}10^{-8}$	2.05
Trapping rate on oxide side ($cm^3.s^{-1}$)	$4{\cdot}10^{-5}$	3.0
Emission rate on oxide side ($cm^3.s^{-1}$)	$5{\cdot}10^{-6}$	2.46
Trap density (cm^{-2})	$6{\cdot}10^{20}$	2.0

3.2 Full process and device simulation, comparison of electrical characteristics

As already known from the simulations performed earlier in this project, simulations using standard simulation tools lead to wrong predictions of the threshold voltages of the CMOS transistors. Especially large deviations were observed for p-channel transistors in which the net doping level near the silicon surface is formed by a difference of the concentrations

of boron and phosphorus doping. If standard models of Sentaurus Process were used, p-channel transistors do not close at zero gate voltage and the leakage current in the simulations is too high. This can be explained either by a too high doping level of boron in PMOSFETs and/or by an uncertainty in the value of the work function of the gate electrode in these transistors. The gate electrode uses the same material for all transistors that were considered in simulations in this project.

The gate electrode in the transistors considered here consists of a double layer: the lower layer is the n-doped polysilicon layer of about 100 nm thickness and the upper layer is made of tungsten silicide. Such electrodes are also called polycide gate electrodes. There are measurements of work function of such electrodes known in the literature and the work function of such polycide gates lies between the workfunction of n^+-doped polysilicon gates (Φ_M = 4.14 eV) and the workfunction of a tungsten silicide gate without a polysilicon layer (Φ_M = 4.82 eV). The measured workfunction of tungsten polycide gate for a polysilicon layer thickness of 100 nm was 4.38 eV [5], i.e., 0.24 V higher than that of an n^+-doped polysilicon gate. Based on these measurements, we used in all electrical simulations of CMOS transistors a workfunction of the tungsten polycide gate electrodes which is 0.2 V higher than that of n^+-doped polysilicon gate.

3.2.1 Process simulation using the two-phase segregation model

When applying a standard segregation model (two-phase segregation model) for boron in Sentaurus Process, we observed that if an oxidation at some lower temperature, e. g. at 800°C, is followed by an inert annealing process at a higher temperature, e.g. at 1000°C, a large amount of boron diffuses back from the oxide into the silicon. This leads to a significant boron concentration peak appearing at the silicon surface. This kind of back-diffusion was also observed in simulations if the transport coefficient between the silicon and oxide was set to zero in Sentaurus Process. Such a back-diffusion, at least for zero transport coefficient, is unphysical and is a consequence of an erroneous numerical implementation of the two-phase segregation model in Sentaurus Process. After we found this, we tried to use an alternative simulator for the simulation of the boron profiles in the channel of CMOS transistors. Therefore, for the simulation of the doping distribution in the channels of CMOS transistors we applied the process simulator ICECREM [4], developed earlier at Fraunhofer IISB. Preliminary tests showed that ICECREM does not create the boron surface peaks associated with an artificial back-diffusion into silicon appearing when the temperature of an inert anneal exceeds that of a preceding oxidation step.

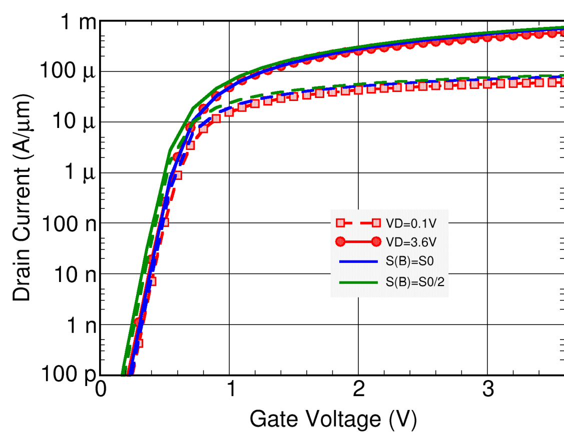

Figure 8: Transfer characteristics of 0.35 µm 3 V NMOS transistor. Comparison of measurement and simulations.

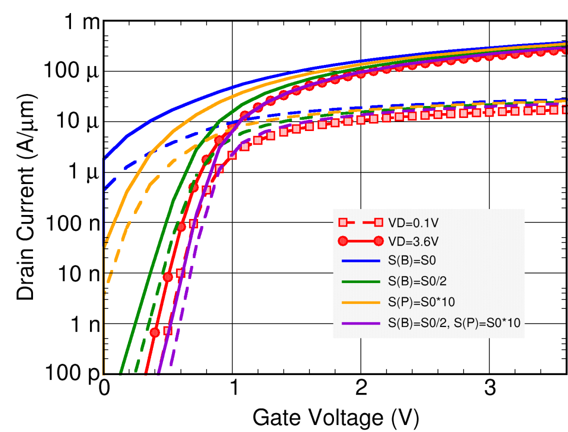

Figure 9: Transfer characteristics of 0.35 µm 3 V PMOS transistor. Comparison of measurement and simulations.

The results of coupled process and device simulations for CMOS transistors for a low-voltage process (supply voltage of 3V) are presented in Figure 8 and Figure 9. The red lines with circle and square symbols represent the results of measurements for two values of the drain voltage VD of 0.1 V and 3.6 V. The blue lines in Figure 8 and Figure 9 show the results of device simulations (solid lines for VD=3.6 V, dashed for VD=0.1 V) using the doping distributions in the channel of the transistors obtained by the default ICECREM segregation and diffusion simulation. The green lines in Figure 8 and Figure 9 show the analogous results obtained using a factor 2 reduced segregation coefficient of boron in comparison to the default segregation coefficient of ICECREM. In Figure 9, also variations of the segregation coefficient of phosphorus are investigated. The yellow lines show the transfer characteristics for the case that segregation coefficient of phosphorus was enlarged by a factor of 10 for a standard segregation of boron, and magenta coloured lines show the combined effect of a reduction of the boron segregation coefficient by a factor of 2 and an increase of the segregation coefficient of phosphorus by a factor of 10. All solid lines are for a drain voltage VD of 3.6 V and the dashed lines are for VD=0.1 V. From Figure 8 and Figure 9 it can be concluded, that if a segregation coefficient of boron equal to one half of the segregation coefficient of the ICECREM standard model is used, threshold voltages of both NMOS and PMOS can be reproduced with a deviation of less than 150 mV. An additional enhancement of the phosphorus segregation coefficient can improve the simulation result for the threshold voltage of PMOS transistors, so that a zero deviation for the threshold voltage of PMOS transistors can be achieved.

To sum up, the simulation can reproduce the values of the threshold voltages for NMOS and PMOS transistors with a supply voltage of 3 V under certain conditions:

1) An about 0.2 V higher workfunction has to be assumed in the polycide gate electrode in comparison to the n^+-doped polysilicon gate electrode;

2) The artificial backward diffusion from the oxide into silicon appearing in Sentaurus Process (Version C-2009.06) when the temperature is increased after an oxidation step has to be eliminated (this is done here using ICECREM simulations for the channel dopants);

3) The segregation coefficient of boron has to be reduced by a factor of about 2 and the segregation coefficient of phosphorus has to be enhanced by a factor between about 2 and 10. The suggested modifications of the segregation coefficients do not contradict the available experiments. The enhancement of the segregation coefficient for phosphorus only means that less phosphorus is remaining in oxide during the oxidation (default is S(P)=0.1, suggested S(P)=0.01).

Figure 10 and Figure 11 show the simulated transfer characteristics obtained for CMOS transistors if the variant of the process flow envisaged for 5 V supply voltage is used. The same simulation tools and models were used for the 5 V CMOS transistors as for the 3V CMOS transistors shown before in Figure 8 and Figure 9. Again, solid lines are for the drain voltage of 3.6 V, dashed ones for VD=0.1 V. Blue lines are for the default segregation and diffusion models in ICECREM simulation of the channel dopant distributions. S(B)=S0/2 means that the default segregation coefficient of boron was divided 2 in ICECREM simulation. S(P)=S0*10 means that the default segregation coefficient of phosphorus in ICECREM was multiplied by 10.

Similar to the results shown before, the same assumptions for the physical models lead to a consistent prediction of the threshold voltages also for 5V CMOS transistors. Approximately equal threshold voltages of about 0.6 V can be obtained for both NMOS and PMOS 5 V transistors if the segregation coefficients are modified as discussed before. This means that a consistent set of segregation coefficients can be found in terms of a standard two-phase segregation model (we call this set “ATHENIS 1” in the following) to reproduce the experimentally observed values of the threshold voltages for all four transistor types considered.

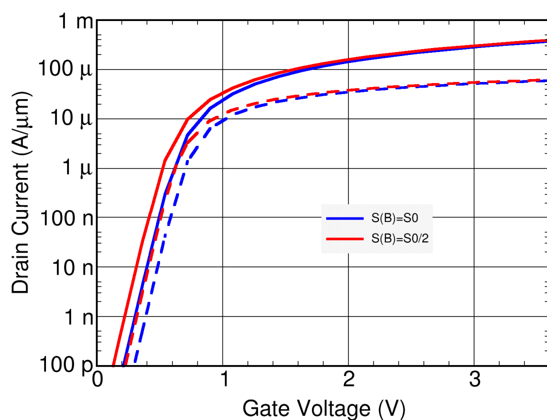

Figure 10: Transfer characteristics of 0.35 µm 5 V NMOS transistor. Impact of different segregation coefficients for boron.

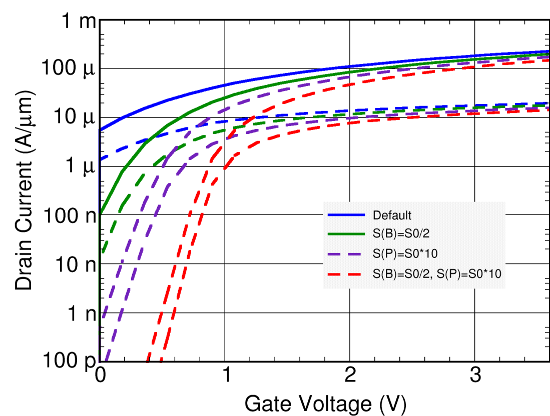

Figure 11: Transfer characteristics of 0.35 µm 5 V PMOS transistor. Impact of different segregation coefficients for boron and phosphorus.

3.2.2 Process simulation using the three-phase segregation model

In the previous section, we demonstrated a successful calibration of the two-phase segregation model for the process flow given by austriamicrosystems as a challenging example for this project. On the other hand side, the erroneous implementation of the two-phase segregation model in Sentaurus Process (Versions C-2009.06 and D-2010.03) did not allow to use this model in practical simulations in an industrial environment. Therefore, to allow our industrial partner to use the results of this project applying only commercial software (Sentaurus TCAD), we decided to perform the calibration of the three-phase segregation model implemented in the Sentaurus Process and recommended by Synopsys as a main choice in their Advanced Calibration package. The calibration of the three-phase segregation model was done in two variants. In the first variant, only electrical characteristics of the simulated transistors were considered as the goal of the model optimization. Since the doping distribution in silicon dioxide does not influence the electrical properties of silicon, only the doping distribution in the silicon was optimized during this kind of model calibration. The boron distribution in the silicon dioxide remains not optimized in this approach and results from the basic properties of the three-phase segregation model. In the second calibration variant, two goals were included in the objectives when optimizing the segregation parameters: the electrical transfer characteristics of the transistors and the value of the relative jump of the concentration of

boron when going from silicon to silicon oxide. The latter was estimated from the evaluation of the SIMS profiles measured in this project. Two versions of Sentaurus Process were used in model calibration: C-2009.06 and D-2010.03. There were some differences found in the results between the two versions but they relate to the activation of the impurities but not to the implementation of the three-phase segregation model for boron. The following graphs (Figure 12) show the main results obtained after the calibration of the parameters of the three-phase segregation model for boron in Sentaurus Process

As it can be seen in Figure 12, the boron profiles in the channel of the NMOS transistors are almost identical for the two versions of the three-phase model calibration. The second calibration version exhibits a larger concentration jump at the silicon-to-oxide interface, and in this manner, better agreement with the SIMS measurements. The electrical characteristics of the NMOS transistors depend only on the doping distribution in silicon, therefore they are expected to be independent of the version of the model calibration.

.

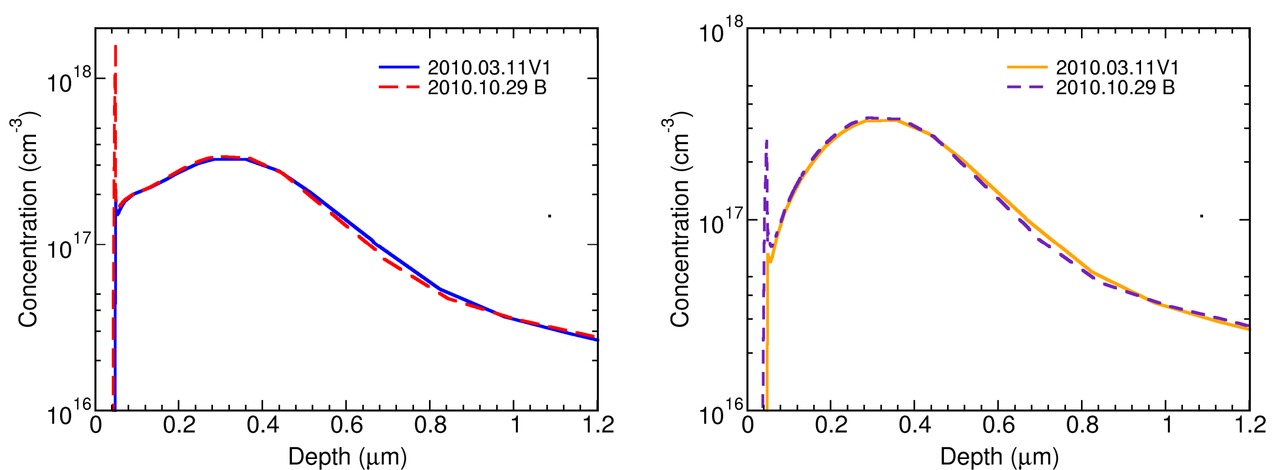

Figure 12: Simulated boron depth profiles in the middle of the channel of NMOS transistors with supply voltages of 3 V (left) and 5 V (right), continuous line is for the calibration version “ATHENIS 2” of March 11, 2010, dashed line is for the calibration version “ATHENIS 3” of October 29, 2010

Figure 13 not only shows the boron profiles but also the profiles of phosphorus and the resulting net doping profiles because both boron and phosphorus profiles are important for the PMOS transistors considered. For both transistors, with 3 V and 5 V supply voltage, an approximately equal concentration of boron and phosphorus near the surface and a deep depletion of the net doping due to a compensation of n and p-doping is observed. Although

the net doping profiles are rather similar for two versions of calibration, there is a slight difference in the boron concentration near the silicon surface. This difference in the profiles causes also some difference in the electrical characteristics.

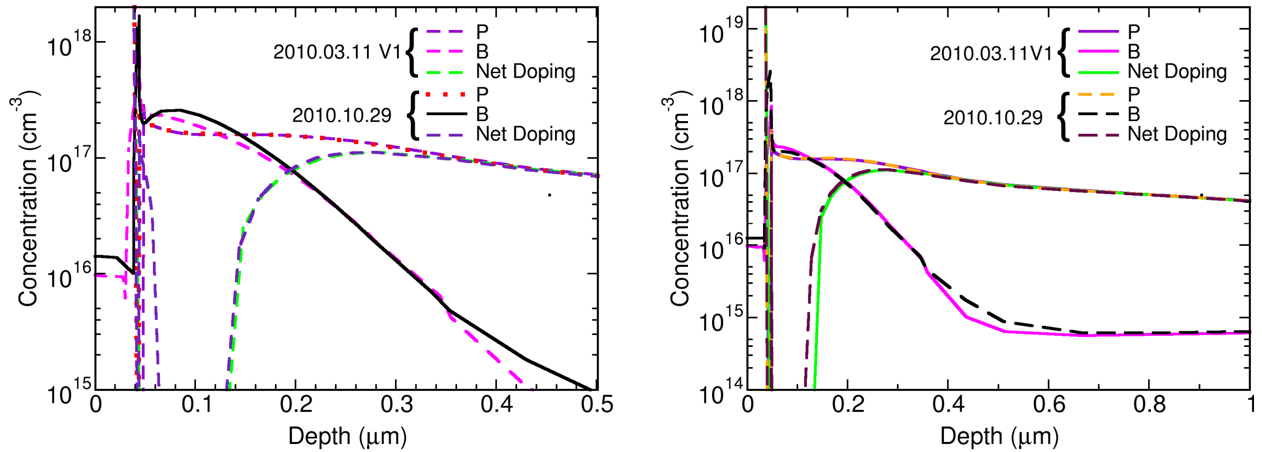

Figure 13: Simulated boron, phosphorus and net doping depth profiles in the middle of the channel

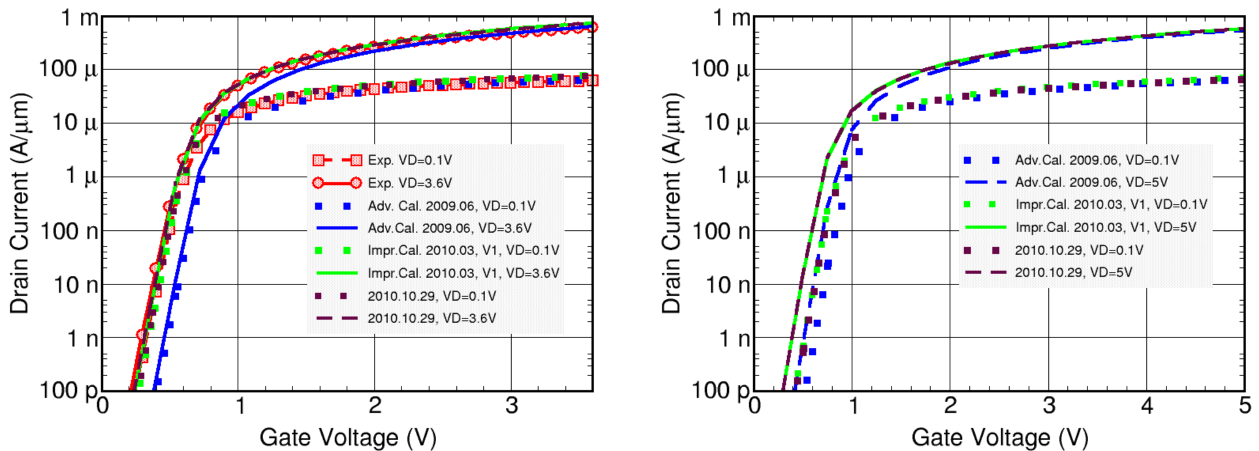

Figure 14: Simulated transfer characteristics of NMOS transistors with supply voltages of 3 V (left) and 5 V (right), legends indicate the experimental results (Exp.) and calibration versions given by the version date, also the drain voltages (VD) are given

Figure 14 shows the transfer characteristics of the NMOS transistors for 3 V and 5 V supply voltage. The simulations shown were performed with three versions of three-phase segregation model for boron. The lines marked “Adv. Cal. 2009.06” were obtained using the Advanced Calibration parameters for the three-phase segregation model in the Sentaurus Process Version C-2009.06. Version “ATHENIS 2” of the three-phase model calibration of this project is marked as “Impr. Cal. 2010.03 V1” and version “ATHENIS 3” is marked as “2010.10.29”. Both calibration versions give equal transfer characteristics for

NMOS transistors. A good agreement of our calibration with experiment is obvious from the left part of Figure 14. The Advanced Calibration parameters of Synopsys produce approximately 200 mV higher values of the threshold voltages for NMOS transistors for 3 and 5 V.

Figure 15 shows the transfer characteristics of the PMOS transistors. It should be noted that the x-axis of this figure corresponds to the absolute values of the gate voltage for an easier comparison to the NMOS transistors. As for the NMOS transistors, the same three variants of the simulations are shown. The Advanced Calibration of Synopsys predicts a completely inadequate threshold voltage for the 3 V PMOS transistors, so that a very high leakage current of 10 µA/µm is obtained in the simulation. Two versions of our calibrations of the three-phase segregation model (Impr. Cal. 2009.03 V1 – ATHENIS 2, and 2010.10.29 – ATHENIS 3) show a good agreement with the measured transfer characteristic for the drain voltage of 3.6 V presented in the left part of the figure. The simulations for transfer characteristics measured at the drain voltage of 0.1 V produce a somewhat lower threshold voltage than in the measured characteristic. This means that the effect of the drain-induced barrier lowering is less pronounced in the simulation. This can be an indication that the simulated boron distribution near the surface differs somewhat from the actual distribution.

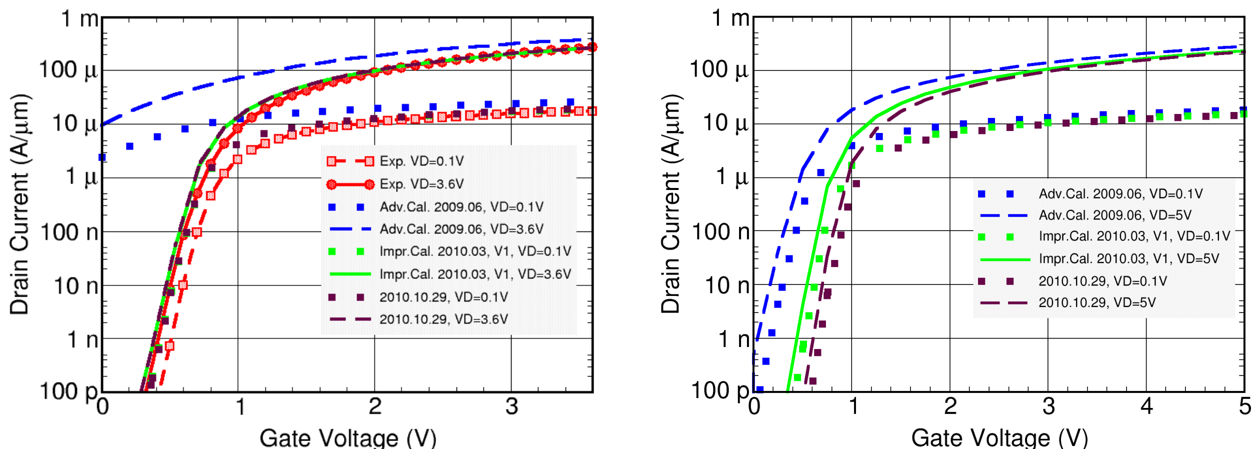

Figure 15: Simulated transfer characteristics of PMOS transistors with supply voltages of 3 V (left) and 5 V (right), legends indicate the experimental results (Exp.) and calibration versions given by the version date, also the drain voltages (VD) are given

For 5 V PMOS transistors, the threshold voltages defined for a constant drain current, for example at 100 nA/µm, vary between 0.4 and 0.9 V, dependent on the parameters of the

segregation model. Table 3 and Table 4 present the calibration results “ATHENIS 2” and “ATHENIS 3”, respectively, that were used in the full process simulation. The lowest threshold voltage is predicted by the Advanced Calibration model, the highest threshold voltage resulted from the calibration version “ATHENIS 3” of this work. The calibration version “ATHENIS 2” of this work is in the middle and corresponds well to the expected threshold voltages.

Table 3: “ATHENIS 2” calibration of the three-phase segregation model obtained using a comparison of full process simulations to electrical data only

Parameter name	Prefactor	Activation energy (eV)
Trapping rate on Si side ($cm^3.s^{-1}$)	$5{\cdot}10^{-13}$	2.5
Emission rate on Si side ($cm^3.s^{-1}$)	$5{\cdot}10^{-13}$	2.2
Trapping rate on oxide side ($cm^3.s^{-1}$)	$4{\cdot}10^{-13}$	2.5
Emission rate on oxide side ($cm^3.s^{-1}$)	$5{\cdot}10^{-17}$	1.96
Trap density (cm^{-2})	$5{\cdot}10^{20}$	1.0

Table 4: Final “ATHENIS 3” calibration of the three-phase segregation model used to simulate the full process flow

Parameter name	Prefactor	Activation energy (eV)
Trapping rate on Si side ($cm^3.s^{-1}$)	$3.1{\cdot}10^{-13}$	2.5
Emission rate on Si side ($cm^3.s^{-1}$)	$5{\cdot}10^{-13}$	2.2
Trapping rate on oxide side ($cm^3.s^{-1}$)	$5{\cdot}10^{-14}$	2.5
Emission rate on oxide side ($cm^3.s^{-1}$)	$1{\cdot}10^{-16}$	1.96
Trap density (cm^{-2})	$5{\cdot}10^{20}$	1.0

4 Discussion of the results

Table 5 summarizes the results of the simulations for the four transistor types considered in this work. The values of the threshold voltages were calculated as gate voltages at which the drain current reaches the value of 100 nA/µm. The table presents the threshold voltages of the transistors simulated using different sets of parameters for different segregation models. The threshold voltages have been extracted from the transfer characteristics simulated at drain voltages equal to the supply voltage, for 3V transistors the supply voltage was equal to 3.6 V and for 5 V transistors, a supply voltage of 5.0 V was used.

Table 5: The V_t values (in V) for 0.35 µm MOSFETs for various sets of coefficients of the segregation model.

Calibration	NMOS 3V	NMOS 5V	PMOS 3V	PMOS 5V
Default Sentaurus	0.62	0.61	+2.4	+1.6
AC-2009.06	0.62	0.71	+1.0	-0.31
ATHENIS 1	0.40	0.41	-0.70	-0.71
ATHENIS 2	0.47	0.59	-0.57	-0.65
ATHENIS 3	0.47	0.59	-0.57	-0.81
ATHENIS Target	0.5	0.6	-0.6	-0.6

The line marked “Default Sentaurus” shows the threshold voltages obtained at the beginning of the projects using the default Sentaurus TCAD models. The default models give an acceptable prediction of the threshold voltages for NMOS transistors. In contrast, the threshold voltages of PMOS transistors both for 3 V and 5 V are completely inadequate and have positive values instead of the negative values expected for PMOS transistors.

The line marked “AC-2009.06” shows the results that have been obtained using the Advanced Calibration model set as recommended by Synopsys in the Release C-2009.06. Besides, a correction of the workfunction for thin tungsten polycide gate electrodes as described above was applied. This correction was also applied for all other simulations in this work except for the first one with the default Sentaurus models. The usage of the Advanced Calibration model set somewhat improves the agreement with the project targets

for the threshold voltages. Nevertheless, the deviation of the threshold voltage from the expected value for PMOS 3V remains too large and amounts more than 1.5 V.

The next line marked “ATHENIS 1” summarizes the results of the simulations using the two-phase segregation model and the process simulator ICECREM in which this model is implemented correctly. The segregation model “ATHENIS 1” uses the segregation coefficients of ICECREM divided by 2 for boron and multiplied by 10 for phosphorus, as presented before. When using this model, threshold voltages of all four transistors are in the proper range and deviate from the target not more than 0.1 V. This means that this model solves the problem of the drastic deviation of the threshold voltages for PMOS transistors. An even more accurate calibration is, in principle, possible with this model, but it was not pursued in the project because a heterogeneous software environment (Sentaurus TCAD and ICECREM) would have to be used in this case creating difficulties in practical usage.

The results named “ATHENIS 2” and “ATHENIS 3” were obtained using the simulations with Sentaurus TCAD in which the three-phase segregation model was applied for boron. The parameters of the three-phase segregation model in the version “ATHENIS 2” were optimized to reproduce the target threshold voltages as specified here. In the calibration “ATHENIS 3”, additionally the concentration jump of boron doping at the silicon to oxide interface was included in the objectives. Both calibration variants produce adequate threshold voltages that are in correspondence with the targets of the project. The deviations from the targets are 50 mV or less in the case of “ATHENIS 2” calibration. Taking into account the special design of the PMOS transistors of this CMOS generation in which both phosphorus and boron doping must be reproduced with high accuracy, and considering a complete failure of the standard software to reproduce the threshold voltage of this kind of PMOS transistors, the achieved accuracy of the calibration means an excellent progress.

The obtained sets of model parameters were transferred to austriamicrosystems and can be used for simulation of CMOS transistors of the 0.35 μm generation and also of smaller transistors in which the requirements for the accuracy of the near surface-profiles are somewhat relaxed because of the usage of n-doped polysilicon for NMOS transistors and p-doped polysilicon for PMOS transistors.

5 Conclusions

A consistent process simulation model was found to predict the threshold voltages of CMOS transistors using the 0.35 µm process flow of austriamicrosystems. We present here three versions of the segregation model which are capable to reproduce the expected threshold voltages of four types of the transistors of the 0.35 µm CMOS generation with the unipolarly doped tungsten polycide gate.

The first version of the model uses the two-phase segregation model for boron and phosphorus segregation and only prefactors of the segregation coefficients of boron and phosphorus were modified, in comparison to the model implemented in the program ICECREM, to obtain a decent calibration of the model with an accuracy of about 0.1 V for the threshold voltages.

The second and third versions of the boron segregation model use the three-phase segregation model implemented in Sentaurus Process of Synopsys. We optimized the model coefficients in such a manner that the threshold voltages of the four types of the transistors can be reproduced with the same set of model parameters with an accuracy of about 50 mV.

The optimized model parameters obtained in this project were transferred to austriamicrosystems for further usage in industrial environment.

6 References

[1] ATHENIS Project, EC ICT 216436, Intermediate Status Report on Boron Segregation and Diffusion in Silicon Dioxide, Fraunhofer IISB, July 2009

[2] Sentaurus TCAD, Synopsys 2009, Release C-2009.06

[3] A Model for Phosphorus Segregation at the Silicon-Silicon Dioxide Interface, F. Lau, L. Mader, C. Mazure, Ch. Werner and M. Orlowski, Applied Physics A: Materials Science & Processing, Volume 49, Number 6, pp. 671-675, 1989

[4] ICECREM, Simulation Program for Processing Steps in Semiconductor Production, Version 4.3, Fraunhofer IISB, 1996

[5] T. J. Hwang, S. H. Rogers, and B. Z. Li, Work function measurement of tungsten polycide gate structures, J. of Electronic Materials, vol. 12, No. 4, pp. 667-678, 1983