Mark Edward Dean

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EDUCATION

Ph.D. Electrical Engineering, Stanford University, Stanford, CA (9/89 - 6/92).
Thesis: "STRiP, A Self-Timed RISC Processor Architecture."
Course work: Computer/processor architecture, VLSI design, and parallel system architecture.
Thesis Advisor: Dr. Mark Horowitz

M.S. Electrical Engineering, Florida Atlantic University, Boca Raton, FL (1/80 - 4/82).
Thesis Project: "Design of a Low-Cost Graphics Terminal."

B.S. Electrical Engineering, University of Tennessee, Knoxville, TN (9/75 - 9/79).
Graduated with Highest Honors.

Academic Experience

University of Tennessee (September 2013 to Present)
319 Min Kao Bldg., 1520 Middle Drive, Knoxville, TN 37996-2250

Position Held:

John Fisher Distinguished Professor, CoE EECS

Focused on research in the area of advanced computer architectures (neuromorphic systems and related devices, structures, architectures and learning models, non-Von Neumann data-centric computer architectures and programming models), big data acquisition and analysis systems (sensor arrays, multi-modal data analysis, evidence based delivery of information and services) and computational science (improved utilization of high performance computing to support scientific study and exploration.)

Established two new minor degree programs in the College of Engineering: Datacenter Technology and Cybersecurity. Each minor degree program requires 16 to 22 credit hours of unique study dependent on the students major. I have also developed and proposed a new undergraduate degree program call Business Engineering and Data Sciences, with a major focus on the application of technology to support business operation, development and innovation. This program would be a joint degree program between the College of Business Administration and the College of Engineering, a first for the two colleges and for the university.

Classes Developed and/or Taught –
COSC/ECE 402 - Senior Design Practicum
ECE463 – Introduction to Data Center Technology
ECE462 – Cyber Physical Systems Security

Teaching (1981)

Positions Held:

- Instructor: *Introduction to Logic Design*, Department of Electrical Engineering, Florida Atlantic University
- Teaching Assistant: *Introductory Electronics Lab*, Department of Electrical Engineering, Florida Atlantic University

Industrial Experience

IBM Corporation (June 2011 to June 2013)
Arenco Towers, P.O. Box 27242, Dubai Internet City, Dubai, UAE

Position Held:

IBM Fellow, VP and Chief Technology Officer, Middle East and Africa

Responsible for technical strategy, technical skills development, academic development and exploring new technology based solutions for the Middle East and Africa region. These responsibilities include the development of solutions specific for the emerging needs of the businesses and governments in segments such as mobile services (banking, healthcare, education, government), natural resource management (oil, gas, mining, forest, water), cloud based business services, and security (fraud protection, risk management, privacy, cybersecurity). Additional responsibilities included development of technology solutions for traditional industries including: banking, telecommunications, oil & gas, government, healthcare and education. Finally, responsible for skills development and research strategies that will enable IBM to significantly grow it business presence in the region (more than double from 2012 to 2015) and support economic growth of businesses through the use of information technology. Key accomplishment: established IBM's first Research Labs in Africa (Kenya).

IBM Corporation (August 2008 to June 2011)
1101 Kitchawan Road, Yorktown Heights, NY 10598

Position Held:

IBM Fellow and Vice President, World Wide Strategy and Operations, IBM Research.

Responsible for setting the direction of IBM's overall Research Strategy across eight worldwide labs and leading the global operations and information systems teams. These responsibilities include management of the division's business model, research strategy, hiring, university relations, internal/external recognition, personnel development, innovation initiatives and the division's operations. The IBM Research division supports 3000 scientist and engineers doing exploratory and applied research in all engineering and science disciplines. IBM Research is the most diverse and productive industrial research operation in the world. This responsibility also includes annual development of the Global Technology Outlook for the corporation. This >100 page annual report is a 9 month process which identifies disruptive technology and business trends and is leveraged to establish IBM's technology strategy each year.

IBM Corporation (August 2004 to July 2008)
650 Harry Road, San Jose, CA 95120

Position Held:

IBM Fellow, Senior Location Executive and Vice President, Almaden Research Center, IBM Research

Responsible for the lab operations, projects, strategy and focus for one of IBM's premier research centers. The Almaden Research Center supports over 400 scientists and engineers doing exploratory and applied research in various hardware, software and services areas, including nanotechnology, materials science, storage systems, data management, web technologies, workplace practices, services science and user interfaces. Key projects and activities in the lab include research in: storage class memory, Spintronics, data analytics (WebFountain), establishing services science as an academic discipline, server and storage systems management, scale-out system software, content management, enhanced services delivery methods and storage systems control software. Almaden Researchers support a tremendous number of invited talks, lectures, conference papers, scientific publications, patents, technology demonstrations and prototypes each year. Their contributions over the past 20 years have been key to the success of IBM in its systems and software businesses.

IBM Corporation (January 2004 to July 2004)
9000 Rita Road, Tucson, AZ 85744

Position Held:

IBM Fellow and Vice President Hardware and Systems Architecture, IBM Systems & Technology Group

Responsible for sustaining and enhancing STG's hardware and systems strategy and architectures to support continued market share growth and industry leadership in IBM's server and storage systems business. Focus areas include server systems technology, architecture and design, system cost and performance optimization, and systems and technology roadmaps. The Hardware and Systems Architecture team is made up of some of the top technical leaders in IBM in the

fields of hardware systems technology, architecture, and design. Key technology strategies being developed include systems virtualization, cluster interconnect, acceleration engines, hypervisors and scalable system structures.

IBM Corporation (September 2002 to January 2004)
9000 Rita Road, Tucson, AZ 85744

Position Held:

IBM Fellow and Vice President Storage Technology, IBM Systems Group

Responsible for architecture, design, technology and strategies in Storage Systems development. This includes responsibility for sustaining and enhancing SSG's technologies, methodologies and system functionality to support continued market share growth and customer satisfaction in IBM's storage systems business. Areas of focus included management console convergence for IBM systems, leveraging of logical partitioning to integrate storage applications with our storage systems solutions , entry level storage solutions for mainframe, UNIX and Windows environments, enterprise storage technology and continued growth of IBM market share in the storage systems industry.

IBM Corporation (May 2000 to September 2002)
P.O. Box 218, Yorktown Heights, NY 10598

Position Held:

IBM Fellow and Vice President of Systems, IBM Research

Responsible for managing the research and application of systems technologies spanning circuits to operating environments. The 300 researchers which make-up this group have a history of great inventions and technology introduction. Key technologies in his research team include cellular systems structures (Blue Gene), digital visualization, DA tools, Linux optimizations for Pervasive, SMPs & Clusters, Settop Box integration, hardware in-memory system compression, S/390 & PowerPC processors (up to 4GHz), super dense servers, formal verification methods and high speed low power circuits. Present innovations from the Systems Research Group include: 405LP embedded processor, TransNote, MetaPad, p690 processor, dynamic web caching, power-aware design automation tools and the Cell processor architecture. Also responsible for the Low Power Computing Initiative in IBM Research.

IBM Corporation (October 1997 to May 2000)
11400 Burnet Road, Austin, TX

Positions Held:

IBM Fellow and Director, IBM Enterprise Server Group, Advanced Technology Development

Responsible for identifying new technologies, structures and architectures (hardware and software) which will support future server market requirements for PowerPC and Intel based Unix environments. Recent work includes development of a server architecture optimized for complex data (video, audio, high-resolution photographs, 3D virtualization, etc.) mining, management, distribution, searching and storage. This system structure is called a "cellular architecture" system.

IBM Fellow and Director of the Austin Research Lab, IBM Research Division

Responsible for managing a highly skilled research team focused on developing technologies for high performance processors, high MIPS/milliwatt embedded controllers, system simulation, EDA tools and new server architectures. Present lab accomplishments include the successful testing of the first 1GHz CMOS microprocessor, design of a high speed DRAM (<5ns latency), prototyping of a highly scalable SMP architecture (NUMA) for Intel and PowerPC, and information caching, compression and filtering to support efficient content delivery to handheld devices or across low-speed networks. Other lab activities include research in low-temperature cooling methods for entry-level systems, OS and application optimizations for large SMPs, formal verification of logic and arrays, and adaptation of SIM-OS to support execution based simulation of PowerPC platforms.

IBM Corporation (June 1995 to October 1997)
11400 Burnet Road, Austin, TX

Positions Held:

IBM Fellow and Director of System Architecture and Performance, RS/6000 Division

Responsible for managing the architecture, performance analysis and standards development for RS/6000 servers and workstations. This includes the architecture development for UNI, SMP and MPP UNIX servers and UNI and SMP workstations based on the PowerPC processors. Much of the architecture work focused on building a balanced system of processor, memory, IO and switch performance to cover both commercial and technical application environments. IBM

Fellow responsibilities included the architecture, design and prototyping of a NUMA based system, including the development of a 4GB/sec/link switch-fabric and adapter. The performance group is responsible for performance analysis and tuning of the server and workstation products, primarily focused on driving design enhancements back into the development organizations. This group also provides performance analysis for database, network, graphics and technical application vendors. Performance metrics include TPC, SPECint/fp, SAP, PLBsurf, SPECweb, LADDIS, NAS, Notesbench, SDET/KENBUS and others.

IBM Corporation (October 1994 to June 1995)
11400 Burnet Road, Austin, TX

Position Held:

Director of System Platforms, Interactive Broadband Systems

Responsible for managing the research, development and procurement of elements required to deliver interactive video services across private and public networks. This included commercial LAN networks (ATM, FDDI, Ethernet), as well as broadband and switched public networks (ATM, T1/T3, QAM, ADSL, etc). The elements developed included settop boxes, video servers and infrastructure software to support the network interfaces, protocols and application environments. Directly managed the development of a family of digital settop boxes targeted as a high-end entertainment terminal with features to support interactive services. Also acquired funding and established IBM's video server development group in the RS/6000 Division resulting in a new family of multimedia server solutions for 1996. Created IBM's Settop Reference Platform Specification and IBM's Video Server Architecture Specification.

IBM Corporation (January 1993 to October 1994)
11400 Burnet Road, Austin, TX

Position Held:

Director of Architecture, Power Personal Systems Division

Responsible for managing the architecture and prototype development for IBM's entry level PowerPC based PCs, workstations and settop boxes. These responsibilities included architecture, design and prototyping of subsystems and buses used in these systems. Created the PowerPC Reference Platform Specification (now know as the Common Hardware Reference Platform), an open industry standard PowerPC system specification. Fostered the initial technical agreements between Apple, Motorola and IBM on a common PowerPC system design. Also provide technical direction for the Power Personal Systems Division and the Advanced Workstation Division design and development groups responsible for more than ten PowerPC based systems and adapters. Responsibilities include hardware/software architecture and design, business planning, development expense management, joint development relationships, customer satisfaction and market research.

IBM Corporation (September 1979 to January 1993)
1000 51st Street, Boca Raton, FL

Positions Held:

Senior Technical Staff Member, Senior Engineer, Advisory Engineer, Staff Engineer, Senior Associate Engineer, Associate Engineer, and Junior Engineer

- Chief Engineer of PRS (Personal RISC Systems), PowerPC system architecture and development group. Responsible for managing technical direction, key technology usage and architectural decisions for system development groups. Also responsible for development schedules, product definition, and chip development for new family of computer systems.
- Provided system consulting to IBM's PC Company and PowerPC system development group while attending Stanford University from September 1989 to June 1992.
- Directed the development of the processor complex and memory subsystems in the PS/2 Model 90, Model 95, and the Power Platform.
- Lead Engineer for architectural definition, design, and test of the IBM PS/2 Model 80 and Model 70-A21 systems and subsystems. Responsible for managing technical direction and architectural decisions for 30 person system development group. Also responsible for development schedules, product definition, and chip development for first PS/2 computer systems.
- Architecture and development team member of the Micro Channel Architecture and related interfaces.

- Lead Engineer for architectural definition, design, and test of the IBM PC/AT system board, memory cards, and the IBM ISA system bus. Responsible for managing technical direction and architectural decisions for 30 person system development group.
- Led the design and test of the IBM PC Color Graphic Adapter and Monochrome Adapter.
- Created a real-time In-Circuit Emulator/Monitor for the Intel 80386/80486 and the Micro Channel Architecture bus. Derivatives of initial emulator used in the manufacturing, debug, and Intel based IBM PC systems.
- Created enhanced functions for the IBM PC and PS/2 architectures (32-bit DMA with SCB support, 32-bit DMA with scatter/gather ping-pong registers, DMA-driven serial port, DMA-driven parallel port, FIFO-based diskette interface, 64KB 386 cache controller, and a Dual-Port system memory controller).

ALCOA Aluminum (1975 - 1979)

Position Held:

Co-op Engineer while attending University of Tennessee (six quarters)

- Supported the design, installation, and start-up of large-scale furnace and mill control systems.
- Researched and developed a plant lighting system.

Career Accomplishments and Recognitions

Honorary Degrees:

- Wheaton College honorary Doctor of Science Degree (2008)
- Lincoln University (PA) honorary Doctor of Science Degree & Commencement Speaker (2003)
- Howard University honorary Doctor of Science degree (2002)

Honors from Academic and Scientific Societies and Organizations:

- National Academy of Inventors (NAI) Fellow (2014 Induction)
- Distinguished Alumni Award, The University of Tennessee (2012 Induction)
- Distinguished Alumni Award, Florida Atlantic University (2009 Induction)
- Percy Julian Award & Outstanding Scientist of the Year, Harvard Society of Black Scientists and Engineers (2007)
- National Institute of Science (NIS) 2006 Outstanding Scientist Award
- The University of Tennessee College of Engineering 2005 Dougherty Award
- American Academy of Arts and Sciences Fellow (May 2004)
- IEEE Fellow (2002)
- National Academy of Engineering - NAE inductee (2001)
- Black Engineer of the Year Award, Career Communications Group (2000)
- Distinguished Engineering, Golden Torch Award, National Society of Black Engineers (1999)
- Ronald H. Brown American Innovators Award (1997)
- Presidents Award, Career Communications Group (1997)
- National Inventors Hall of Fame Inductee, Akron, Ohio (1997)
- Best Presentation, IEEE International Conference on Computer Design (1991)
- Phi Kappa Phi, University of Tennessee (1977-1980)
- Tau Beta Pi, University of Tennessee (1977-1979)
- Minority Engineering Scholarship, University of Tennessee (1975-1979)

Key Career Achievement Awards and Honors:

- 38 Patents Issued, 6 Patents Pending
- Ebony Power 100 Award, Ebony Magazine (November, 2012)
- Association of Black Charities Black History Makers Immortal Award (2008)

- Savoy Magazine's "The 100 Most Influential Blacks In America." Scientists category (August 2003)
- 2002 Architects & Pioneers Research & Development Award, Institute for Strategic Thinking and Technology Development (ISTTD) (Jan. 2003)
- 50 Most Important African-Americans in Technology, Electron Access Inc. (2002)
- Distinguished Science Sponsor, New York Hall of Science (2001)
- Living Legends Award, Baltimore, Maryland (2000)
- PC Magazine World Class Award (1988).
- IEEE Secretary, University of Tennessee (1978-1979)

Advisory Board Appointments, Colleges of Engineering:

- University of Tennessee, Knoxville, Dean Wayne Davis (2000 - 2013)
- University of California Berkeley, Dean Shankar Sastry, (2008 - 2011)
- Stanford University, Dean James Plummer, (2008 - 2010)
- San Jose State University, Dean Belle Wei (2007 - 2010)
- Georgia Tech University, Dean Don Giddens (2001 - 2008)
- University of Arizona, Tuson - interim Dean Jeff Goldberg (2002 - 2006)

University President Advisory Board Appointments:

- California Polytechnic State University President's Cabinet (2007 - Present)
- University of Tennessee Foundation Board (2003 - 2006)
- Huston-Tillotson College Advisory Board (1997 - 2004)

Sustained interactions with University & Academic Organization Presidents:

- Dr. John Hennessey, Stanford University, Stanford, CA
- Dr. John Slaughter, NACME (previously Occidental College)
- Dr. Shirley Jackson, RPI, Albany, NY
- Dr. Ronald Crutcher, Wheaton College, Norton, MA

Sustained interactions with other Engineering College Deans:

- Dean Eugene Deloatch, Morgan State University
- Dean James Johnson (retired), Howard University
- Dean Eric J. Sheppard, Hampton University

Initiatives and Engagements with Academic Institutions and Organizations:

- Keynote Speaker, Engineering College Deans annual meeting, San Francisco, CA (2007)
- Commencement Speech, Lincoln University Graduation Ceremony (2003)
- Commencement Speech, University of Tennessee Graduation Ceremony (2000)
- Sponsored IBM's Services Science Initiative (development of new academic discipline and associated curriculum, grand challenge PhD topics and initial university programs).
- Meetings with HBCU Engineering Deans on IBM's PhD Study programs, SUR grants and university initiatives.
- Sponsored the Makocha Minds Mentoring program - connects engineering students at Universities in Sub-Saharan Africa to technical leaders in IBM.
- Program development and donations of approx. 20,000 technical books to Dodoma University, Tanzania
- IBM's Relationship Executive to the following universities:
    - University of Missouri
    - Stanford University
    - University of California, Berkeley

- Initiated and completed the donation of a IBM supercomputer (Blue Gene) to the Center for High Performance Computing in South Africa, Africa~~n~~'s highest performance computing system. This system was donated as a shared resource to support the development of research programs at universities in sub-Saharan Africa.
- Numerous speaking engagements at US, Europe, Asia, Africa and Canada.

Technical Advisory Committees, Councils and Advisory Boards:

- Mars Advanced Research Institute Advisory Board (2012 – Present)
- Digital Promise (2011 – Present)
- Board of Trustees, Computer History Museum (2005-2010)
- Computer Science and Telecommunications Board, NAE (2003 - 2009)
- Bay Area Science and Innovation Council, Silicon Valley, CA (2004 - 2008)
- Silicon Valley Leadership Group, Silicon Valley, CA (2004 - 2008)
- Board of Directors, Inroads, Inc. (1996 - 1999)

IBM HONORS AND AWARDS

*IBM Invention Achievement Awards are given based on the accumulation of four patents filed or twelve published papers per award level.

- Fourteenth Level IBM Invention Achievement Award* (2004)
- Thirteenth Level IBM Invention Achievement Award* (2000)
- IBM Research Outstanding Accomplishment, NUMA System Design (2000)
- Twelve Level IBM Invention Achievement Award*(1999)
- Eleventh Level IBM Invention Achievement Award*(1999)
- Tenth Level IBM Invention Achievement Award*(1999)
- Ninth Level IBM Invention Achievement Award*(1998)
- IBM Patent Portfolio Award (1998) - Recognizes value of PC bus patents
- Elected to the Technology Council of the IBM Academy of Technology (1997)
- IBM Fellow (1995) (50 of 300,000 employees are IBM Fellows, IBM's highest technical position)
- IBM Master Inventors Award (1995) - >20 patents issued
- IBM Patent Portfolio Award (1995) - Recognizes significant value of personal patent portfolio
- Eighth Level IBM Invention Achievement Award*(1995)
- Seventh Level IBM Invention Achievement Award*(1993)
- Sixth Level IBM Invention Achievement Award* (1993)
- IBM Academy of Technology. Elected Member (1989-present)
- Fifth Level IBM Invention Achievement Award* (1989)
- IBM Outstanding Technical Achievement Award: Development of the PS/2 Model 70-A21. Corporate Award (1988)
- Fourth Level IBM Invention Achievement Award* (1988)
- Third Level IBM Invention Achievement Award* (1988)
- IBM Corporate Award: Development of the PS/2 Micro Channel Architecture. (1988)
- IBM Outstanding Technical Achievement Award: Development of 32-bit PC. Corporate Award (1987)
- IBM Outstanding Innovation Award: Design of the Personal Computer AT Planar Board. Division Award (1985)
- Second Level IBM Invention Achievement Award* (1984)
- First Level IBM Invention Achievement Award* (1984)
- IBM Outstanding Innovation Award: Small System Display Concepts and Design. Division Award (1981)

PATENTS

1. Birdwell, J. Douglas, Mark E. Dean, and Catherine Schuman, Method and Apparatus for Constructing a Dynamic Adaptive Neural Network Array (DANNA), U. S. Patent Application 14/513,297, filed October 14, 2014.

2. Birdwell, J. Douglas, Mark E. Dean, and Catherine Schuman, Method and Apparatus for Providing Random Selection and Long-Term Potentiation and Depression in an Artificial Network, U. S. Patent Application 14/513,334, filed October 14, 2014.

3. Birdwell, J. Douglas, Mark E. Dean, and Catherine Schuman, Method and Apparatus for Constructing, Using and Reusing Components and Structures of an Artificial Neural Network, U. S. Patent Application 14/513,388, filed October 14, 2014.

4. Birdwell, J. Douglas, Mark E. Dean, and Catherine Schuman, Method and Apparatus for Providing Real-Time Monitoring of an Artificial Neural Network, U. S. Patent Application 14/513,447, filed October 14, 2014.

5. Birdwell, J. Douglas, Mark E. Dean, Margaret Drouhard, and Catherine Schuman, Method and Apparatus for Constructing a Neuroscience-Inspired Artificial Neural Network with Visualization of Neural Pathways, U.S. Patent Application 14/513,497, filed October 14, 2014.

6. M. E. Dean, D. Boerstler, Hung Ngo, A. Zimmerman. "Apparatus and Method for High Resolution Frequency Adjustment in a Multistage Frequency Synthesizer." Issued May, 2003, U.S. Patent No. 6566921

7. M. E. Dean, D. Boerstler, Hung Ngo, A. Zimmerman. "Apparatus and Method for Dynamic Frequency Adjustment in a Frequency Synthesizer." Issued February, 2003, U.S. Patent No. 6522207

8. M. E. Dean, Y. Baumgartner. "Non-Uniform Memory Access (NUMA) Data Processing System that Speculatively Forwards a Read Request to a Remote Processing Node." Issued February, 2002, U.S. Patent No. 6338122

9. R. L. Rockhold, J. M. Magee, J. W. Van Fleet, G. G. Sotomayor JR, M. E. Dean. "Method and System in a Distributed Shared-Memory Data System for Determining Utilization of Shared-Memory Included within Nodes by a Designated Application." Issued January 1, 2002, U.S. Patent No. 6336170

10. M. E. Dean. Y. Baumgartner, A. Benavides, J. Hollaway. "Method and System for Supporting Software Partitions and Dynamic Reconfiguration within a Non-Uniform Memory Access System." Issued December 25, 2001, U.S. Patent No. 6334177

11. M. E. Dean, Y. Baumgartner, G. D. Carpenter, A. Elman, J. S. Fields, Jr., D. B. Glasco, "Reservation Management in a Non-Uniform Memory Access (NUMA) Data Processing System." Issued August 14, 2001, U.S. Patent No. 6275907.

12. M. E. Dean, G. D. Carpenter, D. B. Glasco, "Method and System for Avoiding Livelocks Due to Colliding Invalidating Transactions within a Non-Uniform Memory Access System." Issued July 31, 2001, U.S. Patent No. 6269428.

13. M. E. Dean, P. L. de Backer, R. L. Rockhold. "Method and System in a Distributed Shared-Memory Data Processing System for Determining Utilization of Nodes by Each Executed Thread." Issued July 24, 2001, U.S. Patent No. 6,266,745

14. M. E. Dean, G. D. Carpenter, D. B. Glasco, "Method and System for Providing an Eviction Protocol within a Non-Uniform Memory Access System." Issued July 24, 2001, U.S. Patent No. 6266743.

15. M. E. Dean, G. D. Carpenter, D. B. Glasco, "Method and System for Avoiding Livelocks Due to Stale Exclusive/Modified Directory Entries within a Non-Uniform Access System." Issued May 1, 2001, U.S. Patent No. 6226718.

16. M. E. Dean, J. P. Bannister, G. D. Carpenter, D. B. Glasco, R. N. Iachetta, Jr., "Method and System for Avoiding Data Loss due to Cancelled Transactions within a Non-Uniform Memory Access System." Issued February 20, 2001, U.S. Patent No. 6192452.

17. M. E. Dean, D. Glasco, R. L. Rockhold, P. L. De Backer "Interrupt Architecture for a Non-Uniform Memory Access (NUMA) Data Processing System." Issued November 14, 2000, U.S. Patent No. 6148361.

18. M. E. Dean, D. Glasco, G. D. Carpenter, "Non-Uniform Memory Access (NUMA) Data Processing System that Permits Multiple Caches to Concurrently Hold Data in a Recent State from which Data can be Sourced by Shared Intervention." Issued September 5, 2000, U.S. Patent No. 6115804.

19. M. E. Dean, D. P. Beaman, G. D. Carpenter, W. G. Voigt, "Method & System for Arbitrating between Bus Masters having Diverse Bus Acquisition Protocols." Issued July 11, 2000, U. S. Patent No. 6088750.

20. M. E. Dean, D. Glasco, R. N. Iachetta, G. D. Carpenter, "Non-Uniform Memory Access (NUMA) Data Processing System that Speculatively Issues Requests on a Node Interconnect." Issued June 27, 2000, U.S. Patent No. 6081874.

21. M. E. Dean, D. Glasco, R. N. Iachetta, G. D. Carpenter, "Non-Uniform Memory Access (NUMA) Data Processing System that Buffers Potential Third Node Transactions to Decrease Communication Latency." Issued May 23, 2000, U.S. Patent No. 6067611.

22. M. E. Dean, D. Glasco, G. D. Carpenter, "Non-Uniform Memory Access (NUMA) Data Processing System that Speculatively Issues Requests on a Node Interconnect." Issued May 23, 2000, U.S. Patent No. 6067603.

23. M. E. Dean, W. G. Voigt, G. D. Carpenter, D. P. Beaman. "Method and System for Interfacing an Upgrade Processor to a Data Processing System." Issued April, 1999, U.S. Patent No. 5,898,857.

24. M. E. Dean, Thoi Nguyen. "Bus Interface Logic Unit." Issued June, 1998, U.S. Patent No. 5,768,550.

25. M. E. Dean, G. D. Carpenter. "Method and System for Reading from an M-Byte Memory Utilizing a Processor Having an N-Byte Data Bus. " Issued February, 1997, U.S. Patent No. 5,603,041.

26. M. E. Dean. "Method for Dynamically Sequencing Operation of a Self-Timed Processing System." Issued September, 1996, U.S. Patent No. 5,553,276.

27. M. E. Dean. "System and Method for Prefetching Information in a Processing System." Issued August, 1996, U.S. Patent No. 5,544,342.

28. M. E. Dean, M. R. Faucher, J. C. Peterson, H. C. Tanner, G. D. Carpenter. "Non-Contiguous Mapping of I/O Addresses to use Page Protection of a Processor. " Issued August, 1996, U.S. Patent No. 5,548,746.

29. M. E. Dean, M. R. Faucher, J. C. Peterson, H. C. Tanner, S. E. Curry. "Connecting A Short Word Length Non-Volatile Memory to a Long Word Length Address/Data Multiplexed Bus. " Issued September, 1995, US. Patent No. 5,448,521.

30. R. M. Begun, P. M. Bland, and M. E. Dean. "Microcomputer System Employing Address Offset Mechanism to Increase the Supported Cache Memory Capacity." Issued September, 1995, U.S. Patent No. 5,450,559.

31. R. M. Begun, P. M. Bland, and M. E. Dean. "Method and Apparatus for Selectively Posting Write Cycles Using the 82385 Cache Controller." Issued July, 1994, U.S. Patent No. 5,327,545.

32. R. M. Begun, P. M. Bland, and M. E. Dean. "Microprocessor Hold and Lock Circuitry." Issued December, 1992, U.S. Patent No. 5170481.

33. R. M. Begun, P. M. Bland, and M. E. Dean. "Delayed Cache Write Enable Circuit for a Dual Bus Microcomputer System with an 80386 and 82385." Issued December, 1992, U.S. Patent No. 5175826.

34. P. M. Bland and M. E. Dean. "System Bus Preempt for 80386 when Running in an 80386/82385 Microcomputer System with Arbitration." Issued July, 1992, U.S. Patent No. 5,129,090.

35. R. M. Begun, P. M. Bland, and M. E. Dean. "Control of Pipelined Operation in a Microcomputer System Employing Dynamic Bus Sizing with 80386 Processor and 82385 Cache Controller." Issued June, 1992, U.S. Patent No. 5,125,084.

36. P. M. Bland, M. E. Dean, G. J. Gaudenzi, K. G. Kramer, and S. L. Tempest. "Bidirectional Buffer with Latch and Parity Capability." Issued April, 1992, U.S. Patent No. 5,107,507.

37. R. M. Begun, P. M. Bland, and M. E. Dean. "Method and Apparatus for Selectively Posting Write Cycles Using the 82385 Cache Controller." Issued September, 1991, U.S. Patent No. 5,045,998.

38. M. E. Dean, et al. "Apparatus and Method for Accessing Data Stored in a Page Mode Memory." Issued July, 1991, U.S. Patent No. 5,034,917.

39. M. E. Dean and D. L. Moeller. "Data Processing System Including a Main Processor and Co-processor and Co-processor Error Handling Logic." Issued July, 1986, U.S. Patent No. 4,598,356.

40. M. E. Dean. "Refresh Generator System for a Dynamic Memory." Issued March, 1986, U.S. Patent No. 4,575,826.

41. M. E. Dean and D. L. Moeller. "Microcomputer System with Bus Control Means for Peripheral Processing Devices." Issued July, 1985, U.S. Patent No. 4,528,626.

42. M. E. Dean, L. C. Eggebrecht, D. A. Kummer, and J. A. Saenz. "Color Video Display System Having Programmable Border Color." Issued March, 1984, U.S. Patent No. 4,437,092.

43. M. E. Dean, D. A. Kummer, and J. A. Saenz. "Composite Video Color Signal Generation from Digital Color Signals." Issued April, 1984, U.S. Patent No. 4,442,428.

PUBLICATIONS

Ph.D. Thesis:

"STRiP, A Self-Timed RISC Processor Architecture."
By using: (1) a self-timed pipeline sequencing method called *dynamic clocking*, (2) a *zero-level cache* with *predictive prefetching*, and (3) an asynchronous external interfaces, a 32-bit RISC processor is developed which requires no external clocks, provides approximately twice the performance of an equivalent synchronous design and whose operating frequency adapts to the system's environmental conditions. STRiP's sequencing structure and asynchronous external interface eliminates synchronization and meta-stability problems normally encountered when interfacing devices with different operating rates. The dynamic clocking sequencing method also removes the need for dual-rail encoding and completion signaling between functional units (required by other self-timed design styles).

Conference Papers:

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