Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: I

Subject Name: Digital Circuits and Logic Design

Subject Code: 20MDEL11 **L – T – P – C: 4-0-0-4**

Course Objectives:

Sl.No	Course Objectives
1	The objective of this subject is to explore students to advanced concepts of design, simplify, testing and debug of digital circuits using prior knowledge of logic design and advanced logic design concepts

Course Outcomes

Course outcome	Descriptions
CO1	Apply the concepts and laws of logic design to solve logical problems
CO2	Solve complexity of logical equation using simplification techniques and decomposition methods
CO3	Design logical circuits such as encoder, decoder, sine wave.
CO4	Test the digital circuit for faults and design fault free circuit

SYLLABUS

UNIT	Description	Hours
I	Review of digital concepts: Problem statement to truth tables, combinational logic, logic problems simplification of Boolean functions, K-map, Quine-McCluskey method, Map entered variable. Logic design: Analysis of combinational circuits, comparators, data selectors, Encoders – priority encoder, Decoders – BCD to Decimal, Seven segment display, Sine generators, Design of high speed adders – Ripple adder, Carry look ahead adder.	14Hrs
II	Functional Decomposition and Symmetric Functions: Functional Decomposition, Decomposition by expansion, Test for decomposability, Decomposition charts, Symmetric networks, Properties of symmetric functions, synthesis, complemented variables of symmetry, Identification of symmetric functions.	7Hrs
III	Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits, Fault-Location Experiments, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic.	8Hrs
IV	Introduction to synchronous sequential circuits and Iterative networks: Sequential circuits- The finite state model- Memory element and their excitation functions, Synthesis of synchronous sequential circuits, Iterative networks.	9Hrs
V	Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities and Limitations of Finite – State Machines, Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines. Structure of Sequential Machines: State Assignments Using Partitions, The lattice of closed partitions, Reduction of the output dependency, Input independence and autonomous clocks.	14Hrs

Text Books:

Sl No	Title	Authors	Volume and Year of Edition
1	Switching and Finite Automata Theory	Zvi Kohavi	2nd Edition. Tata McGraw Hill Edition, ISBN-10: 0-07-099387-4
2	Fundamentals of Logic Systems	Charles Roth Jr	Cengage learning, 7th edition, 2013, ISBN-13: 978-1133628477

Reference Books:

Sl No	Title	Authors	Volume and Year of Edition
1	Fault Tolerant and fault testable hardware design	Parag K Lala	Prentice Hall Inc. 1985
2	Introductory theory of computer	V. Krishnamurthy	Macmillan Press Ltd, 1983
	Theory of computer science – Automata, Languages and Computation	Mishra & Chandrasekaran	2nd Edition, PHI, 2004

Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: I

Subject Name: CMOS VLSI DESIGN

Subject Code: 20MDEL12 **L – T – P – C: 4-0-0-4**

Course Objectives:

Sl.No	Course Objectives
1	To make the students learn the principles, operations and applications of MOSFET's.
2	To introduce the students to modelling and design of digital VLSI circuits using different CMOS design styles and CMOS sub system.
3	To make the students learn stick diagrams and layouts using Lambda based design rules for a given schematic and to categorize the different MOS technologies

Course Outcomes

Course outcome	Descriptions
CO1	Identify the different design techniques used in modeling the digital VLSI Circuits. (L1)
CO2	Calculate the design parameters for the CMOS circuits and can estimate the parasitic values for different mask layers. (L2)
CO3	Outline the MOS process technology and CMOS sub system design. (L4)

SYLLABUS

UNIT	Description	Hours
I	**Unit 1: MOS Transistor Theory:** n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter. (Text1)	**12**
II	**Unit 2: CMOS Process Technology Silicon Semiconductor technology:** An overview, basic CMOS technology. A basic n-well CMOS process, The p-well process, twin tub process, silicon on insulator. (Text1) **CMOS process enhancements:** Interconnect, circuit elements; Resistors, Capacitors, bipolar transistors, Thin film transistors,3DCMOS (Text1) **MOS Design Processes:** MOS layers, stick diagrams, design rules and layout, symbolic diagrams. (Text3)	**10**
III	**Unit 3: Basic circuit concepts:** Sheet resistance, standard unit of capacitance concepts, delay unit time inverter delays, driving capacitive loads, propagation delays, scaling of MOS circuits (Text3) **Basics of Digital CMOS Design:** Combinational MOS Logic circuits-Introduction, MOS logic circuits with depletion NMOS load. (Text2)	**10**
IV	**Unit 4: Basics of Digital CMOS Design: Contd..** CMOS logic circuits, complex logic circuits, CMOS Transmission Gate. (Text2) **Sequential MOS logic Circuits :** Introduction, Behavior of bi stable elements, SR latch Circuit, (Text2).	**10**
V	**Unit 5: Sequential MOS logic Circuits :Contd..** Clocked latch and Flip Flop Circuits, CMOS D- latch and triggered Flip Flop (Text2). **Dynamic CMOS and clocking:** Introduction, advantages of CMOS over NMOS, CMOS\SOS technology' CMOS\bulk technology, latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements. (Text5)	**10**

Text Books:

Sl No	Title	Authors	Volume and Year of Edition
1	Principles of CMOS VLSI Design: A System Perspective	Neil Weste and K. Eshragian,	2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
2	CMOS Digital Integrated Circuits: Analysis and Design	Sung Mo Kang & Yosuf Lederabic Law,	3 rd edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
3	Basic VLSI Design	Douglas A. Pucknell & Kamran Eshraghian	PHI 3rd Edition (original edition 1994), 2005.
4	Introduction to VLSI Design	Eugene D Fabricius	Mc Graw Hill, International Edition (Original Edition 1990).

Reference Books:

Sl No	Title	Authors	Volume and Year of Edition
1	CMOS VLSI Design: A Circuits and System perspective,	Neil H E Weste, David Haris,Ayan,	3 rd edition, Pearson Education (Asia) Pvt. Ltd., 2000.
2	Introduction to VLSI circuits and systems	John P Uyemura	Wiley Indian Edition,2002
3	Modern VLSI design: System on Silicon	Wayne, Wolf,	Pearson Education, Second Edition.

SRI SIDDHARTHA INSTITUTE OF TECHNOLOGY- TUMAKURU
(A constituent College of Siddhartha Academy of Higher Education, Tumakuru)

Department of Electronics and Communication

MTech in Digital Electronics/VLSI & Embedded Systems

Syllabus for the Academic Year – 2020 - 2021

Semester: I

Subject Name: Advanced Embedded Systems

Subject Code: 20MDEL13 **L – T – P – C : 4-0-0-4**

Course Objectives :

Sl.No	Course Objectives
1	Understand basics in design of embedded hardware and software systems.
2	Outline various development tools.
3	Describe the hardware software co-design and firmware design approaches
4	RTOS design in embedded system.

Course Outcomes

Course outcome	Descriptions
CO1	Understand the fundamentals and general structure of an Embedded System.
CO2	Apply various real time algorithms in building embedded systems.
CO3	Analyze IDE and new trends in embedded industry.

UNIT	Description	Hours
I	**Typical Embedded System:** Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components. Characteristics and Quality Attributes of Embedded Systems	10
II	**Hardware Software Co-Design and Program Modelling**: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modelling Language, Hardware Software Trade-offs.	10
III	**Embedded Firmware Design and Development:** Embedded Firmware Design Approaches, Embedded Firmware Development Languages.	8
IV	**Real-Time Operating System (RTOS) based Embedded System Design**: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS**.**	12
V	**The Embedded System Development Environment**: The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler / Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan**.** Trends in the Embedded Industry, Processor Trends in Embedded System, Embedded OS Trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks.	12

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	**Introduction to Embedded Systems**	Shibu K V	Tata McGraw Hill Education Private Limited, 2009

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	**Embedded Systems – A contemporary Design Tool**	James K Peckol, John Weily	2008.

Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: I

Subject Name: Digital Image Processing

Subject Code: 20MDEL14 **L – T – P – C: 4-0-0-4**

Course Objectives:

Sl.No	Course Objectives
1	To study the image fundamentals and mathematical transforms necessary for image processing.
2	To study the image enhancement techniques
3	To study image restoration and compression procedures.
4	To study the color imaging procedures.

Course Outcomes

Course outcome	Descriptions
CO1	Review the fundamental concepts of a digital image processing system. L2
CO2	Analyze images in the frequency domain using various transforms. And Evaluate the techniques for image enhancement and image restoration. L4
CO3	Categorize various compression techniques and Interpret Image compression standards, segmentation and representation techniques.L5
CO4	Analyze color image processing techniques.L4

UNIT	Description	Hours
I	**Digital Image Fundamentals:** Introduction: Digital Image- Steps of Digital Image Processing Systems-Elements of Visual Perception -Connectivity and Relations between Pixels. Simple Operations- Arithmetic, Logical, Geometric Operations.Mathematical Preliminaries - 2D Linear Space Invariant Systems - 2D Convolution - Correlation 2D Random, Sequence - 2D Spectrum.	11
II	**Image Transforms And Enhancement:** Image Transforms: 2D Orthogonal and Unitary Transforms-Properties and Examples. 2D DFT- FFT – DCT - Hadamard Transform - Haar Transform - Slant Transform - KL Transform - Properties And Examples.Image Enhancement:- Histogram Equalization Technique- Point Processing-Spatial Filtering-In Space And Frequency - Nonlinear Filtering-Use Of Different Masks.	11
III	**Image restoration and construction** Image Restoration: Image Observation And Degradation Model, Circulant And Block Circulant Matrices and Its Application In Degradation Model - Algebraic Approach to Restoration- Inverse By Wiener Filtering - Generalized Inverse-SVD And Interactive Methods - Blind Deconvolution-Image Reconstruction From Projections.	10
IV	**Image compression & segmentation:** Image Compression: Redundancy And Compression Models -Loss Less And Lossy. Loss Less- Variable-Length, Huffman, Arithmetic Coding - Bit-Plane Coding, Loss Less Predictive Coding, Lossy Transform (DCT) Based Coding, JPEG Standard - Sub Band Coding. Image Segmentation: Edge Detection - Line Detection - Curve Detection - Edge Linking And Boundary Extraction, Boundary Representation, Region Representation And Segmentation, Morphology-Dilation, Erosion, Opening And Closing. Hit And Miss Algorithms Feature Analysis	10
V	**Color and multispectral image processing:** Color Image-Processing Fundamentals, RGB Models, HSI Models, Relationship Between Different Models. Multispectral Image Analysis - Color Image Processing Three Dimensional Image Processing-Computerized Axial Tomography-Stereometry-Stereoscopic Image Display-Shaded Surface Display.	10

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Digital Image Processing	Gonzalez.R.C & Woods. R.E.	3/e, Pearson Education,2008.
2	Digital Image Processing	Kenneth R Castleman	Pearson Education,1995.
3	Digital Image Procesing, S.	Jayaraman, S. Esakkirajan, T. Veerakumar	McGraw Hill Education, 2009. Pvt Ltd, NewDelhi
4	Fundamentals of Digital image Processing	Anil Jain.K,	Prentice

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M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 – 2021

Semester: I

Subject Code: 20MDEL151 **L-T-P-C:4-0-0-4**

Subject Name: RESEARCH METHODOLOGY AND IPR

Course Objectives:

Sl.No	Course Objectives
1	To give an overview of the research methodology and objectives of research.
2	Explain the technique of defining a research problem and To explain the functions of the literature review in research
3	To explain carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing a review and to explain various research designs and their characteristics
4	To explain the details of sampling designs, measurement and scaling techniques and also different methods of data collections. •
5	To explain the art of interpretation and the art of writing research reports. • To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment. • To discuss leading International Instruments concerning Intellectual Property Rights.

Course Outcomes

Course outcome	Descriptions
CO1	Understand research problem formulation.
CO2	Analyze research related information to define a research problem & reviewing literature.
CO3	Analyze how to collect the data related to the research.

CO4	Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular. • Understand that IPR protection provides an incentive to inventors for further research.

UNIT	Description	Hours
I	**Research Methodology**: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India.	8
II	**Defining the Research Problem:** Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration. **Reviewing the literature:** Place of the literature review in research, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed.	10
III	**Research Design:** Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs. **Design of Sample Surveys:** Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs.	10
IV	**Data Collection:** Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method. **Interpretation and Report Writing:**	12

	Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout. **Interpretation and Report Writing (continued):** of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports.	
V	**Intellectual Property:**The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999,The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957,The Protection of Plant Varieties and Farmers' Rights Act, 2001,The Semi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organisation (WIPO),WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition, Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights(TRIPS) Agreement, Covered under TRIPS Agreement, Features of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO.	12

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Research Methodology: Methods and Techniques	C.R. Kothari, Gaurav Garg	4th Edition, 2018
2	ResearchMethodologyastep-by-stepguideforbeginners. (For the topic Reviewing the literature under module 2)	Ranjit Kumar	SAGE PublicationsLtd 3rd Edition, 2011

3	Study Material (For the topic Intellectual Property under module 5)	Professional Programme Intellectual Property Rights, Law and Practice, The Institute of Company Secretaries of India, Statutory Body Under an Act of Parliament, September 2013	

Reference Book:

Sl No	**Text Book title**	**Author**	**Volume and Year of Edition**
1	Research Methods: the concise knowledge base	Trochim	Atomic Dog Publishing 2005
2	Conducting Research Literature Reviews: From the Internet to Paper		Fink A Sage Publications 2009

Department of Electronics and Communication

M.Tech in VLSI & Embedded systems

Syllabus for the Academic Year – 2020 - 2021

Semester: I

Subject Name: Advanced Computer Architecture

Subject Code: 20MDEL152 **L – T – P – C:4-0-0-4**

Course Objectives:

Sl.No	Course Objectives
1	To make students know about the Parallelism concepts in Programming
2	To give the students an elaborate idea about the different memory systems and buses.
3	To introduce the advanced processor architectures to the students.
4	To make the students know about the importance of multiprocessor and multicomputer.
5	To study about data flow computer architectures

Course Outcomes

Course outcome	Descriptions
CO1	Demonstrate concepts of parallelism in hardware/software.
CO2	Discuss memory organization and mapping techniques.
CO3	Describe architectural features of advanced processors.
CO4	Interpret performance of different pipelined processors

UNIT	Description	Hours
I	**Parallel Computer Models**: The State of Computing, Computer Development Milestones, Elements of Modern Computers, Evolution of Computer Architecture, System Attributes to Performance, Multiprocessors and Multicomputer Shared –Memory Multiprocessors, Distributed Memory Multiprocessors, A Taxonomy of MIMD Computers, Multi vector and SIMD computers, Vector Supercomputers, SIMD Supercomputers.	6
II	**Parallel Program and network properties**: Conditions for parallelism ,data resource dependencies, Hardware & software parallelism, The role of compilers, Program partitioning and scheduling, grain size &latency, Grain packaging and scheduling, Problems on grain packaging, Program mechanisms, control flow &dataflow, demand driven mechanisms, Comparison of flow mechanisms, network properties and routing, Static connection networks, dynamic connection networks.	10
III	**Advanced Processors**: Advanced Processor technology, Instruction set architecture, CISC scalar processors, RISC scalar processors, and Superscalar Processors, VLIW Architectures Vector and Symbolic processors.	8
IV	**Scalable multiprocessors**: Scalability,: bandwidth scaling, latency scaling, cost scaling, physical scaling, realizing programming models, primitive network transactions, shared address space, message pasiing, common challenges, Physical DMA;	8
V	**Pipeling and superscalar techniques**: Linear pipeline processors synchronous &assynchrous Processors, Cocking & timing control, speedup ,efficency,throughput, Reservation &latency analysis, Collision free scheduling, Instruction execution phases, mechanisms for IP, Dynamic instruction scheduling, Compiler arithmetic principles, Multifunctional arithmetic pipeline, static arithmetic pipeline.	12
VI	**Memory Hierarchy design**: Review: Introduction; Cache performance; Cache Optimizations. Memory Hierarchy design: Introduction; Advanced optimizations of Cache performance; Memory technology and optimizations.	8

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	"Computer Architecture A Quantitative Approach".	Hennessey and Patterson	, 4th Edition, Elsevier, 2007
2	"Advanced Computer Architecture Parallelism, Scalability, Programmability",	Kai Hwang	Tata McGraw-Hill, 2003.
3	"Parallel computer architecture"	David culler, J.P.singh, Anoopgupta,	Margon Kauffman1999

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	computer architecture & organization	John P Hayes	1998
2	parallel computers	V rajaramanna , c s r murthy,;	phi 2000

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M.Tech in Digital Electronics

Syllabus for the Academic Year 2020 - 2021

Semester: I
Subject Name: NANOELECTRONICS

Subject Code: 20MDEL153 **L – T – P – C: 4-0-0-4**

Course Objectives:

Sl.No	Course Objectives
1	the course in nanoelectronics are to understand the importance of nanoelectronics, technology roadmap in nanoelectronics and limitations of existing CMOS technologies for design of electronic circuits
2	The course provides an insight on the advances in nanoelectronics devices such as High-K devices, FINFETs, CNTFETs, Molecular Electronics and Spintronics
3	The course provides a strong theoretical and analytical understanding of nanoelectronic devices and its applications in design of electronic circuits.

Course Outcomes

Course outcome	Descriptions
CO1	Understand and appreciate the importance of nanoelectronics and its impact in next generation electronics and electronic products
CO2	Differentiate between MOS and emerging nanodevices technology, understand the advantages and limitations of MOS based circuits
CO3	Understand the technology migration from MOS to nano devices, process challenges and analyze the mathematical models for emerging Nanoscale devices
CO4	Design logic circuits, sub systems and complex digital circuits using FINFETs and CNTFETs and Evaluate the advances in Nanoscale technology development and understand the importance of emerging devices and technologies of molecular electronics and spintronics

UNIT	Description	Hours
I	**Introduction to nanoelectronics:** Technology roadmap of nano-electronics, Scaling of devices and technology jump, Challenge of the CMOS technologies, More-Moore and More-than-Moore. Review of semiconductor devices, Quantum statistical mechanics, Energy bands in silicon, **Metal Oxide Semiconductor Field Effect Transistors (MOSFET),** MOSFET Operation, Threshold Voltage and Subthreshold Slope, Current/voltage characteristics, Finite Element Modeling of MOS, CMOS technology, Challenges of the CMOS technologies, High-k dielectrics and Gate stack, Future interconnect.	10
II	Nanoscale MOSFETs: MOSFET as digital switch, Propagation delay, Dynamic and static power dissipation Moore's law, Transistor scaling, Constant field scaling theory, Constant Voltage Scaling, Generalized scaling, Short channel effects, Reverse short channel effect, Narrow width effect, Subthreshold conduction leakage, Subthreshold slope, Drain Induced Barrier Lowering, Gate Induced Drain Leakage, Design of NanoMOSFET, Halo implants, Retrograde channel profile, Shallow source/drain extensions, Twin well CMOS process flow, Gate Tunneling : Fowler Nordheim and Direct Tunneling, High k gate dielectrics, Metal gate transistor, Transport in Nanoscale MOSFET, Ballistic transport, Channel quantization.	12
III	Designing with FINFETs: Evolution of FinFET, Principle of FinFET, Finfet Technology, FinFET Schematic, Compact Drain-Current equation, Small Signal Model of Si- Based FinFET, FinFET Fabrication Flow, Power dissipation in FinFETs, Leakage power reduction techniques, Power gating, Dual sleep, Dual stack, Sleepy stack, Basic gate design using FinFET's, combinational logic, sequential logic, Adders, Multiplier, SRAM cell design	10
IV	Designing with CNTFETs: Introduction to CNTs, CNT structure, metallic and semiconductor CNTs, energy bands in CNTs, types of CNTs: Single walled and multiwalled, physical, electrical and thermal properties of CNTs, fabrication of CNTs. CNTFETs, structure and model, small signal model, predictive technology models, N-Channel and P-Channel CNTFETs, model files of CNTFETs, basic gates using CNTFET, VI characteristics of CNTFET based inverter, designing of sub systems using CNTFETs, combinational and sequential circuits using CNTFETs, adders, multipliers and SRAM cell using CNTFETs.	10
V	Advances in Nanoelectronics: MOLECULAR NANOELECTRONICS: Electronic and optoelectronic properties of molecular materials, TFTs-OLEDs- OTFTs – logic switches, SPINTRONICS: Spin tunneling devices - Magnetic tunnel junctions- Tunneling spin polarization, - spin diodes - Magnetic tunnel transistor - Memory devices and sensors - ferroelectric random access memory- MRAMS	10

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Fundamentals of Modern VLSI Devices	Yuan Taur and Tak H. Ning	Cambridge University Press, 2nd edition
2	Nanoelectronics and Nano systems	Karl Goser, Peter Glosekotter, Jan Dienstuhl	Springer (2004)
3	Designing with FINFETs and CNTFETs	Cyril Prasanna Raj P.	MSEC E-Publication (2016)
4	Concepts in Spin Electronics	Sadamichi Maekawa	Oxford University Press (2006)

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Introduction to Nanoelectronics	V. Mitin, V. Kochelap, M. Stroscio	Cambridge University Press (2008)
2	Nanophysics and Nanotechnology: An Introduction to Modern Concepts in Nanoscience‖	Edward L. Wolf	Wiley-VCH (2006)

Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: I

Subject Name: Advanced Embedded Systems Lab

Subject Code: 20MDELL17 **L – T – P – C:0-0-3-1**

Course Objectives:

Sl.No	Course Objectives
1	Identify problems and design challenges involved in an Embedded System and program using Embedded C.
2	Write programs for a specific Application.
3	Learn the concept of memory map and memory interface.
4	Know the characteristics of Real Time Systems.

Course Outcomes:

Course outcome	Descriptions
CO1	Apply the knowledge of Programming for differentapplications.
CO2	Analyze the performance of interrupt
CO3	Understand the Building Blocks of Embedded Systems

	Description
I	Create n number of child threads. Each thread prints the message "I am in thread number …" and sleeps for 50 ms/2 sec and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
II	Implement the multithread application satisfying the following: i. Two child threads are created with normal priority. ii. Thread 1 receives and prints its priority and sleeps for 50ms and then quits. iii. Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits. iv. The main thread waits for the child thread to complete its job and quits.
III	Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.
IV	Test the program application for creating an anonymous pipe with 512 bytes of size and pass the "Read Handle" of the pipe to a second process using memory mapped object. The first process writes a message "Hi from Pipe Server". The 2nd process reads the data written by the pipe server to the pipe and displays it on the console. Use event object for indicating the availability of data on the pipe and mutex objects for synchronizing the access in the pipe.
V	Create a POSIX based message queue for communicating between two tasks as per the requirements given below: - i. Use a named message queue with name "My Queue". ii.Create two tasks (Task1 & Task2) with stack size 4000 & priorities 99 & 100 respectively. iii. Task 1 creates the specified message queue as Read Write and reads the message present, if any, from the message queue and prints it on the console. iv. Task2 open the message queue and posts the message Hi from Task2.

Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: II

Subject Name: Modern DSP

Subject Code: 20MDEL21 **L – T – P – C: 4-0-0-4**

Course Objectives:

Sl.No	Course Objectives
1	The objective of this subject is to explore students to advanced concepts of digital signals processing such as filter design, implementation and mutirate systems.
2	Signals and systems analysis using fourier transform and z-transform is other objective of this subject.

Course Outcomes

Course outcome	Descriptions
CO1	Design IIR and FIR filters
CO2	Realize digital filters
CO3	Explain and illustrate concepts of multirate systems
CO4	Make use of multistage filters to design multirate systems

SYLLABUS

UNIT	Description	Hours
I	Signals and Systems: Basics of Signals and Systems, Discrete time processing of continuous signals, Structure of a digital filter, Frequency domain analysis of a digital filter, Quantization error, Sigma and Sigma Delta Modulation, Fourier analysis – DFT, DTFT, DFT as an estimate of the DTFT for Spectral estimation, DFT for convolution, DFT for compression, FFT.	13 Hrs
II	Filters: Ideal Vs non ideal filters, FIR and IIR Filters, Digital Filter Implementation, Elementary Operations, State Space realization, Robust implementation of Digital Filters, Robust implementation of Equi – ripple FIR digital.	13Hrs
III	Multirate Systems and Signal Processing: Fundamentals – Problems and definitions, Up sampling and Down sampling, Sampling rate conversion by a rational factor.	8Hrs
IV	Multistage implementation of Digital filters: Efficient implementation of multirate systems, DFT filter banks and Transmultiplexers, DFT filter banks, Maximally Decimated DFT filter banks and Transmultiplexers, Application of transmultiplexers in Modulation.	8Hrs
V	Maximally Decimated Filter banks and Time Frequency Expansion: Vector spaces, Two Channel Perfect Reconstruction conditions; Design of PR filters Lattice Implementations of Orthonormal Filter Banks, Applications of Maximally Decimated filter banks to an audio signal, Introduction to Time Frequency Expansion, The STFT, The Gabor Transform, The Wavelet transform, Recursive Multi resolution Decomposition.	10 Hrs

Text Books:

Sl No	Title	Authors	Volume and Year of Edition
1	Modern Digital Signal Processing	Roberto Cristi	Cengage Learning; 1ST edition , 2003, ISBN-13: 978-0534400958
2	Digital Signal Processing: A Computer Based Approach	S.K. Mitra	III edition, Tata McGraw Hill, India,2007, ISBN-13: 978-1259098581

Reference Books:

Sl No	Title	Authors	Volumeand Year of Edition
1	Digital Signal Processing, a practitioners approach	E.C. Ifeachor and B W Jarvis	II Edition, Pearson Education, India, 2002 Reprint.
2	Digital Signal Processing	Proakis and Manolakis	Prentice Hall 1996(third edition)

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Syllabus for the Academic Year – 2020 – 2021

Semester: II

Subject Name: SYTHESIS AND OPTIMIZATION OF DIGITAL CIRCUILTS

Subject Code: 20MDEL22

Course Objectives:

Sl.No	Course Objectives
1	To understand different methods used for the simplification of Boolean functions.
2	To understand the concepts of system modelling and different optimizations of combinational , synchronous, and asynchronous sequential circuits.
3	To outline the formal procedures for the analysis and synthesis of combinational circuits and sequential circuits using computer aided synthesis.

Course Outcomes:

Course outcome	Descriptions
CO1	Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation.
CO2	Understand the process of synthesis and optimization in a top down approach for digital circuits models using HDLs.
CO3	Apply different two level and multilevel optimization algorithms for combinational circuits.
CO4	Apply the different sequential circuit optimization methods using state models and network models.

UNIT	Description	Hours
I	**Introduction:** Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization. **Graphs:** Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.	12
II	**Hardware Modeling:** Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, dataflow and sequencing graphs, compilation and optimization techniques.	10
III	**Two Level Combinational Logic Optimization:** Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations.	10
IV	**Multiple Level Combinational Optimizations:** Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.	10
V	**Sequential Circuit Optimization:** Sequential circuit optimization using state based models, sequential circuit optimization using network models. **Cell Library Binding:** Algorithms for Technology mapping – Structural and Boolean matching, Simulation & Static Timing analysis - Event driven simulation – zero delay, unit delay and nominal delay simulation, Timing analysis at the logic level, Delay models, Delay graph, static sensitization.	10

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Synthesis and Optimization of Digital Circuits	Giovanni De Micheli	Tata McGraw-Hill, 2003.
2	Logic Synthesis	Srinivas Devadas, Abhijit Ghosh, and Kurt Keutzer	McGraw-Hill, USA, 1998.

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Logic Synthesis and Verification Algorithms	G. D. Hachtel and F. Somenzi	Kluwer Academic Publishers, 1996.
2	Logic Synthesis and Verification	S. Hassoun and T. Sasao, (Editors)	Kluwer Academic publishers, 2002

SUPPLEMETARY SOURCE:

- **NPTEL** Video Lectures

Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: II

Subject Name: MEMS (MICRO ELECTRO MECHANICAL SYSTEMS)

Subject Code: 20MDEL23

Course Objectives:

Sl.No	Course Objectives
1	To familiarize with MEMS Materials and Scaling Laws in Miniaturation.
2	To revive various concepts of Engineering Mechanics and Thermo fluid Engineering for Microsystems Design.
3	To study Microsystems Fabrication Process.
4	To familiarize with Microsystems Design, Assembly and Packaging.
5	To explore on various Case Study of MEMS Devices.

Course Outcomes:

Course outcome	Descriptions
CO1	Understand the fundamentals of MEMS and its Design methodology.
CO2	Understand various Mechanical & Electronics Sensors and its applications.
CO3	Analyze various bonding and packaging techniques in MEMS.
CO4	Understand the scaling issues in MEMS.

UNIT	Description	Hours
I	**OVERVIEW OF MEMS AND MICROSYSTEMS, MEMS MATERIALS AND SCALING LAWS IN MINIATURATION:** MEMS and Microsystems - Microsystems and microelectronics, Microsystems and miniaturization, Working principle of micro system - Micro sensors, Micro actuators, MEMS with Micro actuators. Materials for MEMS - Substrate & wafer, Si as a substrate material, Si compound, Si Piezo-resistors, Gallium Arsenide, quartz, Piezoelectric crystals, polymers packaging Materials. Scaling Laws in Miniaturization-Scaling in Geometry, scaling in Rigid-Body Dynamics, scaling in Electrostatic Forces, scaling in Electromagnetic Forces, scaling in Electricity, scaling in Fluid Mechanics, Scaling in Heat Transfer.	12
II	**ENGINEERING MECHANICS AND THERMOFLUID ENGINEERING FOR MICROSYSTEMS DESIGN:** Atomic structure of matter, Ions and ionization, Molecular theory of matter and intermolecular forces, Doping of semiconductors, Diffusion process, Plasma physics, Electrochemistry, Static bending of thin plates, Mechanical vibration analysis, Thermo mechanical analysis, Overview of finite element analysis. Thermo fluid Engineering-Characteristics of Moving Fluids, The Continuity Equation, The Momentum Equation, Incompressible Fluid Flow in Micro conduits, Overview of Heat Conduction in Micro Structures.	10
III	**MICROSYSTEMS FABRICATION PROCESS:** Fabrication Process - Photolithography, Ion implantation, Oxidation, Chemical vapor deposition (CVD), Physical vapor deposition, Deposition by Epitaxy, Etching. Manufacturing Process - Bulk Micromachining, Surface Micromachining and LIGA Process.	10
IV	**MICROSYSTEMS DESIGN, ASSEMBLY AND PACKAGING:** Micro system Design - Design consideration, process design, Mechanical design, Mechanical design using MEMS. Mechanical packaging of Microsystems, Microsystems packaging, interfacings in Microsystems packaging, packaging technology, selection of packaging materials, signal mapping and transduction.	10
V	**CASE STUDY OF MEMS DEVICES:** Case study on strain sensors, Temperature sensors, Pressure sensors, Humidity sensors, Accelerometers, Gyroscopes, RF MEMS Switch, phase shifter, and smart sensors. Case study of MEMS pressure sensor Packaging.	10

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	MEMS and Microsystems: design , manufacture, and nanoscale Engineering	Tai-Ran Hsu, John Wiley and Sons, Inc., Hoboken	New Jersey, 2008. 2nd Edition.
2	Foundations of MEMS	Chang Liu	Pearson Indian Print, 1st Edition, 2012.

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	RF MEMS - Theory Design and Technology	Gabriel M Rebeiz	John Wiley & Sons, 2004.
2	Micro sensors MEMS and smart devices	Julian W Gardner	John Wiley and sons Ltd, 2001.

Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: II

Subject Name: REAL TIME EMBEDDED SYSTEM

Subject Code: 20MDEL24 **L – T – P – C: 4-0-0-4**

Course Objectives:

Sl.No	Course Objectives
1	The objective of the course is to learn and understand the implementation and applications of the embedded system.
2	Discuss the historical background of Real-time systems and its classifications.
3	The course also covers the various software development approaches and a operating system services required. Hence the course is the unified approach of both hardware and software in designing the embedded system.
4	Discuss the languages to develop software for Real- Time Applications. The objective of the course is to learn and understand the implementation and applications of the embedded system.

Course Outcomes

Course outcome	Descriptions
CO1	Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems.
CO2	Become aware of the architecture of the ARM processor and its programming aspects (assembly Level)
CO3	Become aware of interrupts, software optimization., Design real time embedded systems using the concepts of RTOS, commercially available RTO's, Analyze various examples of embedded systems

	:

SYLLABUS

UNIT	Description	Hours
I	**Unit 1:** Introduction: Real Time System, Types, Real Time Computing, Design Issue, Sample Systems, Hardware Requirements- Processor in a system, System Memories, System I/O, Other Hardware Devices (A/D, D/A, USART, Watchdog Timers, Interrupt Controllers). Device Drivers, Interrupt Servicing Mechanism & Interrupt Latency.	**12**
II	**Unit 2:** ARM Processor Fundamentals and ARM7TDMI: ARM Processor Registers, current program status register, Pipeline Exceptions, Interrupt and vector table, Reset operation. ARM7 TDMI processor block diagram, ARM7TDMI Features, programmer's model, sample programs [Text: 2 chapter1.1 to 1.4 & chapter 2.1 to 2.4]	**10**
III	**Unit 3:** Real Time Operating System: Fundamental Requirements of RTOS, Real Time Kernel Types, Schedulers, Various Scheduling modules with examples, Latency (Interrupt Latency, Scheduling Latency and Context Switching Latency), Tasks, State Transition Diagram, Task Control Block. Inter-task communication and synchronization of tasks.	**10**
IV	**Unit 4:** Memory and File management: Pipelining and Cache Memories, Paging and Segmentation, Fragmentation, Address Translation.	**10**
V	**Unit 5:** Introduction to VX Works/Mucos/pSOS; Example systems., development and Verification of Real Time Software: Building Real Time applications; Considerations such as double buffing.	**10**

Text Books:

Sl No	Title	Authors	Volume and Year of Edition
1	"An Embedded software primer", Pearson Education Inc.,	David E. Simon	2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
2	ARM System Developer's Guide	Andrew N. Sloss, Dominic Symes and Chris Wright..	
3	"Real-Time Systems Design and Analysis- an Engineer's Handbook"-	Philip. A. Laplante,	Second Edition, PHI Publications.

Reference Books:

Sl No	Title	Authors	Volume and Year of Edition
1	"Real-Time Systems",	3.Jane W.S. Liu,	Pearson Education Inc., 2000.
2	"Embedded Systems: Architecture, Programming and Design",	Rajkamal	Tata McGraw Hill, New Delhi.
3	"Embedded Real Time Systems: Concepts Design and Programming",	Dr. K.V.K K Prasad,	Dream tech Press New Delhi.

Department of Electronics and Communication

M.Tech in VLSI & Embedded systems

Syllabus for the Academic Year – 2020 - 2021

Semester: II

Subject Name: Digital System Design using Verilog

Subject Code: 20MDEL251 **L – T – P – C : 4-0-0-4**

Course Objectives :

Sl.No	Course Objectives
1	Understand the concepts of Real world circuits, Models and Design Methodology.
2	Discuss the Combinational Circuits and Sequential Circuits , its verilog code and its Verification.
3	Implement the design of systems like Memories, interconnect etc.
4	Design and develop the processor basics and I/O interfacing.

Course Outcomes

Course outcome	Descriptions
CO1	Analyze the knowledge of Digital Systems and Embedded Systems.
CO2	Design and Understand the concepts of Combinational circuits and its Verification.
CO3	Design and Understand the concepts of sequential basics and memories.
CO4	Understand the Concepts of Design methodology and I/O Interfacing circuits

SYLLABUS

UNIT	Description	Hours
I	**Unit 1:** **Introduction and Methodology:** Digital Systems and Embedded Systems, Binary Circuit Elements, Real-World Circuits, Models, Design Methodology. **Combinational Basics:** Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.	**11Hrs .**
II	**Unit 2:** **Number Basics**: Unsigned and Signed Integers, Fixed and Floating-point Numbers. **Sequential Basics**: Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology.	**11Hrs**
II	**Unit 3:** **Memories:** Concepts, Memory Types, Error Detection and Correction. Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity	**10Hrs**
III	**Unit 4:** **Processor Basics:** Embedded Computer Organization, Instruction and Data, Interfacing with memory. **I/O interfacing:** I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.	**10Hrs**
IV	**Unit 5:**. **Accelerators**: Concepts, case study, Verification of accelerators. **Design Methodology:** Design flow, Design optimization, Design for test.	**10Hrs**

Text Book:

Sl No	Text Book title	Authors	Volume and Year of Edition
1	Digital Design: An Embedded Systems Approach Using VERILOG	Peter J. Ashenden	Elsevier, 2010.

Reference Books:

Sl No	Text Book title	Authors	Volume and Year of Edition
1	A Verilog HDL Primer	J. Bhasker	Second Edition, Star Galaxy, 2005
2	A Verilog Synthesis: A Practical Primer	J. Bhasker	Star Galaxy, 1998

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Department of Electronics and Communication

M. Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: II

Subject Name: DSP Integrated Circuits

Subject Code: 20MDEL252 **L – T – P – C: 4-0-0-4**

Course Objectives :

Sl.No	Course Objectives
1	To familiarize the concept of DSP and DSP algorithms.
2	Introduction to Multirate systems and finite word length effects
3	To know about the basic DSP processor architectures and the synthesis of the processing elements

Course Outcomes

Course outcome	Descriptions
CO1	Get to know about the Digital Signal Processing concepts and its algorithms
CO2	Get an idea about finite word length effects in digital filters.
CO3	Concept behind multi rate systems is understood
CO4	Get familiar with the DSP processor architectures and how to perform synthesis of processing elements

UNIT	Description	Hours
I	**INTRODUCTION TO DSP INTEGRATED CIRCUITS:** Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Application specific ICs for DSP.	12
II	**DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS:** FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels.	10
III	**DSP ARCHITECTURES:** DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures.	10
IV	**SYNTHESIS OF DSP ARCHITECTURES:** Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks- Storage elements.	10
V	**ARITHMETIC UNIT AND PROCESSING ELEMENTS :** Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator.	10

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Digital Signal Processors	B.Venkatramani, M.Bhaskar	Tata McGraw-Hill, 2002.
2	DSP Integrated Circuits	Lars Wanhammer	Academic press, New York, 1999.

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	VLSI Digital Signal Processing Systems design & Implementation	Keshab Parhi	John Wiley & Sons, 1999.
2	Digital Signal Processing	John J. Proakis, Dimitris G. Manolakis	Pearson Education, 2002.

Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: II

Subject Name: Neural networks and Fuzzy Logic

Subject Code: 20MDEL253 **L – T – P – C : 4-0-0-4**

Course Objectives :

Sl.No	Course Objectives
1	To master the various fundamental concepts of fuzzy logic and artificial neural networks.
2	Learn the architecture and algorithm of Cognitron, Neo cognitron and the concepts of fuzzy associative memory and fuzzy systems.
3	Helps to gain sufficient knowledge to analyze and design the various intelligent control systems

Course Outcomes

Course outcome	Descriptions
CO1	Understand the basic concepts of fuzzy sets, fuzzy logic, fuzzy associative memory, defuzzification principle of competitive neural networks.
CO2	Design, develop and implement a fuzzy logic based decision-making system.
CO3	Analyze various techniques in feedback and feed forward neural networks.
CO4	Select and train an artificial neural network to be able to perform a certain task or simulate a specific function or system.

UNIT	Description	Hours
I	**FUNDAMENTALS OF FUZZY LOGIC** Basic concepts: fuzzy set theory-basic concept of crisp sets and fuzzy sets- complements- union intersection-combination of operation- general aggregation operation fuzzy relations compatibility relations-orderings- morphisms- fuzzy relational equations-fuzzy set and systems	10
II	**ARCHITECTURE OF NEURAL NETWORKS** Architectures: motivation for the development of natural networks-artificial neural networksbiological neural networks-area of applications-typical Architecture-setting weights-common activations functions- Basic learning rules- Mcculloch-Pitts neuron-Architecture, algorithm,applications-single layer net for pattern classification-Biases and thresholds, linear separability -Hebb'srule- algorithm -perceptron - Convergence theorem-Delta rule.	12
III	**BASIC NEURAL NETWORK TECHNIQUES:** Back propagation neural net:standard back propagation-architecture algorithm- derivation of learning rules-number of hidden layers--associative and other neural networks- hetro associative memory neural net, auto associative net- Bidirectional associative memory-applications-Hopfield nets-Boltzman machine.	10
IV	**COMPETITIVE NEURAL NETWORKS** Neural network based on competition: fixed weight competitive nets- Kohonenself organizing maps and applications-learning vector quantization-counter propagation nets and applications adaptive resonance theory: basic architecture and operation-architecture, algorithm, application and analysis of ART1 & ART2	10
V	**SPECIAL NEURAL NETWORKS** Cognitron and Neocognitron-architecture, training algorithm and application-fuzzy associate memories, fuzzy system architecture- comparison of fuzzy and neural systems	10

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	**Fuzzy sets and fuzzy logic: theory and applications**	**George j. Klir and bo yuan**	Prentice hall,1994
2	**Fundamentals of Neural Networks: Architectures, Algorithms And Applications**	**Laurene V. Fausett**	**Prentice hall, 1st Edition**

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Neural network and Fuzzy System	Bart Kosko	Prentice Hall-1994.
2	Fuzzy sets‖ University and information	J.Klin and T.A.Folger	Prentice Hall -1996
3	Introduction to artificial neural systems	J.M.Zurada	Jaico Publication house,Delhi 1994
4	C++ Neural network and fuzzy logic	VallusuRao and HayagvnaRao	BPB and Publication, New Delhi,1996

Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: II

Subject Name: Modern DSP Lab

Subject Code: 20MDELL27 **L – T – P – C: 0-0-3-1**

Course Objectives:

Sl.No	Course Objectives
1	To train students to simulate digital filters
2	To design DSP systems to perform filtering and other basic operations

Course Outcomes

Course outcome	Descriptions
CO1	Design IIR and FIR filters
CO2	Realize digital filters
CO3	Simulate DSP systems using MATLAB tool

SYLLABUS

Description
USING MATLAB, write program for the following and simulate. 1. A LTI system is defined by the difference equation y[n] = x[n] +x [n-1] +x [n-2]. (a) Determine the impulse response of the system and sketch it. (b) Determine the output y[n] of the system when the input is x[n] = u[n]. (c) Determine the output of the system when the input is a complex exponential x[n] = $2e^{(j0.2\pi n)}$ 2. Computation of FFT when N is not a power of 2. 3. Sampling rate conversion and spectrum plot. 4. Record machinery noise like fan or blower or diesel generator and obtaining its spectrum. 5. Fourier Transform and its inverse Fourier Transform of an image. 6. Design a simple digital FIR filter with real co-efficients to remove a narrowband (i.e., sinusoidal) disturbance with frequency F0=50 Hz. Let Fs=300 Hz is the sampling frequency. (a) Determine the desired zeros and poles of the filter. (b) Determine the filter coefficients with the gain K=1. (c) Sketch the magnitude of the frequency response. 7. Design an IIR filter with real co-efficients with same specifications mentioned in Q2 and repeats the steps (a) to (c). 8. Generate a signal with two frequencies x(t)=3cos(2πF1t) + 2cos(2πF2t) sampled at Fs=8 kHz. Let F1=1 kHz and F2=F1+Δ and the overall data length be N=256 points. (a) From theory, determine the minimum value of Δ necessary to distinguish between the two frequencies. (b) Verify this result experimentally. Using the rectangular window, look at the DFT with several values of Δ so that you verify the resolution. 9. Generate the sequence x[n] = n - 64 for n = 0,…127.

(a) Let X[k] = DFT{x[n]}. For various values of L, set to zero the "high frequency coefficients" X [64 – L] =….X[64]=…….=X[64+L]=0 and take the inverse DFT. Plot the results.

(b) Let XDCT[k]=DCT(x[n]}. For the same values of L, set to zero the "high frequency coefficients" XDCT[127-L]=…….XDCT[127]. Take the inverse DCT for each case and compare the reconstruction with the previous case.

10. Design a discrete time low pass filter with the specifications given below:

Sampling frequency = 2 kHz.

Pass band edge = 260 Hz

Stop band edge = 340 Hz

Max. pass band attenuation = 0.1 dB

Minimum stop band attenuation = 30 dB

Use the following design methodologies:

Hamming windowing, Kaiser Windowing and Applying bilinear transformation to a suitable, analog Butterworth filter.

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Syllabus for the Academic Year – 2020 - 2021

Semester: IV

Subject Name: Memory Technologies

Subject Code: 20MDEL411 **L – T – P – C:4-0-0-4**

Course Objectives :

Sl.No	Course Objectives
1	Understand the various benefits involved in Memory Technologies design and typical design goals related to Memories.
2	Apply the concepts of memory hybrids.
3	Understand the concepts related to advanced memory technologies, co-design and various memory packaging issues.

Course Outcomes

Course outcome	Descriptions
CO1	Interpret the different challenges involved in Memory Technologies and compare different Memories such as RAMS,DRAMS and Non-Volatile Memories.(L2).
CO2	Explain variousmemory architecture and high density memory packaging technologies in Memory Technologies.(L2).

CO3	Explain the design concepts of Memory design with reference to hybrid memory packaging related problems.(L2).

SYLLABUS

UNIT	Description	Hours
I	**Random Access Memory Technologies:** Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.	10
II	**DRAM:** MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers	**10**
III	**Non-Volatile Memories:** Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.	**10**
IV	**Advanced Memory Technologies and High-density Memory Packing Technologies:** Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.	**12**
V	**Memory Hybrids:** Memory Hybrids – 2D & 3D, Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging	**10**

Text Books:

Sl No	Text Book title	Authors	Volume and Year of Edition
1	"Advanced Semiconductor Memories: Architectures, Designs and Applications"	Ashok K Sharma	Wiley Publications, 2002.

Reference Book:

Sl No	Text Book title	Authors	Volume and Year of Edition
1	"VLSI memory chip design"	KiyooItoh	1st Edition, Springer Series in Advanced Microelectronics, 2001.
2	"Semiconductor Memories: Technology, Testing and Reliability"	Ashok K Sharma,	PHI, 1997.

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M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: IV

Subject Name: RF Microelectronics chip design

Subject Code: 20MDEL412 **L – T – P – C : 4-0-0-4**

Course Objectives :

Sl.No	Course Objectives
1	To introduce the theory and concept of radio frequency integrated system.
2	To analyze the performance parameters of radio frequency circuits and identify design trade-off of radio frequency communication systems
3	To enhance their understanding of the design problems encountered in RF integrated circuits.
4	To cover the circuit design theory and their implementation techniques at RF frequencies

Course Outcomes

Course outcome	Descriptions At the end of this course students will be able
CO1	To understand basics of RF and wireless technology.
CO2	To analyze the circuits in analog and digital modulation.
CO3	To understand vlsi technology involved in RF systems.
CO4	To analyze design issues in RF integrated circuits.

UNIT	Description	Hours
I	Introduction to RF and Wireless Technology: Complexity, design and applications. Choice of Technology. Basic concepts in RF Design: Nonlinearly and Time Variance, inters symbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion.	10 Hours
II	Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non coherent defection. Mobile RF Communication systems and basics of Multiple Access techniques. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation.	16 hours
III	Basic blocks in RF systems and their VLSI implementation : Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonatorless VCO design. Quadrature Single-sideband generators.	12 Hours

IV	Radio Frequency Synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearisation techniques	8 Hours
V	Design issues in integrated RF filters., Some discussion on available CAD tools for RF VLSI designs	6 Hours

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	RF Microelectronics,.	B.Razavi,	Prentice-Hall PTR,1998
2	The Design of CMOS Radio-Frequency Integrated Circuits	T.H.Lee	Press, 1998.

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	CMOS Circuit Design ,Layout and Simulation, •	R.Jacob Baker,H.W.Li, and D.E. Boyce	Prentice-Hall of ,1998.
2	Mixed Analog and Digital VLSI Devices and Technology.	Y.P. Tsividis	McGraw Hill,1996

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Syllabus for the Academic Year – 2020 - 2021

Semester: IV

Subject Name: Reliability Engineering

Subject Code:20MDEL413 **L – T – P – C: 4-0-0-4**

Course Objectives:

Sl.No	Course Objectives
1	Understand and emphasizes dependability in the lifecycle management of a product.
2	Apply and identify and manage assets reliability risks that could adversely affect plant or business operations.
3	Understand the concepts related to reliability engineering

Course Outcomes

Course outcome	Descriptions
CO1	Interpret the basic concepts of reliability engineering and its measures
CO2	Predict the reliability at system level using various models
CO3	Design the test plan to meet the reliability requirements
CO4	Predict and estimate the reliability from failure data

UNIT	Description	Hours
I	**Introduction** :Basic definitions: Reliability, Availability, Serviceability, Failure rate,ReliabilityMathematics, Failure distribution - constant failure rate model, Time dependent failure rate models and its types, Bath tub curve. case study or Videos on Human Reliability,Software Reliability.	10
II	**System Reliability:** Reliability Block Diagram - Series, Parallel & combined seriesparallelconfigurations;redundant-active and passive types, Failure Mode, Effects and Criticality Analysis (FMECA), Failure Reporting, Analysis and Corrective Action System (FRACAS),Fault Tree Analysis (FTA), System state analysis-Markov Model, Availability, Downtime.	10
III	**Reliability testing:** Failures and types of failures; Intrinsic & extrinsic failures;Failurecascade; Failure mode; Failure rate, MTTF, MTBF, Accelerated life testing (ALT) -Qualitative ALT, Quantitative ALT & its types, AF, Samples	10
IV	**Reliability estimation and life Prediction:** Types of Failure data - Datacensoring,Parametric and Non Parametric distribution, Probability density function,Exponential, Normal, lognormal &weibull distributions, weibull Goodness of fit distributions,Electronics reliability prediction-parts count, parts stress method, MIL standard, Naval Surface Warfare Center (NSWC).	10
V	**Reliability Management:** Design for Reliability, Relationship between Reliability and safetyfactor, Stress-Strength interference theory, Reliability growth testing, Reliability centered maintenance (RCM), Spares planning.	12

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	**Reliability Engineering**,	Kailash C. Kapur, Michael Pecht,	John Wiley & Sons, 2014.
2	**"Reliability Engineering"**	Srinath L.S	East-West Press Pvt Ltd, New Delhi,1998.

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	**Reliability and Risk analysis**	Modarres	Marshal Dekker Inc.1993.
3	**"Introduction to Reliability in Design"**	Smith C.O.Roy Billington and Ronald N. Allan	, McGraw Hill, London, 1976.
4	"**An introduction to Reliability and Maintainability engineering"**,	Charles E. Ebeling,	TMH, 2004

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Syllabus for the Academic Year – 2020 - 2021

Semester: IV

Subject Name: Internet of Things

Subject Code: 20MDEL421 **L – T – P – C : 4-0-0-4**

Course Objectives: The students will be able to:

Sl.No	Course Objectives
1	Understand the way the number of devices in the Physical world, with different type of technologies, the mode of interconnections and the integration is enabled in order that intelligent services are provided.
2	Obtain information about collaborating and integrating the data from different objects subjected to non-uniformity, inconsistency and inaccuracy
3	Understand the Complete way of realizing smart services like surveillance networks.

Course Outcomes

Course outcome	Descriptions
CO1	Outline the OSI model for the IOT/M2M Systems. (L1)
CO2	Interpret the architecture and design principles for IOT. (L3)
CO3	Study the Programming for IOT applications. (L3 & L4)
CO4	Describe the conventional Protocols which are adaptive to the Wireless Sensor networks. (L2)

UNIT	Description	Hours
I	**Overview of Internet of Things**: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT,XMPP) for IoT/M2M devices.	10
II	**Architecture and Design Principles for IoT**: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports.	10
III	**Data Collection, Storage and Computing using a Cloud Platform**: Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits.	10
IV	**Prototyping and Designing Software for IoT Applications:** Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development. Programming MQTT clients and MQTT server. Introduction to IoT privacy and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model.	10
V	**Communication Protocols:** Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering.	10

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Internet of Things-Architecture and design principles	Raj Kamal	McGraw Hill Education
2	Protocols and Architectures for Wireless Sensor Networks	Holger Karl & Andreas Willig	John Wiley, 2005.
3	Wireless Sensor Networks- An InformationProcessing Approach	Feng Zhao & Leonidas J. Guibas.	Elsevier, 2007

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Wireless Sensor Networks Technology, Protocols and Applications	Kazem Sohraby, Daniel Minoli & Taieb Znati.	John Wiley, 2007
2	Wireless Sensor Network Designs	Anna Hac	John Wiley, 2003.

Department of Electronics and Communication

M.Tech in VLSI & Embedded systems

Syllabus for the Academic Year – 2020 - 2021

Semester: IV
Subject Name: DEEP LEARNING

Subject code : 20MDEL422 **L – T – P – C:4-0-0-4**

Course Objectives

Sl.No	Course Objectives
1	To present the mathematical, statistical and computational challenges of building neural network.
2	To study the concepts of deep learning and introduce dimensionality reduction techniques.
3	To enable the students to know deep learning techniques to support real-time applications.
4	To examine the case studies of deep learning techniques.

Course Outcomes

Course outcome	Descriptions
CO1	Understand basics of deep learning Implement various deep learning models.
CO2	Realign high dimensional data using reduction techniques.
CO3	Analyze optimization and generalization in deep learning.
CO4	Explore the deep learning applications.

UNIT – I: INTRODUCTION Introduction to machine learning- Linear models (SVMs and Perceptrons, logistic regression)- Intro to Neural Nets: What a shallow network computes- Training a network:loss functions, back propagation and stochastic gradient descent- Neural networks as universalfunction approximates. **12Hours**
UNIT-II:DEEP NEWORKS History of Deep Learning- A Probabilistic Theory of Deep Learning- Backpropagation and regularization, batch normalization- VC Dimension and Neural Nets- Deep VsShallow Networks, Convolutional Networks- Generative Adversarial Networks (GAN), SemisupervisedLearning.**10Hours**
UNIT-III: DIMENTIONALITY REDUCTION Linear (PCA, LDA) and manifolds, metric learning – Autoencoders and dimensionality reduction in networks - Introduction to Convnet - Architectures –AlexNet, VGG, Inception. **10Hours**
UNIT-IV:OPTIMIZATION AND GENERALIZATION Optimization in deep learning– Non-convex, optimization for deep networks- Stochastic Optimization Generalization in neural networks- SpatialTransformer Networks- Recurrent networks. **10Hours**
UNIT-V: CASE STUDY AND APPLICATIONS Imagenet- Detection-Audio Wave Net-Natural LanguageProcessing Word2Vec - Joint Detection BioInformatics- Face Recognition- Scene Understanding-Gathering Image Captions. **10Hours**

Text Books:

Sl No	Title	Authors	Volume and Year of Edition
1	Advanced Data Analysis from an Elementary Point of View	CosmaRohillaShalizi,	2015.

Reference Books:

Sl No	Title	Authors	Volumeand Year of Edition
1	Deep Learning: Methods and Applications	Deng & Yu,	NEw Publishers, 2013
2	Deep Learning	Ian Goodfellow, YoshuaBengio, Aaron Courville	MIT Press, 2016.
3	Neural Networks and Deep Learning	Michael Nielsen	Determination Press, 2015

Department of Electronics and Communication

M.Tech in Digital Electronics

Syllabus for the Academic Year – 2020 - 2021

Semester: IV

Subject Name: AD HOC Wireless Networks

Subject Code: 20MDEL423 **L – T – P – C : 4-0-0-4**

Course Objectives :

Sl.No	Course Objectives
1	To make students learn fundamentals of Adhoc networks and sensor nodes.
2	To provide in depth knowledge on sensor node architecture, design issues and routing algorithms.
3	To understand transport layer and security issues possible in Ad-hoc and sensor networks
4	To provide exposure on mote programming platforms and tools

Course Outcomes

Course outcome	**Descriptions**
CO1	Technical know how the fundamentals of Adhoc networks and wireless sensor Networks. (L2)
CO2	Apply this knowledge to identify appropriate routing technique suitable to user requirements. (L3)
CO3	Applying this knowledge to identify suitable physical and MAC and transport layer Protocols. (L3)
CO4	Familiarize with the OS and energy significance of WSN to build basic modules. (L4)

UNIT	Description	Hours
I	Ad Hoc Networks – Introduction And Routing Protocols Elements of Ad hoc Wireless Networks, Issues in Ad hoc wireless networks, Example commercial applications of Ad hoc networking, Ad hoc wireless Internet, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classifications of Routing Protocols, Table Driven Routing Protocols – Destination Sequenced Distance Vector (DSDV), On–Demand Routing protocols –Ad hoc On–Demand Distance Vector Routing (AODV).	11
II	Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks, WSN application examples, Single-Node Architecture – Hardware Components, Energy Consumption of Sensor Nodes, Network Architecture – Sensor Network Scenarios, Transceiver Design Considerations, Optimization Goals and Figures of Merit	10
III	MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts – S-MAC, The Mediation Device Protocol, Contention based protocols – PAMAS, Schedule based protocols – LEACH, IEEE 802.15.4 MAC protocol, Routing Protocols, Energy Efficient Routing, Challenges and Issues in Transport layer protocol.	11
IV	Network Security Requirements, Issues and Challenges in Security Provisioning, Network Security Attacks, Layer wise attacks in wireless sensor networks, possible solutions for jamming, tampering, black hole attack, flooding attack. Key Distribution and Management, Secure Routing – SPINS, reliability requirements in sensor networks.	10
V	Sensor Node Hardware – Berkeley Motes, Programming Challenges, Node-level software platforms – TinyOS, nesC, CONTIKIOS, Node-level Simulators – NS2 and its extension to sensor networks, COOJA, TOSSIM, Programming beyond individual nodes – State centric programming.	10

Text Books:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Ad-hoc Wireless Networks	C. Siva Ram Murthy & B. S. Manoj:	2nd Edition, Pearson Education, 2011

Reference Book:

Sl No	Text Book title	Author	Volume and Year of Edition
1	Ad-hoc Wireless Networks	Ozan K. Tonguz and Gianguigi Ferrari:	John Wiley, 2007.
2	Ad-hoc Wireless Networking	Xiuzhen Cheng, Xiao Hung, Ding-Zhu Du:	Kluwer Academic Publishers,2004.
3	Ad-hoc Mobile Wireless Networks-Protocols and Systems,	C.K. Toh	Pearson Education, 2002