DESIGN & TESTING OF A RC COUPLED SINGLE STAGE BJT AMPLIFIER

Aim: Wiring of a RC coupled single stage BJT amplifier and determination of the gain-frequency response, input and output impedances.

Apparatus required: Transistor BC107, power supply, capacitors 0.22μF, 47μF, resistors, connecting board, signal generator, digital multimeter and CRO.

Theory:

This is the most popular type of coupling because it is cheap and provides excellent audio fidelity over a wide range of frequency. It is usually employed for voltage amplification. Fig.3.1 shows the single stage of an RC coupled amplifier. The coupling does not affect the Q point of the next stage since the C_2 blocks the dc voltage of the first stage from reaching the base of the second stage or output. The function of C_1 is to couple the signal source v_i to the base of the transistor. At the same time it prevents the dc current of V_{cc} from reaching the signal source v_i and also prevents any dc component present in v_i from reaching of base.

The bypass capacitor C_e is used to prevent the loss of gain due to negative feedback across the resistor R_e.

Resistors R_1, R_2, and R_e are used to bias the transistor so that the operating point lie on the middle of the dc load line.

The resistor R_c acts as ac load for the amplifier.

The RC network is broadband in nature. Therefore, it gives a wideband frequency response and hence used to cover AF range of amplifier.

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Procedure to obtain frequency response:

1) Before wiring the circuit, check all the components using multimeter.

Connect the circuit as shown in the figure. Set Vcc for the designed value, and check the DC biasing conditions such as $V_{BE,}$ $V_{CE.}$ $V_{BE}\approx 0.6V$ (for Silicon transistor), $V_{CE}\approx V_{CC}/2$.

2) If the DC biasing conditions satisfy then set the signal generator (input-voltage) amplitude (peak-to-peak sine wave) so that the output remains sinusoidal. Note the maximum signal handling capacity (MSHC) of the amplifier. It is the input signal to the amplifier at which output remains just sinusoidal. This means that if the input increased beyond this value, output no longer remains sinusoidal.
3) Keep the input signal less than MSHC (do not change the input further) and vary the frequency of the input from lower range to higher range. Observe both input and output simultaneously on the CRO. Note the input value (peak to peak) and outputs across R_L corresponding to the variation in frequencies of the input signal at different intervals. The output voltage remains constant at mid frequency range.
4) Plot the graph with frequency along X-axis and gain dB along Y-axis.
5) From graph determine bandwidth.

Procedure to find input impedance:

1) Connect the circuit as shown in Fig 3.2.
2) Connect a resistance R_S in series with the input signal and amplifier as shown in the figure 3.2.
3) Set the signal generator (input voltage) amplitude (peak to peak sine wave) less than MSHC at a mid frequency band.
4) Measure and note down the input voltage V_i before R_S and voltage V'_i after $R_{S.}$
5) Calculate the input impedance.

Procedure to find output impedance:

1) Connect the circuit as shown in Fig 3.3.
2) Connect a resistance R_L across the output terminals of the amplifier as shown in the figure 3.3.
3) Set the signal generator (input voltage) amplitude (peak to peak sine wave) less than MSHC at a mid frequency band.
4) Measure and note down the output voltage V_o across output terminals when R_L is open circuited and output voltage V'_o when R_L connected across the output terminals.
5) Calculate the output impedance.

CIRCUIT DIAGRAM

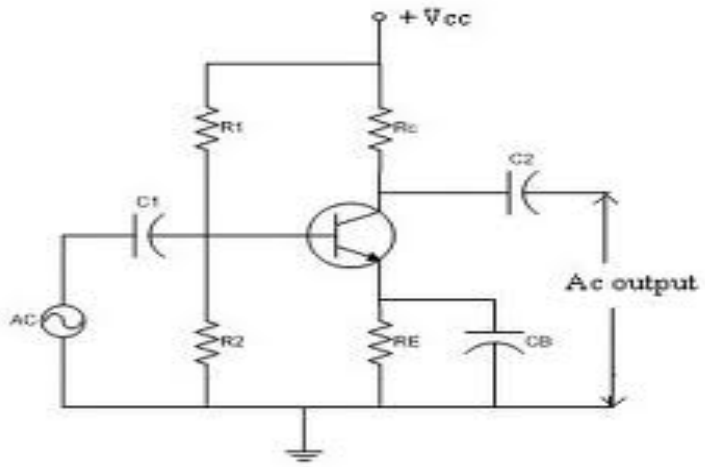


Figure 3.1

DESIGN

Let **Vcc=20V** Ic=10mA ;V_{CE}=Vcc/2=10V ;Pd=$V_{CEQ}I_{CEQ}$=10*10*1e-3=100mw

$V_E \approx Vcc/10=20/10=2V$;$I_E \approx Ic$;$R_E=V_E/I_E=2/10*1e-3=200\Omega$

select standard value RE=220Ω

$V_E=2*10*1e-3=2.2V$

$Rc=(Vcc-V_{CE}-V_E)/Ic=(20-10-2)/10*1e-3=780\Omega$

select standard value Rc=820Ω

$R2 \leq \beta R_E/10$ $\beta=G_{FE}=125(min)$

$\leq 2750\Omega$

select R2=2.7KΩ

$V_B=0.7+2.2=2.9V$

$2.9=(2.7*1e3*20)/(R1+2.7*1e3)$

$= 15920$

select standard value of 18KΩ

Lower cut off frequency f1=100Hz

C2≈0.22µF

C1=C2=0.22µF

$C_F=1/(2\Pi f1Xc2)$ $Xc2=hie/(1+hfe)$ hie=1.5K, hfe=60

$=24.6\Omega$

C_F=64.69µF

Select standard value of 47µF or 100µF

Circuit Diagram to Measure Input Impedance:

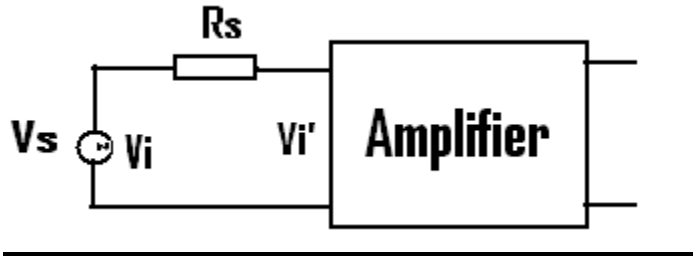


Fig.3.2

Circuit Diagram to Measure Output Impedance:

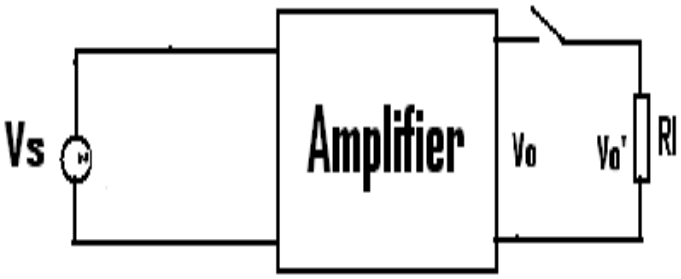


Fig.3.3

Tabulation:

Maximum Signal Handling Capacity =_____mV
Input Voltage V_i = _____mV

Sl. No.	Frequency f in Hz	Output voltage V_0 in mV	Gain in dB= $20\log(V_0/V_i)$

Calculations:

Input Impedance $Z_i = V_i`*R_S/(V_i-V_i`)$
Output Impedance $Z_O = (V_o-V_o`)R_L/V_o`$
Current gain $A_I = -A_V(Z_i/R_L)$
Voltage gain $A_v = V_o/V_i$

DESIGN AND TESTING OF DARLINGTON EMITTER FOLLOWER

Aim: Design and testing of Darlington emitter follower.

Apparatus required: Transistor (SL100), Resistor, DC regulated power supply, voltmeter, Ammeter, signal Generator, CRO and capacitors.

Theory:

A very popular connection of two BJTs for operation as one **super beta** transistor is the Darlington connection. The main feature of Darlington connection is that the composite transistor acts, as a single unit with a current gain is equal to product of individual current gains.

i.e. $\beta_D=\beta_1 x \beta_2$ **if** $\beta_1= \beta_2= \beta$ **Then** $\beta_D= \beta^2$

To make the two transistors Darlington pair, the emitter terminal of the first transistor is connected to the base of the second transistor and the collector terminals of the two transistors are connected together. The result is that emitter current of the first transistor is the base current of the second transistor.

The biasing analysis is similar to that for single transistor except that two V_{BE} drops are to be considered.

In a circuit if the output voltage is approximately equal to the input voltage, such a circuit is known as emitter follower. In the transistor emitter follower circuit the output is taken from the emitter terminal. The voltage gain is approximately equal to unity and output voltage is in phase with the input voltage. The emitter follower configuration is frequently used for impedance matching and to increase the current gain.

Sometimes the current gain and input impedance of emitter followers are insufficient to meet the requirement. In order to increase the overall values of circuit current gain (Ai) and input impedance, two transistors are connected in series in emitter follower configuration to obtain Darlington connection.

Procedure to obtain frequency response:

1) Before wiring the circuit, all the components using multimeter.
2) Make the connection as shown in circuit diagram.
3) Set V_{CC}, measure the DC biasing voltages using multimeter atV_{C2} (collector voltage), V_{E2} (emitter voltage) with respect to ground then verify

   $V_{CE2}=V_{C2}-V_{E2}$

   $I_{C2}=I_{E2}=V_{E2}/R_E$

   $Q_{point}= (V_{CE2}, I_{C2})$
3) Set the signal generator (input voltage) amplitude to such that the output remains sinusoidal and observe the input and output signals simultaneously on CRO.
4) By varying the frequency of the input from low value to high value note down peak-to-peak values of output and corresponding frequency. The output voltage V_o remains constant in mid frequency range. Tabulate the readings in tabular column.
5) Calculate the gain in dB and Plot the variation of gain in dB as a function of frequency in semi log sheet.
6) From graph determine the bandwidth.

Procedure to find input impedance:

1) Connect the circuit as shown in Fig 3.2.
2) Connect a resistance R_S in series with the input signal and amplifier as shown in the figure 3.2.
3) Set the signal generator (input voltage) amplitude (peak to peak sine wave) less than MSHC at a mid frequency band.
4) Measure and note down the input voltage V_i before R_S and voltage V'_i after R_S.
5) Calculate the input impedance.

Procedure to find output impedance:

1) Connect the circuit as shown in Fig 3.3.
2) Connect a resistance R_L across the output terminals of the amplifier as shown in the figure 3.3.
3) Set the signal generator (input voltage) amplitude (peak to peak sine wave) less than MSHC at a mid frequency band.
4) Measure and note down the output voltage V_o across output terminals when R_L is open circuited and output voltage V'_o when R_L connected across the output terminals. Calculate the output impedance.

CIRCUIT: without Bootstrapping

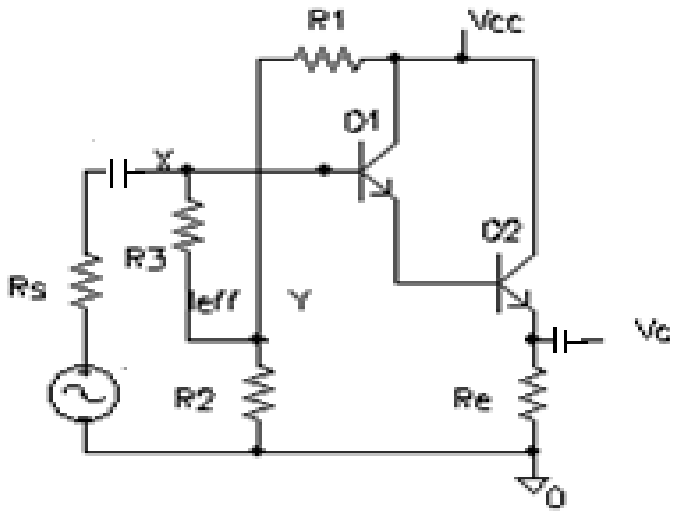
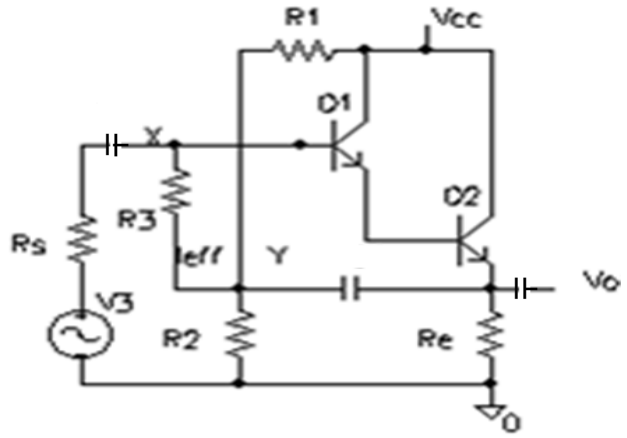


Fig.10.1

V_{CC}=10V
R_1=680 Ω
R_2=1kΩ
R3=10kΩ
R_E =2.2kΩ
C1=C2=0.1μF

CIRCUIT: with Bootstrapping



C_B=10uF

Circuit Diagram to Measure Input Impedance:

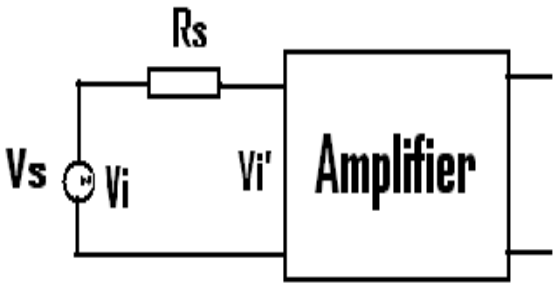


Fig.3.2

Circuit Diagram to Measure Output Impedance:

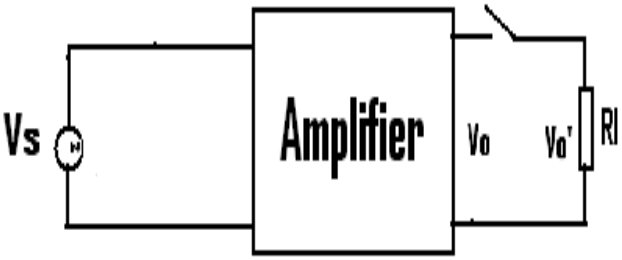


Fig.3.3

Tabulation:

Input Voltage $\mathbf{V_i}$ = _____mV

Sl. No.	Frequency f in Hz	Output voltage $\mathbf{V_0}$ in mV	Gain in dB= $20\log(V_0/V_i)$

Calculations:

Input Impedance $Z_i = V_i` * R_S/(V_i - V_i`)$

Output Impedance $Z_O = (V_o - V_o`)R_L/V_o`$

Current gain $A_I = -A_V(Z_i/R_L)$

Voltage gain $A_v = V_o/V_i$

Experiment No. :
Date of Conduction:

TESTING OF A SERIES VOLTAGE FEEDBACK AMPLIFIER.

Aim: Testing of a series voltage feedback amplifier to obtain frequency response with and with out feedback.

Apparatus required: BJTs, Resistors, Capacitors, Signal generators, DC power supply, connecting board and CRO.

Theory: Feedback plays an important role in almost all electronic circuits. It is almost invariably used in the amplifier to improve its performance and to make it more ideal. In the process of feedback, a part of output is sampled and feedback to the input of the amplifier. Therefore, at input we have two signals. Input signal and part of the output, which is feedback to the input. Feedback can be negative or positive and hence, depending on the sign of the feedback signal, feedback system can be classified as negative feedback system and positive feedback system.

There are four basic ways of connecting the negative feedback signal. Both voltage and current can be fed back to the input either in series or parallel. Specifically, there can be.

1) Voltage – series feedback
2) Voltage – shunt feedback
3) Current – series feedback
4) Current – shunt feedback

In the list above, voltage refers to connecting the output voltage as input to the feedback network; current refers to tapping off some output current through the feedback network; Series refers to connecting the feedback signal in series with the input signal voltage; shunt refers to connecting the feedback signal in shunt (parallel) with an input current source.

Series feedback connections tend to increase the input resistance while shunt feedback connections tend to decrease the input resistance, voltage feedback tends to decrease

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the output impedance while current feedback tends to increase the output impedance. Typically, higher input and lower output impedances are desired for most cascade amplifiers. Both of these are provided using the voltage-series feedback connection.

Procedure:

1) Before wiring the circuit, check the entire component using multimeter.
2) Make the connections as shown in the circuit diagram.
3) Check the DC biasing conditions.
4) If the DC biasing conditions are satisfactory, then apply the input ac signal (less than MSHC).
5) Vary the frequency of the input signal and note the corresponding frequency of signal and output voltage across the load resistor (R_L) with respect to ground.
6) Vary frequency so that the output voltage V_o remains constant in mid-frequency range and output voltage is lesser than mid frequency range at lower and higher frequencies.
7) Plot the graph of gain in dB Vs frequency.
8) From graph determine bandwidth.

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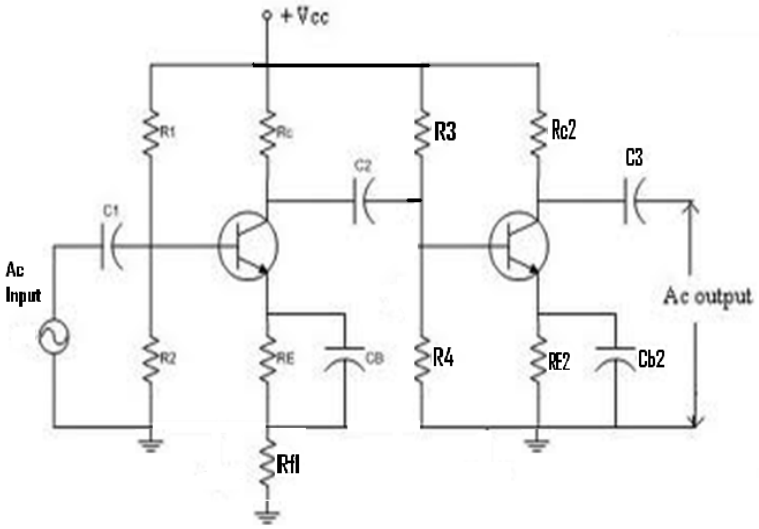
Amplifier with out feedback:



Q1=Q2=BC107
VCC=12V
R1=47kΩ
R2=42kΩ
Rc=780Ω
RE=4.7kΩ
R3=22kΩ
R4=27kΩ
Rc2=330Ω
RE2=2,7kΩ
Rf1=330 Ω
C1=0.25µF
C2=10µF
C3=10µF
CB2=CB=47µF

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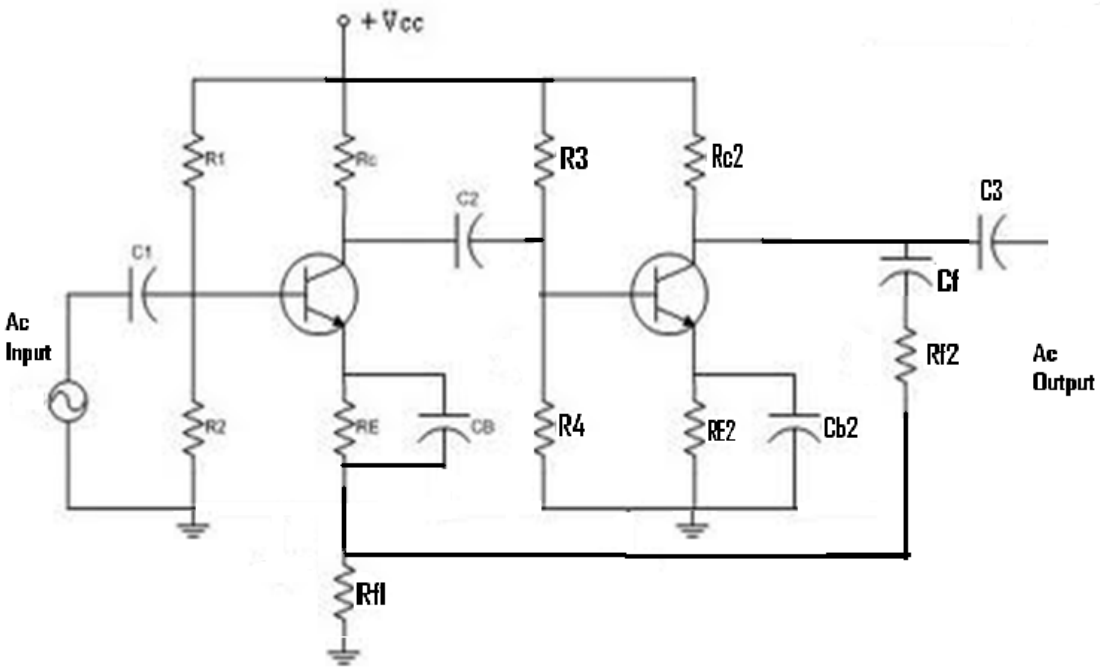
Amplifier with feedback:



Q1=Q2=BC107
VCC=12V
R1=47kΩ
R2=42kΩ
Rc=780Ω
RE=4.7kΩ
R3=22kΩ
R4=27kΩ
Rc2=330Ω
RE2=2,7kΩ
Rf1=330 Ω
Rf2=10k Ω
Cf=10µF
C1=0.25µF
C2=10µF
C3=10µF
CB2=CB=47µF

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Circuit Diagram to Measure Input Impedance:

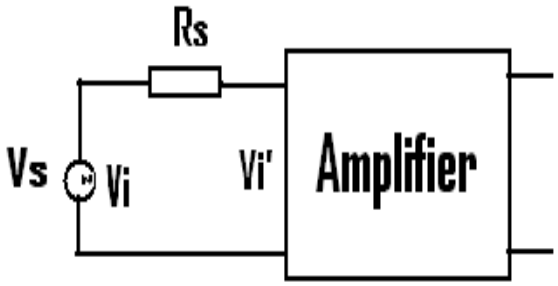

Fig.3.2

Circuit Diagram to Measure Output Impedance:

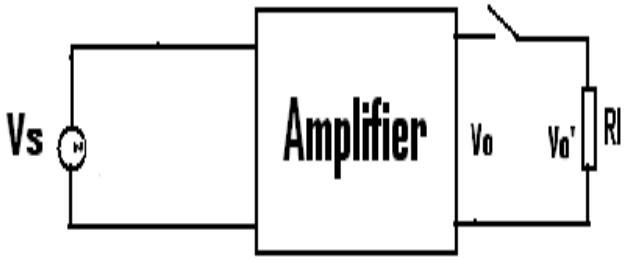

Fig.3.3

Tabulation:

Input Voltage $\mathbf{V_i}$ = _____mV

Sl. No.	Frequency f in Hz	Output voltage $\mathbf{V_0}$ in mV	Gain in dB= $20\log(V_0/V_i)$

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Calculations:

Input Impedance $Z_i = V_i` * R_S/(V_i - V_i`)$

Output Impedance $Z_O = (V_o - V_o`)R_L/V_o`$

Current gain $A_I = -A_V(Z_i/R_L)$

Voltage gain $A_v = V_o/V_i$

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WIRING AND TESTING OF RC PHASE SHIFT OSCILLATOR

Aim: Wiring and testing of RC phase shift oscillator.

Apparatus required: Power supply (0-30V), Transistor-BC107, Resistors: 1kΩ, 82kΩ, 15kΩ, 4.7kΩ, pot.:0-5kΩ, Capacitors: 47μF, 0.01μF, Signal generator, CRO and multimeters..

Theory: Oscillator is a circuit used to generate different wave forms. The use of positive feedback which results in a feedback amplifier having closed loop gain greater than 1 and satisfies phase condition will result in operation as an oscillator.

The RC phase-shift oscillator consists of a conventional CE amplifier and RC phase-shift network as a feedback system. The voltage shunt feedback is provided using three sections of RC. At some particular frequency for the phase shift in each RC section is 60^o, so that total phase shift produced by the RC network is 180^o. The frequency of oscillation is given by

$$f_o=1/(2\Pi RC\sqrt{6+4k})$$

Where, $k=R_C/R\geq 1$

Procedure:

1) Select pot of 0-10k resistor in the last section of phase shifting network to get a overall phase shift of 180^o at the frequency of oscillation.
2) Connect the circuit as shown in the figure and set V_{CC}= 10V.
3) Then verify the DC biasing conditions: $V_{CE}=V_{CC}/2$ and V_{BE}=0.7 V
4) The 10K pot is adjusted to get a stable sinusoidal output wave.
5) Measure the frequency of oscillation of the output wave using the CRO.
6) Note the phase shift between 3 sections of RC network with respect to the output wave.
7) Sketch the output wave and waveforms at 3 sections of RC network.

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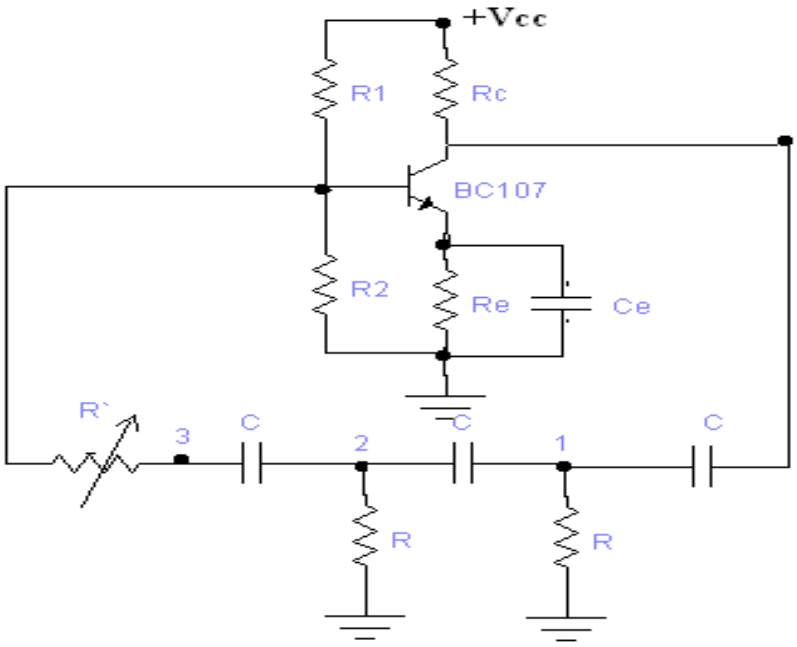
CIRCUIT DIAGRAM:



V_{CC}=10v
R_e=1kΩ
R_c=4.7kΩ
R_1=82kΩ
R_2=15kΩ
C_e=47μF
R=4.7kΩ (k=1)
For f=10kHz C=1000pF
Pot.: R'=0-5kΩ

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TESTING OF HARTLEY AND COLPITTS OSCILLATORS

Aim: Testing of Hartley and Colpitt`s oscillators.

Apparatus required: BJT, Resistors, Capacitors, Inductors, DC power supply and CRO.

Theory:

Hartley and Colpitts oscillators are the tuned circuit oscillators.

Hartley oscillator

If the oscillator consists of two inductors, and one capacitor in the feedback network that is tank circuit then it is called Hartley oscillator.

Hartley oscillator consists of a BJT CE amplifier with tank circuit (feedback network). The resistances R1, R2, R_C and R_E bias the BJT. The CE amplifier provides a phase shift of 180º and tank circuit provides phase shift of another 180º, this satisfies the required oscillating condition of total phase shift of 360^o.

Frequency of oscillations in the output wave is:

$$f_o=1/[2\Pi\sqrt{(CL_{eq})}, \qquad \text{where } L_{eq}=L_1+L_2$$

Colpitts oscillator:

If the oscillator uses two capacitors and one inductor in the feedback network then it is called a Colpitts oscillator.

Colpitts oscillator consists of a BJT CE amplifier with tank circuit (feedback network). The resistances R1, R2, R_C and R_E bias the BJT. The CE amplifier provides a phase shift of 180º and tank circuit provides phase shift of another 180º, this satisfies the required oscillating condition of total phase shift of 360^o.

Frequency of oscillations in the output wave is:

$$f_o=1/[2\Pi\sqrt{(LCeq)} \qquad \text{where } C_{eq}=C_1C_2/(C_1+C_2)$$

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Procedure:

1) Before wiring the circuit, check all the component using multimeter.
2) Make the connections as shown in circuit diagram.
3) Design the tank circuit where fo = 100 KHz.
4) Set the values of inductor and capacitor so as to get the required frequency of oscillation.
6) Compare the values of theoretical and practical values of frequency.

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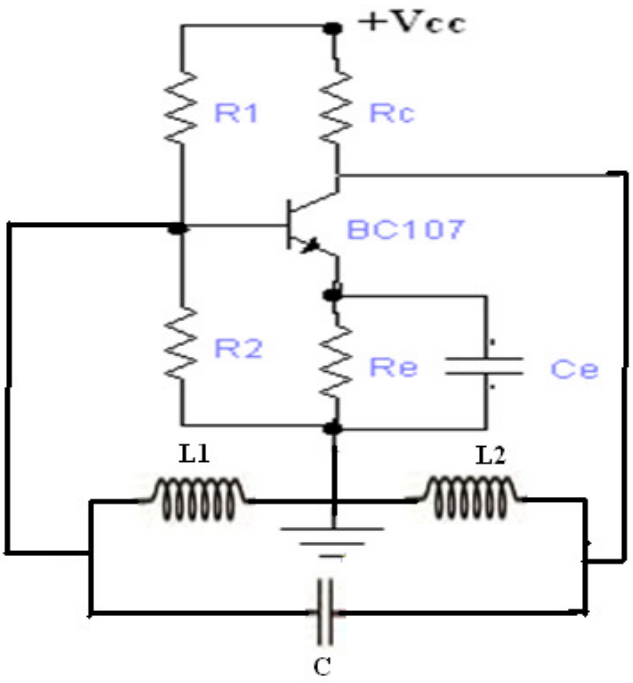
Circuit Diagram for Hartley Oscillator:



Frequency of oscillation $f=1/2\pi\sqrt{(L_{eq}C)}$
Where, $L_{eq}=L_1+L_2$
Frequency of oscillation required: f=100 kHz
Let $L_1=L_2=0.1$mH
C= 0.127 nF
(Select standard value of 0.1 nF)

V_{CC}=10v
R_e=1kΩ
R_c=4.7kΩ
R_1=82kΩ
R_2=15kΩ
C_e=47μF
$L_1=L_2$=0.1mH
C=0.1nF

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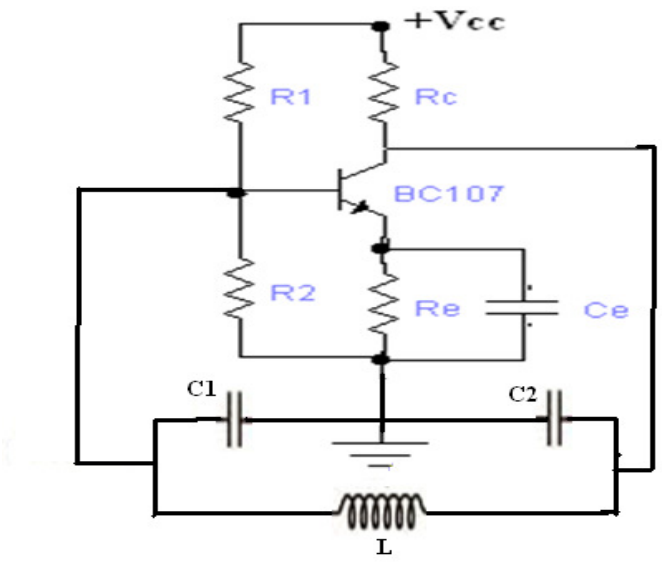
Circuit Diagram for Colpitts Oscillator:



Frequency of oscillation $f=1/2\pi\sqrt{(LC_{eq})}$
Where, $C_{eq}=C_1C_2/(C_1+C_2)$
Frequency of oscillation required: f=100 kHz
Let $C_1=C_2=2.2nF$
L= 2.3 mH
(Select standard value of 2 mH)
$V_{CC}=10v$
$R_e=1k\Omega$
$R_c=4.7k\Omega$
$R_1=82k\Omega$
$R_2=15k\Omega$
$C_e=47\mu F$
$C_1=C_2=2.2$ nF
L=2 mH

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TESTING OF DIODE CLIPPING CIRCUITS

Aim: Testing of diode clipping circuits.

Apparatus required: Diode (1N4007/BY127), Resistor, DC regulated power supply, signal generator and CRO.

Theory:

The circuit with which the waveform is shaped by removing (or clipping) a portion of the applied wave is known as a clipping circuit.

Clippers find extensive use in radar, digital and other electronic systems, although several clipping circuit have been developed to change the wave shape, we shall confine our attention to diode clippers. These clippers can remove signal voltages above or below a specified level.

The important diode clippers are:

1. Parallel clipper circuits
2. Series clipper circuits

Further it can also be classified into:

1. Positive clippers
2. Biased clippers.
3. Combinational clippers.

A clipping circuit comprises of linear elements like resistors and non-linear elements like junction diodes or transistor, but it does not contain energy storage elements like capacitors. Clipping circuits are used to select, for purposes of transmission, that part of a signal wave from which lies above or below a certain reference voltage level.

There are generally two categories of clippers: series and parallel. The series configuration is defined as one where diode is in series with the load while the parallel variety has the diode in a branch parallel to the load.

The analysis of any clipping circuit involves the following stages.

1) A study of the working of the diode.

2) Formulation of the transfer characteristic equations and

3) Plotting the output waveform V_0 by transfer characteristics.

Transfer characteristics is the plot of output voltage V_o vs V_i that depends upon whether a diode is ON or OFF. By the switching action of nonlinear element definite relationship can be obtained between V_o and V_i, in practical clipper circuits. The equation connecting V_o and V_i is termed as transfer characteristic equation.

Procedure:

1) Before wiring the circuit, check all the components using multimeter.

2) Make the connection as shown in circuit diagrams.

3) Apply input wave using function generator (Sine/triangular/square wave at 1 KHz and amplitude of 8V P-P) to the clipping circuit and observe the clipped output waveform on CRO.

4) Note output waveform corresponding to the input wave from the CRO.

5) Verify the practical results with theoretical calculations.

6) Apply V_i and V_o to the X and Y channel of CRO and observe the transfer Characteristic waveform and verify it.

Test the diode clipping circuit to peak clip off.

CIRCUIT 1

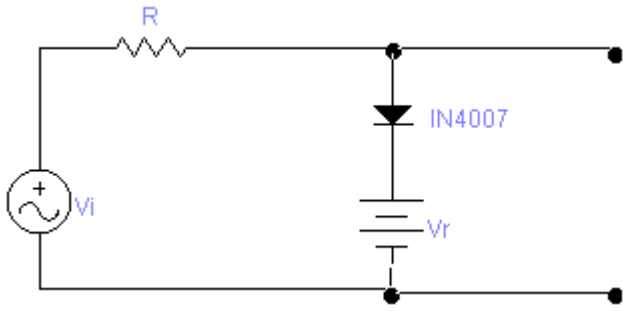

Figure 1.1

$R = \sqrt{(R_f \times R_r)}$

R_f → Forward resistance of the diode.
R_r → Reverse resistance of the diode.
V_T → Threshold voltage of the diode.
V_R → Reference voltage.

(i) For $V_i \leq V_R + V_T$, Diode is OFF

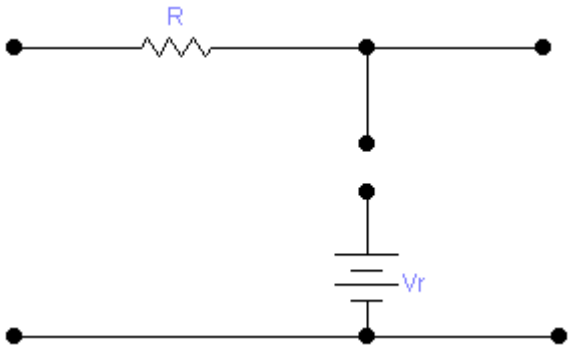

Figure 1.2

(ii) For $V_i > V_R+V_T$, Diode is ON

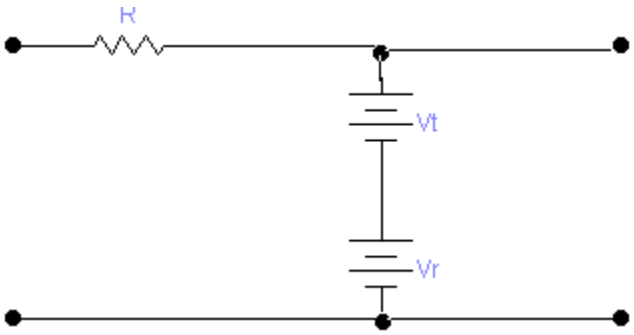

Figure1.3

CIRCUIT 2

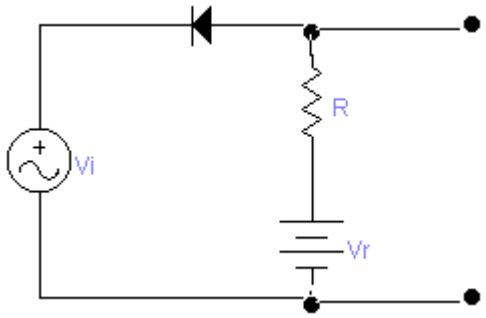

Figure1.4

(i) $V_i \geq V_R-V_T$, Diode is OFF
$V_o = V_R$
(ii) Vi < VR-VT, Diode is ON
$V_o \approx V_i$

CIRCUIT 3

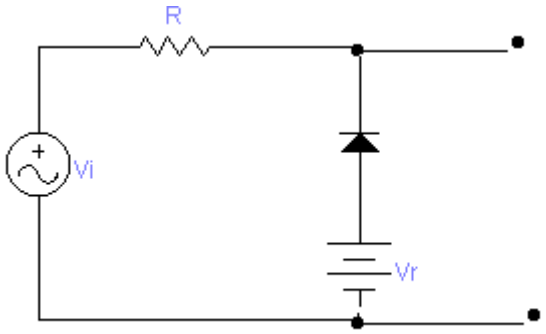

Figure 1.5

For $V_i \leq (V_R - V_T)$, Diode is ON

$$\mathbf{V_o = V_R - V_T}$$

For $V_i > (V_R - V_T)$, Diode is OFF

$$\mathbf{V_o = V_i}$$

CIRCUIT 4

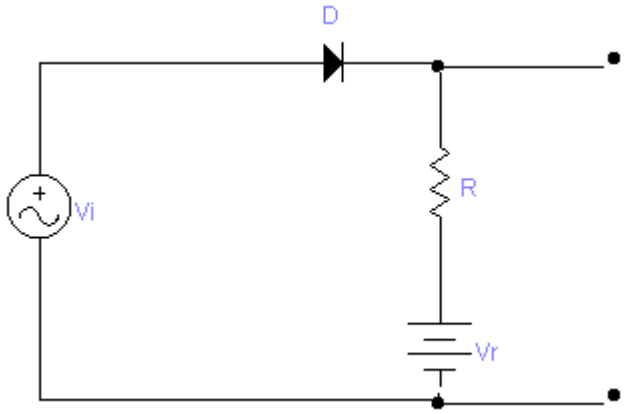

Figure 1.6

$V_i \leq V_R + V_T$, Diode is OFF

$V_o = V_R$

$V_i > V_R + V_T$, Diode is ON

$V_o \approx V_i$

Double ended clipping circuits

CIRCUIT 5

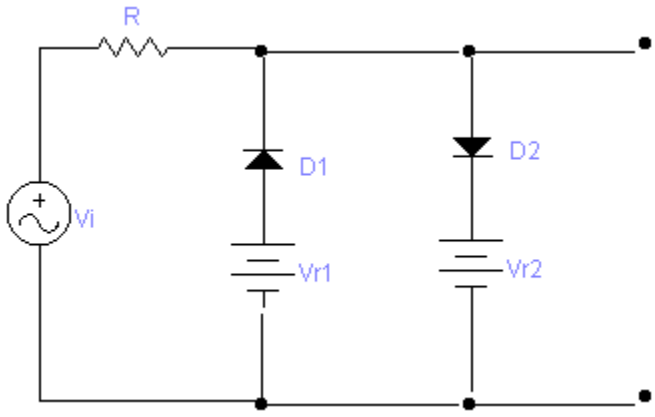

Figure 1.7

$V_{R2} > V_{R1}$

For $V_i \leq V_{R1}$, Diode D_1 is ON, diode D_2 is OFF

$V_o = V_{R1}$

For $V_i \geq V_{R2}$, Diode D_1 is OFF, diode D_2 is ON

$V_o = V_{R2}$

For $V_{R1} < V_i < V_{R2}$, Diode D_1 is OFF, diode D_2 is OFF

$V_o = V_i$

DESIGN AND TESTING OF CLAMPING CIRCUITS FOR SPECIFIC NEEDS

Aim: Design and testing of clamping circuits for specific needs.

Apparatus required: Diode IN4007, Resistors, capacitor, signal generator and CRO.

Theory:

A circuit that places either the +ve or –ve peak of a signal at a desired d.c. level is known as a clamping circuit positive clamper.

A clamping circuit (or a clamper) essentially adds dc component to the signal. The network must have a capacitor, a diode and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The clamping circuit does not make the shape of the original signal to change; but makes a vertical shift in the signal. The magnitude of R and C must be chosen such that the time constant is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non-conducting. The clamping circuit which shifts the signal vertically upwards is called a positive clamper. The negative clamper does the reverse that is it pushes the signal downwards so that the positive peak falls on the zero level.

The input signal is assumed to be a square wave with time period T. The clamped output is obtained across R_L. The circuit design incorporates two main features. Firstly, the values of C and R_L are so selected that time constant $T=CR_L$ is very large. The clamped output is taken across R_L.

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Procedure:

1) Before wiring the circuit, check all the components using multimeter.
2) Make the connection as shown in circuit diagrams.
3) Apply input wave, usually a square wave (or sinusoidal wave/triangular wave) to the circuit and observe the output wave using CRO.
4) Note down the input wave and corresponding output wave.

Design

5ζ (time constant) $=5RC>>T/2$
Let $R = 1K\Omega$
Then $C \approx 1\mu F$ (For a frequency of 50 Hz to 500 Hz)

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CIRCUIT 1

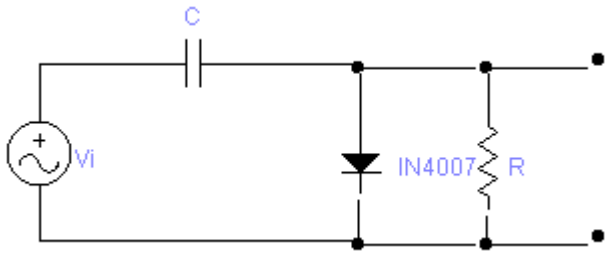

Figure 2.1

CIRCUIT 2

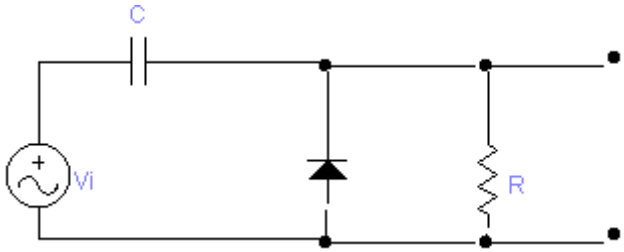

Figure 2.2

CIRCUIT 3

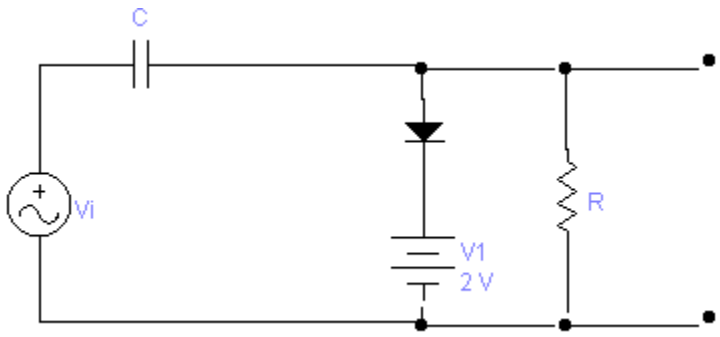

Figure 1.3

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TESTING OF TRANSFORMERLESS PUSH PULL POWER AMPLIFIER

Aim: Testing of a complementary symmetry Class B power amplifier (Transformer less Push Pull power amplifier.

Apparatus required: Power Transistors (SL100 and SK100), Resistors, load resistor, Capacitors, function generator, DC power supply and CRO.

Theory:

Class B amplifier is one which gives half (180º) cycle as output signal for one complete cycle (360º) of input signal.

Complementary symmetry class B power amplifier needs two power transistors, among that one is npn and other is pnp power transistor. The main advantage of this amplifier is that the absence of the transformer which is more expensive, bulky and heavy. This type of transformer has maximum efficiency equal to 78.5%.

A single input signal is applied to the base of both transistors, the transistors, being opposite type, will conduct on opposite half cycles of the input.

Both the transistors are biased at cut off regions of their output characteristics, so that one of the transistors conducts during each half cycle. During a complete cycle of the input a complete cycle of output signal is developed across the load. One disadvantage of the circuit is the need for two separate voltage supplies.

Procedure:

1. Make the connections as shown in the Fig. and take proper care while giving biasing voltage.
2. Apply the input signal at a frequency of 1 kHz-10 kHz.
3. Adjust the input voltage (peak) equal to DC supply i.e. $V_m=V_{CC}$. If the output voltage is sine wave then note the magnitude of output voltage, otherwise decrease the input till the output remain sinusoidal and then note the magnitude of output voltage.
4. Calculate Power input, output and efficiency.

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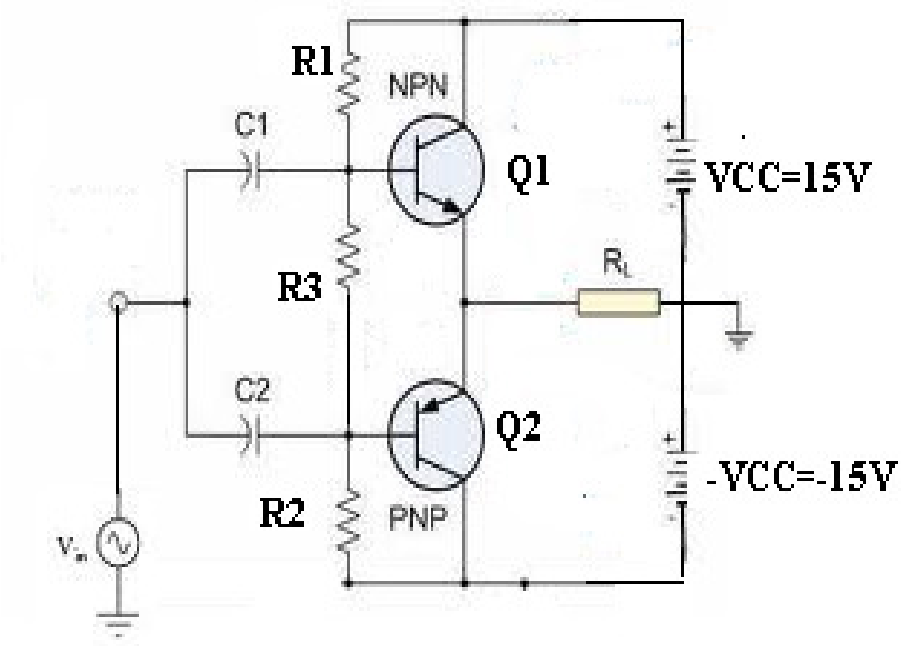
Circuit Diagram:



Q1-SL100

Q2-SK100

R1=R2=1kΩ

R3=100Ω

C1=C2=10F

RL=12 Ω

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TESTING OF HALF WAVE, FULL WAVE AND BRIDGE RECTIFIERS WITH AND WITHOUT CAPACITOR

Aim: To determine the ripple factor, efficiency and regulation of the half wave, full wave and bridge rectifier circuits with and without capacitor.

Apparatus: Diode-1N4007, load resistor -1kΩ & 1/2W, capacitor 100μF, transformer -15V-0-15V, ammeter 0-25mA (MI) and 0-25mA (MC), voltmeter 0-25V.

Theory:

Rectification is the process of converting the alternating quantity (AC) to the unidirectional quantity (DC with pulsation). The transformer is used to step down the voltage from 230V to the desired level. Then, the diode is responsible for the conversion of ac available at the secondary of the transformer into DC with pulsation. Hence, the diode used for this application is also referred as rectifier. The capacitor connected across the load (resistor) is behaving as a filter. Filter is responsible to smooth the pulsating DC into pure DC.

Half wave rectifier is one which converts the ac into pulsating dc during one half of the cycle. It has poor ripple factor, conversion efficiency and voltage regulation.

Full wave rectifier is one which converts the ac into pulsating dc during both cycles. For this process two diodes and centre tapped transformer are required. It has better ripple factor, conversion efficiency and voltage regulation compare to the half wave rectifier.

The centre tapped transformer is costly compare to without centre tap. This can be overcome by using 4 diodes in a bridge. The bridge rectifier has same ripple factor and conversion efficiency as that of full wave rectifier, but better utilization factor.

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Procedure:

Without Capacitor:

1. Connections are made as shown in the figure for half wave rectifier circuit.
2. Measure the voltage across the terminals when the resistor is open circuited (No load).
3. Connect the load resistor across the output terminals and note, the voltmeter reading and ammeter readings (I_{rms} and I_{DC}).
4. Repeat the above procedure for full wave rectifier and bridge rectifier.

With Capacitor:

1. Connections are made as shown in the figure for half wave rectifier circuit with capacitor.
2. Measure the voltage across the terminals when the resistor is open circuited (No load) but capacitor is connected.
3. Connect the load resistor across the output terminals and note, the voltmeter reading and ammeter readings (I_{rms} and I_{DC}).
4. Repeat the above procedure for full wave rectifier and bridge rectifier with capacitor.

CIRCUIT-Half Wave Rectifier

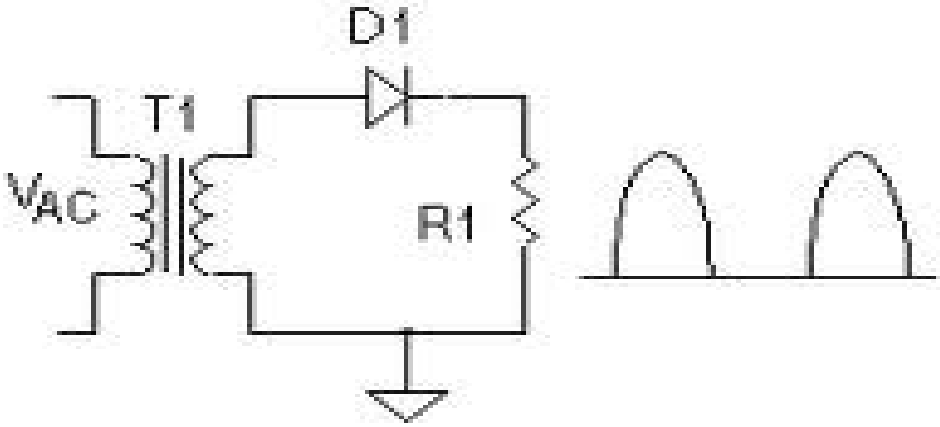

Fig.1

CIRCUIT-Half Wave Rectifier with capacitor

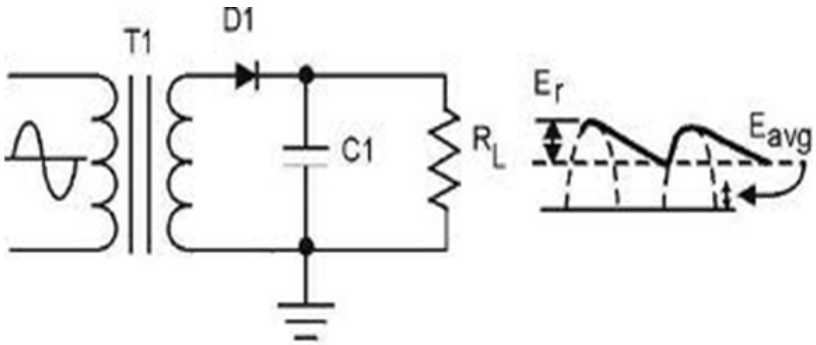

Fig.2

CIRCUIT-Full Wave Rectifier

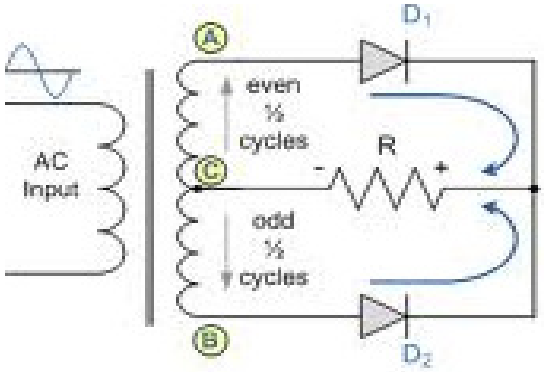

Fig. 3

CIRCUIT-Full Wave Rectifier with filtor

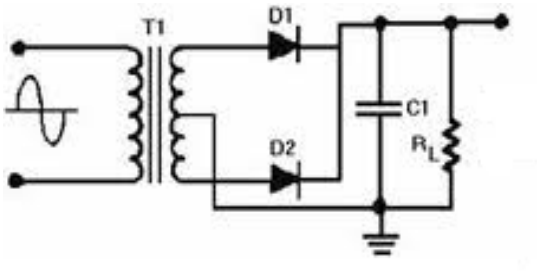

Fig .4

CIRCUIT-Bridge Rectifier

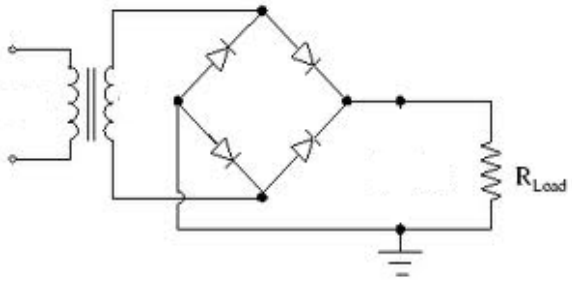

Fig.5

CIRCUIT-Bridge Rectifier with capacito

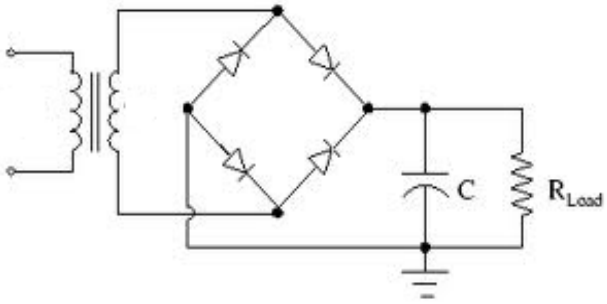

Fig.6

Tabulation:

Position of the switch	I_{DC}	I_{RMS}	V_M	V_{DC}
Open				
Closed				

Calculations:

Without Capacitor:

$\gamma = [(I_{RMS}/I_{DC})^2-1]^2$

$\%\eta = (P_{DC}/P_{AC})x100$ $P_{DC}=I_{DC}^2R_L$ $P_{AC}=I_{RMS}^2R_L$

$\%VR = (V_{NL}-V_L/V_L)x100$

With capacitors:

$\gamma = 1/(2(3)^{1/2}R_LfC)$

$\%\eta = (P_{DC}/P_{AC})x100$ $P_{DC}=I_{DC}^2R_L$ $P_{AC}=I_{RMS}^2R_L$

$\%VR = I_{DC}/2fC$

VERIFICATION OF THEVENIN'S AND MAXIMUM POWER TRANSFER THEOREM

Aim: Verification of Thevenin's and Maximum Power Transfer theorem.

Apparatus required: Resistors, DC supply, ammeter and multimeter.

Theory:

Thevinin's Theorem states that "Any linear, bilateral, two terminal network can be replaced by a voltage source in series with a resistance, where value of voltage source is equal to open circuited voltage between the load terminals and the resistance is equal to the resistance looking from the open circuited terminals replacing all the source by their internal resistances if any".

Let V_{OC} be the open circuited voltage across the load resistance,

R_{TH} be the Thevenin's resistance of the circuit.

Then, current through the load resistance is given by,

$$I_L=V_{OC}/(R_{TH}+R_L)$$

Maximum Power Transfer Theorem states that "In any linear, bilateral network the maximum power will be transferred from the circuit to the load if and only if load impedance is complex conjugate of the internal impedance"

OR

For DC circuit it states that ".In any linear, bilateral network the maximum power will be transferred from the circuit to the load if and only if load resistance is equal to the internal resistance"

Let V_{OC} be the open circuited voltage across the load resistance,

R_I be the internal resistance of the circuit.

Then, maximum power will be delivered to the load resistance is given by,

$$P_{max}=V_{OC}^2/4R_I$$

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Procedure:

Thevinin's Theorem

1. Make the connections as shown in the Fig.1
2. Adjust the DC supply voltage using multimeter.
3. Note the current flowing through the load resistor.
4. Switch off the DC source; remove the load resistor from the terminals (open circuit).
5. Switch on DC source and note V_{OC} across the open circuited terminals (Fig. 2).
6. Make connections as shown in the Fig. 3 and find R_{TH}.
7. Make connections as shown in the Fig. 4 to obtain Thevenin's equivalent circuit and adjust V_{OC} and R_{TH} as obtained in steps 5 and 6.
8. Note the current flowing through the load resistor.
9. Verify the current obtained in step 3 and 8.

Maximum Power Transfer Theorem

1. Make the connections as shown in the Fig.1
2. Adjust the DC supply voltage using multimeter.
3. Vary the load resistance from 100 ohm to 1kohms.
4. Note the current corresponding to each value of load resistance.
5. Calculate the power and verify the load resistance at which the power will be maximum.

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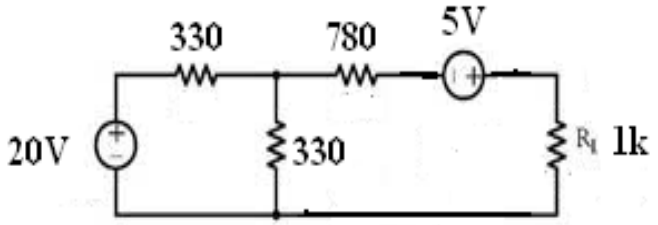
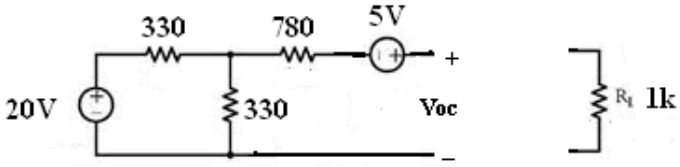
Thevenin's theorem

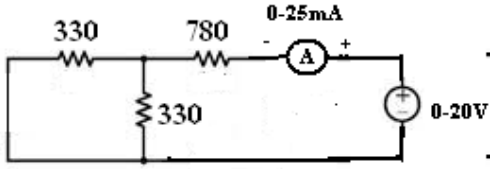
Circuit Diagram:



Circuit to find V_{oc}:

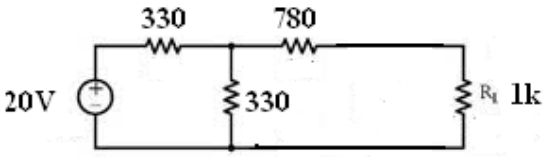


Circuit to find R_{th}:



Maximum Power transfer theorem

Circuit Diagram



To find V_{oc}:

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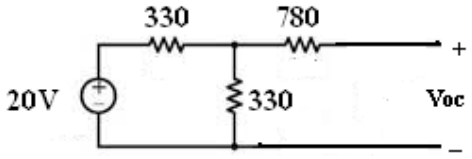
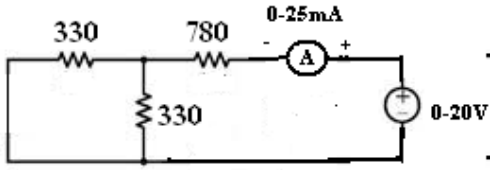
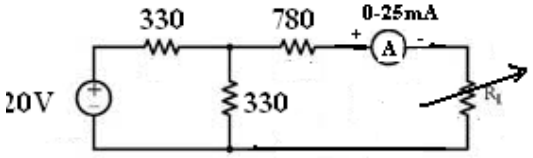


$P_{max}=V_{oc}^2/4R_L$

To find internal resistance R_{in} at which power transfer to the load R_L is maximum:



To obtain a plot of power Vs R_L:



Tabulation:

Sl. No	R_L in Ohms	I_L in mA	P_L in mW

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Series and Parallel Resonant Circuits

Aim: To obtain the characteristics of series and parallel resonant circuits.

Apparatus required: Decade resistance box, Decade inductance box, Decade capacitance box and ammeter.

Theory:

Series Resonant Circuit:

In a series RLC circuit there becomes a frequency point were the inductive reactance of the inductor becomes equal in value to the capacitive reactance of the capacitor. The point at which this occurs is called the **Resonant Frequency**, (f_r) and as we are analysing a series RLC circuit this resonance frequency produces a **Series Resonance** circuit. Series resonance circuits are one of the most important circuits used electronics. They can be found in various forms in mains AC filters, and also in radio and television sets producing a very selective tuning circuit for the receiving the different channels.

In a series resonant circuit, the resonant frequency, f_r point can be calculated as follows.

$$f_r=1/2\pi\sqrt{(LC)}$$

We can see then that at resonance, the two reactances cancel each other out thereby making a series LC combination act as a short circuit with the only opposition to current flow in a series resonance circuit being the resistance, R. In complex form, the resonant frequency is the frequency at which the total impedance of a series RLC circuit is purely *"real"* as no imaginary impedances exist, they are cancelled out, so the total impedance of the series circuit becomes just the value of the resistance and: $Z = R$. Therefore, at resonance the impedance of the circuit is at its minimum value and equal to the resistance of the circuit.

The frequency response curve of a series resonance circuit shows that the magnitude of the current is a function of frequency and plotting this onto a graph shows us that the response starts at near to zero, reaches maximum value at the resonance frequency when $I_{MAX} = I_R$ and then drops again to nearly zero as f becomes infinite.

These -3dB points give us a current value that is 70.7% of its maximum resonant value as: $0.5(I^2 R) = (0.707 \times I)^2 R$. Then the point corresponding to the lower frequency at half the power is called the "lower cut-off frequency", labelled f_L with the point corresponding to the upper frequency at half power being called the "upper cut-off frequency", labelled f_H. The distance between these two points, i.e. ($f_H - f_L$) is called the **Bandwidth**, (BW) and is the range of frequencies over which at least half of the maximum power and current is provided.

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Parallel Resonant Circuit:

A parallel circuit containing a resistance, R, an inductance, L and a capacitance, C will produce a **parallel resonance** (also called anti-resonance) circuit when the resultant current through the parallel combination is in phase with the supply voltage. At resonance there will be a large circulating current between the inductor and the capacitor due to the energy of the oscillations. A parallel resonant circuit stores the circuit energy in the magnetic field of the inductor and the electric field of the capacitor. This energy is constantly being transferred back and forth between the inductor and the capacitor which results in zero current and energy being drawn from the supply. This is because the corresponding instantaneous values of I_L and I_C will always be equal and opposite and therefore the current drawn from the supply is the vector addition of these two currents and the current flowing in I_R.

Procedure:

Series Resonant Circuit:

1) Before wiring the circuit, check the entire component using multimeter.
2) Make the connections as shown in the circuit diagram.
3) Apply voltage across RLC series circuit using function generator.
4) Vary the frequency (or inductance/capacitance) in suitable steps and note the current flow through the circuit. Current reaches maximum value at series resonance.
5) Plot the curve of current against the frequency.

Parallel Resonant Circuit:

1) Before wiring the circuit, check the entire component using multimeter.
2) Make the connections as shown in the circuit diagram.
3) Apply voltage across the parallel resonant circuit using function generator.
4) Vary the frequency (or inductance/capacitance) in suitable steps and note the total current flow through the circuit. Current reaches minimum value at parallel resonance.
5) Plot the curve of current against the frequency.

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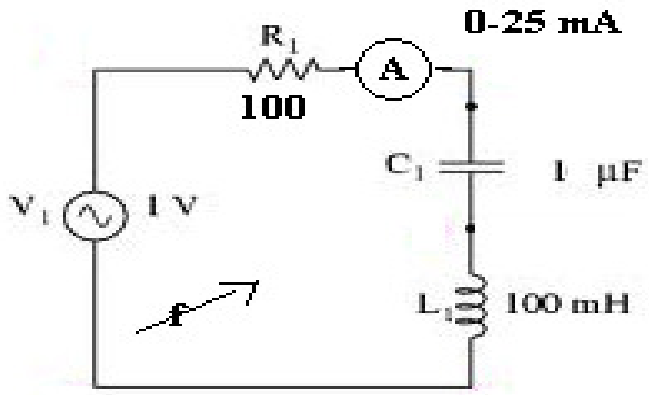
Circuit Diagram for Series Resonant Circuit:

Varying Frequency



Tabulation:

Sl. No.	Frequency in Hz	Current in mA

Varying Inductance

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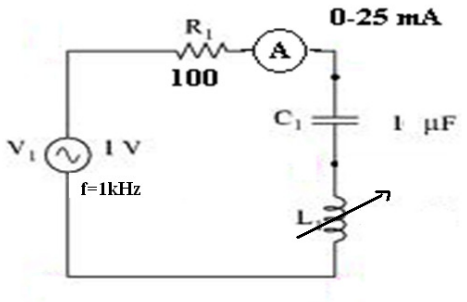
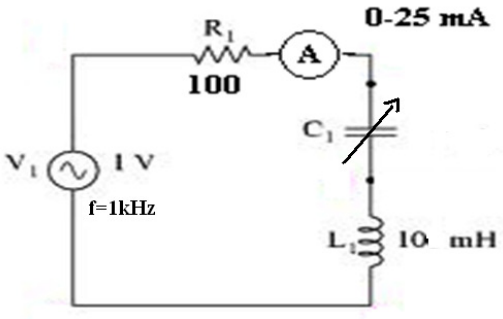


Tabulation:

Sl. No.	Inductance in mH	Current in mA

Varying Capacitance



Tabulation:

Sl. No.	Capcitance in µF	Current in mA

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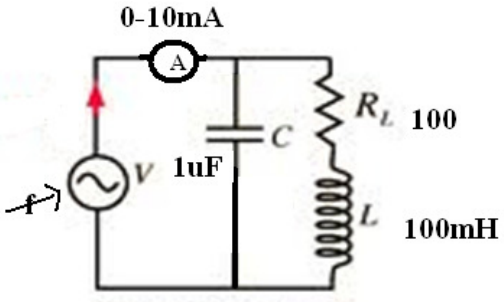
Circuit Diagram for Parallel Resonant Circuit:

Varying frequency



Tabulation:

Sl. No.	Frequency in Hz	Current in mA

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